Technical Article

The Five Benefits of Multifaceted Clocking Devices

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In today's world, most highly integrated systems serve more than one function and are designed to interface with other systems and peripheral devices. In addition, the same piece of hardware is often re-configured to suit the needs of various regions or end-users, thereby reducing the amount of inventory overhead for equipment manufacturers. The average end user is usually unaware of changes at the core of these systems, including - the mode of operation of the integrated circuits (ICs), which control the functionality of the end equipment. In this post, I will address an important feature of clock and timing ICs that provides the "heartbeat" or reference frequency for highly integrated systems. I like to call this feature "pin-selectable personality." In a nutshell, a pin-selectable personality is a device's ability to take on different configurations (personalities) depending on the state of its external control pins.

Before exploring potential scenarios for these pin-selectable personalities, let's review the different ways you can store a power-on-reset (POR) configuration in a clocking device. Device configurations selected using external control pins are typically stored in nonvolatile memory (NVM). The simplest memory option is a mask read-only memory (ROM), which is a type of ROM whose contents are hard-coded during the integrated circuit (IC) manufacturing process. While the main advantage of a mask ROM is its low cost per bit of storage, its one-time masking cost is high. Generating a mask ROM to support a new configuration requires IC redesign, fabrication, assembly and testing, and is often not a quick process. Continuously evolving system requirements demand faster product design cycle times.

The second option is a one-time programmable (OTP) NVM that is programmed only once after IC manufacturing by blowing fuses at each bit. In comparison to mask ROM NVM discussed earlier, configuring this form of NVM is often quicker. As the name implies, you can write to OTP NVM only once. This limitation during system prototyping could negatively impact project schedules.

An elegant solution to these problems exists in the form of nonvolatile electrically erasable programmable ROM (EEPROM), which gives you the flexibility to quickly try out different configurations during the prototype phase of your design cycle. EEPROM NVMs give clocking devices the flexibility to take on different pin-selectable personalities.

Figure 1 highlights the five most important system-level benefits of using clocking solutions with integrated EEPROM NVMs.

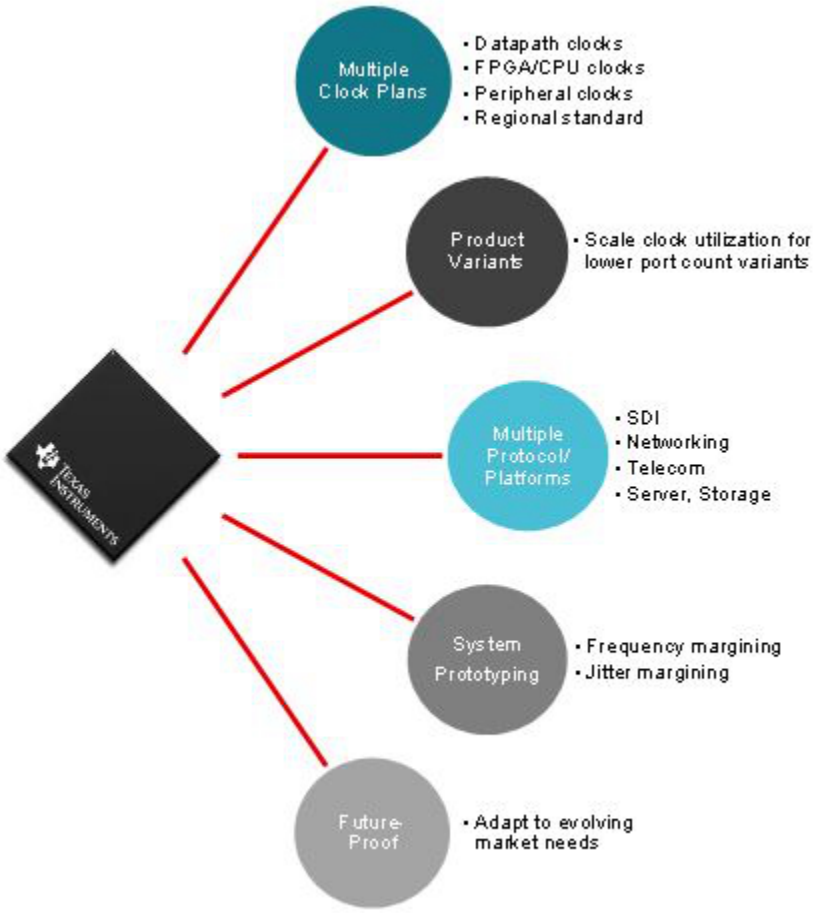

Figure 1. System-level Benefits of Clocking Solutions with Integrated EEPROM NVMs

Below, I will expand on each of these five benefits shown in Figure 1:

1. **Minimize system bill-of-materials (BOM) with multiple clock plans:** In several of my conversations with hardware designers, they have expressed a desire to minimize the number of ICs from clocking vendors that they choose to qualify for use in their systems. Moreover, different product lines within their respective companies have varied clocking needs depending on the end equipment. Clocking devices offering multiple integrated EEPROM NVM pages, that store unique configurations that can be accessed easily via control pin-strapping, help to greatly reduce system BOM and minimize IC qualification time.
2. **Manage requirements for product variants:** Your system could have different operating modes. In one mode, you may need to enable normally disabled processor banks to handle surge data-processing needs, for example. In another mode, you might need to turn off logic to minimize overall system power. The clocking device must accommodate these operation modes and their configurations, which different EEPROM pages can store.
3. **Address needs of multiple protocols/platforms:** In broadcast and professional video applications, clocking requirements for various video standards such as serial digital interface (SDI), high-definition multimedia interface (HDMI) and DisplayPort can differ significantly. Regional standards dictate the frequency of the video reference clock (148.5MHz or 148.5/1.001MHz for phase alternating line [PAL] or National Television System Committee [NTSC]-based systems, respectively). Region-specific frequency plans can be stored in unique EEPROM pages enabling one clocking IC to satisfy the needs of multiple platforms and protocols simultaneously.
4. **Streamline system prototyping:** Frequency and/or jitter margining are popular techniques to test system robustness and compliance during the engineering validation test/design validation test (EVT/DVT) phase of a system development cycle. In the case of frequency margining, the frequency at which the system starts to malfunction is measured using an iterative process. EEPROM pages on the clocking device can

store frequency variants from the nominal frequency (ranging from a few hertz to megahertz offset from nominal), that are selectable via control pins. Having the necessary hooks to do a frequency margining test in a clocking device helps streamline prototyping and validation.

5. **Future-proof your system:** Unused EEPROM pages can serve as placeholders for future configurations. You don't need to worry about qualifying a new clocking device when it is time to upgrade your system.

Let's now review a real-life application scenario where a clock generator IC with integrated EEPROM NVM offers the system benefits highlighted above:

Table 1 shows an EEPROM configuration plan for the LMK03328 ultra-high-performance clock generator. The pin-strapping GPIO2 and GPIO3 pins on the clocking device can select region specific video frequencies, the central processing unit (CPU) and Ethernet clocks as shown in the table. The table also highlights configurations where you could margin the CPU clock frequency by +/-5%.

Table 1. Pin Selectable Clock Configuration Using the LMK03328

EEPROM Page	Page 0	Page 1	Page 2	Page 3	Page 4	Page 5
GPIO3	LO	LO	LO	HI	HI	HI
GPIO2	LO	MID	HI	LO	MID	HI
PLL1 VCO	5 GHz	5 GHz	5 GHz	5 GHz	5 GHz	5.346/1.001 GHz
PLL2 VCO	5.346 GHz	5.346 GHz	5.346/1.001 GHz	5.346 GHz	5.346 GHz	5.346 GHz
OUT0	297 MHz	297 MHz	297/1.001 MHz	148.5 MHz	297 MHz	297 MHz
OUT3	125 MHz	125 MHz	125 MHz	125 MHz	125 MHz	Disabled
OUT4	156.25 MHz	156.25 MHz	156.25 MHz	156.25 MHz	156.25 MHz	297/1.001 MHz
OUT7	100 MHz	100 MHz	100 MHz	100 MHz	100 MHz	Disabled
OUT1,2,5,6	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
STAT0/CLK	66.6 MHz	69.4 MHz (+5% margining)	66.6 MHz	66.6 MHz	62.5 MHz (-5% margining)	Disabled

I hope that I have sparked some curiosity about clocking devices with mask ROM and integrated EEPROM NVM, providing cost-effectiveness and flexibility. My favorite high-performance clock generator is the LMK03328. Other popular choices are the CDCM6208 and CDCE949.

Log in to post a comment below or to speak to other engineers in the TI E2E™ Community Clock and Timing forum.

Additional Resources

- To learn more about frequency margining, download the application note, "Frequency Margining Using TI High Performance Clock Generators."
- Find out more about TI's clock and timing portfolio.

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