Application Report
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Enabling SmartReflex on the TMS320DM6467

Paul Yin, Randy Preskitt, Tom Guerin, and Daniel Meeks

ABSTRACT

This application report describes the concepts and benefits of SmartReflex™ technology implemented in the DM6467 device. Two reference power supply designs that support the SmartReflex feature are also discussed. With the SmartReflex feature enabled, an average of 1W in power savings can be achieved for strong devices. The included reference designs show that additional components are required in the voltage regulation circuitry, but the cost can be kept to a minimum.

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1 Introduction

1.1 Power and Performance Definitions

- Silicon performance: The maximum frequency that the device can operate with. Due to manufacturing variation, each device has different silicon performance.
- Weak device: A weak device has the lowest performance tolerated for a device distribution. Considered as the worst case, weak devices are used to constrain the target frequency of all the devices.
- Strong device: A strong device has the highest performance tolerated for device distribution.

- Performance target: The clock configuration that any device in the device distribution is able to support.
- Nominal voltage: The minimum voltage required for the weakest device to achieve the associated performance target. Therefore, strong devices operating at the nominal voltage show some performance margin.
- Optimized voltage: The minimum voltage required for a given device to achieve the associated performance target. The optimized voltage is reached when the performance target matches the device performance.
- Nominal operating performance point (OPP): A (performance target, nominal voltage) pair for the entire device distribution.
  - For weak device: silicon performance = performance target
  - For strong device: silicon performance > performance target
- Optimized OPP: A (performance target, optimized voltage) pair for a particular device.
  - For weak device: optimized voltage = nominal voltage, silicon performance = performance target
  - For strong device: optimized voltage < nominal voltage, silicon performance = performance target.

1.2 DM6467 Power and Performance Overview

The DM6467 device is the latest high-performance digital multimedia platform from Texas Instruments, Inc. With its high performance comes an increased consumption of power. It is desirable to minimize the power consumption while maintaining the target performance. The power estimation model used in the DM6467 power analysis tool breaks the overall power consumption into two parts: baseline power and active power. The baseline power is the power consumed independent of silicon activity, and it is dominated by leakage power. The active power is the power consumed by active parts of the device; this power can be separated by the major modules within the device. If a module is not enabled, there is no active power consumption from that module. For more information on the power consideration, see the *TMS320DM6467 Power Consumption Summary* (SPRAAS2).

The theoretical performance and power consumption for a general bell-curved manufacturing distribution is shown in Figure 1, with (P1, V1) representing the nominal OPP and P2 representing the performance for the strong device at V1. The extra performance margin cannot be utilized and a significant amount of extra power (both leakage power and active power) is consumed for strong devices operating at (P1, V1). In the case for DM6467, the nominal OPP for the DM6467 core is (594 MHz, 1.2 V); a strong device is capable of running at the same speed with a much lower supplied voltage or running at a much higher speed with the same supplied voltage. Table 1 provides an example of the DM6467 core power consumption comparison between a weak device and a strong device when different demos are running under Linux™.

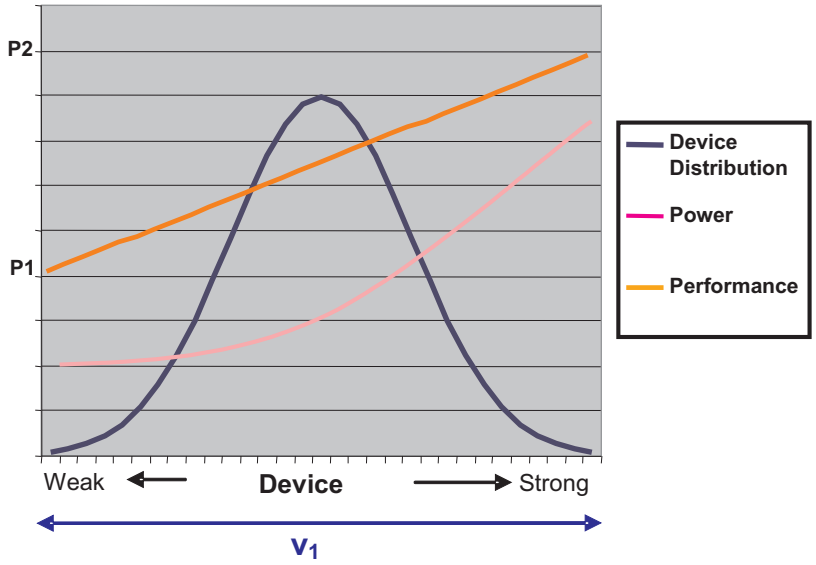

Figure 1. Performance and Power at Constant Voltage

Table 1. DM6467 Core Power Consumption Comparison

Linux Application	Core Power @ 25°C for Weak Device	Core Power @ 25°C for Strong Device
4-D1 Encoding (1)	1003.2mW	2262.7mW
HD-SD Transcoding (1)	926.4mW	2201.9mW

(1) For additional detail on the demos, see the *TMS320DM6467 Power Consumption Summary* (SPRAAS2).

Power consumption is one of the most important aspects in system design. First of all, from a power efficiency point of view, the average power consumption needs to be minimized provided that the required performance level is maintained. Secondly, the worst-case power consumption needs to be minimized so that an appropriate power supply module can be planned accordingly. From a device performance uniformity point and ease of board manufacturing point of view, the average and worst-case power consumption for all the devices on the device distribution should be similar so that not only their performance on a design is similar, but their power consumption is also similar. Therefore, during board mass production, devices of different strengths can be treated the same, and placed on boards with the same design criteria.

1.3 SmartReflex Overview on DM6467

To achieve optimal power and performance ratio, SmartReflex class-0 (SR) is implemented on the DM6467. Not all DM6467 parts support SR; for details on the SR part numbers and SR control pins, see the *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403).

SmartReflex is a technology that uses adaptive power supply to reduce active power consumption. The voltage is adjusted within the defined range by SR to minimize power consumption. SR assures that the voltage applied is sufficient for each device (of different strength) to operate at the nominal OPP frequency. The performance is measured at manufacturing test and the required operating voltage for that device is determined. This information is permanently stored into the device. During booting, the SR control ouptut signals are sent to the onboard adjustable power supply for the appropriate voltage level.

1.4 SmartReflex Implementation on DM6467

Devices with different strengths are partitioned into two groups: weak and strong devices. Weak devices should run at 1.2 V core power supply, whereas, strong devices can run at 1.05 V. During manufacturing test, the device characterization information is stored permanently on the DM6467 device.

The SmartReflex feature is disabled by default. It can be enabled by pulling the configuration pin VADJEN high before releasing the device from reset. The VADJEN input value is latched into Boot Configuration Register (BOOTCFG) (VADJEN bit) at the rising edge of RESET. Once SR is enabled, the pins CVDDADJ0 and CVDDADJ1 function as SR control outputs to the adjustable power supply, and the GPIO functionality for these pins is disabled. After the device comes out of reset (RESET signal is high), the device characterization information is retrieved and is reflected on the SR control output pins CVDDADJ[1:0]. As shown in Table 2, the CVDDADJ[1:0] value of '00' corresponds to the need for a 1.2 V core power supply; and the value of '11' indicates that the device can operate at 1.05 V core power supply. The value of these pins is also stored in the read only register SMTREFLEX. The 1.8 V and 3.3 V power supplies remain the same for all devices.

Table 2. SmartReflex Pinmuxing

VADJEN Pin	Pin Function (GP[7:6] / CVDDADJ[1:0])
0	GP[7:6] - SmartReflex is disabled. Pins function as GPIO.
1	CVDDADJ[1:0] - SmartReflex is enabled. GPIO feature is disabled. 00 - Device operate at only 1.2 V core power supply. 11 - Device can operate at 1.05 V core power supply.

Figure 2 illustrates how the power consumption is improved when SmartReflex is enabled on DM6467 and Table 3 shows the actual power savings for different applications.

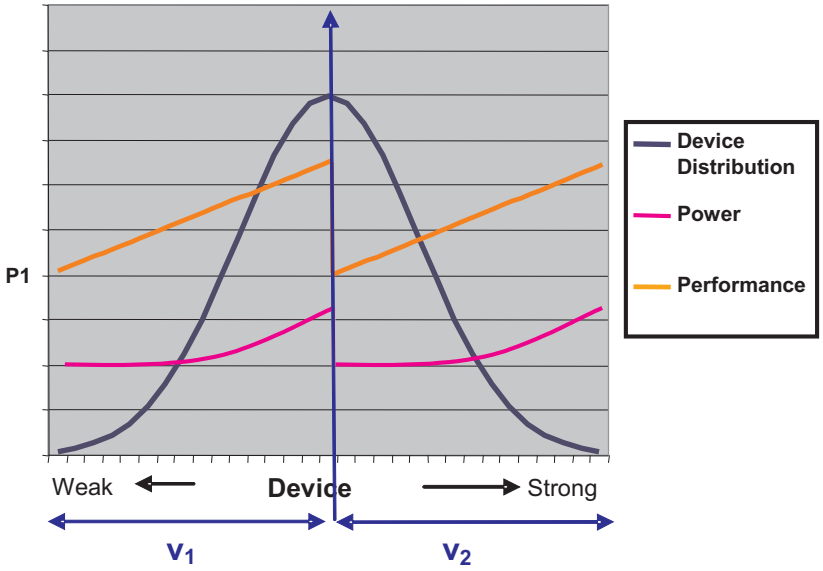

Figure 2. Maximum Performance and Power Consumption with SmartReflex Enabled

Table 3. DM6467 Core Power Consumption Comparison with SmartReflex Enabled

Linux Application	Core Power @ 85°C for Weak Device (with or without SR enabled)	Core Power @ 85°C for Strong Device (without SR enabled)	Core Power @ 85°C for Strong Device (with SR Enabled)	Power Saving for Strong Device (by enabling SR)
Worst-Case Leakage (Theoretical)	1200mW	1920mW	1575mW	345mW
4-D1 Encoding (1)	2235.3mW	3456.3mW	2457.2mW	999.1mW
HD-SD Transcoding (1)	2291.5mW	3395.5mW	2410.7mW	984.8mW

(1) For additional detail on the demos, see the *TMS320DM6467 Power Consumption Summary* (SPRAAS2).

For a weak device, Table 3 shows that there is no power savings when SR is enabled. On the other hand, an average of approximately 1W in power savings can be achieved for a strong device. In addition, the table shows that, when SR is enabled, the overall core power consumption for a given application is similar regardless whether it is ran on a strong device or a weak device.

SmartReflex on DM6467 provides a significant power savings on both the average and worst-case power consumption on strong devices. For an estimate on the average and worst-case power consumption for a specific application, see the *TMS320DM6467 Power Consumption Summary* (SPRAAS2).

2 Timing and Voltage Level Consideration on DM6467

To maintain correct functionality of the device, the SmartReflex adjustable power supply must be designed to provide either 1.2 V or 1.05 V core voltage as directed by the state of the CVDDADJ[1:0] pins with a maximum 5% error. The possible states of CVDDADJ[1:0] and the voltage requirement are detailed in Table 4.

Table 4. Possible States of GP[7:6]/CVDDADJ[1:0] and Core Voltage

$\overline{\text{RESET}}$	VADJEN	GP[7:6]/CVDDADJ[1:0]	CV_{DD}
0	0	0	1.2 V (SR disabled)
Rising Edge	0	GPIO function	1.2 V (SR disabled)
1	0	GPIO function	1.2 V (SR disabled)
0	1	0	1.2 V (SR disabled)
Rising Edge	1	0	1.2 V (SR enabled)
1	1	Invalid for 62 µs	1.2 V (SR enabled)
1	1	After 62 µs, 0 (for weak device)	1.2 V (SR enabled)
1	1	After 62 µs, 1 (for strong device)	1.05 V (SR enabled)

To enable SmartReflex, VADJEN must be pulled high using an external resistor. This state is latched into the BOOTCFG register (VADJEN bit) when reset is released ($\overline{\text{RESET}}$'s rising edge). The CVDDADJ0 and CVDDADJ1 pins are configured as SmartReflex control outputs and control the adjustable power supply to obtain the desired core voltage level for the device.

Immediately following release of $\overline{\text{RESET}}$, there is a 62 µs invalid period during which pulses will be present on the CVDDADJ[1:0] pins. The pattern of pulses will be consistent for a single device, but the pattern may vary from one device to another. Such a waveform for a strong device is shown in Figure 3.

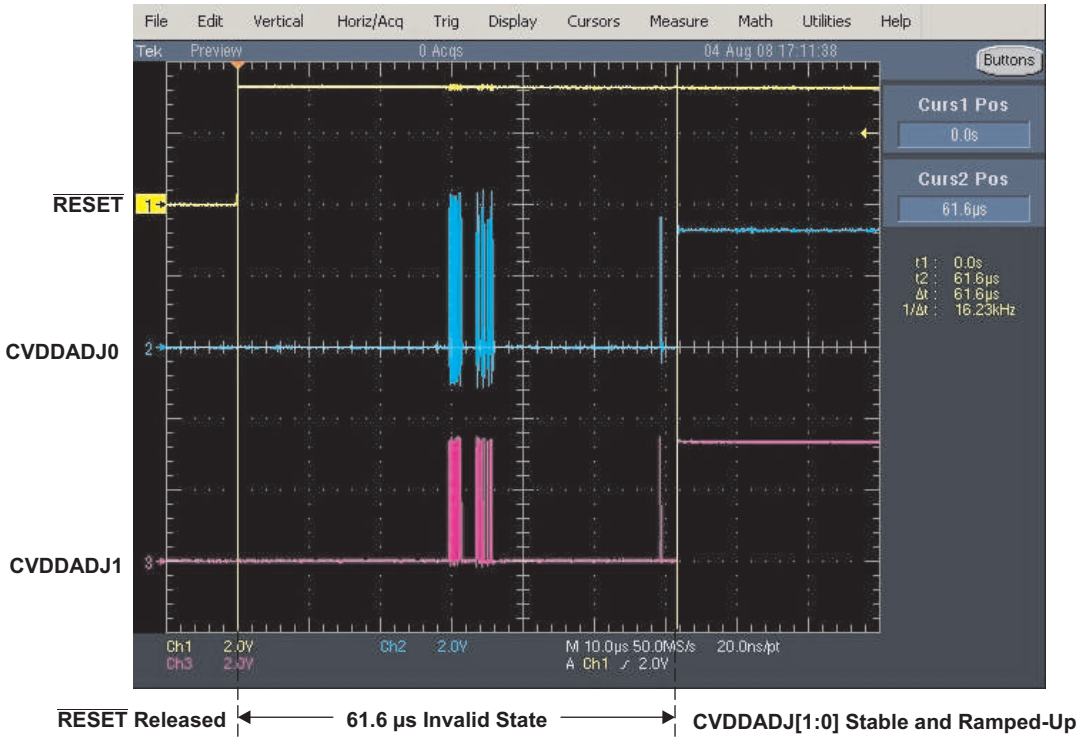

Figure 3. Behavior of CVDDADJ[1:0] Following the Release of $\overline{\text{RESET}}$

For a weak device, if the core voltage drops below 1.14 V (1.2 V (100% – 5%)), the device might fail to initialize properly. However, if the pulses are not handled carefully during the *invalid state*, they might accidentally cause the power supply to output a voltage that is below 1.14 V. It is critical to maintain the output above 1.14 V during this state. Therefore, the power supply solution must be designed to eliminate the impact of the *invalid state* period by either masking out any pulses on CVDDADJ[1:0] with timing logic or by using a filter to smooth out any pulses on these pins to avoid unexpected voltage. Since the actual pattern of pulses cannot be known before the board is built, the safest way to eliminate the impact of the *invalid state* period is to use a one-shot pulse to gate out the CVDDADJ[1:0] pulses during this period. During the pulse, the output of the adjustable power supply will stay at 1.2 V; the output will not be changed until the gating pulse is over.

Once the *invalid state* period has ended, CVDDADJ[1:0] outputs become stable. For a strong device, as soon as the *gating* pulse is over, the CVDDADJ[1:0] value becomes '11', which drives the adjustable power supply to output 1.05 V.

3 DM6467 SmartReflex Class-0 Reference Design

Two reference designs for the adjustable power supply for SR Class-0 are included in this section.

3.1 Reference Design I

Figure 4 shows a simple design for the voltage control on the 1.2 V core power rail. Figure 5 shows the complete power solution for the whole device (1.2 V, 1.8 V, and 3.3 V). This reference design is a straightforward circuit that can be implemented if cost is not a critical concern. The overall cost of the circuit in Figure 5 is less than $30 USD; and the cost for the 1.2 V core power supply circuit in Figure 4 is less than $18 USD. The *pulse gating* logic, which is not yet included in this system, is still being worked on and will be included in the next revision of the document. For more information on Reference Design I, contact http://support.ti.com.

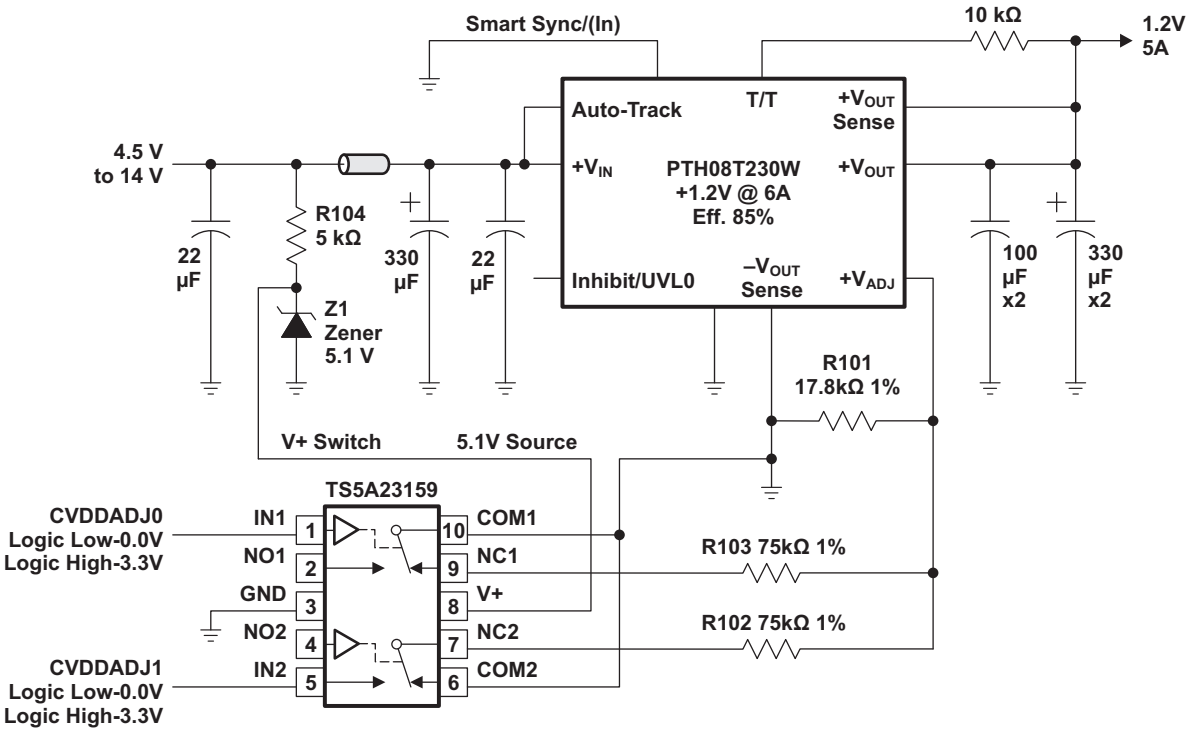

Figure 4. SR Power Supply Reference Design (Core)

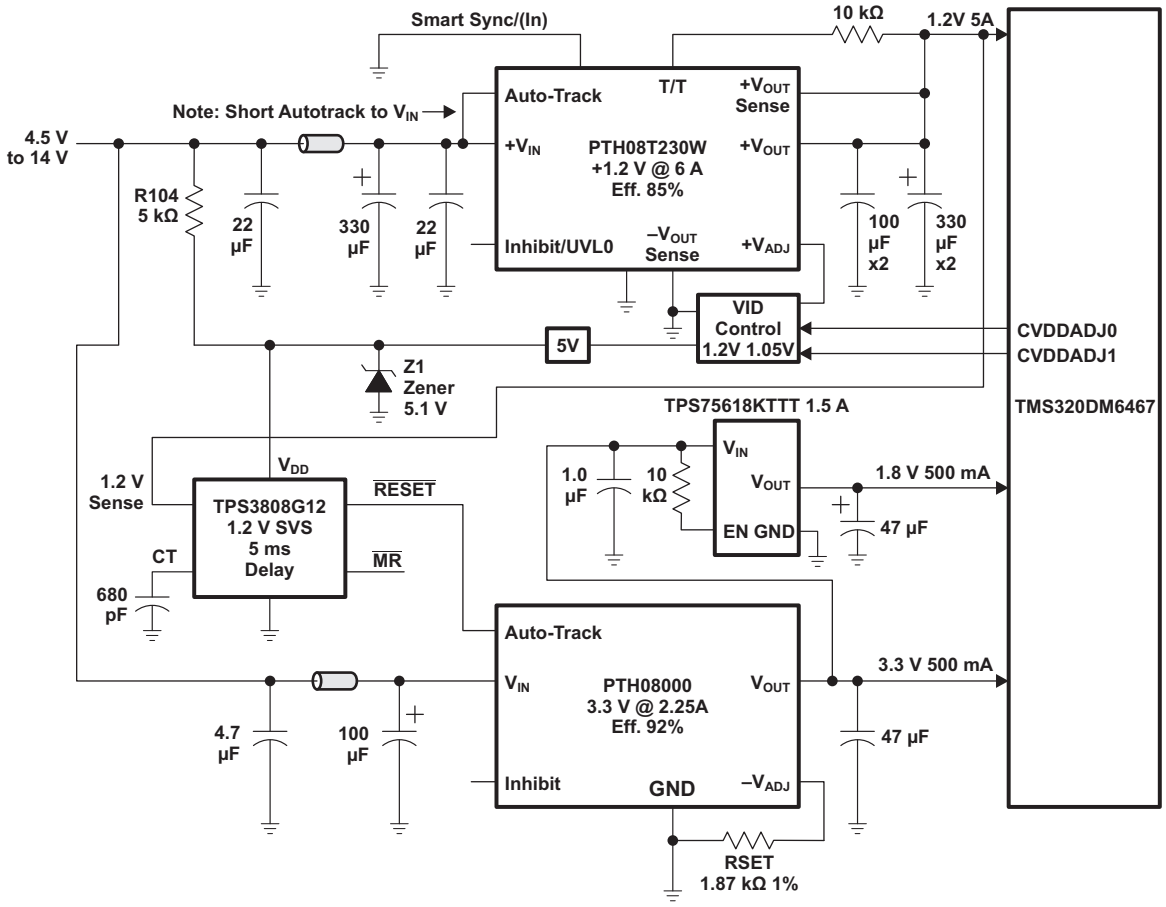

Figure 5. SR Power Supply Reference Design (Complete System)

3.2 Reference Design II

Figure 6 shows another power solution for the 1.2 V power rail with *pulse gating* logic. The design in Figure 6 is a cost effective design (the cost of the circuit is less than $4 USD) that can be used for mass production. However, it is more complicated than Reference Design I in Figure 4. In this design, only CVDDADJ0 is used to control the output; however it can be replaced with CVDDADJ1 as these two pins have identical functionality when SR is enabled. The *pulse gating* logic in this design gates out CVDDADJ0 up to 120 µs after both $\overline{\text{RESET}}$ and $\overline{\text{POR}}$ are released. For more information on Reference Design II, contact http://support.ti.com.

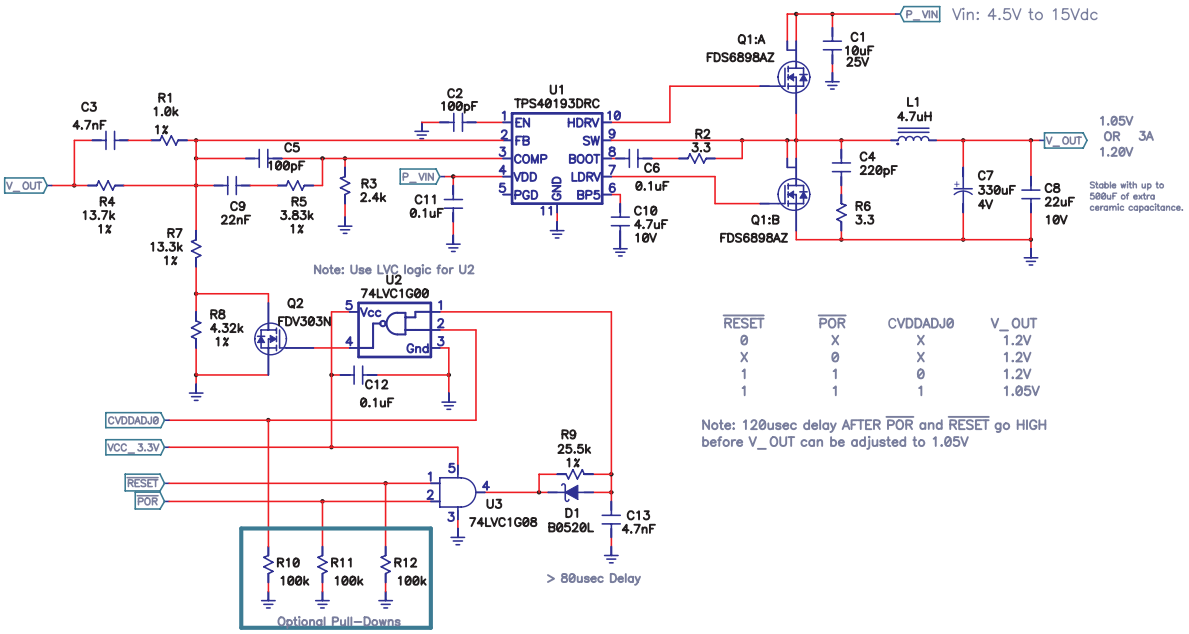

Figure 6. SR Power Supply Reference Design With Pulse Gating (Core)

4 References

- *TMS320DM6467 Power Consumption Summary* (SPRAAS2)
- *TMS320DM6467 Digital Media System-on-Chip Data Manual* (SPRS403)

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