Controlling switch-node ringing in synchronous buck converters

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Introduction

As power-supply efficiency becomes more important, faster switching speeds are necessary to reduce the losses. However, as switching speeds are increased, there are negative trade-offs that must be taken into account, such as a consequential increase in electromagnetic interference (EMI).

In a synchronous buck converter, fast-switching field-effect transistors (FETs) can experience significant voltage overshoots and ringing on the switch node. The magnitude of the ringing is a function of the high-side MOSFET's switching speed and the stray inductances in the layout and FET package. Proper techniques for circuit and layout design must be observed to keep the ringing below the absolute maximum rating of the synchronous FET.

This article focuses on three circuit designs that control switch-node ringing with either a boot resistor, a high-side gate resistor, or a snubber. Data is presented for each approach, and the benefits of each are also discussed. These techniques can be nullified by poor power-supply layout, so it is important to take this into consideration as well. Please see Reference 1 for more information about layout.

Ringing caused by synchronous buck converter's parasitics

The circuit in Figure 1 shows the power-stage components for a synchronous buck converter. Included in this model are the parasitic inductances and capacitances responsible for switch-node ringing.

Assume that the converter is in steady state. During the portion of the switching cycle when the low-side FET is on, the power to the load is being provided only from the output inductance and capacitance. At this point, energy is being stored in the parasitic inductances of the low-side FET relative to $E = \frac{1}{2}L \times I^2$. At the end of the switching

Figure 1. Schematic showing parasitics of a buck converter
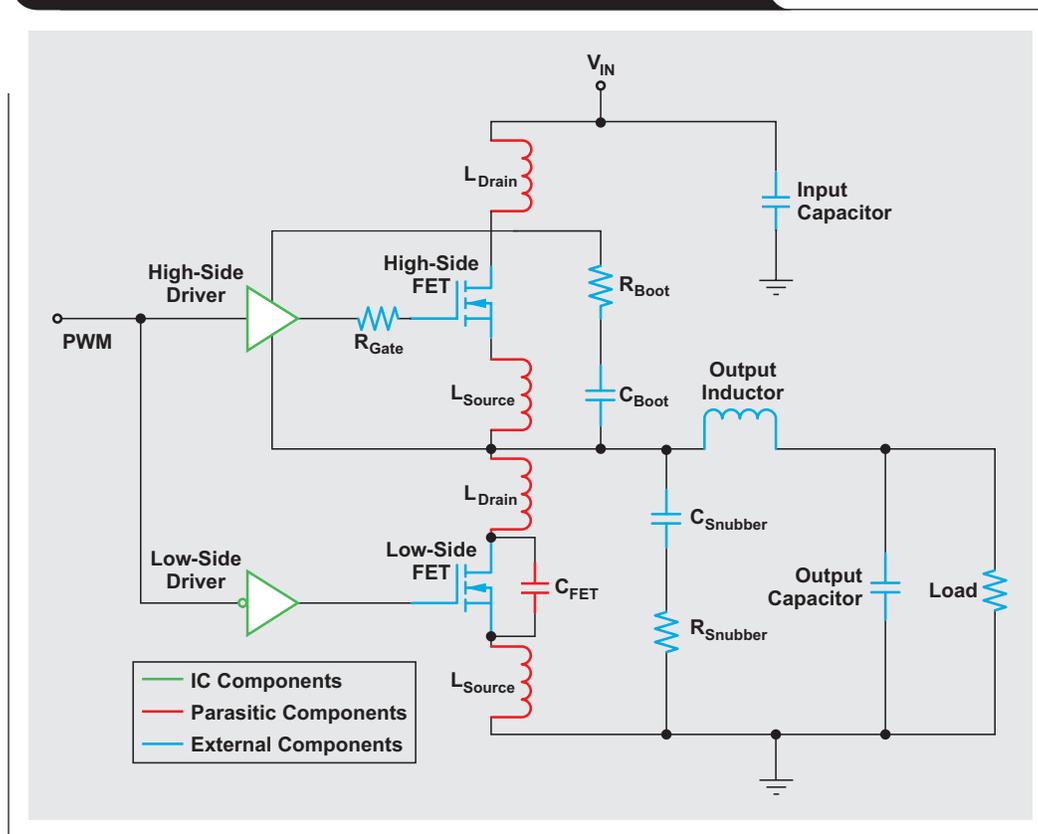
cycle, the converter prepares to switch the low-side FET off and the high-side FET back on to replenish power to the output L.

Strong gate drivers and a fast-switching FET allow the low-side FET to be turned off quickly. Assuming load conditions are sufficient to keep the inductor current flowing to the output, current is bypassed to the body diode of the low-side FET, and energy remains in the parasitic drain and source inductances of the low-side FET. After a fixed dead time, the high-side FET turns on, and the energy from the low-side and high-side FETs' parasitic inductances appears as an LC ringing waveform on the switch node.

The voltage magnitude of this ringing can exceed the absolute maximum drain-to-source voltage of the low-side MOSFET. Fast-switching MOSFETs such as the Texas Instruments (TI) CSD87350Q5D incorporate a stacked MOSFET pair that limits the parasitic inductances through innovative packaging techniques.

Reducing ringing

A test circuit with a 1.1-V/20-A buck converter was used to show the effects of switch-node ringing. This circuit used the TI TPS40304 600-kHz buck controller and the CSD87350Q5D fast-switching NexFET™ power block. The input-voltage range was 8 to 16 V. As a baseline reference, a switch-node waveform (Figure 2) and an efficiency plot (Figure 3) were generated without a boot resistor, high-side gate resistor, or snubber connected. The peak ringing with a 12-V input was 23.4 V. The efficiency at maximum load was 87.2%.

The boot resistor, high-side gate resistor, and snubber were optimized to reduce the overshoot to less than 20 V. This overshoot limit provided some margin to protect the FET, which had a 30-V maximum voltage rating. Figure 2 shows the overshoot for the baseline circuit and the reduced-ringing overshoot for the boot resistor, gate resistor, and snubber. The waveform for the gate resistor is very similar to that of the boot resistor. It is important to notice that only the magnitude of the ringing was affected by the boot-resistor and gate-resistor methods. The snubber method also changed the ringing frequency and damped out the ringing waveform. Figure 3 shows the measured efficiency for each of these conditions.

Figure 2. Waveforms of switch-node ringing with 12-V input

(a) Baseline ringing (5 V/div)

(b) Ringing with boot resistor (5 V/div)

(c) Ringing with high-side gate resistor (5 V/div)

(d) Ringing with snubber (5 V/div)
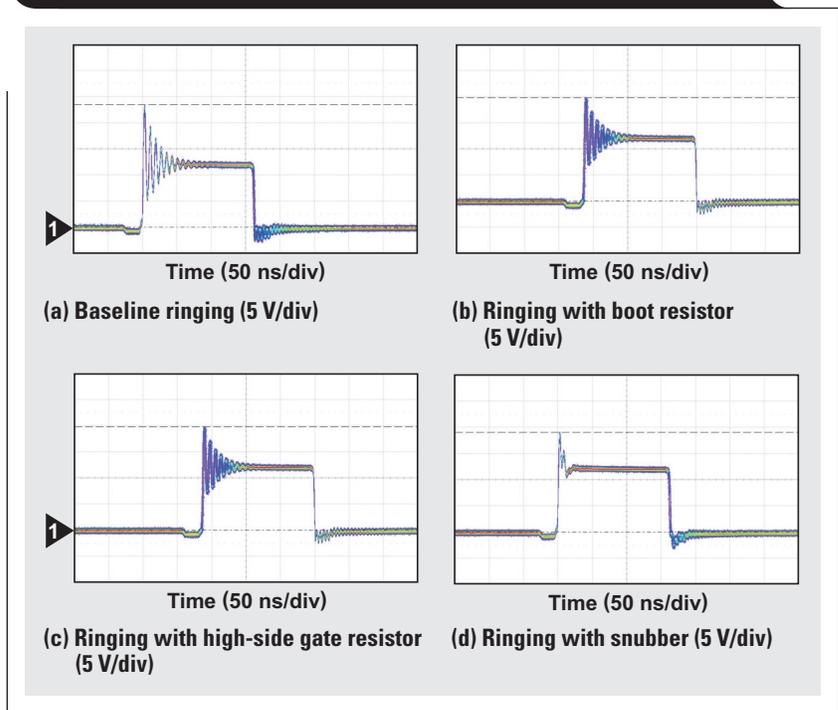
Using a boot resistor

The charge-pump circuit in Figure 1 uses C_{Boot} to boost the high-side gate supply above the supply voltage of the power stage. One way to reduce ringing is to include a boot resistor in series with the boot capacitor, which slows down the turn-on of the high-side FET. This allows more time for the parasitic network to discharge, ultimately limiting the ringing. The value of the boot resistor is determined by starting at 0 Ω and increasing the resistance until the desired ringing is achieved. To reduce the ringing for this design to below 20 V, a 6.8-Ω boot resistor was

Figure 3. Efficiency versus load current
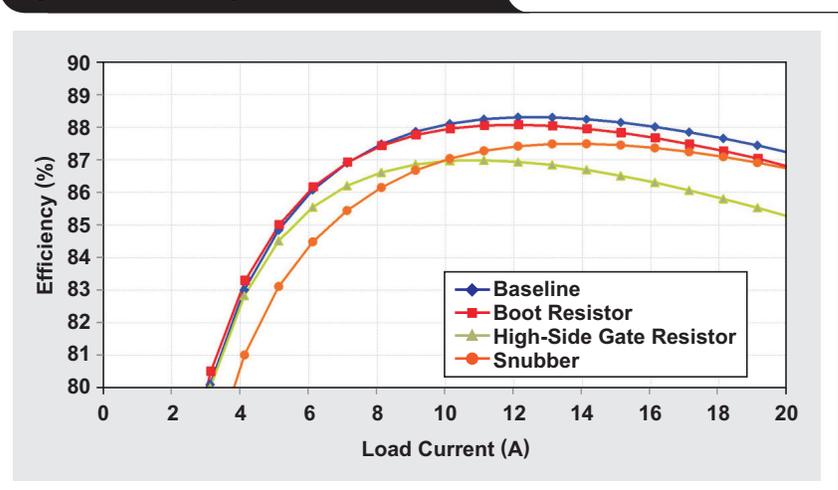
Table 1. Test data for three methods of reducing ringing

METHOD	RINGING (V)			FULL-LOAD EFFICIENCY (%)		
	$V_{IN} = 8\ V$	$V_{IN} = 12\ V$	$V_{IN} = 16\ V$	$V_{IN} = 8\ V$	$V_{IN} = 12\ V$	$V_{IN} = 16\ V$
Baseline	18.0	23.4	28.3	88.3	87.2	85.4
Boot Resistor	15.9	19.8	22.6	88.1	86.8	85.1
Gate Resistor	15.4	19.8	23.2	87.1	85.2	83.1
Snubber	14.2	19.1	23.7	88.1	86.7	84.7

required. It is interesting to note that the boot resistor affects only the turn-on of the high-side FET, making this method an efficient way to reduce ringing. However, if the boot resistor is made too large, the boot capacitor may not get fully charged in each cycle. In this case, the gate driver would not have sufficient voltage to keep the high-side FET on and could turn off in the middle of the cycle. This limits the amount of ringing that can be reduced with the boot-resistor method.

Using a high-side gate resistor

Using a resistor in series with the gate of the high-side FET is another effective way to reduce ringing. Similar to the boot-resistor method, this resistor slows down the turn-on of the high-side FET. However, because this resistor is in series with the gate, it is also in the discharge path, so it slows down the turn-off as well. To reduce the ringing for this design to below 20 V, a 6.8-Ω gate resistor was used. This method is the least efficient of the three choices.

Using a snubber

The third option to consider for reducing ringing is a snubber. The snubber circuit consists of a resistor and capacitor that are connected in series from the switch node to ground. The snubber circuit is used to damp the parasitic inductances and capacitances during the switching transitions. This circuit reduces the ringing voltage and frequency and also reduces the number of ringing cycles. This helps to reduce the EMI emitted by the system.

The procedure for choosing the capacitor and resistor components starts with measuring the ringing frequency of the original circuit. Once the frequency is determined, a capacitor is put in parallel with the low-side FET to change the ringing frequency to half the original value. When the frequency is half the original value, the parallel capacitor is equal to three times the parasitic capacitance of the original circuit. With the capacitance and frequency known, the parasitic inductance can be calculated by using the formula $f = \frac{1}{2}\pi\sqrt{LC}$, where f is the original ringing frequency and C is the parasitic capacitance. The resistor to critically damp the circuit is calculated from the equation $R = \sqrt{L/C}$. This resistor may or may not provide the necessary ringing reduction. Increasing the resistance results in an underdamped system, which allows more ringing but decreases power dissipation. Increasing the capacitance reduces the ringing but increases power dissipation. For the example, using a 2200-pF capacitor and a 1-Ω resistor reduced ringing to 19.1 V.

Conclusion

As MOSFET switching speeds continue to increase, controlling the switch-node ringing of a synchronous buck converter is critical. Doing so requires a good layout and proper analog-circuit design with a boot resistor, a high-side gate resistor, or a snubber. Table 1 shows the amount of ringing reduction achieved with the test circuit and the corresponding efficiency for each technique.

The boot resistor slows down the turn-on of the high-side FET without affecting the turn-off. In the design example, the boot resistor was the most efficient approach. However, if this method is used, proper care must be taken to prevent starving the gate. A resistor in series with the gate increases both the turn-on and turn-off times of the high-side MOSFET, which controls ringing on the rise and fall of the switch node. This approach burns the most power in the upper FET, reducing efficiency. An RC snubber reduces the frequency and overshoot of ringing, but it requires two extra components and has low efficiency at light loads.

Every power-supply design is unique, so each method should be inspected for its cost/benefit to the supply. Often, the best approach may even be a combination of all three circuits. The ultimate goal is to maintain a sufficient margin below the MOSFET's absolute maximum voltage rating while maintaining as much efficiency in the power stage as possible.

Reference

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Document Title   **TI Lit. #**

1. Robert Kollmann, "Constructing your power supply — layout considerations," 2004–05 TI Unitrode Design Seminar Series – SEM1600, Topic 4 . . . . SLUP230

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