TPS7A47xxEVM-094 Evaluation Module

This user's guide describes the functional operation of the TPS7A47xxEVM-094 Evaluation Module (EVM) for use as a design reference and as a general engineering demonstration for the TPS7A47xx low dropout linear (LDO) regulator. Included in this User's Guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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1 Introduction

This EVM is designed to help engineers evaluate the operation and performance of the TPS7A47xx linear regulator for possible use in their own circuit application. Notable features of this LDO regulator include thermal and current limit shutdown protection, pin selectable output voltage, low dropout, and low noise (~3.5 µV / $\sqrt{Hz}$). The EVM contains a single linear regulator in a 5 mm × 5 mm, QFN (RGW), thermally enhanced (PowerPad™) package. This regulator, including external components, is capable of delivering up to 1.0 A to a dynamic load across the full recommended input and output voltage range of the LDO. A multi-pin header with jumpers is provided to enable easy manual selection of the output voltage.

PowerPad is a trademark of Texas Instruments.

2 Setup

This section describes the connectors and headers on the EVM as well as how to properly connect, setup and use the TPS7A47xxEVM-094. See the assembly layer diagram, Figure 5, for the location and orientation of referenced components.

2.1 Input/Output Connector-Headers and Jumper Descriptions

- J1 V_{IN} – Positive (+) input power supply voltage test and measurement header
- J2 GND – Ground and measurement header
- J3 V_{OUT} – Regulator output (up to 1 A)
- J4 GND – Ground return from the load (up to 1 A)
- J5 (S+) – V_{OUT}, Kelvin connection V_{OUT}
- J5 (S–) – GRD, Kelvin connection Ground
- J6 and J7 – Extra GRD connections
- J8 – Enable jumper for external resistor divider
- J9 – Enable jumper for the EVM
- J10 – Header for selecting the appropriate output voltage

NOTE: The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI and source inductance. Additional bulk capacitance in the form of a Tantalum cap (47 µF; 35 V) has been added to the EVM at C1 to counter source inductances that may cause ringing on the load transient waveform during higher current transients. This bulk capacitance should not be necessary in a typical application circuit.

Output Voltage Set Note: Set the output voltage by connecting J10 header pins, each assigned to a given voltage level, to ground where $V_{OUT} = V_{REF}$ + (Sum of the jumper voltages). J10 header pins are numbered sequentially, odd pins (1, 3, 5...15) ascending leftward of pin 1 on the top row. All odd pins are connected to ground. Each even pin is numbered right to left sequentially (2, 4, 6…16) on the bottom row and each even pin is assigned a unique voltage level. See the pin-to-pin output voltage assignments in Table 1.

Table 1. J10 Jumper Voltages

$V_{OUT} = V_{REF}$ (1) + Sum of Voltage Levels		
Voltage Level	**Voltage Set Pins**	**Ground Pins**
100 mV	16	15
200 mV	14	13
400 mV	12	11
800 mV	10	9
1.6 V	8	7
3.2 V	6	5
6.4 V	4	3
6.4 V	2	1

(1) See the data sheet for V_{REF} value. Publication: SBVS204

Example: Set V_{OUT} to 3.0 V by connecting a shorting jumper from pin 8 to pin 7.

$V_{OUT} = V_{REF} + 1.6\ V = 3.0\ V$

2.2 Soldering Guidelines

Any solder rework to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC).

2.3 Initial Setup and Equipment Interconnect

- Select the desired V_{OUT} by programming the output voltage according to the instructions listed above in the ***Output Voltage Set Note in Section 2.1***.
- Disable the EVM by adding a shorting jumper to J9 from EN (Pin 2) to OFF (Pin3).
- Before connecting the input power supply to the EVM, verify that the output voltage is set to the desired supply voltage (+3 V to +35 V range) and that it is current limited to 2 A. With the input power supply turned off, connect the positive voltage lead (+) from the power supply to V_{IN} (J1, Pin 1) of the EVM. Next, connect the ground lead (-) from the power supply to GND (J2, Pin 1).
- Connect a 0- to 1-A load between V_{OUT} (J3, Pin 1) and GND (J4, Pin 1).

3 Operation

1. Turn on the input power supply and verify that the output voltage, V_{OUT}, is near 0 V.
2. Enable the output by reconnecting the jumper on J9 to short the EN (Pin 2) to the ON (Pin 1).
3. Vary the load current and V_{IN} voltage as necessary for test purposes.

NOTE: **Note:** Power dissipation (P_{DISP}) across the TPS7A47xx is dependent on the V_{IN} to V_{OUT} voltage drop and the output load current, I_{Load} ($P_{DISP} = (V_{IN} – V_{OUT}) \times I_{Load}$). If the power dissipation is high, the output voltage may continuously transition on-off-on, due to the shutdown effect of the thermal limit shutdown circuit.

4 Test Results

This section provides typical performance waveforms for the EVM, characteristic of this design.

4.1 Turn On Characteristic

Figure 1 shows the V_{OUT} ramp-up waveform at turn-on (ENable) as well as the input surge current into the IN pin of the LDO itself when the LDO starts-up into a fully loaded output.

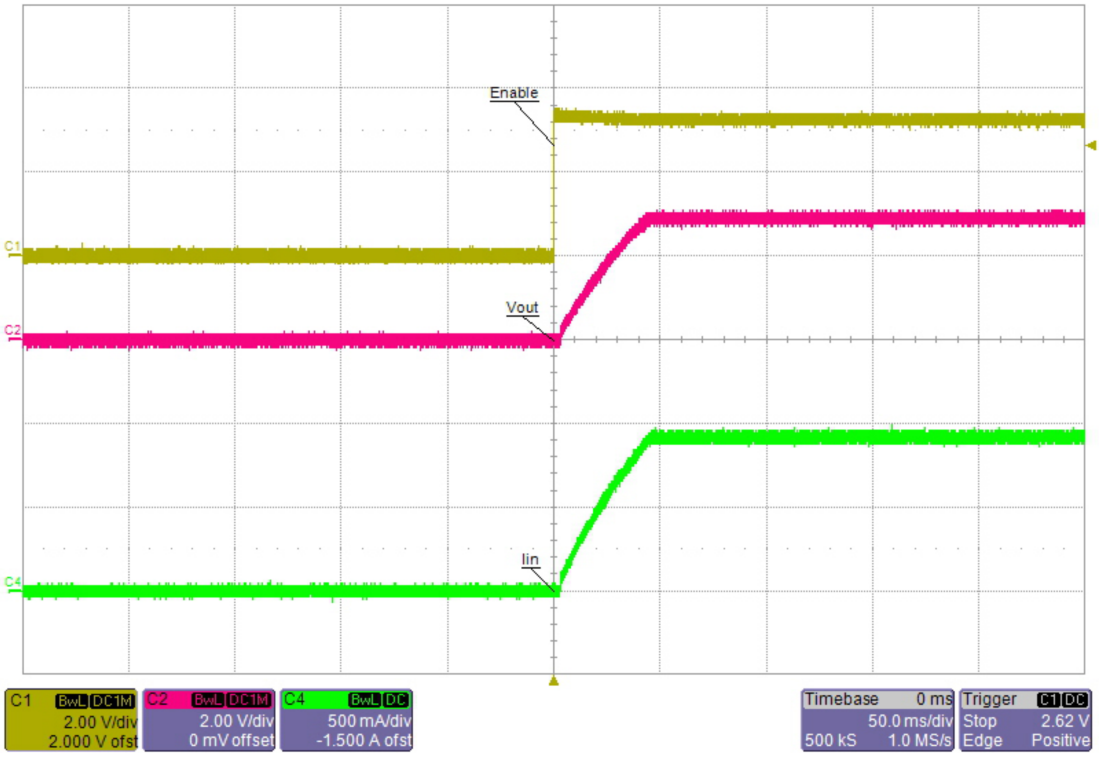

Figure 1. Turn On Sequence

4.2 Output Load Transient

Figure 2 shows the V_{OUT} transient response

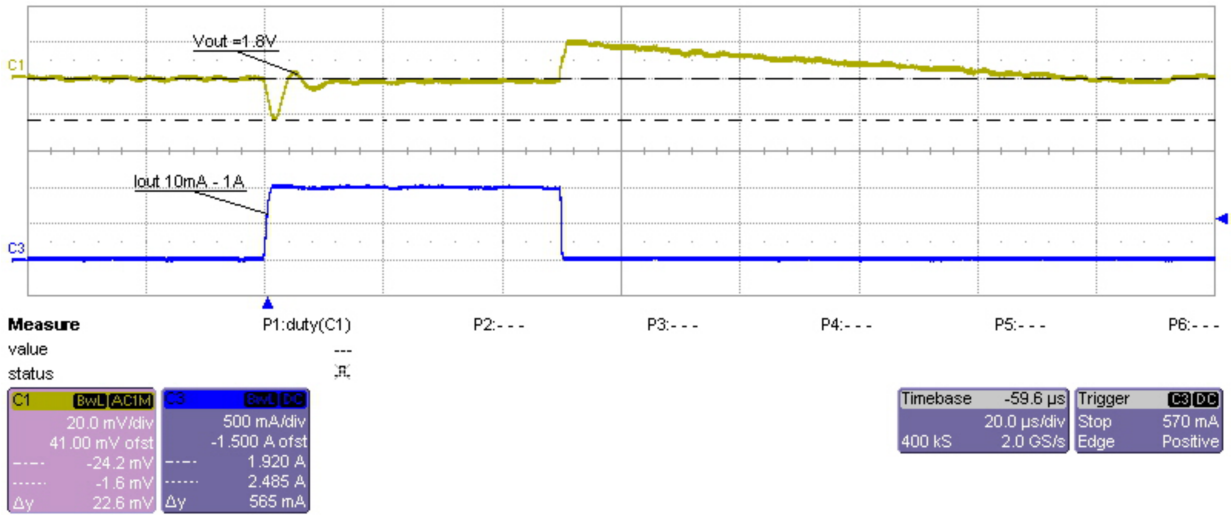

Figure 2. Step Load and Output Voltage Transient Response

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key consideration in the design of any dc-dc converter but is especially important for an LDO when the power dissipation is high. Use the equation below to approximate the worst case junction temperature for the application:

$$T_J = T_A + P_d \times \theta_{JA} \quad (1)$$

where T_J is the junction temperature (°C), T_A is the ambient temperature (°C), P_d is the power dissipation in the device (Watts), and θ_{JA} is the thermal resistance from junction to ambient (°C/W). The maximum silicon junction temperature should not be allowed to exceed 125°C for reliable operation. The layout design must use copper traces and plane areas smartly, as thermal sinks, so as to not allow T_J to exceed the absolute maximum rating under all load, voltage, and temperature conditions for a given application.

The layout should consider carefully the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 4 shows that the RGW package footprint employs a square thermal pad, centered under the part, for conducting heat to the copper spreading layers of the PCB. The thermal pad is soldered directly to a pad on the PCB containing a 5 × 5 pattern of 10.mil vias for conducting heat to the bottom side ground plane copper. Approximately 4.0 in^2 of 2 ounce copper is used on the bottom side of the EVM for dissipating heat generated by the LDO.

Table 2 relies on thermal resistance information from the thermal information table of the TPS7A47xx data sheet for comparison with the approximate thermal resistance, θ_{JA}, calculated for this EVM layout to show the variation in junction-ambient thermal resistances for varying copper areas. The High-K thermal resistance, θ_{JA}, is determined using a standard JEDEC high-k (2s2p) board having dimensions of 3 in × 3 in with two 1-ounce internal power and ground planes and one 2-ounce copper bottom plane for spreading/sinking heat from the IC component.

Table 2. Thermal Resistance, θ_{JA}, and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation without Derating (T_A = 25°C)	Max Dissipation without Derating (T_A = 70°C)
High-K	RGW	30.5°C/W	3.27 W	1.8 W
TPS7A47xxEVM-094	RGW	21°C/W	4.76 W	2.6 W

The thermal resistance for the TPS7A47xxEVM-094 is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package.

6 Board Layout

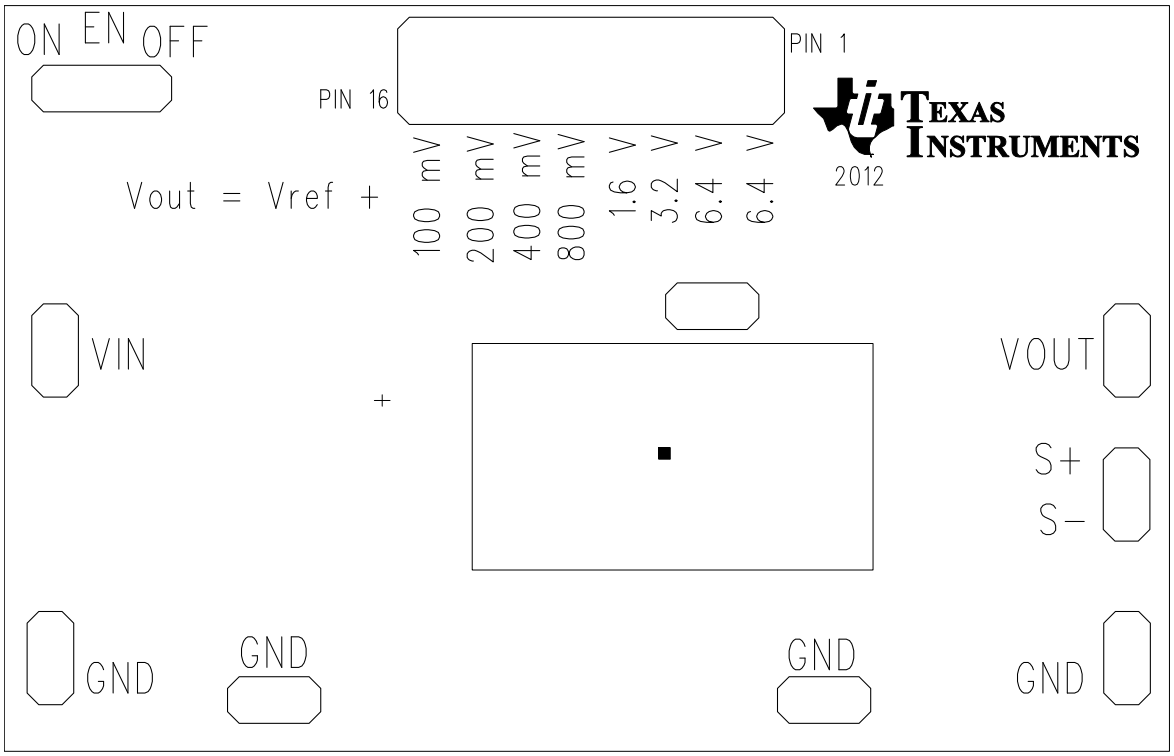

Figure 3. Assembly Layer

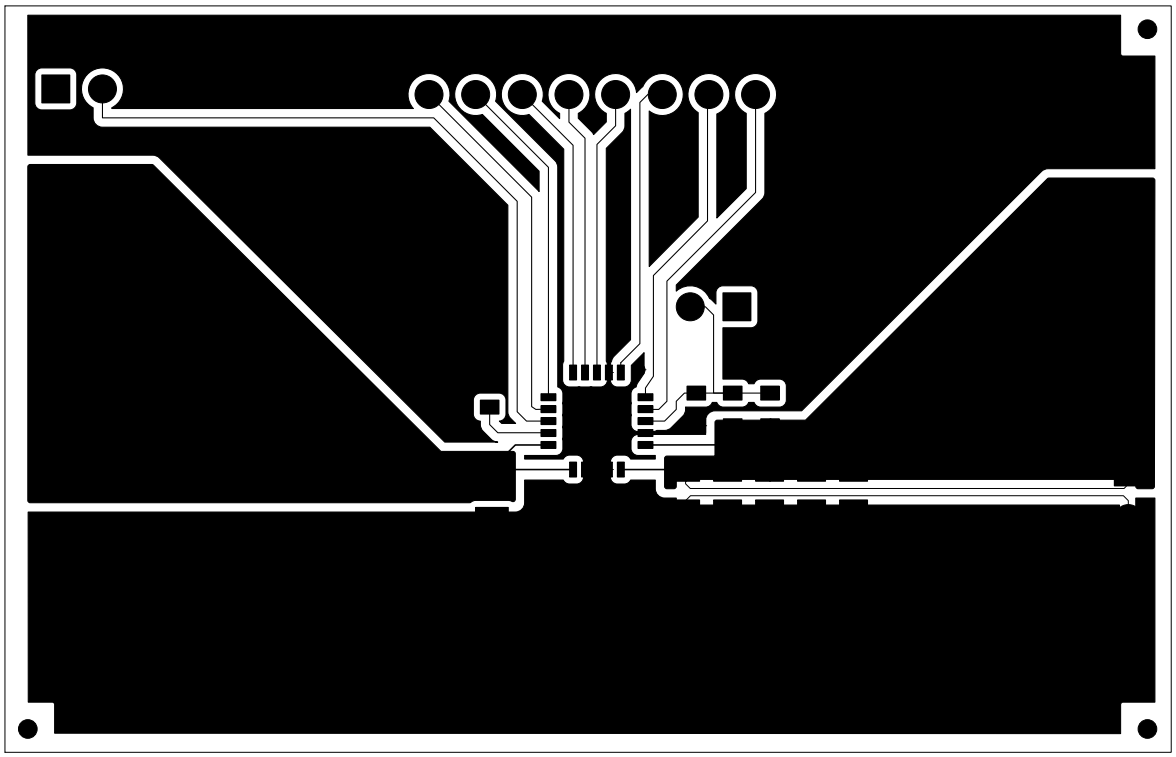

Figure 4. Top Layer Routing

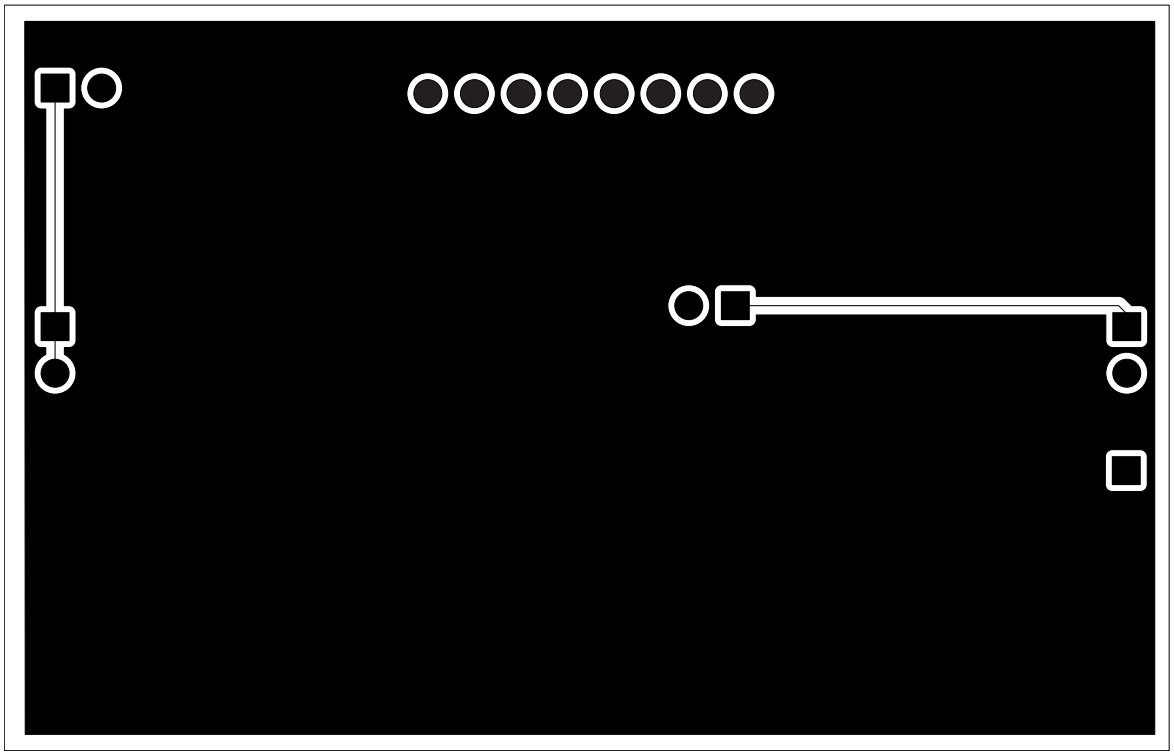

Figure 5. Bottom Layer Routing

7 Schematic and Bill of Materials

7.1 Schematic

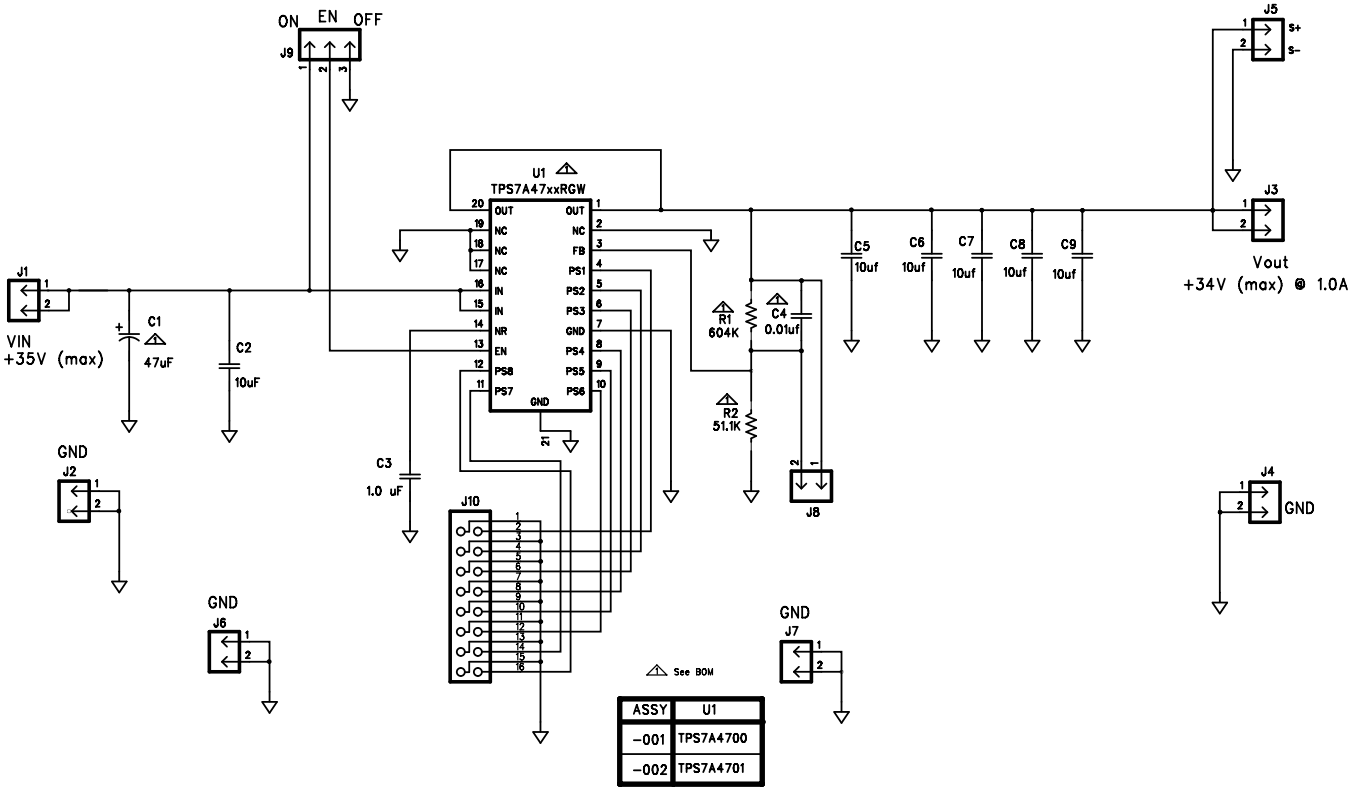

Figure 6. TPS7A47xxEVM-094 Schematic

7.2 Bill of Materials

Table 3. TPS7A47xxEVM-094 Bill of Materials

-001	-002						
COUNT	COUNT	RefDes	Value	Description	Size	Part Number	MFR
0	0	C1	47uF	Capacitor, Tantalum, 35V, X5R, 20%	7343	TAJE476M035RNJ	AVX
1	1	C2	10uF	Capacitor, Ceramic, 50V, X5R, 10%	1206	C3216X5R1H106K	TDK
1	1	C3	1.0 uF	Capacitor, Ceramic, 50V, X5R,10%	0603	C1608X5R1H105K080AB	TDK
0	1	C4	0.01uF	Capacitor, Ceramic, 25V, X7R,10%	0603	GRM188R71E103KA01D	Murata
5	5	C5-9	10uf	Capacitor, Ceramic, 35V, X5R,10%	0805	C2012X5R1V106K085AC	TDK
8	8	J1- J8	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	1	J9	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	1	J10	PEC08DAAN	Header, Male 2 x 8 pin, 100mil spacing	0.100 inch X 2 X 8	PEC08DAAN	Sullins
0	1	R1	604K	Resistor, Chip, 1/10W, 1%	0603	CRCW0603604KFKEA	Vishay-Dale
0	1	R2	51.1K	Resistor, Chip, 1/10W, 1%	0603	CRCW060351K1FKEA	Vishay-Dale
1	0	U1	TPS7A4700RGW	IC, Low Noise Power Solution For High Performance Signal Chain Applications	QFN-20	TPS7A4700RGW	TI
0	1	U1	TPS7A4701RGW	IC, Low Noise Power Solution For High Performance Signal Chain Applications	QFN-20	TPS7A4701RGW	TI
5	5			Shunt, Black	100-mil	929950-00	3M
1	1	--	PCB	PCB, 1.60 In x 2.50 In x 0.062 In	1.6 x 2.5 x0.062 in.	PWR094	Any
1		--		Label (See note 5)	1.25 x 0.25 inch	THT-13-457-10	Brady

	Notes:	1. These assemblies are ESD sensitive, ESD precautions shall be observed.
		2. These assemblies must be clean and free from flux and all contaminants. Do not use no clean flux.
		3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
		4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.
		5. Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per Table 1.

Table 1

Assembly Number	Text
PWR094-001	TPS7A4700EVM-094
PWR094-002	TPS7A4701EVM-094

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

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If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

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