Application Report
SLUAA31A–April 2020–Revised April 2020

BQ7718 Functional Safety FIT Rate, Failure Mode Distribution, and Pin FMA

Sandy Xu

1 Overview

This document contains information for BQ7718 DPJ and DGK packages to aid in a functional safety system design. Information provided is as follows:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

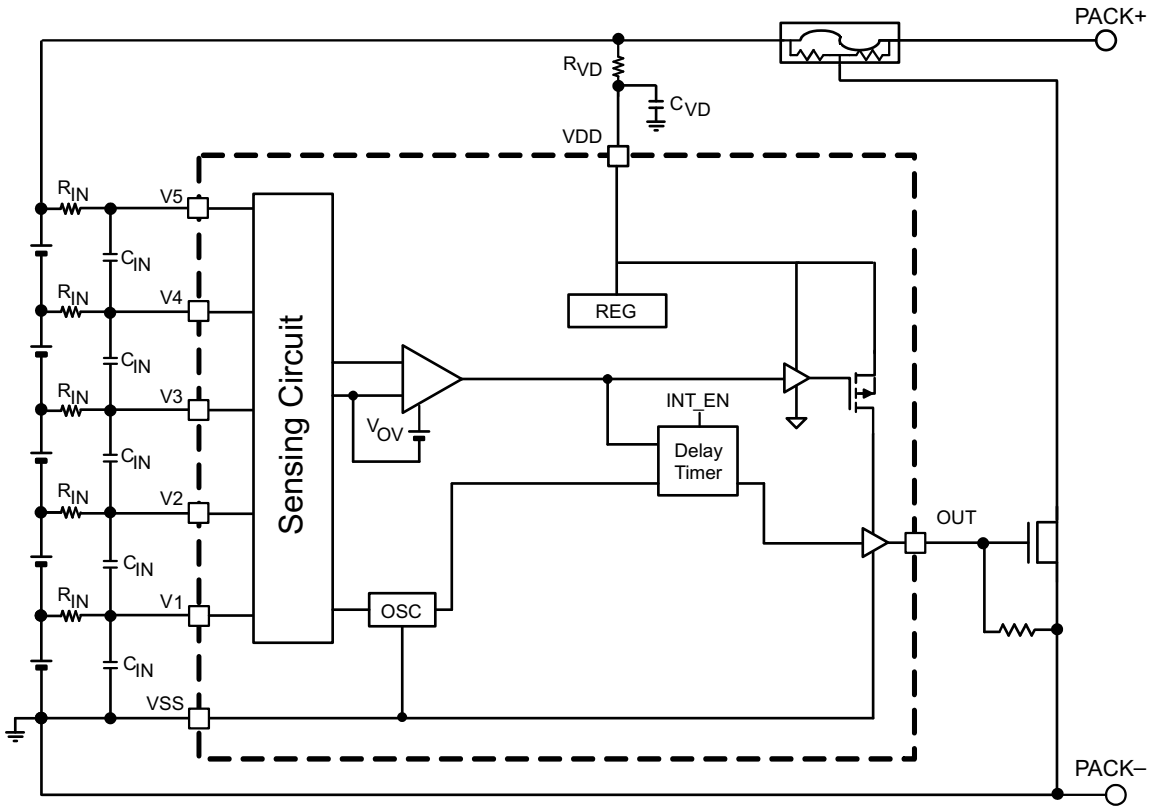

Figure 1. Functional Block Diagram

BQ7718 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DPJ Package

This section provides Functional Safety Failure In Time (FIT) rates for the DPJ package of BQ7718 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	8
Die FIT Rate	3
Package FIT Rate	5

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: TBD mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DGK Package

This section provides Functional Safety Failure In Time (FIT) rates for the DGK package of BQ7718 based on two different industry-wide used reliability standards:

- Table 3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.
- Table 4 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	8
Die FIT Rate	3
Package FIT Rate	5

The failure rate and mission profile information in Table 3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: TBD mW
- Climate type: World-wide Table 8

- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for BQ7718 in Table 5 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 5. Die Failure Modes and Distribution

Failure Modes	Failure Mode Distribution (%)
OUT fails to trip – stuck high	15%
OUT fails to trip – stuck low	15%
OUT open HIZ	5%
OUT functional out of specification timing or threshold	60%
Pin to Pin short any to pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the BQ7718 DPJ (and DGK package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 7 and Table 11)
- Pin open-circuited (see Table 8 and Table 12)
- Pin short-circuited to an adjacent pin (see Table 9 and Table 13)
- Pin short-circuited to supply (see Table 10 and Table 14)

Table 7 through Table 14 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 6.

Table 6. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- RC filter on every cell pin, Vx

4.1 DPJ Package

Figure 2 shows the BQ7718 pin diagram for the DPJ package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the BQ7718 datasheet.

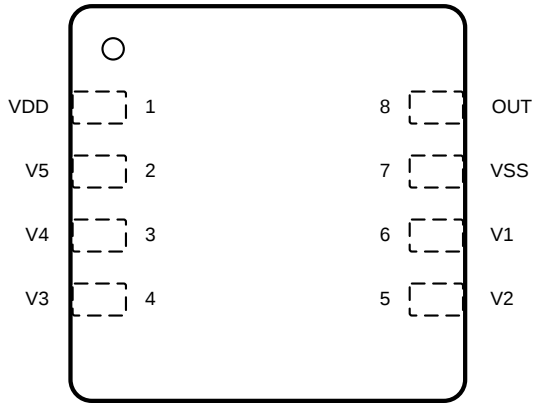

Figure 2. Pin Diagram DPJ (Package)

Table 7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power to part	B
V5	2	No OV detection on cell 5	B
V4	3	Automatic OV detection	D
V3	4	Automatic OV detection	D
V2	5	Automatic OV detection	D
V1	6	Automatic OV detection	D
VSS	7	Function as normal	D
OUT	8	No output signal to system	B

Table 8. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power to part	B
V5	2	No OV detection on cell 5	B
V4	3	Automatic OV detection	D
V3	4	Automatic OV detection	D
V2	5	Automatic OV detection	D
V1	6	Automatic OV detection	D
VSS	7	No power to part	B
OUT	8	No output signal to system	B

Table 9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	V5	Function as normal	D
V5	2	V4	No OV detection on Cell 5	B

Table 9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V4	3	V3	Automatic OV detection	D
V3	4	V2	Automatic OV detection	D
V2	5	V1	Automatic OV detection	D
V1	6	VSS	Automatic OV detection	D
VSS	7	OUT	No output signal to system	B
OUT	8	VDD	Automatic OV detection	D

Table 10. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Function as normal	D
V5	2	Function as normal	D
V4	3	Automatic OV detection	D
V3	4	Automatic OV detection	D
V2	5	Automatic OV detection	D
V1	6	Automatic OV detection	D
VSS	7	No power to part	B
OUT	8	Automatic OV detection	D

4.2 DGK Package

Figure 3 shows the BQ7718 pin diagram for the DGK package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the BQ7718 datasheet.

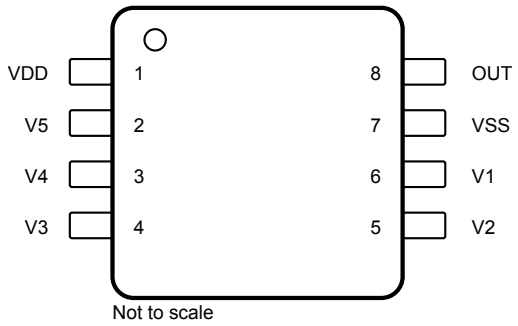

Figure 3. Pin Diagram DGK(Package)

Table 11. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power to part	B
V5	2	No OV detection on cell 5	B
V4	3	Automatic OV detection	D
V3	4	Automatic OV detection	D
V2	5	Automatic OV detection	D
V1	6	Automatic OV detection	D

Table 11. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VSS	7	Function as normal	D
OUT	8	No output signal to system	B

Table 12. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power to part	B
V5	2	No OV detection on cell 5.	B
V4	3	Automatic OV detection	D
V3	4	Automatic OV detection	D
V2	5	Automatic OV detection	D
V1	6	Automatic OV detection	D
VSS	7	No power to part	B
OUT	8	No output signal to system	B

Table 13. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	V5	Function as normal	D
V5	2	V4	No OV detection on cell 5	B
	3	V3	Automatic OV detection	D
V3	4	V2	Automatic OV detection	D
V2	5	V1	Automatic OV detection	D
V1	6	VSS	Automatic OV detection.	D
VSS	7	OUT	No output signal to system	B
OUT	8	VDD	Automatic OV detection	D

Table 14. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Function as normal	D
V5	2	Function as normal	D
V4	3	Automatic OV detection	D
V3	4	Automatic OV detection	D
V2	5	Automatic OV detection	D
V1	6	Automatic OV detection	D
VSS	7	No power to part	B
OUT	8	Automatic OV detection	D

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2020) to A Revision	Page
• Changed the title of the document	1

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265