High Speed Communications Solutions

TSW1000: ADS5500 and CDC7005 14-bit, 125 MSPS ADC Coupled with Low-Jitter Clock Distribution Device

Texas Instruments Offers a Leading-Edge Portfolio of High Speed Communications Solutions

Unleash the full potential of your device with Texas Instrument's Real World Signal Processing™ solutions by coupling the CDC7005 low-jitter clock synchronizer chip with the industry leading 14-bit ADS5500 ADC device.

TI introduces the TSW1000 evaluation module (EVM). This new EVM provides a complete solution for clocking the industry leading ADS5500 with the CDC7005 clock synchronizer. The ADS5500 is a 14-bit analog-to-digital converter (ADC) that can be clocked up to 125 MSPS and is capable of sampling IF frequencies up to 750 MHz. In addition, the CMOS architecture results in minimal power dissipation for high-efficiency applications.

The ADS5500 is designed for base station applications using high IF sampling, I/Q demodulation sampling, or digital predistortion feedback. The 14-bit resolution allows unprecedented sensitivity for high dynamic-range applications associated with 3G multi-carrier applications such as WCDMA, CDMA2K, GSM/EDGE and OFDM.

Key Features – ADS5500

- 14-bit resolution at 125 MSPS
- 780 mW power dissipation
- Single 3.3 V supply

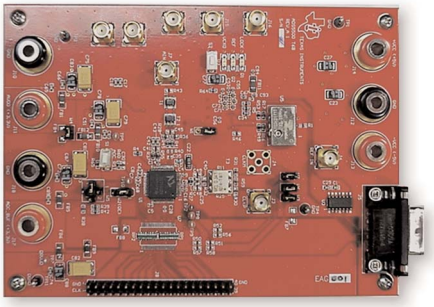
Key Features – CDC7005

- Jitter cleaner
- Five independent frequency outputs selectable by $/2^n$
- LVPECL interface
- Single 3.3 V supply

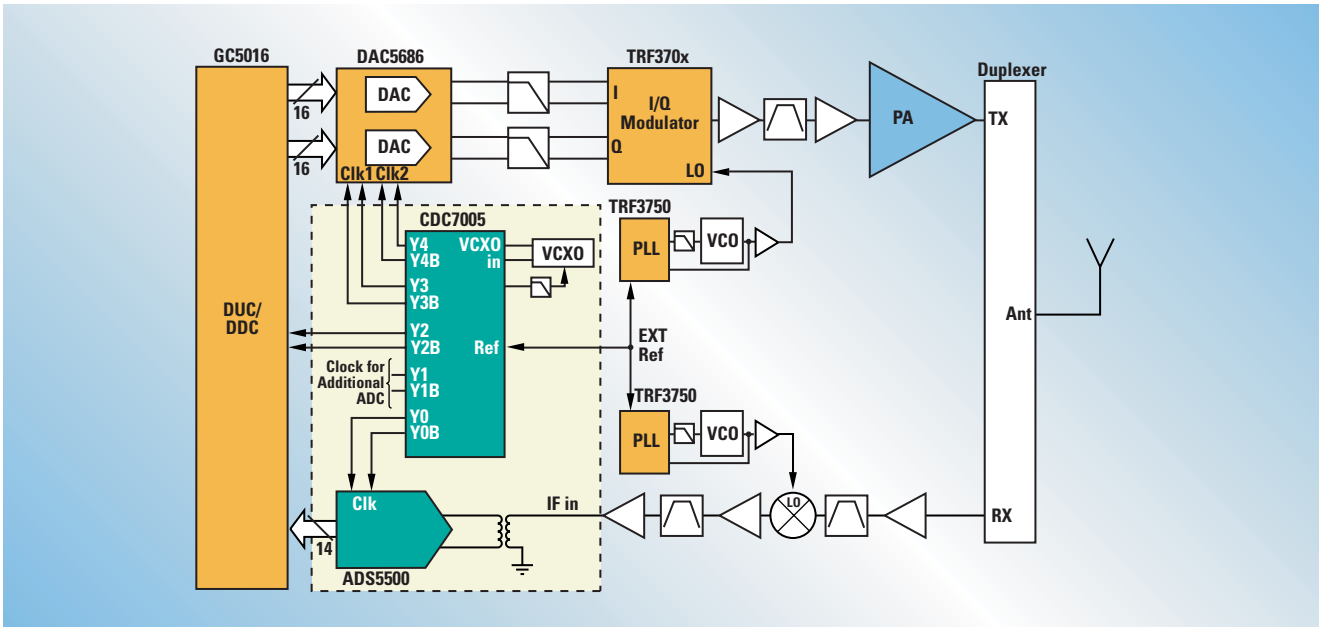
Applications

- Wireless base station receivers
- Digital predistortion feedback
- High IF direct sampling
- Medical imaging and monitoring
- Communication test equipment
- Digital imaging

TSW1000 Evaluation Module



TSW1000: ADS5500 and CDC7005 Solution as an Integral Part of the Transceiver

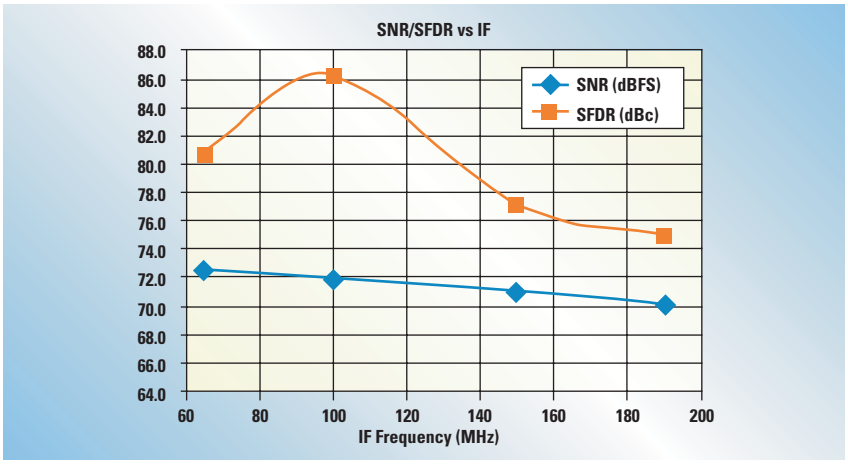


In order to achieve the full performance of the ADS5500, a suitable low-jitter clock is required at the desired sampling rate. The CDC7005 is a high performance, low-jitter clock solution that synchronizes an on-board voltage controlled crystal oscillator (VCXO) to an external reference clock. The CDC7005 has five independent outputs that can be used to satisfy the most stringent clocking requirements. Each output can be independently divided down by 2^n (n = 0 to 4) to supply the clock signal for a multitudinous of devices within the base station transceiver (BTS) including digital up and down converters (DUC/DDC), digital-to-analog converters (DAC), and other ADCs.

The TSW1000 EVM is equipped with a low-phase noise 122.88 MHz VCXO. The user is only required to provide the reference signal and proper programming. For operation within the first Nyquist zone, the CDC7005 can be directly interfaced to the ADC for excellent performance. For the more demanding high IF applications, the CDC7005 output is coupled with an amplifier and a narrow band pass filter.

With this modification, the CDC7005 supplies a suitable clock to achieve around 70 dBFS or better SNR up to 190 MHz. The EVM provides an on-board, real-world clocking solution and a convenient way to complete the evaluation of the ADS5500 for all of your BTS requirements to reduce your time-to-market.

For more information about the TSW1000, please visit us at **www.ti.com/hscsolutions**



TSW1000: SNR and SFDR Measurements Clocked at 122.88 MSPS with CDC7005 Plus Amp-BPF

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