Application Note

TAS6x84 Output Current and Voltage Measurement

Derek Gong

ABSTRACT

TI's digital input automotive Class-D audio amplifier, TAS6x84-Q1, supports the measurement of output current and voltage of each channel independently. The TAS6x84-Q1 transmits selected data through the serial audio output port, SDOUT, in either I2S mode or TDM mode. This application note provides an application guide of the measurement of output current and voltage predict.

Table of Contents

Trademarks

1 Introduction

During audio playback, TAS6x84-Q1 internal DSP can calculate output voltage of each channel according to audio input, supply voltage, analog gain, and digital gain setting. This voltage is defined as Vpredict, as this is a scaled signal of output signal level. The speaker impedance is not linear in audio band, so the output current is not fixed even though output voltage is same. The output current sense, Isense, is as scaled value of the actual current. The output current sense is monitored for each channel and reports the measurement to a host processor through SDOUT pin in either I^{2}S mode or TDM mode with minimal delay. Isense and Vpredict can be transmitted on SDOUT pin. The following data groups can be transmitted through SDOUT:

- **Isense Ch1-4** – Scaled Current Sense feedback per channel
- **Vpredict Ch1-4** – Scaled Output voltage estimate based on supply voltage and input signal by channel. Vpredict data is only available at 48kHz sampling frequency and not supported at 96kHz or 192kHz.
- **Aux Ch1-4** - Auxiliary data channels. For more details see the *Auxiliary Data Channels* section in the data sheet.

Each of the SDOUT pins can transmit only one device's measurement data. In a multi-device system, the SDOUT pins can be connected together to share one TDM line to save DSP/SOC pins and resources.

2 SDOUT Configuration

The SDOUT requires the serial audio port to operate in I^{2}S or TDM mode data formats. Left-justified and DSP mode formats are not supported. The audio input serial clock (SCLK) and audio frame clock (FSYNC) are reused, and the outgoing data on SDOUT has the same sampling frequency and maximum audio frame size as the audio input signal. The output format follows the audio input format. The data output configuration is mainly controlled by registers 0x25 and 0x31. If output data has a bit offset as SDIN, configure the optional 10-bit offset in registers 0x2C, 0x2D, 0x2E and 0x2F to avoid overlapping data.

Table 2-1 shows the registers tables for SDOUT with descriptions:

Table 2-1. Register 0x25 Register Descriptions

Bit	Field	Type	Reset	Description
7-4	SDOUT selection	R/W	0x1	These bits control the SDOUT output place on SDOUT1 line or SDOUT2 line. These bits are used in conjunction with reg_tx_sel and reg_i2s_chsel Non-TDM mode **0001: For output channel 1/2 in SDOUT1 line and channel 3/4 in SDOUT2 line; (reg_tx_sel=4'b0011)** 0010: For output channel 3/4 in SDOUT1 line and channel 1/2 in SDOUT2 line; (reg_tx_sel=4'b0011) TDM Mode 0000: SDOUT1 output Isense and Vpredict and Aux
3-2	I2S Word Length	R/W	0x2	I^{2}S Word Length These bits control output audio interface sample word lengths for channel 1/2 output in non-TDM mode and vpredict output channels in TDM mode. 00: 16 bits 01: 20 bits **10: 24 bits** 11: 32 bits

Table 2-1. Register 0x25 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	I2S Word Length	R/W	0x2	I²S Word Length These bits control output audio interface sample word lengths for channel 3/4 output in non-TDM mode and isense output channels in TDM mode. 00: 16 bits 01: 20 bits **10: 24 bits** 11: 32 bits

Table 2-2. Register 0x31 Register Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	
5-4	reg_i2s_chsel	R/W	0x0	Select output which channel group in non-TDM mode for SDOUT output, need to set reg_i2s_shift5/6 and reg_word_length5/6 to corresponding channel's shift and length. **00: vpredict ch1/2/3/4;** 01: isense ch1/2/3/4; 10: auxiliary channels group1(aux 1/2/3/4);
3-0	reg_tx_sel	R/W	0x0	Enable or disable the output data channel **0000: Disable all the output data channels** xxx1: Enable Vpredict Ch1/2/3/4 output xx1x: Enable Isense Ch1/2/3/4 output x1xx: Enable Aux Ch1/2/3/4 output In non-TDM mode, if user needs to output 4 channels, 4'b0011 needs to be set

Table 2-3. Register 0x2C Register Descriptions

Bit	Field	Type	Reset	Description
7-6	reg_Vpredict _shift5_msb	R/W	0x3	Vpredict shift offset MSB, work with register 0x2D(LSB)
5-4	reg_Isense_ shift6_msb	R/W	0x0	Isense shift offset MSB, work with register 0x2E(LSB)
3-2	reg_Aux_ shift7_msb	R/W	0x3	Aux shift offset MSB, work with register 0x2F(LSB)
1-0	RESERVED	R/W	0x3	Reserved

Table 2-4. Register 0x2D Register Descriptions

Bit	Field	Type	Reset	Description
7-0	reg_Vpredict _shift5_lsb	R/W	0xFF	**Vpredict shift offset LSB, work with register 0x2C(MSB)** These bits control the offset of audio data in the audio frame for **output**. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio. reg_ Vpredict_shift5 = {reg_Vpredict_shift5_msb, reg_Vpredict_shift5_lsb}; reg_ Vpredict_shift5 controls the offset in **Vpredict** ch1/2/3/4 path. 0000000000: offset = 0 BCK (no offset) 0000000001: offset = 1 BCK 0000000010: offset = 2 BCKs ... **1111111111: offset = 1023 BCKs**

Table 2-5. Register 0x2E Register Descriptions

Bit	Field	Type	Reset	Description
7-0	reg_Isense _shift6_lsb	R/W	0xFF	**Isense shift offset LSB, work with register 0x2C(MSB)** These bits control the offset of audio data in the audio frame for **output**. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio. reg_Isense_shift6 = {reg_Isense_shift6_msb, reg_Isense_shift6_lsb}; reg_Isense_shift6 controls the offset in **Isense** ch1/2/3/4 path. 0000000000: offset = 0 BCK (no offset) 0000000001: offset = 1 BCK 0000000010: offset = 2 BCKs ... **1111111111: offset = 1023 BCKs**

Table 2-6. Register 0x2F Register Descriptions

Bit	Field	Type	Reset	Description
7-0	reg_Aux _shift7_lsb	R/W	0xFF	**Aux shift offset LSB, work with register 0x2C(MSB)** These bits control the offset of audio data in the audio frame for **output**. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio. reg_ Aux_shift7 = {reg_ Aux_shift7_msb, reg_ Aux_shift7_lsb}; reg_ Aux_shift7 controls the offset in **Aux** ch1/2/3/4 path. 0000000000: offset = 0 BCK (no offset) 0000000001: offset = 1 BCK 0000000010: offset = 2 BCKs ... **1111111111: offset = 1023 BCKs**

2.1 SDOUT – I²S Configuration

Using SDOUT in I²S mode requires the usage of two data output pins (SDOUT1 and SDOUT2) to transmit data for all for four channels. A GPIO pin must be configured as SDOUT2. Bits [7:4] of register 0x25 determine which channel information is assigned to SDOUT1 and SDOUT2. Register 0x31 enables the output current and the voltage predict data to be transmitted on the SDOUT pins. In I2S mode, the output current and the voltage predict cannot be transmitted simultaneously.

Table 2-7. SDOUT – I2S Configuration

Register 0x25, bit[7:4]	Register 0x31, bit[3:0]	Register 0x31, bit[5:4]	Pin	Slot 1	Slot 2
0001	0011	01	SDOUT1	Isense Ch1	Isense Ch2
			SDOUT2	Isense Ch3	Isense Ch4
0010	0011	01	SDOUT1	Isense Ch3	Isense Ch4
			SDOUT2	Isense Ch1	Isense Ch2
0001	0011	00	SDOUT1	Vpredict Ch1	Vpredict Ch2
			SDOUT2	Vpredict Ch3	Vpredict Ch4
0010	0011	00	SDOUT1	Vpredict Ch3	Vpredict Ch4
			SDOUT2	Vpredict Ch1	Vpredict Ch3
0001	0011	10	SDOUT1	Aux Ch1	Aux Ch2
			SDOUT2	Aux Ch3	Aux Ch4
0010	0011	10	SDOUT1	Aux Ch3	Aux Ch4
			SDOUT2	Aux Ch1	Aux Ch2

Following are the example PPC3 script and Figure 2-1 of the first row of the Table 2-7, to operate SDOUT to transmit Isense of four channels in I²S mode.

```
w c0 96 08          # configure GPIO_2 for SDOUT2
w c0 A0 40          # configure GPIO_2 as output
w c0 25 1A          # output channel 1/2 in SDOUT1 line and channel 3/4 in SDOUT2 line. 24 bits
word length
w c0 31 13          # enable Ch1/2/3/4 Isense output
w c0 2C 0F          # MSB offset of Vpredict, Isense and Aux
w c0 2D 00          # Vpredict LSB offset, MSB in 0x2C
w c0 2E 00          # Isense LSB offset, MSB in 0x2C

Note: Script format: write/read, device address, register address, data
      w: I2C write command
      r: I2C read command
     c0: device address
For example: w c0 96 08 action is: write c0 device register address 0x96 to value 0x08
```

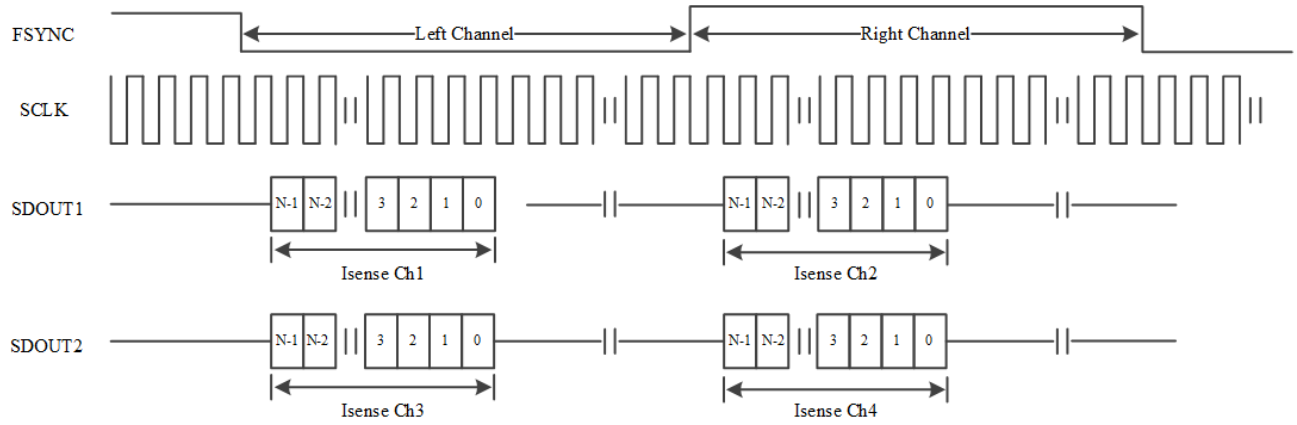

Figure 2-1. Timing Diagram Example for SDOUT in I2S Configuration

2.2 SDOUT – TDM Configuration

The recommendation is to transmit data through the SDOUT1 pin in TDM mode. Bits [7:4] of register 0x25 determine which SDOUT pin can transmit the desired data. Register 0x31 is used to enable output current and voltage predict transmitted on SDOUT pin. The recommendation is to place the 4 channels outputs of one TAS6584-Q1 device in consecutive slots. If the input data has a bit offset set SDOUT to the same offset to avoid overlapping data, this is configured using the 10-bit offset in registers 0x2C, 0x2D, 0x2E and 0x2F. When multiple data groups (Isense, Vpredict, Aux) are enabled at the same time on designated slots, the configuration of the offset is mandatory. The offset is defined as the number of SCLK cycles from the start (MSB) of the audio frame to the start of the data group. Figure 2-2 is typical timing diagram for SDOUT in TDM configuration with bit offsets.

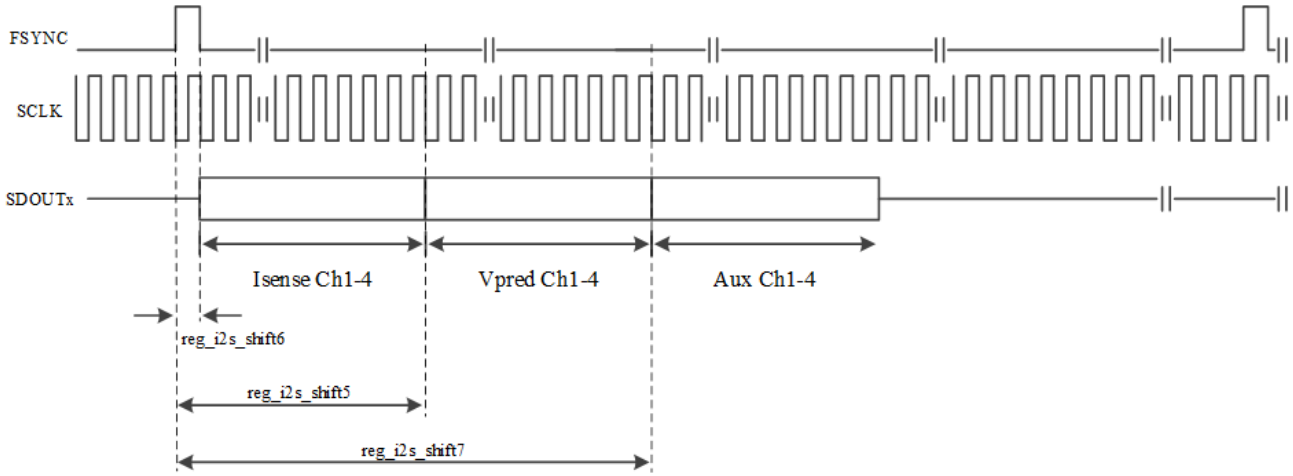

Figure 2-2. Timing Diagram for SDOUT in TDM Configuration

Table 2-8 and Figure 2-3 are SDOUT configuration and timing diagram example of one TAS6584-Q1 device in TDM8 mode without one bit shift offset. Isense of Ch1 to 4 data is placed on slots 1 to 4, and Vpredict of Ch1 to 4 data is placed on slots 5 to 8.

Table 2-8. SDOUT – TDM8 Configuration Example

Register 0x25, bit[7:4]	Register 0x31, bit[3:0]	Register 0x2C	Register 0x2D	Register 0x2E	Register 0x2F	Pin	Slot 1-4	Slot 5-8
0000	0011	0x0F	0x80	0x00	0xFF	SDOUT1	Isense Ch1-4	Vpredict Ch1-4

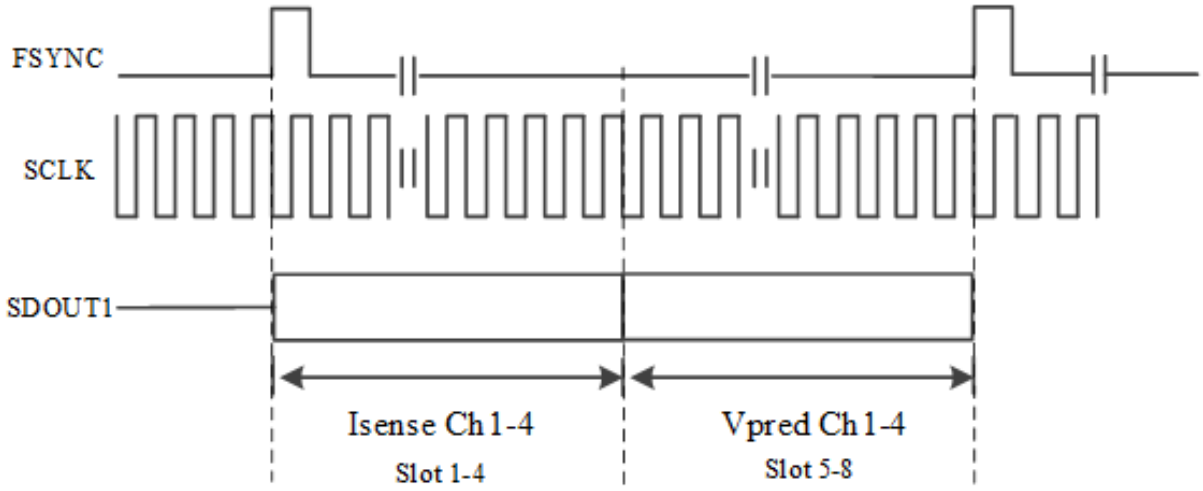

Figure 2-3. Timing Diagram Example for SDOUT in TDM8 Configuration

This is PPC3 script of above TDM8 configuration example.

```
w c0 25 0F          # TDM mode and 32 bit length for Vpredict and Isense
w c0 26 32          # 32 bit length for Aux
w c0 31 03          # enable Ch1/2/3/4 Vpredict and Isense output.
w c0 2C 0F          # MSB offset of Vpredict, Isense and Aux
w c0 2D 80          # Vpredict LSB offset: 128 bits, slot 5-8
w c0 2E 00          # Isense LSB offset: 0 bit, slot 1-4
w c0 2F FF          # Aux1 LSB, work with 0x2C register to remove Aux1 out of 8 slots
w c0 30 FF          # Aux2 LSB, work with 0x2C register to remove Aux2 out of 8 slots
```

The maximum SCLK frequency of serial audio port which TAS6x84-Q1 can support is 24.576MHz. The higher the clock frequency, the signal timing design can be more stringent. In the 24.576MHz SCLK clock frequency

application, SCLK must be configured to inverted mode to make sure timing stability, and DVDD power must be only supplied to 3.3V. The invert mode configuration register address is 0x20, Table 2-9.

Table 2-9. Register 0x20 Register Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5	BCK_INV_TX	R/W	0x0	BCK Polarity of TX This bit is to set the SDOUT sent at the rising edge of BCK. This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the SDOUT edges are aligned to the rising edge of the BCK. Normally it's assumed to be aligned to the falling edge of the BCK. **0: Normal BCK mode** 1: Inverted BCK mode
4	BCK_INV_RX	R/W	0x0	BCK Polarity of RX This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally LRCK and DIN edges are assumed to be aligned to the falling edge of the BCK. **0: Normal BCK mode** 1: Inverted BCK mode
3-0	RESERVED	R/W	0x0	Reserved

If SCLK frequency is 24.576MHz (96kHz sample rate in TDM8 mode), the PPC3 script of Table 2-8 TDM8 configuration example must add register 0x20 configuration. Because Vpredict data is only available at 48kHz sampling frequency and not supported at 96kHz or 192kHz, so below script only enables current output.

```
w c0 20 20          # configure SCLK to TX inverted mode
w c0 25 0F          # TDM mode and 32 bit length for Vpredict and Isense
w c0 26 32          # 32 bit length for Aux
w c0 31 03          # enable Ch1/2/3/4 Vpredict and Isense output.
w c0 2C CF          # MSB offset of Vpredict, Isense and Aux
w c0 2D FF          # Vpredict LSB, work with 0x2C register to remove Vpredict out of 8 slots
w c0 2E 00          # Isense LSB offset: 0 bit, slot 1-4
w c0 2F FF          # Aux1 LSB, work with 0x2C register to remove Aux1 out of 8 slots
w c0 30 FF          # Aux2 LSB, work with 0x2C register to remove Aux2 out of 8 slots
```

3 SDOUT Connection in Multi-Device System

Each SDOUT pin only can transmit one device measurement data. In multi-device systems, multiple devices SDOUTs data can share one TDM line can save DSP/SOC pins and resources. The SDOUT pin is a tri-state (0, 1, Hi-Z) output pin. Multiple SDOUT pins can be tied together directly. In multi-device systems the offset must be used to shift data groups to available slots and allow multiple devices to share one TDM line. The recommendation is to synchronize multiple devices through SCLK as Figure 3-1. To avoid SDOUT delay which caused by SCLK layout trace on PCB board, SCLK synchronization can be configured by register 0x60. The setup sequence is as follows:

1. Halt the Audio input Serial clock (SCLK). The I2C communication remains enabled
2. In register RAMP_PHASE_CTRL0 (Address = 0x60)
   - Set the reg_phase_sync_en bit to “1” to enable phase sync function
   - Set reg_phase_sync_sel bit to “1” to enable internal sync
3. Select the output phase settings for each device and the respective channels
   - Manual phase mode can optionally be used to select preferable output channel phase offsets across all channels in the systems. More details can be found in High-Frequency Pulse-Width Modulator (PWM)
4. Set all channels on each synchronized device to Hi-Z state
5. Provide the Audio input Serial clock (SCLK) and wait a minimum of 2ms before proceeding to the next step
6. Set each channel to PLAY state

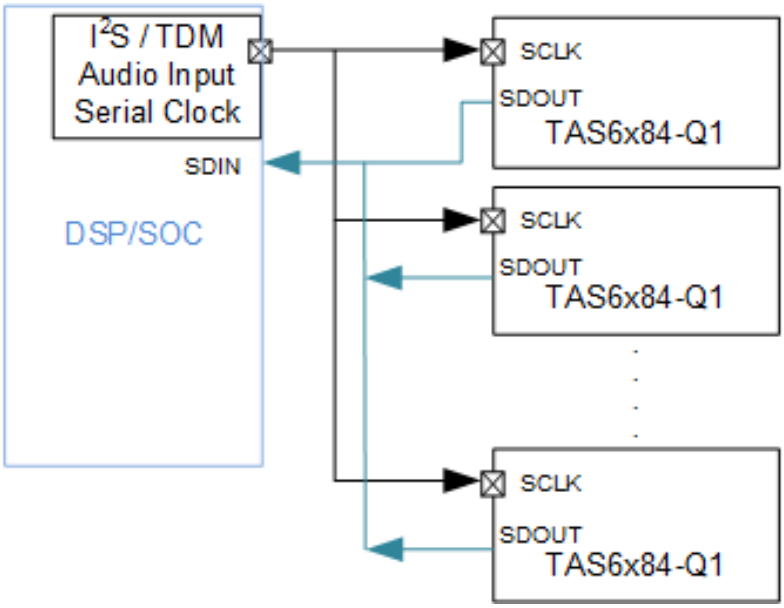

Figure 3-1. SCLK Synchronization architecture and SDOUT connection

Table 3-1 and Figure 3-2 are the SDOUT configuration and timing diagram example of four TAS6x84-Q1 devices in TDM16 mode. Each device only enables four channels of current sense output. The four SDOUT1 pins are tied together.

Table 3-1. SDOUT – TDM16 Configuration Example

	Register 0x25, bit[7:4]	Register 0x31, bit[3:0]	Register 0x2C	Register 0x2D	Register 0x2E	Register 0x2F	Pin	Slot 1-4	Slot 5-8	Slot 9-12	Slot 13-16
Device 1	0000	0010	0xCF	0xFF	0x00	0xFF	SDOUT1	Isense Ch1-4	-	-	-
Device 2	0000	0010	0xCF	0xFF	0x80	0xFF	SDOUT1	-	Isense Ch1-4	-	-
Device 3	0000	0010	0xDF	0xFF	0x00	0xFF	SDOUT1	-	-	Isense Ch1-4	-

Table 3-1. SDOUT – TDM16 Configuration Example (continued)

	Register 0x25, bit[7:4]	Register 0x31, bit[3:0]	Register 0x2C	Register 0x2D	Register 0x2E	Register 0x2F	Pin	Slot 1-4	Slot 5-8	Slot 9-12	Slot 13-16
Device 4	0000	0010	0xDF	0xFF	0x80	0xFF	SDOUT1	-	-	-	Isense Ch1-4

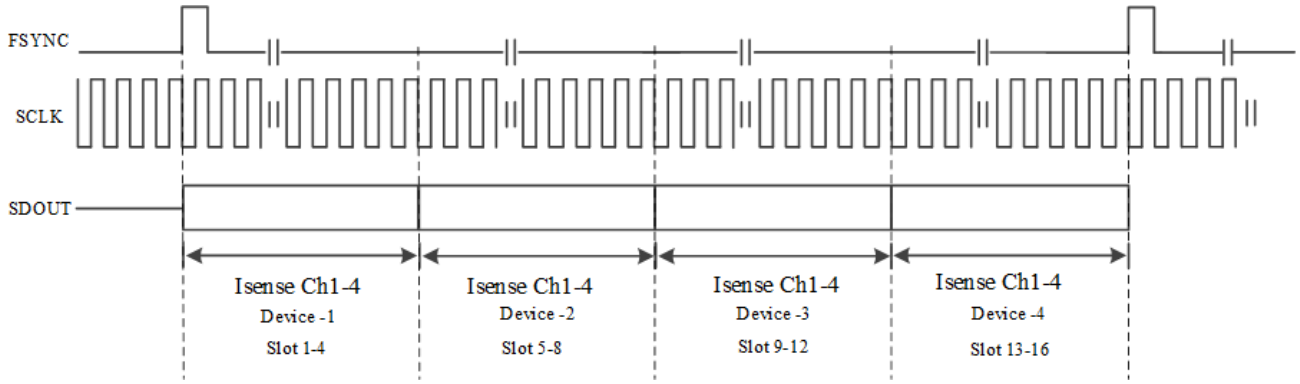

Figure 3-2. Timing Diagram Example for SDOUT in TDM8 Configuration

The following are SDOUT configuration PPC3 script for the four devices.

Note

The four I2C addresses need to be adjusted accordingly.

```
### Device 1 SDOUT configuration script  ####
w c0 60 03          # sync devices through SCLK
w c0 20 10          # configure SCLK to inverted mode if SCLK is 24.576MHz
w c0 25 0F          # TDM mode and 32 bit length for Vpredict and Isense
w c0 26 32          # 32 bit length for Aux
w c0 31 02          # enable Ch1/2/3/4 Isense output.
w c0 2C CF          # MSB offset of Vpredict, Isense and Aux
w c0 2D FF          # Vpredict LSB offset, work with 0x2C register to remove Vpredict out of 16
slots
w c0 2E 00          # Isense LSB offset, work with 0x2C register to place Isense on slot 1-4
w c0 2F FF          # Aux1 LSB, work with 0x2C register to remove Aux1 out of 16 slots
w c0 30 FF          # Aux2 LSB, work with 0x2C register to remove Aux2 out of 16 slots
```

```
### Device 2 SDOUT configuration script  ####
w c0 60 03          # sync devices through SCLK
w c0 20 10          # configure SCLK to inverted mode if SCLK is 24.576MHz
w c0 25 0F          # TDM mode and 32 bit length for Vpredict and Isense
w c0 26 32          # 32 bit length for Aux
w c0 31 02          # enable Ch1/2/3/4 Isense output.
w c0 2C CF          # MSB offset of Vpredict, Isense and Aux
w c0 2D FF          # Vpredict LSB offset, work with 0x2C register to remove Vpredict out of 16
slots
w c0 2E 80          # Isense LSB offset, work with 0x2C register to place Isense on slot 5-8
w c0 2F FF          # Aux1 LSB, work with 0x2C register to remove Aux1 out of 16 slots
w c0 30 FF          # Aux2 LSB, work with 0x2C register to remove Aux2 out of 16 slots
```

```
### Device 3 SDOUT configuration script  ####
w c0 60 03          # sync devices through SCLK
w c0 20 10          # configure SCLK to inverted mode if SCLK is 24.576MHz
w c0 25 0F          # TDM mode and 32 bit length for Vpredict and Isense
w c0 26 32          # 32 bit length for Aux
w c0 31 02          # enable Ch1/2/3/4 Isense output.
w c0 2C DF          # MSB offset of Vpredict, Isense and Aux
w c0 2D FF          # Vpredict LSB offset, work with 0x2C register to remove Vpredict out of 16
slots
w c0 2E 00          # Isense LSB offset, work with 0x2C register to place Isense on slot 9-12
```

```
w c0 2F FF          # Aux1 LSB, work with 0x2C register to remove Aux1 out of 16 slots
w c0 30 FF          # Aux2 LSB, work with 0x2C register to remove Aux2 out of 16 slots
```

```
### Device 4 SDOUT configuration script  ####
w c0 60 03          # sync devices through SCLK
w c0 20 10          # configure SCLK to inverted mode if SCLK is 24.576MHz
w c0 25 0F          # TDM mode and 32 bit length for Vpredict and Isense
w c0 26 32          # 32 bit length for Aux
w c0 31 02          # enable Ch1/2/3/4 Isense output.
w c0 2C DF          # MSB offset of Vpredict, Isense and Aux
w c0 2D FF          # Vpredict LSB offset, work with 0x2C register to remove Vpredict out of 16 slots
w c0 2E 80          # Isense LSB offset, work with 0x2C register to place Isense on slot 13-16
w c0 2F FF          # Aux1 LSB, work with 0x2C register to remove Aux1 out of 16 slots
w c0 30 FF          # Aux2 LSB, work with 0x2C register to remove Aux2 out of 16 slots
```

4 Output Current and Voltage Calculation

TAS6x84-Q1 output current and voltage predict can be measured through SDOUT data. Peak output voltage at full scale digital input is 43V/FS, and peak output current at full scale digital input is 30.9A/FS. The calculation of the output current and voltage predict is:

$$\mathrm{Isense}_{\mathrm{peak}} = \mathrm{Current}_{\mathrm{SDOUT}} \times 30.9(\mathrm{A}) \quad (1)$$

$$\mathrm{Isense}_{\mathrm{rms}} = \mathrm{Current}_{\mathrm{SDOUT}} \times \frac{30.9}{\sqrt{2}}(\mathrm{A}) \quad (2)$$

$$\mathrm{Vpredict}_{\mathrm{peak}} = \mathrm{Voltage}_{\mathrm{SDOUT}} \times 43(\mathrm{V}) \quad (3)$$

$$\mathrm{Vpredict}_{\mathrm{rms}} = \mathrm{Vpredict}_{\mathrm{SDOUT}} \times \frac{43}{\sqrt{2}}(\mathrm{V}) \quad (4)$$

The load impedance is also can be calculated through output current and voltage predict. Below is one example of calculation of current and voltage predict according to SDOUT data. Obtain the $\mathrm{Current}_{\mathrm{SDOUT}}$ and $\mathrm{Voltage}_{\mathrm{SDOUT}}$ data from designated slots with the scaling factors,

$$\mathrm{Current}_{\mathrm{SDOUT}} = 4.31(\%\mathrm{FS}) \quad (5)$$

and

$$\mathrm{Voltage}_{\mathrm{SDOUT}} = 12.6(\%\mathrm{FS}) \quad (6)$$

The output current, voltage predict and load impedance value are:

$$\mathrm{Isense}_{\mathrm{peak}} = 0.0431 \times 30.9 = 1.332(\mathrm{A}) \quad (7)$$

$$\mathrm{Isense}_{\mathrm{rms}} = 0.0431 \times \frac{30.9}{\sqrt{2}} = 0.942(\mathrm{A}) \quad (8)$$

$$\mathrm{Vpredict}_{\mathrm{peak}} = 0.126 \times 43 = 5.42(\mathrm{V}) \quad (9)$$

$$\mathrm{Vpredict}_{\mathrm{rms}} = 0.126 \times \frac{43}{\sqrt{2}} = 3.83(\mathrm{V}) \quad (10)$$

$$R_{\mathrm{load}} = \frac{\mathrm{Vpredict}_{\mathrm{rms}}}{\mathrm{Isense}_{\mathrm{rms}}} = 4.066\ (\Omega) \quad (11)$$

5 Summary

The TAS6x84-Q1 output current sense and voltage predict can be monitored for each channel and reports the measurement to a host processor through the SDOUT pin in either I2S mode or TDM mode. This application note serves as a guide to enable the measurement through configuration and the calculation of measurement value. Register configuration, example script and calculation are provided for easier use under some applications.

6 References

- Texas Instruments, *TAS6584-Q1 - 45-V, 10-A Digital Input 4-Channel Automotive Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics*, data sheet.
- Texas Instruments, *TAS6684-Q1 - 45V, 13A Digital Input 4-Channel Automotive Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics*, data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265