Radiation Report

TPS7H3301-SP & TPS7H3302-SP Single-Event Effects Summary

ABSTRACT

The purpose of this study was to characterize the effect of heavy-ion irradiation on the SEE performance of the TPS7H3301-SP/TPS7H3302-SP (QMLP version of the QMLV TPS7H3301-SP) sink/source DDR termination regulator. Heavy-ions with LET_{EFF} of 44.5, 52.5, 70, and 75MeV-cm^2 / mg (QMLP was only done at 75MeV-cm^2 / mg) were used to irradiate nine production devices in more than one hundred experiments with fluences ranging from 1 × 10^6 to 5 × 10^7 ions/cm^2 per run, over a variety of DDR modes, input and output voltage conditions, load conditions, and temperatures. The TPS7H3301-SP is completely SEL-free up to LET_{EFF} = 75MeV-cm^2 / mg at 125°C under all DDR modes. For DDR1 and DDR4, the device is also SET-free and SEFI-free up to LET_{EFF} = 70 MeV-cm^2 / mg. Under DDR2 and DDR3 modes, a very small number of SETs were observed at 70 MeV-cm^2 / mg but most were too small to pose risk to proper memory operation. In a few rare cases, SETs exceeded the JEDEC DDR specification and were categorized as SEFIs since they can potentially impact downstream memory operation. However, each of the few SEFIs observed generated a valid PGOOD transition thus protecting against any invalid memory accesses. Although most data recorded in this report is with respect to the QMLV device, the QMLP device that was tested shows to correlate to QMLV in both destructive and transient performance.

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Trademarks

1 Overview

The TPS7H3301-SP is a radiation-hardened, sink/source, double-data-rate (DDR) 3A termination regulator designed to provide a complete, compact, and low-noise design for space DDR termination applications where small form-factor and low weight are key considerations. The TPS7H3301-SP integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that ceramic capacitors can be used to support the fast load transient response. The TPS7H3301-SP contains a dedicated pin, V_{LDOIN}, for the VTT power supply to minimize the LDO power dissipation on user applications. The device also features a remote sensing function and meets all power requirements for DDR, DDR2, DDR3, low-power DDR, and DDR4 VTT bus termination applications. The fast transient response of the TPS7H3301-SP VTT regulator allows for a stable supply during read and write conditions. Additionally, the TPS7H3301-SP provides an open-drain P_{GOOD} signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications. The operating temperature range of the TPS7H3301-SP is specified from –55°C to +125°C. To enable simple power sequencing, both an enable input and a power-good output (P_{GOOD}) are integrated into the TPS7H3301-SP. The TPS7H3301-SP is packaged in a 16-pin thermally-enhanced dual ceramic flat pack package (HKR). Table 1-1 lists general device information and test conditions. For more detailed technical specifications, user guides, and application notes, see the TPS7H3301-SP product page.

Table 1-1. Overview Information

Description	Device Information
TI Part Number	TPS7H3301-SP
SMD Number	5962R1422801VXC
Device Function	DDR termination regulator
Technology	LBC7 (250-nm linear BiCMOS)
Exposure Facility	Radiation Effects Facility, Cyclotron Institute, Texas A&M University
Heavy Ion Fluence per Run	$1 \times 10^6 – 3 \times 10^7$ ions / cm^2
Irradiation Temperature	25°C, 85°C, and 125°C (for SEL testing)

2 SEE Mechanisms

The TPS7H3301-SP device does not operate at high voltages or high currents, so single-event burnout (SEB) and single-event gate-rupture (SEGR) events are not expected to be an issue. The primary SEE events of interest in the TPS7H3301-SP are single-event latch-up (SEL), single-event functional interrupt (SEFI), and single-event transient (SET).

From a risk and impact point-of-view, the occurrence of a SEL is potentially the most destructive SEE event and the biggest concern for space applications. In mixed technologies such as the Linear BiCMOS 7 process used for the TPS7H3301-SP, the CMOS circuitry introduces a potential SEL susceptibility. SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-substrate and n-well and n+ and p+ contacts) [1, 2]. The parasitic bipolar structure creates a high-conductance path (creating a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between power and ground that persists (is latched) until power is removed or until the device is destroyed by the high-current state. For the design of the TPS7H3301-SP, SEL susceptibility was reduced by maximizing anode-cathode spacing (tap spacing) while increasing the number of well and substrate ties in the CMOS portions of the layout. Additionally, junction isolation techniques were also used with buried wells and guard ring structures isolating the CMOS p- and n-wells (4, 5). The design techniques applied for SEL-mitigation were sufficient as the TPS7H3301-SP exhibited no signs of SEL during all of the heavy-ions up to an LET_{EFF} = 70MeV-cm^2 / mg at a fluence of 10^7 ions / cm^2 and a die temperature of 125°C.

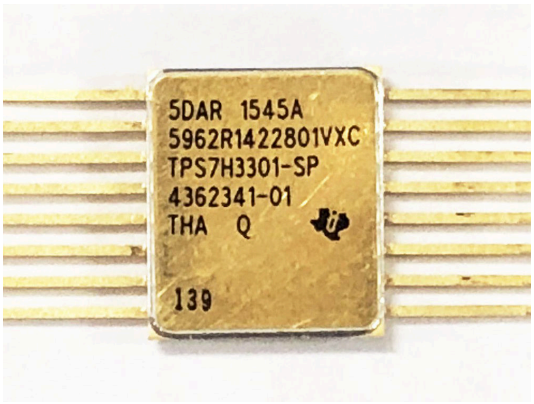
Unlike the varied and unique failure signatures of SEFI events in complex digital processors that require an external reboot or reset to clear, (such as the TPS7H3301-SP voltage regulator), SEFI is defined as anything that can affect downstream electronic components, in this case, DDR memories using the TPS7H3301-SP to generate VTT / V_O and V_{TTREF} signals. It was assumed that SEFIs might manifest as an upset in the control logic causing either a system reset or inducing a false P_{GOOD}, an event where P_{GOOD} is pulled down without a concurrent collapse of VTT/V_O. To mitigate this, all logic was triplicated with a hardened voter on key outputs. Another potential source of SEFI was an ion erroneously triggering the current-limiting clamp. To mitigate this type of SEFI, a redundant regulator loop with each loop containing separate current limiting clamps was included in the design. Each regulator loop features a separate independent biasing circuit. The design techniques applied for SEFI-mitigation (triple modular redundancy with hardened voters in key functional blocks) were sufficient because the TPS7H3301-SP exhibited no signs of these type of SEFIs either in the logic or in the regulator loop under heavy-ions with LET_{EFF} of up to 70MeV-cm^2 / mg at fluences of up to 5 × 10^7 ions / cm^2.

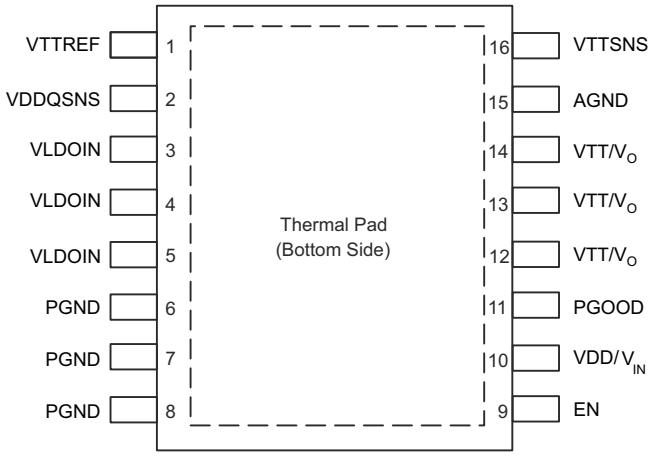
Voltage regulators can exhibit positive, negative, and bipolar SETs, where the magnitude and polarity depend on how the ionization is distributed (a function of the ion LET, location, trajectory, energy, the thickness and composition of the BEOL stack, and so forth) and what part of the circuit is impacted (6, 7, 8, 9). All of the design techniques (previously mentioned) to mitigate SEFI can also mitigate some of the SETs from affecting the output. However, if the output transistors are impacted, avoiding a transmission of the transient to the outputs can be difficult. The shape and duration of the SETs is a strong function of output capacitance and can be affected by the load conditions. SETs are only a concern if the magnitude and duration cause a disruption in downstream power.

In the case of the TPS7H3301-SP, the difference between VTT/V_O and V_{TTREF} signals is the most important feature. The two signals can vary, but the signals must track so that the voltage margin during DDR memory accesses is stable. SETs of primary concern were those that caused the difference between these two signals to exceed a specified value. The JEDEC DDR specification states that any difference between VTT/V_O and V_{TTREF} signals exceeding ±40mV is problematic for the reliable read-write operation of a DDR memory system. The TPS7H3301-SP did not exhibit signs of SETs up to an LET_{EFF} = 52.5MeV-cm^2 / mg at a fluence of 10^7 ions / cm^2. A few SET events were observed at LET_{EFF} = 70MeV-cm^2 / mg but most were less than ±5mV, well within the JEDEC DDR specification. A few of the SETs were larger in magnitude and exceeded the JEDEC DDR specification. Since each of these bigger SETs generated a valid P_{GOOD} signal, downstream memory is protected from invalid accesses. Note that these rare larger SET events were characterized as SEFIs since the events can impact downstream systems (although since a valid P_{GOOD} signal was generated, the only impact is to halt memory operation for the 20µs to 40µs duration of the event).

3 Test Device and Evaluation Board Information

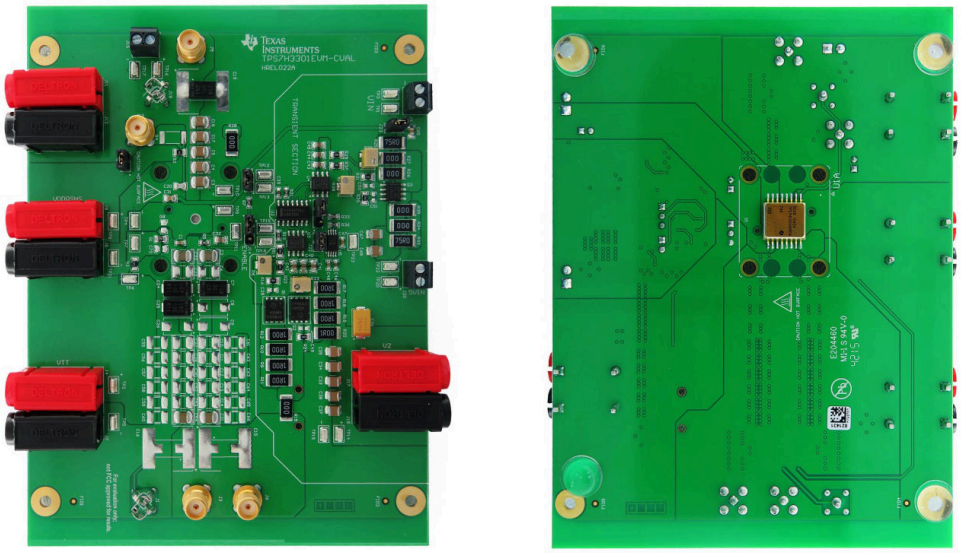
The TPS7H3301-SP is packaged in a 16-pin thermally-enhanced dual ceramic flat pack package (HKR) shown with the pinout in Figure 3-1 . The TPS7H3301 evaluation board, the TPS7H3301EVM-CVAL (HREL022) is designed to evaluate the performance and characteristics of the DDR, DDR2, DDR3, and DDR4 VTT termination regulator (the TPS7H3301-SP.) Figure 3-2 shows the top and bottom views of the evaluation board used for radiation testing. For more information about the device or evaluation board, see the TPS7H3301-SP product page.





The package lid was removed to reveal the die face for all heavy ion testing

Figure 3-1. Photograph of the TPS7H3301-SP Space DDR Termination Regulator (Left) and Pinout Diagram (Right)



The TPS7H3301-SP is mounted on the bottom side. This board was used for all testing.

Figure 3-2. TPS7H3301EVM-CVAL (HREL022) Board Top View (Left) and Bottom View (Right)

Figure 3-3 shows a simplified schematic of the configuration used for this radiation testing based on the evaluation module for the TPS7H3301-SP (TPS7H3301EVM-CVAL). For more information, see *TPS7H3301EVM-CVAL (HREL022)*.

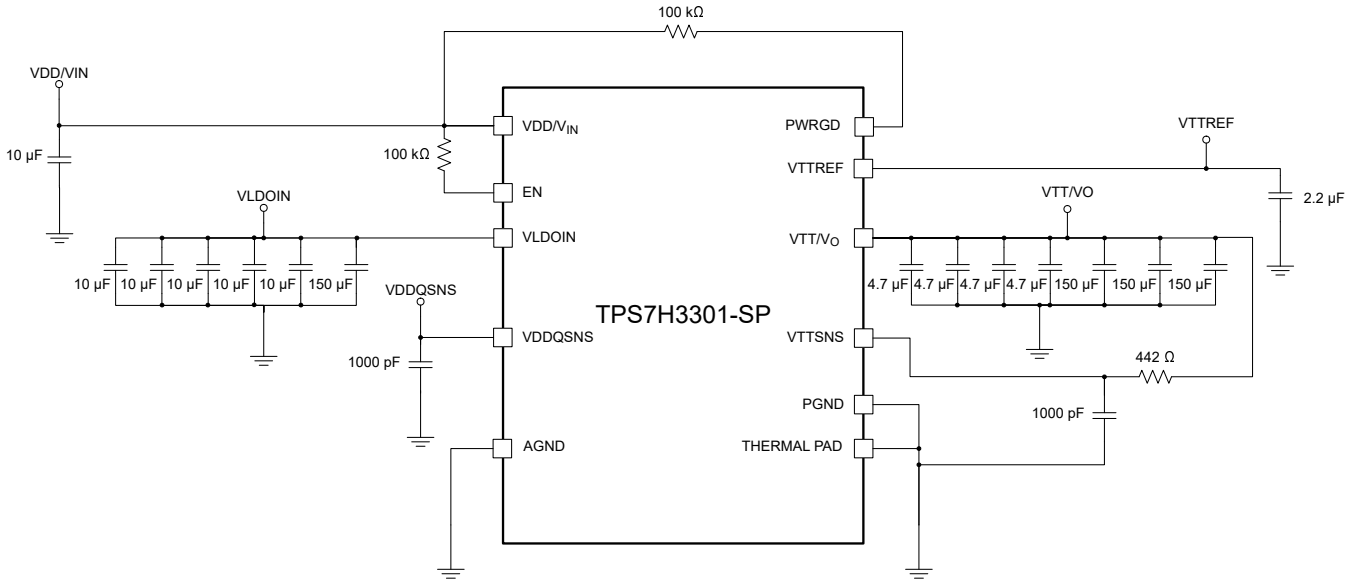


Figure 3-3. Schematic of the Prototype TPS7H3301EVM-CVAL (HREL022) Evaluation Board Used to Perform the SEE Tests on the TPS7H3301-SP Devices

4 Irradiation Facility and Setup

The heavy ion species used for the SEE studies on this product were provided and delivered by the Texas A&M University (TAMU) Cyclotron Radiation Effects Facility (12) using a superconducting cyclotron and advanced electron cyclotron resonance (ECR) ion source. Ion beams are delivered with high uniformity over a 1in diameter circular cross sectional area for the in-air station. Uniformity is achieved by means of magnetic defocusing. The intensity of the beam is regulated over a broad range spanning several orders of magnitude. For the bulk of these studies, ion fluxes between 10^4 and 10^5 ions / cm^2-s were used to provide heavy ion fluences between 10^6 and 10^7 ions / cm^2. For these experiments, Krypton (^{84}Kr) at a 45° angle, Silver (^{109}Ag) at a 22° and 45° angle, and Holmium (^{165}Ho) at incident angle ions were used for a LET_{EFF} of 44.5, 52.5, 70, and 75MeV-cm^2 / mg respectively. The total kinetic energy for each of the ions is as follows:

- 84Kr = 1.259GeV (15MeV / amu line)
- 109Ag = 1.634GeV (15MeV / amu line)
- 165Ho = 2.47GeV (15MeV / amu line)

Ion beam uniformity for all tests was in the range of 84% to 93%. The TPS7H3301-SP test board is shown in Figure 4-1 as the board was used at the TAMU facility. The board was also rotated 90° for some of the experiments to check for the possibility of different sensitivities due to asymmetric layouts. Note the 1in diameter ion beam port to the right (aluminum cylinder with gold-colored window). The 1mil Aramica window allows in air testing while maintaining the vacuum within the accelerator with only minor ion energy loss. Note that the de-lidded TPS7H3301-SP DDR regulator unit is mounted on the opposite side of the EVM board specifically for beam testing. The air space between the device and the ion beam port window was maintained at 40mm.

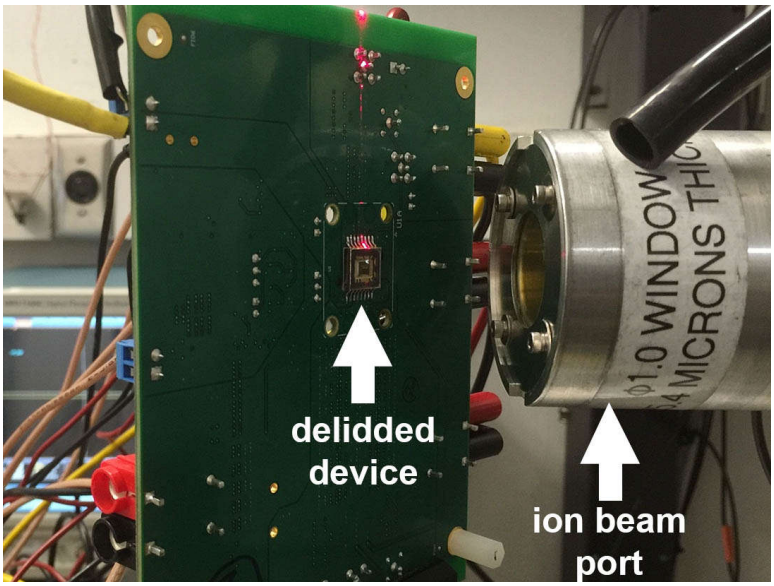


Figure 4-1. Photograph of the TPS7H3301-SP Evaluation Board Mounted in Front of the Heavy Ion Beam Exit Port at the TAMU Accelerator Facility

5 Depth, Range, and LET_{EFF} Calculation

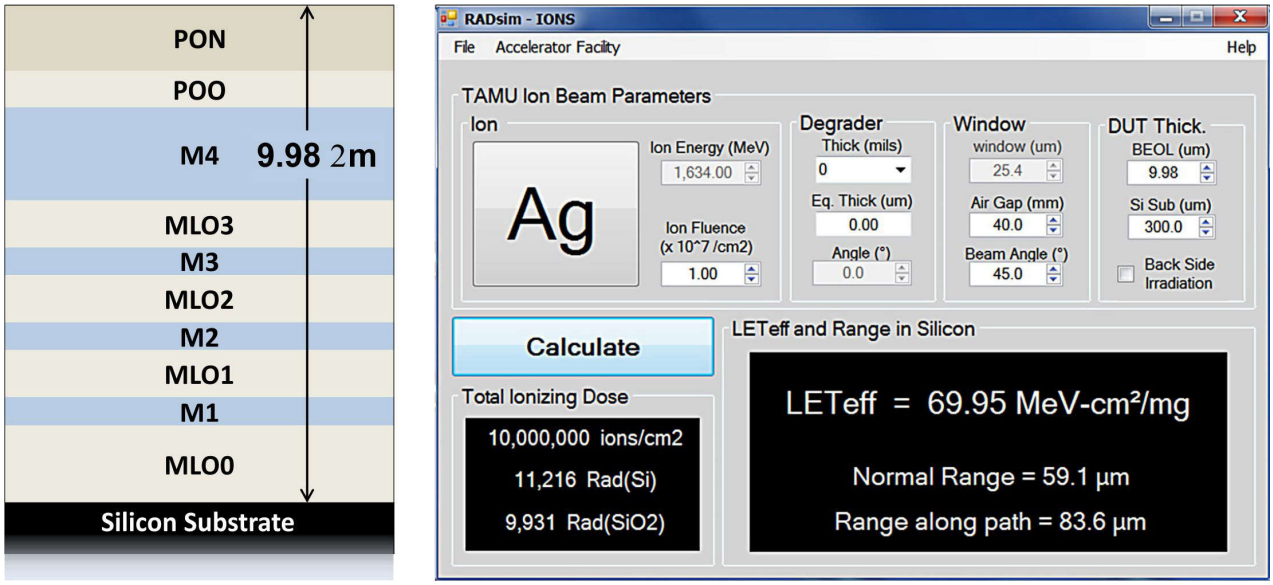


Figure 5-1. Layer Stack of TPS7H3301-SP (Left) and RADsim-IONS Program (Right) Used to Determine Key Ion Parameters

The TPS7H3301-SP is fabricated in the Texas Instruments Linear BiCMOS 0.25µm process (LBC7) with a back-end-of-line (BEOL) stack consisting of three levels of standard thickness aluminum metal on a 0.6µm pitch, and a fourth level of thick aluminum. The total stack height from the surface of the passivation to the silicon surface is 9.98µm based on nominal layer thickness as shown in Figure 5-1. No polyimide or other coating was present so the uppermost layer was the nitride passivation layer (PON). Accounting for energy loss through the 1mil thick Aramica (Kevlar®) beam port window, the 40mm air gap, and the BEOL stack over the TPS7H3301-SP, the effective LET (LET_{EFF}) at the surface of the silicon substrate and the depth and ion range was determined with the custom RADsim-IONS application (custom tool developed at Texas Instruments and based on SRIM [13] simulations) for the two primary ions used for the experiments. Table 5-1 lists the results. The stack was modeled as a homogeneous layer of silicon dioxide.

Table 5-1. Krypton and Silver LET_{EFF}, Depth, and Range in Silicon

Ion Type	Angle of Incidence	Depth in Silicon (µm)	Range in Silicon (µm)	LET_{EFF} (MeV-cm^2 / mg)
^{84}Kr	45°	72.5	102.5	44.5
^{109}Ag	22°	80.7	87	52.5
^{109}Ag	45°	59.1	83.6	70
^{165}Ho	0°	97.2	97.2	75

6 Test Setup and Procedures

SEE testing was performed on a TPS7H3301-SP device mounted on a prototype of the TPS7H3301EVM-CVAL (HREL022) evaluation board. The board was powered with three different voltage rails using three of four channels of an Agilent N6702A precision power supply. All voltage rails were connected in a 4-wire configuration. The device was loaded with two source meters, one to provide a load for the VTT/V_O output and one to independently provide a load for VTTREF output. The SEE events were monitored by using the NI-PXI 5105 Scope Card and a Tektronix® DPO7104C Digital Phosphor Oscilloscope (four channels, 20GSPS).

The DPO oscilloscope was used to verify that pulses were not missed due to re-arming of the 5105 scope card. In all tests the results from both capture devices agreed so the higher speed, longer capture capabilities of the DPO oscilloscope were redundant. The inputs to the NI PXIe 5105 scope card were AC-coupled. Five channels were captured, PGOOD, EN, VLDOIN, VTT/V_O, and VTTREF. The VTT/V_O signal was used as a trigger, with a trigger window set to ±20mV so any event greater than 20mV is captured. Note that according to JEDEC DDR standards, any excursion beyond ±40mV are considered problematic. The device was actively loaded on VTT and VTTREF. Events were captured with a resolution of 50k samples at a rate of 50MSPS. Because the scope was capturing data continuously, samples were acquired and saved prior a trigger event. The capture voltage range was set from ±6V with an input impedance of 1MΩ.

With the exception of the DPO digital oscilloscope, all equipment was controlled and monitored using a custom-developed LabVIEW® program (PXIRadTest) running on a National Instruments™ NI-PXIe-8135 controller. Figure 6-1 shows a block diagram of the set-up used for SEE testing the TPS7H3301-SP, and Table 6-1 lists the connections, limits and compliances used. The TPS7H3301-SP was tested at room temperature, 85°C, and 125°C. For higher temperature tests, the device was heated using a convection heat gun aimed at the die. The die temperature was monitored during the testing using a K-type thermocouple attached to the heat slug of the TPS7H3301-SP package with thermal paste.

Table 6-1. Equipment Set Used for the SEE Testing

Pin Name	Equipment Used	Capability	Compliance	Range of Values Used
VIN/VDD	Agilent™ N6700B (Ch 2)	3A	100mA	2.375V to 3.5V
VLDOIN	Agilent N6700B (Ch 3)	3A	5A	1.2V to 2.5V
VDDQSNS	Agilent N6700B (Ch 4)	3A	500mA	1.2V to 2.5V
VTTREF	Keithley SourceMeter® 2400	±1A	Sink and source	—
VTT/V_O	Yokogawa™ GS610	±3A	Sink and source	0.60V to 1.25V
Oscilloscope card	HSDIO NI-PXIe 5105	50MSPS	—	—
Digital oscilloscope	Tektronix DPO7104C	20GSPS	—	—

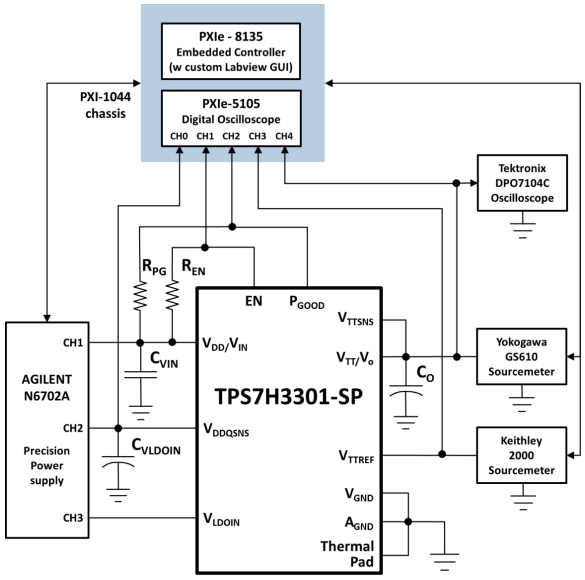


Figure 6-1. Block Diagram of Heavy-Ion SEE Test Set-Up With the TPS7H3301-SP on a TPS7H3301EVM-CVAL (HREL022) Evaluation Board

The VTT/V_O output was used to trigger the oscilloscopes. The Agilent N6702A provided the precision power inputs and the Yokogawa GS610 and Keithley 2000 source meters provided active loading.

All boards used for SEE testing were checked for functionality and dry runs performed to make sure that the test system was stable under all bias and load conditions prior to being taken to the TAMU facility. During the heavy-ion testing, the LabVIEW control program powered up the TPS7H3301-SP device and set the external sourcing and monitoring functions of the external equipment. After functionality and stability had been confirmed, the beam shutter was opened to expose the device to the heavy ion beam. The shutter remained open until the target fluence was achieved (determined by external detectors and counters).

During the irradiation the PXIe–5101 scope card continuously monitored the P_{GOOD}, EN, V_{LDOIN}, VTT/V_O and V_{TTREF} outputs of the TPS7H3301-SP with any events on VTT/V_O output exceeding ±20mV triggered a capture. During a trigger event, the digital scope card can capture 50k samples (the card was continuously digitizing so when triggered, a predefined 20% of the samples that preceded the event were stored). The scope card captured events lasting up to 1ms (50k samples at 50MSPS).

In addition to continuously monitoring the voltage levels of the five digital scope inputs, the currents into or out of the V_{DOQSNS}, V_{IN}, and V_{LDOIN} pins were also monitored during each test to enable the detection of the occurrence of an SEL event. No sudden increases in current were observed (outside of normal fluctuations) on any of the test runs which indicated that no SEL events occurred during any of the testing.

7 Results

7.1 SEL Results

All SEL characterizations were performed with forced hot air to maintain the device temperature at 125°C with the Silver (^{109}Ag) or Holmium (^{165}Ho) heavy ion beam incident on the die surface at 45° or 0° for a LET_{EFF} of 70 or 75MeV-cm^2 / mg, respectively. A flux of 10^5 ions / cm^2-s was used for a total fluence of 10^7 ions / cm^2. Run duration to achieve this fluence was approximately two minutes. The current versus time data was obtained by current monitoring the V_{DDQSNS}, V_{LDOIN}, and V_{IN} pins for each run; representative data plots for these data are shown in Figure 7-1 for DDR1 modes (the plots looked similar for all DDR modes). No discontinuous increases in current were observed in any of the three monitored signals. No SEL events were observed for any of the DDR modes under the full range of load conditions. Table 7-1 lists the SEL results for all DDR modes.

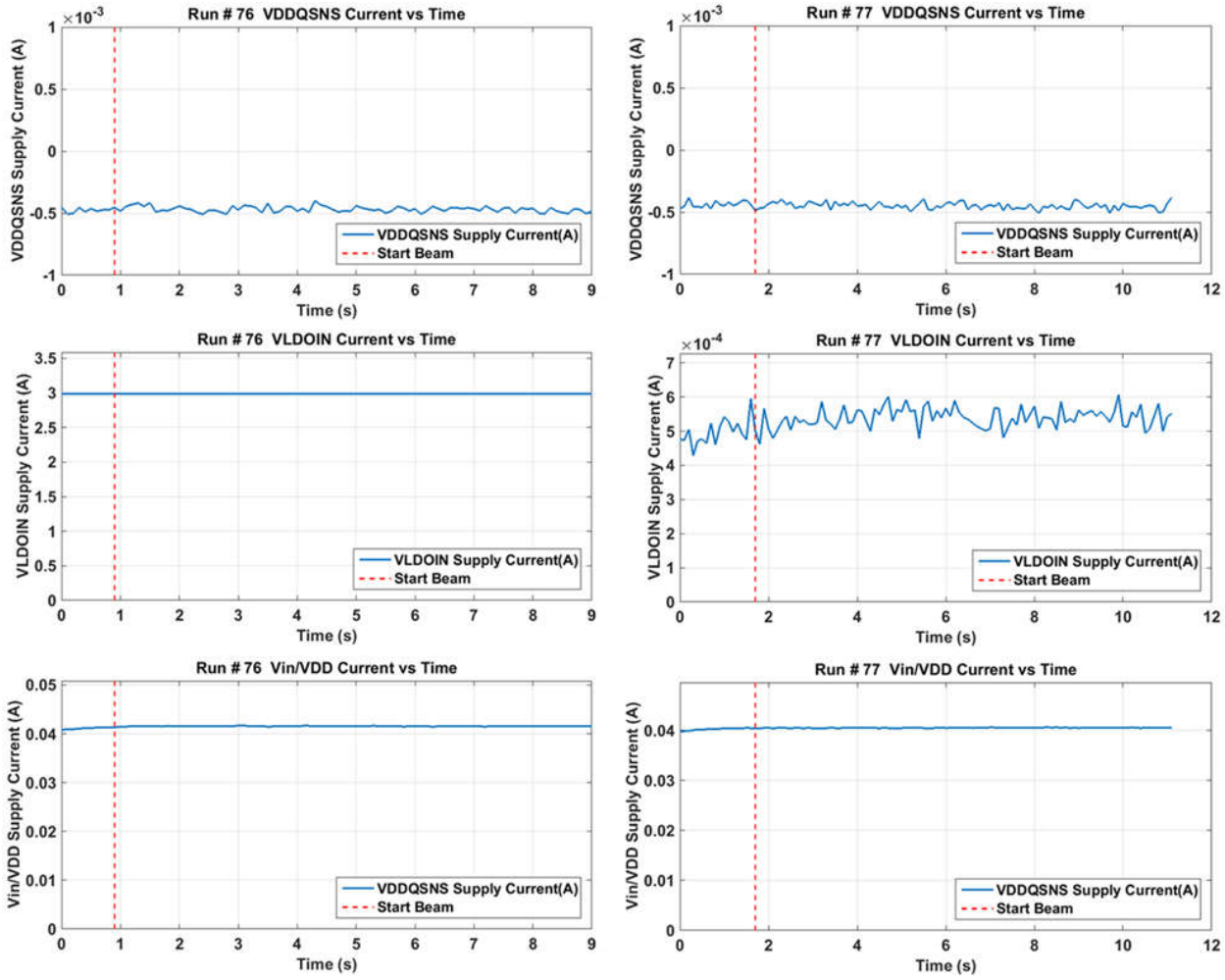


Figure 7-1. SEL Current versus Time (I Versus t) Data in DDR1 Mode for Sourcing (Left) and Sinking 3A (Right)

Table 7-1. TPS7H3301-SP and TPS73302-SP SEL Results

Device Number	Run Number	T (°C)	LET_{EFF} (MeV-cm^2 / mg)	DDR Mode	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	VTT/V_O (V)	VTT/V_OLoad (A)	V_{TTREF} Load (mA)	Events On VTT/V_O	Events on P_{GOOD}	I vs t Events
2	74	125	70	DDR1	3.5	2.95	2.5	1.25	0	–10	0	0	0
2	75	125	70	DDR1	2.5	2.95	2.5	1.25	0	–10	0	0	0
2	76	125	70	DDR1	2.5	2.95	2.5	1.25	–3	–10	0	0	0
2	77	125	70	DDR2	2.5	2.95	2.5	1.25	3	–10	0	0	0
2	78	125	70	DDR2	2.5	3.5	2.5	1.25	0	–10	0	0	0
2	79	125	70	DDR2	2.5	3.5	2.5	1.25	–3	–10	0	0	0
2	80	125	70	DDR2	2.5	3.5	2.5	1.25	3	–10	0	0	0
2	81	125	70	DDR2	1.2	2.9	1.2	0.6	0	–10	0	0	0
2	82	125	70	DDR4	1.2	2.9	1.2	0.6	–3	–10	0	0	0
2	83	125	70	DDR4	1.2	2.9	1.2	0.6	3	–10	0	0	0
2	84	125	70	DDR4	1.2	3.5	1.2	0.6	0	–10	0	0	0
2	85	125	70	DDR4	1.2	3.5	1.2	0.6	–3	–10	0	0	0
2	86	125	70	DDR4	1.2	3.5	1.2	0.6	3	–10	0	0	0
8	118	125	75	DDR1	3.5	3.5	3.5	1.75	3	-10	0	0	0
8	119	125	75	DDR1	3.5	3.5	3.5	1.75	-3	-10	0	0	0
8	120	125	75	DDR3	1.5	3.5	1.5	0.75	-3	-10	0	0	0
8	121	125	75	DDR4	1.2	3.5	1.2	0.6	-3	-10	0	0	0
9	122	125	75	DDR4	1.2	3.5	1.2	0.6	-3	-10	0	0	0
9	123	125	75	DDR3	1.5	3.5	1.5	0.75	-3	-10	0	0	0
9	124	125	75	DDR1	3.5	3.5	3.5	1.75	-3	-10	0	0	0
10	125	125	75	DDR1	3.5	3.5	3.5	1.75	3	10	0	0	0
10	126	125	75	DDR1	3.5	3.5	3.5	1.75	3	-10	0	0	0
10	127	125	75	DDR1	3.5	3.5	3.5	1.75	-3	10	0	0	0
10	128	125	75	DDR1	3.5	3.5	3.5	1.75	-3	-10	0	0	0

No SEL events were observed under any of the test runs in any of the DDR modes over minimum and maximum load conditions, indicating that the TPS7H3301-SP DDR termination regulator is SEL-immune at T = 125°C and LET = 75MeV-cm^2/ mg.

The upper-bound SEL cross section based on a 95% confidence interval (see *Single-Event Effects (SEE) Confidence Interval Calculations* for discussion of confidence limits) for the TPS7H3301-SP for each DDR mode is the same because the fluence for each test was identical and no SEL was observed in any DDR mode. Note that for each DDR mode the multiple tests over different load conditions were combined:

$$\sigma_{SEL,\,DDR1} \leq 1.77 \times 10^{-7} \text{cm}^2/\text{device for LET}_{EFF} = 70\text{MeV} \times \text{cm}^2/\text{mg and T}_J = 125°\text{C}. \quad (1)$$

$$\sigma_{SEL,\,DDR2} \leq 1.32 \times 10^{-7} \text{cm}^2/\text{device for LET}_{EFF} = 70\text{MeV} \times \text{cm}^2/\text{mg and T}_J = 125°\text{C}. \quad (2)$$

$$\sigma_{SEL,\,DDR3} \leq 2.64 \times 10^{-7} \text{cm}^2/\text{device for LET}_{EFF} = 70\text{MeV} \times \text{cm}^2/\text{mg and T}_J = 125°\text{C}. \quad (3)$$

$$\sigma_{SEL,\,DDR4} \leq 1.77 \times 10^{-7} \text{cm}^2/\text{device for LET}_{EFF} = 70\text{MeV} \times \text{cm}^2/\text{mg and T}_J = 125°\text{C}. \quad (4)$$

The 95% confidence upper-bound for the SEL cross section based on single runs for each unique load condition within each DDR mode is:

$$\sigma_{SEL,\,BY\_LOAD} \leq 5.30 \times 10^{-7} \text{cm}^2/\text{device for LET}_{EFF} = 70\text{MeV} \times \text{cm}^2/\text{mg and T}_J = 125°\text{C}. \quad (5)$$

7.2 SEB Results

All SEB characterizations were performed at room temperature with Holmium (^{165}Ho) heavy ion beam incident on the die surface at 0° for a LET_{EFF} of 75MeV-cm^2 / mg, respectively. A flux of 10^5 ions / cm^2-s was used for a total fluence of 10^7 ions / cm^2. Run duration to achieve this fluence was approximately two minutes. No discontinuous increases in current were observed in any of the three monitored signals. No SEB events were observed for any of the DDR modes under the full range of load conditions in both enabled and disabled modes.

Table 7-2. TPS7H3301-SP and TPS7H3302-SP SEB Results

Device Number	Run Number	Part Enabled	T (°C)	LET_{EFF} (MeV-cm^2 / mg)	DDR Mode	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	VTT/V_O (V)	VTT/V_O LOAD (A)	V_{TTREF} LOAD (mA)	Events ON VTT/V_O	Events ON P_{GOOD}	I vs t Events
8	129	Enabled	25	75	DDR1	3.5	3.5	3.5	1.75	3	-10	0	0	0
8	130	Disabled	25	75	DDR1	3.5	3.5	3.5	0.47	3	-10	0	0	0
8	131	Enabled	25	75	DDR3	1.5	3.5	1.5	0.75	-3	-10	0	0	0
8	132	Disabled	25	75	DDR3	1.5	3.5	1.5	0.47	-3	-10	0	0	0
8	133	Enabled	25	75	DDR4	1.2	3.5	1.2	0.6	-3	-10	0	0	0
8	134	Disabled	25	75	DDR4	1.2	3.5	1.2	0.47	-3	-10	0	0	0
9	135	Disabled	25	75	DDR1	3.5	3.5	3.5	0.47	-3	-10	0	0	0
9	136	Disabled	25	75	DDR3	1.5	3.5	1.5	0.47	-3	-10	0	0	0
9	137	Disabled	25	75	DDR4	1.2	3.5	1.2	0.47	-3	-10	0	0	0
9	138	Enabled	25	75	DDR1	3.5	3.5	3.5	1.75	-3	-10	0	0	0
9	139	Enabled	25	75	DDR3	1.5	3.5	1.5	0.75	-3	-10	0	0	0
9	140	Enabled	25	75	DDR4	1.2	3.5	1.2	0.6	-3	-10	0	0	0
10	141	Enabled	25	75	DDR1	3.5	3.5	3.5	1.75	1	10	0	0	0
10	142	Enabled	25	75	DDR1	3.5	3.5	3.5	1.75	1	-10	0	0	0
10	143	Disabled	25	75	DDR1	3.5	3.5	3.5	0.47	3	-10	0	0	0
10	144	Enabled	25	75	DDR1	3.5	3.5	3.5	1.75	-3	10	0	0	0
10	145	Enabled	25	75	DDR1	3.5	3.5	3.5	1.75	-3	-10	0	0	0

1. Device 10 is the TPS7H3302-SP.

7.3 SET and SEFI Results

The primary concern for DDR regulators such as the TPS7H3301-SP in a space environment is the occurrence of a SET that creates a transient difference exceeding ±40mV (as per the JEDEC DDR specification) between the nominal output (VTT/V_O) and reference voltage (V_{TTREF}). Under nominal conditions, V_{TTREF} = ½ VTT/V_O, where V_{TTREF} serves as a reference for memory read-write operations such that the sense amplifiers in the memories can reliably discriminate between a one and a zero data state.

Once it was determined that destructive events did not occur in the TPS7H3301-SP, nor were any false PGOOD signals (if the PGOOD control circuits were sensitive, can be possible for an ion event to generate a PGOOD while the output was still valid). Thus voltage transients on the outputs induced by ions are the key concern. There are fundamentally two categories that must be considered.

1. SET that causes a transient on output where $VTT/V_O - V_{TTREF}$ is less than ±40mV. This type of event is categorized as an SET and does not impact the downstream memory.
2. SET that causes a $VTT/V_O - V_{TTREF}$ to exceed ±40mV. This type of event is categorized as a SEFI since the event can potentially impact the performance of downstream memory. If the SEFI in number two occurs, there are two possible outcomes:
   a. P_{GOOD} transition is properly triggered, temporarily halting memory access until the transient has recovered. While this represents a brief loss of availability (approximately 20µs to 40µs), there is no impact to the memory since no illegal accesses (when VTT/V_O and VTTREF are not tracking) were allowed.
   b. P_{GOOD} transition is NOT triggered so memory access continues despite potential memory errors (when VTT/V_O and V_{TTREF} are not tracking). This type of event was not observed.

The TPS7H3301-SP was completely SEE-free up to LET_{EFF} = 52.5MeV-cm^2 / mg. The regulator was also completely SEE-free up to LET_{EFF} = 70MeV-cm^2 / mg for DDR1 and DDR4 modes. During operation in DDR2 and DDR3 modes, in a few rare instances, events were observed at LET_{EFF} = 70MeV-cm^2 / mg. The observed events were transients and as a result, is normally be categorized as SETs, however, as mentioned above, SETs that cause an interruption of down-stream memory were categorized as SEFIs. Unlike the conventional definition of SEFI in the context of complex digital systems, these SEFIs are self-recovering without any external reset needed.

Of the few events observed most were SET. By the definition, all of the SET events induced less than ±40mV difference between the nominal output (VTT/V_O) and reference voltage (V_{TTREF}) – as per the JEDEC DDR specification. In fact, of the events categorized as SETs, none induced more than approximately ±20mV transient. Such small glitches do not affect memory components. An example of the VTT/V_O and V_{TTREF} signals during the biggest SET are shown in Figure 7-2. The difference between the VTT/V_O and reference voltage V_{TTREF} is shown in Figure 7-3, clearly within the allowed JEDEC limits of ±40mV. Note that no P_{GOOD} transition occurred since the signal never exceeded the specification, as shown in Figure 7-4.

The TPS7H3301-SP did exhibit a few transients larger than the JEDEC DDR specification. Of the few SEFI observed, all generated a valid P_{GOOD} signal in each case, protecting downstream memory from illegal read-write operations for the duration of the event (20µs to 40µs). SETs exceeding the JEDEC DDR specification without generating a P_{GOOD} signal were not observed. These would be problematic because without a P_{GOOD} signal, the downstream memory read/write operations would continue even though VTT/V_O and V_{TTREF} were not tracking, which risks data errors. An example of the VTT/V_O and V_{TTREF} signals during a SEFI are shown in Figure 7-5. The difference between the VTT/V_O and reference voltage V_{TTREF} is shown in Figure 7-6, clearly exceeding the JEDEC limits of ±40mV for a short period, with a P_{GOOD} transition occurring where the signal exceeded the specification, as shown in Figure 7-7.

The following are examples of captured waveforms for an SET event that occurred during run number 114.

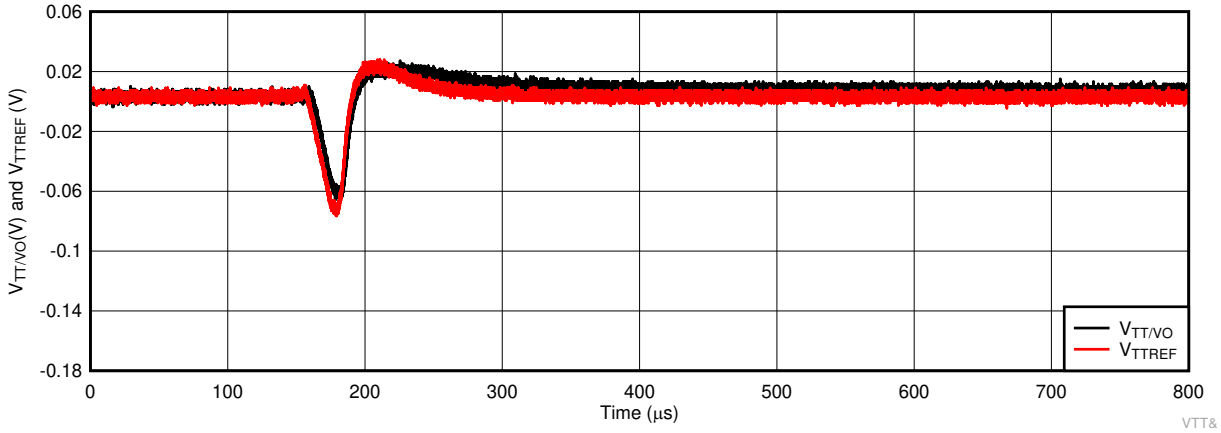


Figure 7-2. VTT/V_O and VTTREF Signals Track During the Event

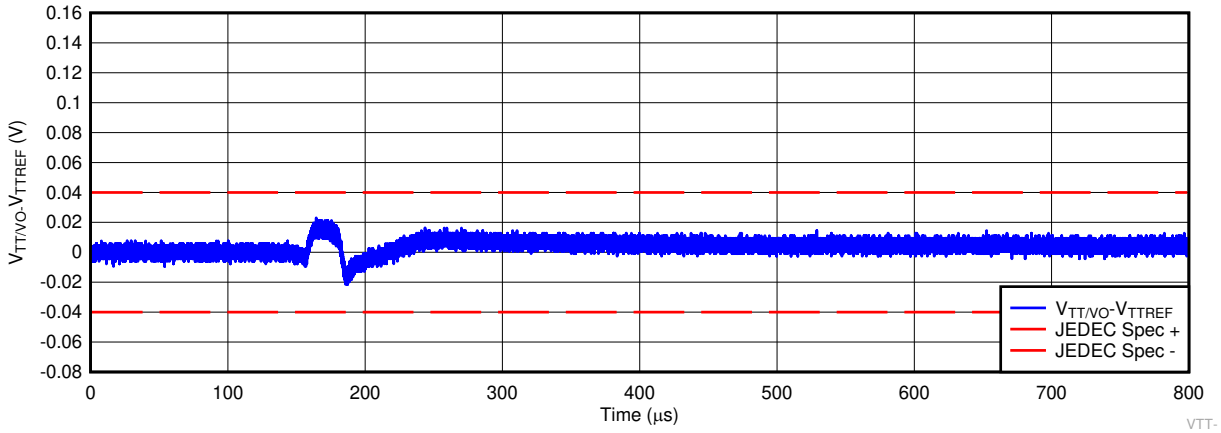


Figure 7-3. The Difference Between VTT/V_O and VTTREF is Approximately ±20mV

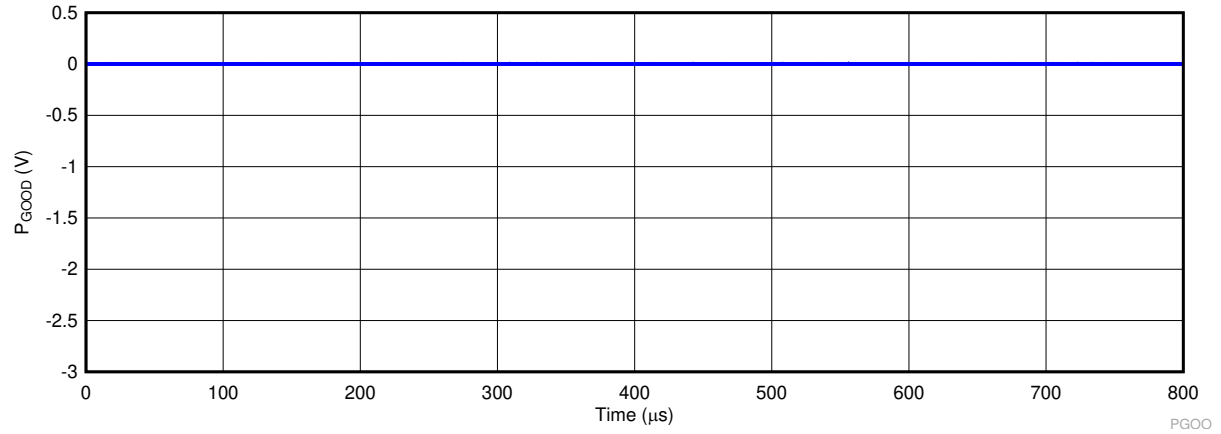


Figure 7-4. P_{GOOD} Signal is Not Triggered Since the Set Was Not Big Enough to Cause a Tracking Error

The following are examples of captured waveforms for an SEFI events from run number 109.

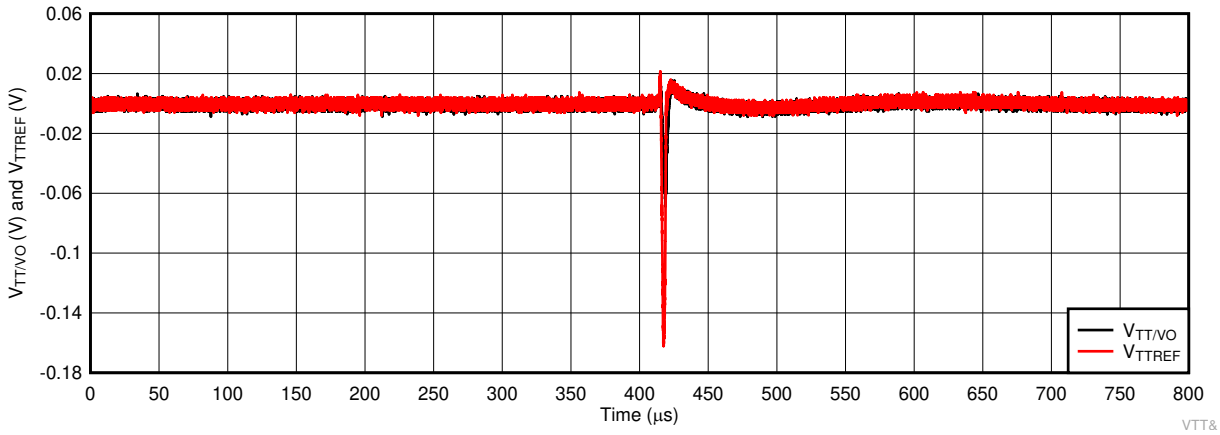


Figure 7-5. VTT/V_O and VTTREF Signals Tracking With Some Disparities During the Event

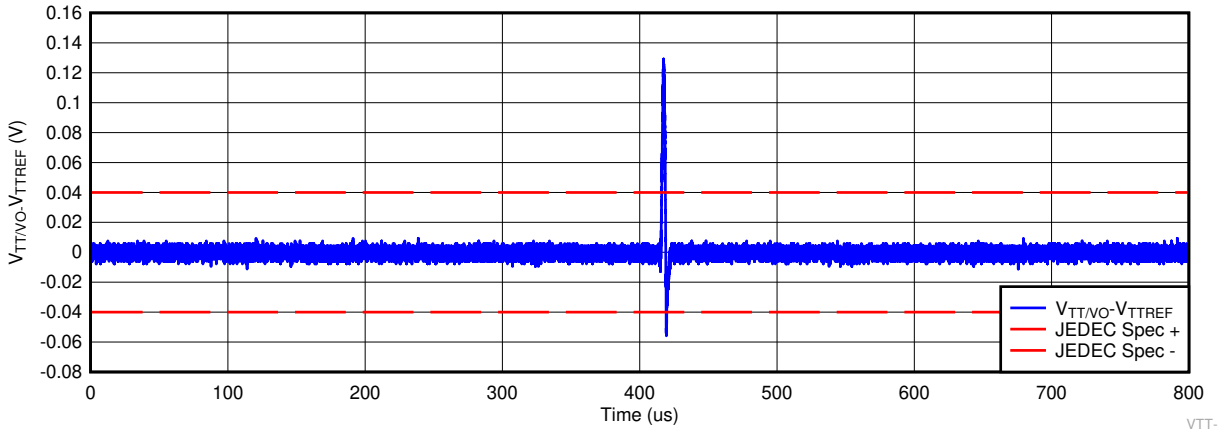


Figure 7-6. The Difference Between VTT/V_O and VTTREF, Exceeding ±40mV

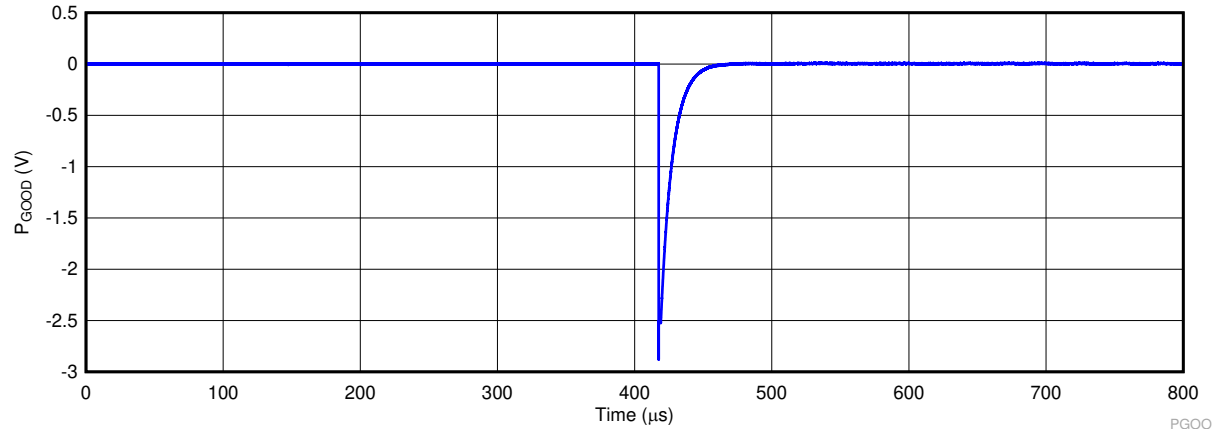


Figure 7-7. The Corresponding P_{GOOD} Signal Which Flags the Tracking Error Between VTT/V_O and VTTREF

7.3.1 DDR1 Mode

No SET or SEFI events of any kind were observed on any of the three TPS7H3301-SP devices tested over 32 runs in the DDR1 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3301-SP operating in DDR1 mode is SEFI-free up to a LET_{EFF} = 70 MeV-cm^2/ mg for fluences of up to 1 × 10^7 ions / cm^2. Table 7-3 shows a summary of the SET and SEFI tests.

Table 7-3. SET and SEFI Results for DDR1 Mode

Device Number	Run Number	T (°C)	LET_{EFF} (MeV-cm^2 / mg)	Fluence (ions / cm^2)	DDR Mode	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	V_{OUT} (V)	VTT/V_O LOAD (A)	V_{TTREF} LOAD (mA)	EVENTS ON VTT/V_O	EVENTS V_{TT} – V_{TTREF} > 40mV	EVENTS ON P_{GOOD}
1	1	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	–3.0	–10	0	0	0
1	2	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	10.0	0	0	0
1	3	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	10.0	0	0	0
1	4	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	10.0	0	0	0
1	5	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	10.0	0	0	0
1	6	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	0.0	0.0	0	0	0
1	7	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	–10	0	0	0
1	8	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	–3.0	10.0	0	0	0
1	9	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	–10	0	0	0
1	10	25	44.5	10^6	DDR1	2.50	2.95	2.50	1.25	–3.0	10.0	0	0	0
1	11	25	44.5	10^6	DDR1	2.50	3.50	2.50	1.25	–3.0	–10	0	0	0
1	12	25	44.5	10^6	DDR1	2.50	3.50	2.50	1.25	3.0	–10	0	0	0
1	17	25	44.5	10^6	DDR1	2.50	3.50	2.50	1.25	–3.0	–10	0	0	0
1	18	25	44.5	10^6	DDR1	2.50	3.50	2.50	1.25	3.0	–10	0	0	0
1	19	25	44.5	10^6	DDR1	2.50	2.90	2.50	1.25	–3.0	–10	0	0	0
1	20	25	44.5	10^6	DDR1	2.50	2.90	2.50	1.25	3.0	–10	0	0	0
1	30	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	0.0	–10	0	0	0
1	31	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	–3.0	–10	0	0	0
1	32	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	3.0	10.0	0	0	0
1	33	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	3.0	10.0	0	0	0
1	34	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	3.0	10.0	0	0	0
2	35	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	3.0	–10	0	0	0
2	64	25	70	10^6	DDR1	2.50	3.50	2.50	1.25	1.0	–10	0	0	0
2	65	25	70	10^7	DDR1	2.50	2.95	2.50	1.25	–1.0	–10	0	0	0
2	74	125	70	10^7	DDR1	2.50	2.95	2.50	1.25	0.0	–10	0	0	0
2	75	125	70	10^7	DDR1	2.50	2.95	2.50	1.25	0.0	–10	0	0	0
2	76	125	70	10^6	DDR1	2.50	2.95	2.50	1.25	–3.0	–10	0	0	0
2	77	25	70	10^6	DDR1	2.50	2.95	2.50	1.25	3.0	–10	0	0	0
3	93	25	52.5	10^7	DDR1	2.50	2.95	2.50	1.25	–3.0	–10	0	0	0
3	94	25	52.5	10^7	DDR1	2.50	2.95	2.50	1.25	3.0	–10	0	0	0
3	95	25	52.5	10^7	DDR1	2.50	2.95	2.50	1.25	0.0	–10	0	0	0
3	96	25	52.5	10^7	DDR1	2.50	2.95	2.50	1.25	0.0	–10	0	0	0

7.3.2 DDR2 Mode

A few SET and SEFI events were observed on two of the four TPS7H3301-SP devices tested over 23 runs in the DDR2 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3301-SP in DDR2 mode is SEE-free up to a LET_{EFF} = 52.5 MeV-cm^2 / mg for fluences of up to 2 × 10^7 ions/cm^2. Some SET/SEFI events and SEFIs were recorded in tests up to LET_{EFF} = 70 MeV-cm^2/mg for fluences of up to 5 × 10^7 ions / cm^2. The SET were all less than ±5mV (no risk to memory operation) and the SEFIs all generated valid P_{GOOD} signals. The cross section for the SEFIs is extremely low and calculated later. Table 7-4 lists a summary of the SET and SEFI results.

Table 7-4. SET/SEFI Results for DDR2 Mode

Device Number	Run Number	T (°C)	LET_{EFF} (MeV-cm^2 / mg)	Fluence (ions / cm^2)	DDR Mode	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	V_{OUT} (V)	VTT/V_O LOAD (A)	V_{TTREF} LOAD (mA)	EVENTS ON VTT/V_O	EVENTS V_{TT} – V_{TTREF} > 40mV	Events On P_{GOOD}
2	43	25	70	10^6	DDR2	1.8	2.5	1.8	0.9	0	–10	2	0	0
2	44	25	70	10^6	DDR2	1.8	2.5	1.8	0.9	0	–10	1	0	0
2	45	25	70	10^6	DDR2	1.8	2.5	1.8	0.9	–3	–10	0	0	0
2	46	25	70	10^6	DDR2	1.8	2.5	1.8	0.9	3	–10	0	0	0
2	47	25	70	10^6	DDR2	1.8	2.5	1.8	0.9	0	0	0	0	0
2	48	25	70	10^6	DDR2	1.8	3.5	1.8	0.9	0	10	0	0	0
2	49	25	70	10^6	DDR2	1.8	3.5	1.8	0.9	–3	–10	0	0	0
2	50	25	70	10^6	DDR2	1.8	3.5	1.8	0.9	3	–10	0	0	0
2	62	25	70	10^6	DDR2	2.5	3.5	1.8	0.9	1.9	–10	0	0	0
2	63	25	70	10^6	DDR2	2.5	3.5	1.8	0.9	–1.9	10	0	0	0
2	78	125	70	10^7	DDR2	2.5	3.5	1.8	0.9	0	–10	0	0	0
2	79	125	70	10^7	DDR2	2.5	3.5	1.8	0.9	–3	–10	0	0	0
2	80	125	70	10^7	DDR2	2.5	3.5	1.8	0.9	3	10	0	0	0
2	81	125	70	10^7	DDR2	1.2	2.9	1.8	0.9	0	–10	0	0	0
2	90	25	70	10^6	DDR2	2.5	2.5	1.8	0.9	0	–10	0	0	0
3	97	25	52.5	10^7	DDR2	1.8	2.5	1.8	0.9	–3	–10	0	0	0
3	98	25	52.5	10^7	DDR2	1.8	2.5	1.8	0.9	3	–10	0	0	0
3	99	25	52.5	10^7	DDR2	1.8	2.5	1.8	0.9	0	0	0	0	0
3	100	25	52.5	2 × 10^7	DDR2	1.8	2.5	1.8	0.9	0	0	0	0	0
6	111	25	70	2.7 × 10^7	DDR2	1.8	2.5	1.8	0.9	0	–10	28	10	10
6	112	25	70	5 × 10^7	DDR2	1.8	2.5	1.8	0.9	–3	–10	19	0	0
7	116	25	70	10^7	DDR2	1.8	2.5	1.8	0.9	0	–10	3	0	0
7	117	25	70	10^7	DDR2	1.8	2.5	1.8	0.9	0	–10	0	0	0

LEGEND

	Description	System Impact
	SET within JEDEC allowance of < ±40mV	None
	SET exceeding JEDEC allowance of < ±40mV	None if P_{GOOD} transition occurs
	SEFI with proper P_{GOOD} transition	Brief interruption of memory access – no data loss
	SEFI without proper P_{GOOD} transition	Potential data loss during illegal memory access

7.3.3 DDR3 Mode

A few SET and SEFI events were observed on two of the five TPS7H3301-SP devices tested over 27 runs in the DDR3 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3301-SP in DDR3 mode is SEE-free up to a LET_{EFF} = 52.5 MeV-cm^2 / mg for fluences of up to 2 × 10^7 ions / cm^2. Some SET and SEFI events and SEFIs were recorded in tests up to LET_{EFF} = 70MeV-cm^2/mg for fluences of up to 1 × 10^7 ions / cm^2. The SET were all less than ±5mV (no risk to memory operation) and the SEFIs all generated valid P_{GOOD} signals. The cross section for the SEFIs is extremely low and calculated later. Table 7-5 lists a summary of the SET and SEFI results.

Table 7-5. SET/SEFI Results for DDR3 Mode

Device Number	Run Number	T (°C)	LET_{EFF} (MeV-cm^2/mg)	Fluence (ions/cm^2)	DDR Mode	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	V_{OUT} (V)	VTT/V_O LOAD (A)	V_{TTREF} LOAD (mA)	Events on VTT/V_O	Events V_{TT} – V_{TTREF} > 40mV	Events on P_{GOOD}
2	51	25	70	10^6	DDR3	1.5	2.5	1.5	0.75	0	–10	0	0	0
2	52	25	70	10^6	DDR3	1.5	2.5	1.5	0.75	0	10	0	0	0
2	53	25	70	10^6	DDR3	1.5	2.5	1.5	0.75	–3	–10	0	0	0
2	54	25	70	10^6	DDR3	1.5	2.5	1.5	0.75	3	–10	0	0	0
2	55	25	70	10^6	DDR3	1.5	3.5	1.5	0.75	0	–10	0	0	0
2	56	25	70	10^6	DDR3	1.5	3.5	1.5	0.75	0	10	0	0	0
2	57	25	70	10^6	DDR3	1.5	3.5	1.5	0.75	–3	–10	0	0	0
2	58	25	70	10^6	DDR3	1.5	3.5	1.5	0.75	3	–10	0	0	0
2	66	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	0.5	10	0	0	0
2	67	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	–0.5	–10	0	0	0
2	68	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	1.5	10	2	0	0
2	69	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	1.5	10	0	0	0
2	70	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	1.5	10	0	0	0
2	71	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	–1.5	–10	0	0	0
2	72	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	3	10	0	0	0
2	73	25	70	10^6	DDR3	1.2	2.375	1.5	0.75	–3	–10	0	0	0
2	91	25	70	10^6	DDR3	1.5	2.375	1.5	0.75	1.5	10	0	0	0
2	92	25	70	10^6	DDR3	1.5	2.375	1.5	0.75	–1.5	–10	0	0	0
3	101	25	52.5	10^7	DDR3	1.5	2.375	1.5	0.75	-3	–10	0	0	0
3	102	25	52.5	10^7	DDR3	1.5	2.375	1.5	0.75	3	–10	0	0	0
3	103	25	52.5	10^7	DDR3	1.5	2.375	1.5	0.75	0	–10	0	0	0
3	104	25	52.5	2 × 10^7	DDR3	1.5	2.375	1.5	0.75	0	–10	0	0	0
4	109	25	70	10^7	DDR3	1.5	2.5	1.5	0.75	3	–10	1	1	1
4	110	25	70	10^7	DDR3	1.5	2.5	1.5	0.75	–3	–10	2	2	2
5	113	25	70	10^7	DDR3	1.5	3	1.5	0.75	0	–10	1	1	1
5	114	25	70	10^7	DDR3	1.5	3	1.5	0.75	–3	–10	3	0	0
6	115	25	70	10^7	DDR3	1.5	2.375	1.5	0.75	0	–10	6	2	2
8	146	25	75	10^7	DDR3	1.5	3	1.5	0.75	-3	-10	0	0	0
9	147	25	75	10^7	DDR3	1.5	3	1.5	0.75	-3	-10	0	0	0
10	148	25	75	10^7	DDR3	1.5	3	1.5	0.75	1	-10	0	0	0

LEGEND

	Description	System Impact
	SET within JEDEC allowance of less than ±40mV	None
	SET exceeding JEDEC allowance of less than ±40mV	None if P_{GOOD} transition occurs
	SEFI with proper P_{GOOD} transition	Brief interruption of memory access – no data loss
	SEFI without proper P_{GOOD} transition	Potential data loss during illegal memory access

1. Device number 10 is the TPS7H3302-SP.

7.3.4 DDR4 Mode

No SET or SEFI events of any kind were observed on any of the three TPS7H3301-SP devices tested over 30 runs in the DDR4 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3301-SP operating in DDR4 mode is SEE-free up to a LET_{EFF} = 70 MeV-cm^2 / mg for fluences of up to 2 × 10^7 ions / cm^2.

Table 7-6 shows a summary of the SET and SEFI tests. In DDR4 mode, the TPS7H3301-SP termination regulator was entirely SEE-free to a LET_{EFF} = 70 MeV-cm^2 / mg.

Table 7-6. SEFI Results for DDR4 Mode

Device Number	Run Number	T (°C)	LET_{EFF} (MeV-cm^2/mg)	Fluence (ions/cm^2)	DDR Mode	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	V_{OUT} (V)	VTT/V_O Load (A)	V_{TTREF} Load (mA)	Events On VTT/V_O	Events V_{TT} – V_{TTREF} > 40mV	Events On P_{GOOD}
1	13	25	44.5	10^6	DDR4	1.20	3.50	1.20	0.6	–3	–10	0	0	0
1	14	25	44.5	10^6	DDR4	1.20	3.50	1.20	0.6	3	–10	0	0	0
1	15	25	44.5	10^6	DDR4	1.20	2.375	1.20	0.6	–3	–10	0	0	0
1	16	25	44.5	10^6	DDR4	1.20	2.375	1.20	0.6	3	0	0	0	0
1	21	85	44.5	10^6	DDR4	1.20	3.50	1.20	0.6	–3	–10	0	0	0
1	22	85	44.5	10^6	DDR4	1.20	3.50	1.20	0.6	3	–10	0	0	0
1	23	85	44.5	10^6	DDR4	1.20	2.50	1.20	0.6	–3	–10	0	0	0
1	24	85	44.5	10^6	DDR4	1.20	2.50	1.20	0.6	3	0	0	0	0
1	25	25	44.5	10^6	DDR4	2.50	3.50	1.20	0.6	1.9	–10	0	0	0
1	26	25	44.5	10^6	DDR4	2.50	3.50	1.20	0.6	1	–10	0	0	0
1	27	25	44.5	10^6	DDR4	1.20	2.375	1.20	0.6	0	10	0	0	0
1	28	25	44.5	10^6	DDR4	1.20	2.375	1.20	0.6	1	10	0	0	0
1	29	25	44.5	10^6	DDR4	1.20	2.375	1.20	0.6	3	10	0	0	0
1	36	85	70.0	10^7	DDR4	1.20	3.50	1.20	0.6	–3	–10	0	0	0
1	37	85	70.0	10^7	DDR4	1.20	3.50	1.20	0.6	3	10	0	0	0
2	41	25	70.0	10^6	DDR4	1.20	2.375	1.20	0.6	–3	–10	0	0	0
2	42	25	70.0	10^6	DDR4	1.20	2.375	1.20	0.6	3	0	0	0	0
2	59	25	70.0	10^6	DDR4	1.20	2.375	1.20	0.6	0	–10	0	0	0
2	60	25	70.0	10^6	DDR4	1.20	3.50	1.20	0.6	0	–10	0	0	0
2	61	25	70.0	10^6	DDR4	1.20	3.50	1.20	0.6	0	–10	0	0	0
2	81	125	70.0	10^7	DDR4	1.20	2.90	1.20	0.6	0	–10	0	0	0
2	82	125	70.0	10^7	DDR4	1.20	2.90	1.20	0.6	–3	–10	0	0	0
2	83	125	70.0	10^7	DDR4	1.20	2.90	1.20	0.6	3	10	0	0	0
2	84	125	70.0	10^7	DDR4	1.20	3.50	1.20	0.6	0	–10	0	0	0
2	85	125	70.0	10^7	DDR4	1.20	3.50	1.20	0.6	–3	10	0	0	0
2	86	125	70.0	10^7	DDR4	1.20	3.50	1.20	0.6	3	–10	0	0	0
3	105	25	52.5	10^7	DDR4	1.20	2.375	1.20	0.6	–3	–10	0	0	0
3	106	25	52.5	10^7	DDR4	1.20	2.375	1.20	0.6	3	–10	0	0	0
3	107	25	52.5	10^7	DDR4	1.20	2.375	1.20	0.6	0	–10	0	0	0
3	108	25	52.5	2 × 10^7	DDR4	1.20	2.375	1.20	0.6	0	–10	0	0	0
8	149	25	75.0	10^7	DDR4	1.20	3	1.20	0.6	-3	-10	0	0	0
9	150	25	75.0	10^7	DDR4	1.20	3	1.20	0.6	-3	-10	0	0	0
10	151	25	75.0	10^7	DDR4	1.20	3	1.20	0.6	1	-10	0	0	0

1. Device number 10 is the TPS7H3302-SP.

8 Cross Section and Event Rate Calculations

A cross section for SET events was not calculated since, by definition, SET events were all smaller than the minimum event as specified by the JEDEC DDR specification, so SETs do not effect the operation or reliability of downstream memory components.

Cross sections for SEFI events were calculated for each DDR mode. In the case of DDR1 and DDR4 modes where no SEFI events occurred, the upper bound was calculated by a fluence limited test as shown in *Single-Event Effects (SEE) Confidence Interval Calculations*. All cross sections were done assuming a 95% confidence upper bound. Note that fluences for multiple runs were combined even though all the test conditions were not identical. For example, several input and output voltages were used. Given the small variation of input and output voltage ranges that were used, these must not strongly affect the occurrence of a SEE. Data from heavy-ion runs with LET_{EFF} = 70MeV-cm^2 / mg were used since these were the only ions capable of producing SEFIs in the TPS7H3301-SP during extensive testing.

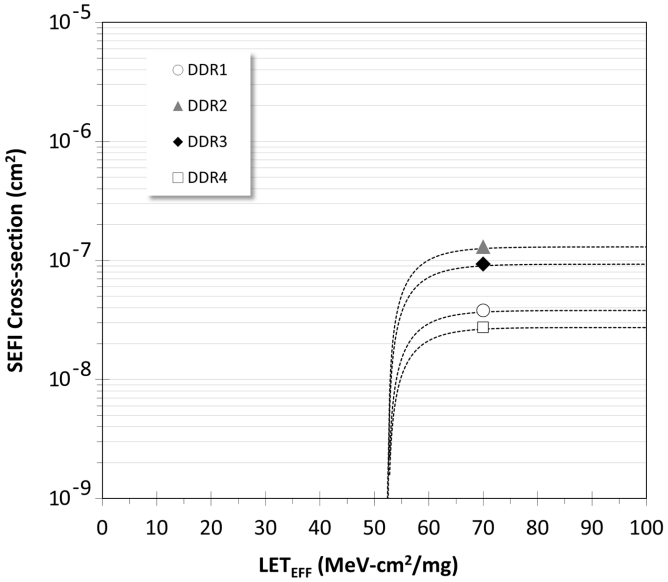


Figure 8-1. SEFI Cross Sections for TPS7H3301-SP as a Function of LET_{EFF}

Table 8-1. Weibull Fitting Parameters for SEFI Cross Sections

Parameter	DDR1	DDR2	DDR3	DDR4
Saturation cross section	3.8E–08	1.3E–07	9.3E–08	2.7E–08
Onset LET	52.5	52.5	52.5	52.5
Width	5	5	5	5
Fitting	1	1	1	1

Event rates were calculated for LEO(ISS) and GEO environments by combining CREME96 orbital integral flux estimations and simplified SEE cross-sections according to methods described in *Heavy Ion Orbital Environment Single-Event Effects Estimations*. A minimum shielding configuration of 100mils (2.54mm) of aluminum, and *worst-week* solar activity (which is similar to a 99% upper bound for the environment) is assumed. Using the 95% upper-bounds for the SEL and SEFI the event-rates of the TPS7H3301-SP are listed in Table 8-2 and Table 8-3, respectively.

Table 8-2. SEL Event Rate Calculations for Worst-Week LEO and GEO Orbits

Orbit Type	Mode	Onset LET (MeV–cm^2 / mg)	CREME96 Integral Flux (/ day–cm^2)	σ_{SAT} (cm^2)	Event Rate (/ day)	Event Rate (FIT)	MTBE (years)
LEO(ISS)	DDR1	70	8.6E–05	1.2E–07	1.1E–11	4.4E–04	2.6E+08
GEO			2.5E–04		3.0E–11	1.3E–03	9.1E+07
LEO(ISS)	DDR2	70	8.6E–05	7.4E–08	6.4E–12	2.7E–04	4.3E+08
GEO			2.5E–04		1.8E–11	7.5E–04	1.5E+08
LEO(ISS)	DDR4	70	8.6E–05	7.4E–08	6.4E–12	2.7E–04	4.3E+08
GEO			2.5E–04		1.8E–11	7.5E–04	1.5E+08

Table 8-3. SEFI Event Rate Calculations for Worst-Week LEO and GEO Orbits

Orbit Type	Mode	Onset LET (MeV–cm^2 / mg)	CREME96 Integral Flux (/ day–cm^2)	σ_{SAT} (cm^2)	Event Rate (/ day)	Event Rate (FIT)	MTBE (years)
LEO(ISS)	DDR1	52.5	3.3E–04	3.8E–08	1.3E–11	5.3E–04	2.2E+08
GEO			1.1E–03		4.1E–11	1.7E–03	6.8E+07
LEO(ISS)	DDR2	52.5	3.3E–04	1.3E–07	4.3E–11	1.8E–03	6.3E+07
GEO			1.1E–03		1.4E–10	5.8E–03	2.0E+07
LEO(ISS)	DDR3	52.5	3.3E–04	9.3E–08	3.1E–11	1.3E–03	8.9E+07
GEO			1.1E–03		9.9E–11	4.1E–03	2.8E+07
LEO(ISS)	DDR4	52.5	3.3E–04	2.7E–08	9.0E–12	3.7E–04	3.1E+08
GEO			1.1E–03		2.9E–11	1.2E–03	9.5E+07

MTBE is the mean-time-between-events in years at the given event rates. These rates clearly demonstrate the SEE robustness of the TPS7H3301-SP DDR Termination Regulator in two harshly conservative space environments. Customers using the TPS7H3301-SP must only use the above estimations as a rough guide and TI recommends that event rate calculations based on specific mission orbital and shielding parameters be performed to determine if the product satisfies the reliability requirements for the specific mission.

9 Summary

The purpose of this study was to characterize the effect of heavy-ion irradiation on the single-event effect (SEE) performance of the TPS7H3301-SP/TPS7H3302-SP DDR termination regulator. Table 9-1 lists a tabulated summary of the results of all of the SEE testing. Heavy-ions with LET_{EFF} of 44.5, 52.5, 70, 75.0MeV-cm^2 / mg were used to irradiate three production devices in hundreds of experiments with heavy-ion fluences ranging from 1×10^6 to 5×10^7 ions / cm^2 per run, over a variety of DDR modes, input and output voltage conditions, load conditions, and temperatures.

The results demonstrate that the TPS7H3301-SP is SEE-free (no SEL, SET, or SEFI observed) under almost all conditions up to LET_{EFF} = 70MeV-cm^2 / mg. DDR2 and DDR3 modes exhibited a small number of SET and SEFI events. SET events do not impact on memory function because the events were significantly below the allowed JEDEC DDR specification. The SEFI events were rare (less than 1.4×10^{-10} events per day in GEO) and generated valid P_{GOOD} transitions during the brief events, and as a result, completely protecting downstream memory from illegal accesses. The few SEFI events do not effect downstream memory reliability.

Table 9-1. Summary of All Heavy-Ion SEE Results for the TPS7H3301-SP

LET_{EFF} (MeV-cm^2/mg)	DDR1	DDR2	DDR3	DDR4
44.5	SEE-free	SEE-free	SEE-free	SEE-free
52.5	SEE-free	SEE-free	SEE-free	SEE-free
75	SEE-free	SEL-free SEFI, low σ	SEL-free SEFI, low σ	SEE-free

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11 Revision History

Changes from Revision B (December 2023) to Revision C (January 2024)	Page
• Updated to include QMLP version of the TPS7H3301-SP, the TPS7H3302-SP	1
• Updated formatting to document	1
• Updated SEL results table to include QMLP device #10 and updated TPS7H3302-QMLP to TPS7H3302-SP	10
• Updated SEB results table to include QMLP device #10 updated TPS7H3302-QMLP to TPS7H3302-SP	12
• Updated SET and SEFI results table for DDR3 Mode to include QMLP device #10 updated TPS7H3302-QMLP to TPS7H3302-SP	18
• Updated to include QMLP device updated TPS7H3302-QMLP to TPS7H3302-SP	22

Changes from Revision A (January 2018) to Revision B (December 2023)	Page
• Updated SET and SEFI results table for DDR4 Mode to include QMLP device number 10	19

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