Application Note

A Methodology to Achieve Full-Range ZVS for Half-Bridge SRDAB in Active Pack Balancing Applications

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ABSTRACT

Due to its cost-effective half-bridge configuration, inherent bidirectional power flow capabilities, and wide input-to-output voltage operability, the Dual-Half-Bridge Series Resonant (DBSRC) DC/DC converter stands as a highly suitable topology for Active Pack Balancing (APB) applications across series-connected battery packs in Energy Storage Systems (ESS). Implementing soft-switching control for the active power devices within this topology yields distinct operational merits: mitigating switching losses to secure elevated conversion efficiency, suppressing the voltage derivative (dv/dt) to alleviate electromagnetic interference (EMI), and bolstering converter reliability by eliminating deleterious high-voltage ringing across the power transistors. Consequently, this application note elucidates Variable Frequency Modulation (VFM) and Phase Shift Modulation (PSM) methodologies that deliver unmitigated Zero Voltage Switching (ZVS) turn-on capabilities across the entire operating input voltage and load profile, achieving this without incurring any supplementary hardware costs.

Trademarks

1 Introduction

Figure 1-1 shows the schematic diagram of the DBSRC topology, wherein all active power devices are modulated via single-phase-shift control. Under this modulation scheme, the complementary switches within the same bridge leg (for example, Q1) and (Q2) operate with a 50% duty cycle, while a controlled phase-shift time is introduced between the primary and secondary bridge legs (Q1 and Q3). The effect of dead time is neglected in this baseline operational analysis.

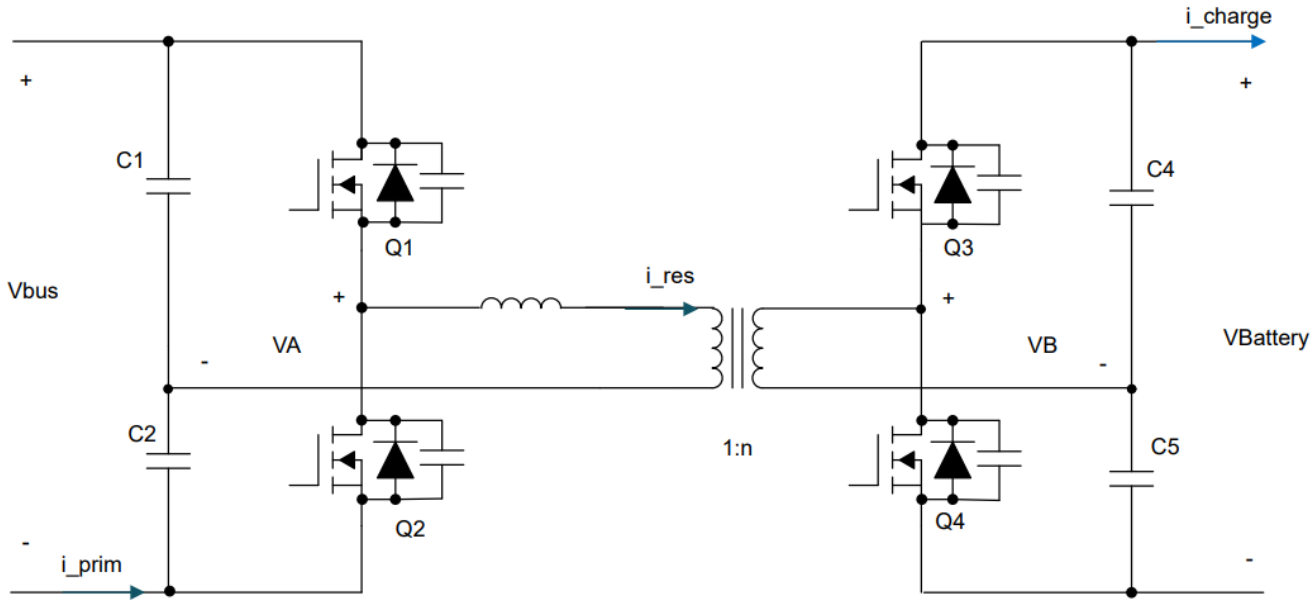

Figure 1-1. DBSRC Topology

To effectively achieve Zero Voltage Switching (ZVS) for an active device, a sufficient negative channel current must flow through the switch prior to the turn-on, thereby discharging the energy stored in its parasitic junction capacitance until the drain-to-source voltage drops to zero. Figure 1-2 shows the operational waveforms of the DBSRC, including the primary- and secondary-side leg voltages VA and VB, alongside the resonant inductor current i_res. Taking the ZVS process of Q3 as an illustrative example: prior to the conduction of Q3, switches Q1 and Q4 are turned on. Due to the positive voltage drop applied across the resonant inductor, i_res transitions from a negative to a positive value. At this juncture, when the complementary secondary-side switches are gated off, the secondary-side current is diverted through the anti-parallel diode or body diode of Q3, forcing the junction capacitance to fully discharge. Once this capacitance voltage drops to 0V, Q3 is turned on under zero-voltage conditions, thereby securing a soft-switching transition. The ZVS mechanisms for the remaining active power devices follow an identical operational sequence.

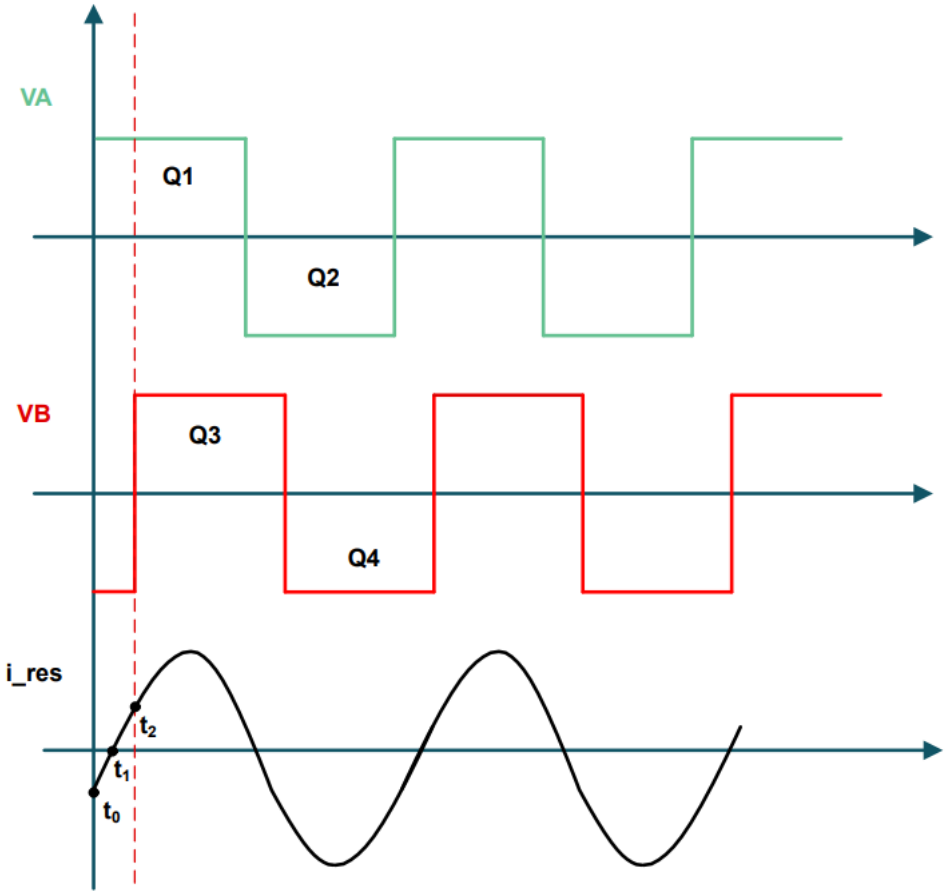

Figure 1-2. Operational Waveforms and Time-Domain Analysis

Defining the turn-on instance of Q3 as t0, the current zero-crossing instance as t1, and the turn-on instance of Q3 as t2, the interval from t0 to t2 represents the phase-shift time duration, denoted as θ. To guarantee that a sufficient negative boundary current flows through the respective active power devices prior to their conduction, thereby ensuring that the parasitic junction capacitance is thoroughly discharged to achieve unmitigated ZVS control.

2 Mathematical Derivation of ZVS Phase-Shift Timing

The theoretical evaluation is conducted utilizing the Fundamental Harmonic Analysis (FHA) method, which selectively isolates and analyzes the fundamental components of the normalized leg voltages, VA and VB. Following normalization, the mathematical expressions for the fundamental components of VA and VB are formulated as follows:

$$v_{A\_pu}(t) = \frac{4}{\pi}\sin(wt) \tag{1}$$

$$v_{B\_pu}(t) = \frac{4M}{\pi}\sin[wt - \theta] \tag{2}$$

where M denotes the voltage gain ratio, ω is the switching angular frequency

$$M = \frac{VBattery}{nVbus} \tag{3}$$

Consequently, the fundamental component of the resonant inductor current, i_res, can be derived and expressed as follows:

$$i_{res}(t) = \frac{v_{A\_pu}(t) - v_{B\_pu}(t)}{Xres} \tag{4}$$

where *X*res represents the total impedance of the resonant network. The resonant tank consists of a series resonant inductor Lr and a resonant capacitor Cr. Since the current loop operates the system above the resonant frequency (fs > fr) to maintain an inductive tank for zero-voltage switching, the net fundamental inductive reactance Xres at any given switching frequency is defined as:

$$Xres = \omega Lr - \frac{1}{\omega Cr} > 0 \tag{5}$$

Using phasor analysis $v_{A\_pu}(t)$ with as the reference phasor, the net voltage phasor driving the resonant tank is $\dot{V}_A - \dot{V}_B$. Solving the system equation $\dot{I_{res}} = (\dot{V}_A - \dot{V}_B)/jXres$ yields the rigorous time-domain fundamental resonant current $i_{res}(t)$:

$$i_{res}(t) = \frac{2Vbus}{\pi \cdot Xres} \cdot [M \cdot \sin\theta \cdot \cos(\omega t) + (1 - M \cdot \cos\theta) \cdot \sin(\omega t)] \tag{6}$$

To solve for the precise moment the inductor current crosses zero $i_{res}(t) = 0$, we set the inner bracket of the time-domain current equation to zero:

$$M \cdot \sin\theta \cdot \cos(\omega t_{zero}) = -(1 - M \cdot \cos\theta) \cdot \sin(\omega t_{zero}) \tag{7}$$

Dividing both sides by $\cos(\omega t_{zero})$ yields the tangent relationship:

$$\tan(\omega t_{zero}) = \frac{-M\sin\theta}{1 - M\cos\theta} \tag{8}$$

Thus, the exact electrical angle at which the fundamental current crosses zero during the half-cycle is:

$$\omega t_{zero} = \arctan\left(\frac{-M\sin\theta}{1 - M\cos\theta}\right) \tag{9}$$

To ensure perfectly symmetrical switching current amplitudes and eliminate high circulating reactive currents when $M \neq 1$, your ideal physical target is to position this zero-crossing point exactly at the midpoint between the primary turn-on instance t_0 ($\omega t_0 = 0$) and the secondary turn-on instance t_2 ($\omega t_2 = 0$) :

$$\omega t_{zero} = \frac{0 + \theta}{2} = \frac{\theta}{2} \tag{10}$$

Substituting this target into the tangent relationship:

$$\frac{\sin\left(\frac{\theta}{2}\right)}{\cos\left(\frac{\theta}{2}\right)} = \frac{1 - M + 2M\sin^2\left(\frac{\theta}{2}\right)}{2M\sin\left(\frac{\theta}{2}\right)\cos\left(\frac{\theta}{2}\right)} \Rightarrow 0 = 1 - M \Rightarrow M = 1 \quad (11)$$

This mathematical proof reveals a critical hardware constraint of the Half-Bridge SPS architecture: **it is mathematically impossible to force the current zero-crossing point exactly to the midpoint** $(\theta/2)$ **when** $M \neq 1$ **.** Because a half-bridge cannot utilize an inner-phase shift angle to match the voltage amplitudes, the current waveform is naturally skewed. Forcing the system to stay at the absolute ZVS boundary creates massive reactive current stress on one side. Therefore, a dynamic tracking function must be established.

To resolve this conflict, we introduce a dynamic tracking factor $\lambda(M)$ that dictates the zero-crossing position relative to θ as a function of the real-time voltage gain M:

$$\omega_s t_{\text{zero}} = \lambda(M) \cdot \theta \quad (12)$$

Where $\lambda\left(M\right) = \frac{1}{1+M}$

- When **M = 1**, $\lambda(1) = 0.5$, forcing the zero-crossing to converge perfectly at the midpoint ($\omega_s t_{\text{zero}} = 0.5\theta$).
- When **M > 1** (Boost mode), $\lambda < 0.5$, the zero-crossing smoothly shifts toward t_0 , securing primary ZVS while clamping down on excessive secondary peak currents.
- When **M < 1** (Buck mode), $\lambda > 0.5$, the zero-crossing smoothly shifts toward t_2 , securing secondary ZVS while preventing primary current spikes.

Substituting $\lambda(M)$ into our zero-crossing equation yields:

$$\tan\left(\frac{1}{1+M}\theta\right) = \frac{1 - M\cos\theta}{M\sin\theta} \quad (13)$$

Since this expression is a transcendental equation, it cannot be solved analytically for θ . To run this on a microcontroller (like the TI C2000 F28P55) with minimal computational latency, we perform a multi-point least-squares error minimization fitting against the strict mathematical bounds ($\theta_{\text{strict}} = \arccos[\min(M, 1/M)]$) over the operational range $M \in [0.5, 2.0]$.

The optimized trajectory-tracking phase shift angle can be accurately generalized by a first-order absolute error envelope polynomial:

$$\theta_{\text{track}} = \arccos\left[\min\left(M, \frac{1}{M}\right)\right] \cdot (1 - 0.25 \cdot |M - 1|) \quad (14)$$

Considering the margin for deadtime and Coss of switches,

$$\theta_{\text{track}} = \arccos\left[0.8 \cdot \min\left(M, \frac{1}{M}\right)\right] \cdot (1 - 0.25 \cdot |M - 1|) \quad (15)$$

3 Simulation in PLECS

A 300W DBSRC power stage model was constructed within the PLECS simulation software to perform the evaluation. The designated electrical specifications for this simulation platform comprise a nominal system input voltage Vin of 24V, a regulated output voltage range Vout spanning from 40V to 60V, and a rated full-load output current Iout of 5A.

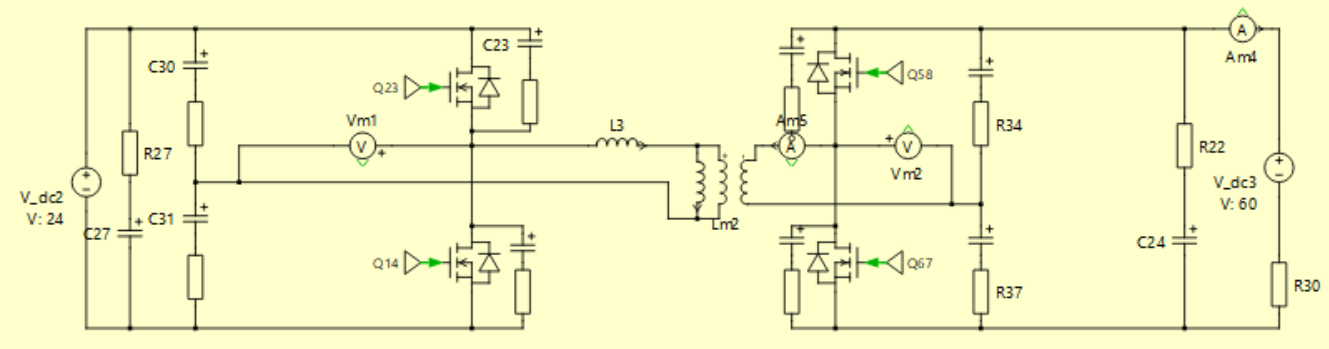

Figure 3-1. PLECS Schematic and Control Model of the DBSRC Topology

Figure 3-2 shows the architecture of the PWM control module. Mechanically, this module generates phase-shifted PWM gating signals for the full-bridge networks on both sides of the DBSRC. Based on the real-time power flow direction and the calculated phase-shift time duration, the module dynamically selects appropriate phase-offset edge instances to ultimately deliver four independent gate-drive output signals.

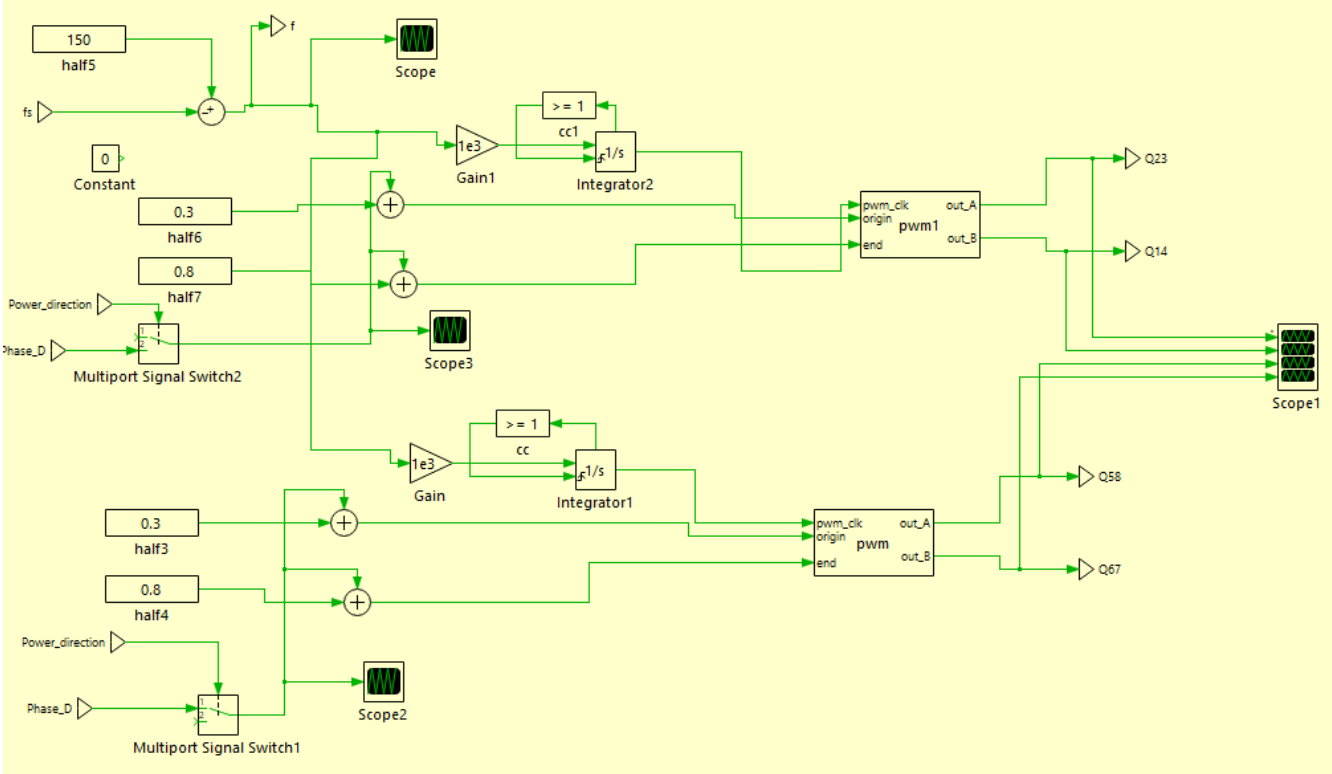

Figure 3-2. Implementation of the PWM Control Module

Under forward operation, with an electrical test condition of Vin = 24V, Vout= 60V, and Iout = 5A, the explicit Zero Voltage Switching (ZVS) transition and control process for the four active power switches are captured and illustrated in Figure 3-3.

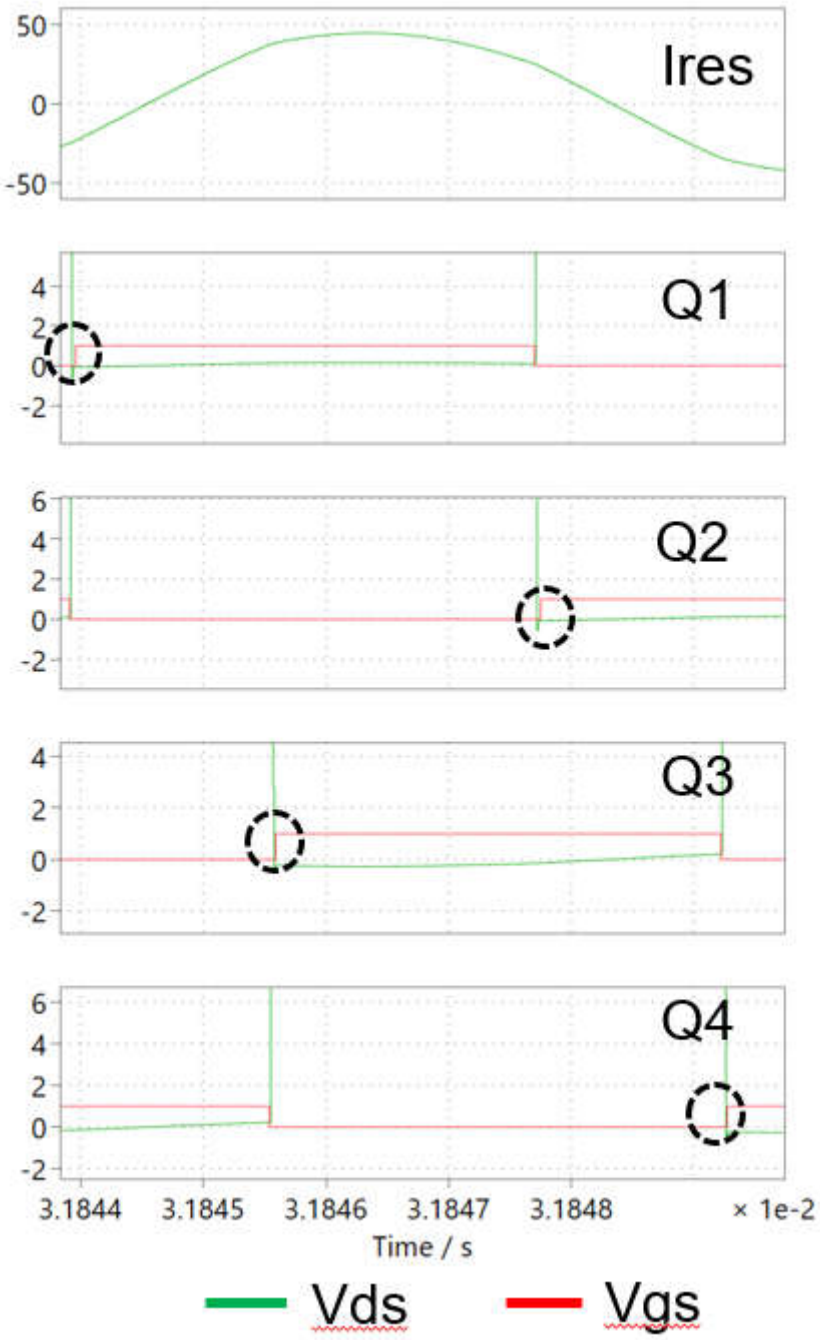

Figure 3-3. ZVS Control and Switching Transitions of All Power Switches Under Forward Operation

Under reverse operation, with an electrical test condition of Vin = 60V, Vout= 24V, and Iout = 5A, the explicit Zero Voltage Switching (ZVS) transition and control process for the four active power switches are captured and shown in Figure 3-4.

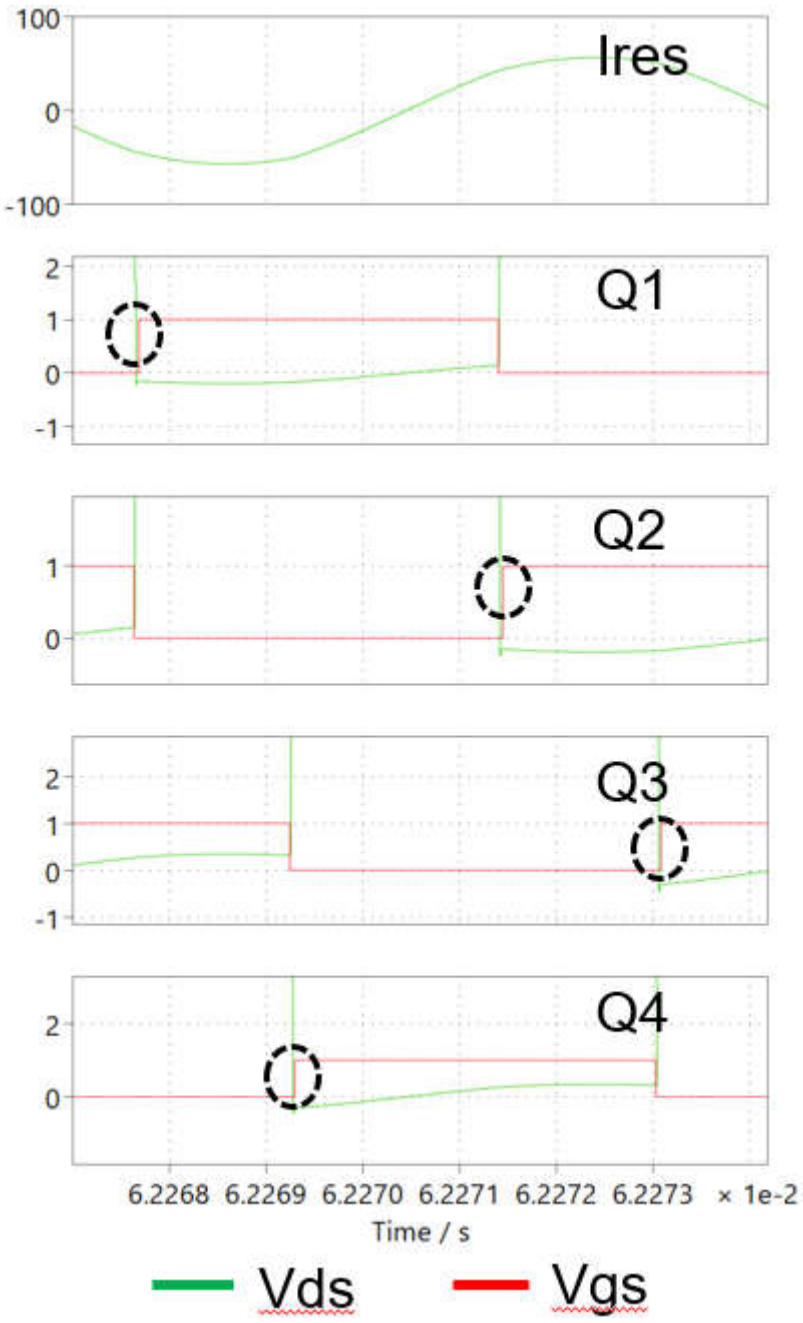

Figure 3-4. ZVS Control and Switching Transitions of All Power Switches Under Reverse Operation

4 Summary

Aimed at Active Pack Balancing (APB) applications for series-connected battery packs in Energy Storage Systems (ESS), this application note proposed a robust soft-switching control methodology tailor-made for the Dual-Bridge Series Resonant (DBSRC) DC/DC converter. To bolster conversion efficiency and system reliability, the control strategies centered around Variable Frequency Modulation (VFM) and Phase Shift Modulation (PSM) were comprehensively formulated and analyzed. Without incurring any supplementary hardware costs, the proposed scheme successfully achieves unmitigated Zero Voltage Switching (ZVS) turn-on control across the entire operating input voltage spectrum and full-load profile. Consequently, this design significantly mitigates switching losses, suppresses dv/dt induced electromagnetic interference (EMI), and minimizes the detrimental risks of high-voltage ringing across power transistors.

5 References

1. Texas Instruments, *Bidirectional Isolated Dual-Bridge Series Resonant DC/DC Converter Reference Design for Pack Balance*, design guide.

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