Application Note

Demystifying CSI-2 Aggregation Bandwidth for FPD-Link III Deserializers

Jiawei Hu

ABSTRACT

ADAS FPD-Link III deserializer devices are designed to take sensor data from multiple remote serializers and aggregate the data to processors using the MIPI CSI-2 video format. A deeper understanding of the input and output bandwidth accurate calculation of FPD-Link III deserializer devices is important when selecting the right device. This application note will break down the details of CSI-2 aggregator of ADAS FPD-Link III deserializer devices and provide guidance on how to account for the input and output bandwidth when aggregating multiple image sensors.

1 Introduction

FPD-Link III deserializer devices are capable of aggregating video streams from either two or four incoming serializers to the processors with MIPI CSI-2 interface. CSI-2 protocol divides video data into packets at a line level so the line length of each image sensor is a critical factor in determining the aggregated bandwidth at the deserializer output. During the transmission of data on the CSI-2 port, the D-PHY output port will transition between low power (LP) and high speed (HS) modes. In HS mode, CSI-2 data packets will be transmitted such as long packets (each long packet contains a single video line) and short packets (containing video timing information like frame start and frame end). In LP mode, the interface is idle with no data being sent on the interface. This application note will provide an overview of MIPI CSI-2 as it relates to camera SerDes, break down the details of FPD-Link III deserializer CSI-2 aggregation capabilities and provide the guidance on how to evaluate FPD-Link deserializer devices' input and output bandwidth.

2 ADAS FPD-Link III Deserializer Overview

ADAS CSI-2 FPD-Link III deserializer products support either two or four FPD-Link inputs and with either single or dual MIPI CSI-2 outputs, the Table 2-1 lists the supported data rates of devices in the FPD-Link III deserializer portfolio.

Table 2-1. ADAS FPD-LINK Deserializer Devices

Part Number	FPD-Link RX Ports	CSI-2 Ports	Nominal CSI-2 Output Bandwidth	Max CSI-2 input Bandwidth Per Port
DS90UB936-Q1	2	1x4 Lane	6.656Gbps	2.528Gbps
		2x2 Lane		
DS90UB954-Q1	2	1x4 Lane	6.656Gbps	3.328Gbps
		2x2 Lane		
DS90UB964-Q1	4	2x4 Lane	12.8Gbps (6.4Gbps/port)	1.330Gbps
DS90UB962-Q1	4	1x4 Lane	6.656Gbps	2.528Gbps
DS90UB662-Q1	4	1x4 Lane	6.656Gbps	2.528Gbps
DS90UB960-Q1	4	2x4 Lane	13.312Gbps (6.656Gbps/port)	3.328Gbps

3 MIPI CSI-2 Overview

3.1 MIPI CSI-2 Frame Break Down

There are two different packet types of MIPI CSI-2, long and short packets. Short packets use a 32-bit frame structure and are commonly used for signaling frame start, frame end, or other synchronization information from the source. Long packets have a variable byte count based on the format of the data to be transmitted and are typically used to transmit a single video line. In each long and short packet, there is a header which stores information about the type of packet (data ID) and which virtual channel (VC) source the information came from.

One typical video frame transmitted via CSI-2 can be broken down into the following items.

- Frame start – 32-bit short packet
- Low-Power State (LPS)
- The 1st line of valid video data – Long packet, which is further divided into:
  - 32-bit packet header (packet header)
  - Valid data, for example, for RAW12, two pixels have 24 bits
  - 16-bit packet footer (packet footer)
- Low-Power State (LPS)
- The 2nd line of valid video data
- Low-Power State (LPS)
- The 3rd line of valid video data
- …
- Frame end – 32-bit short packets

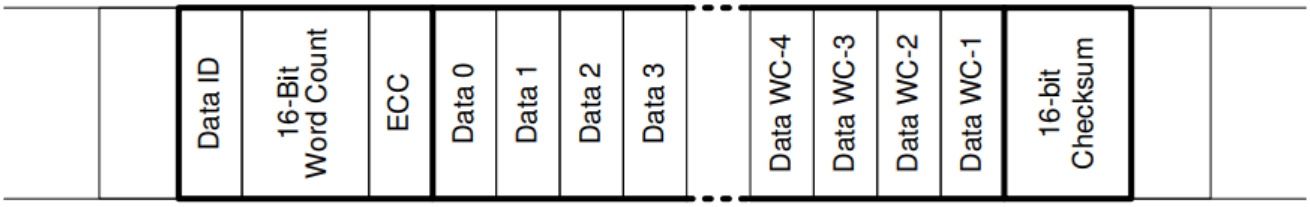

Figure 3-1. MIPI CSI-2 Long Packets

Figure 3-2. MIPI CSI-2 Short Packets

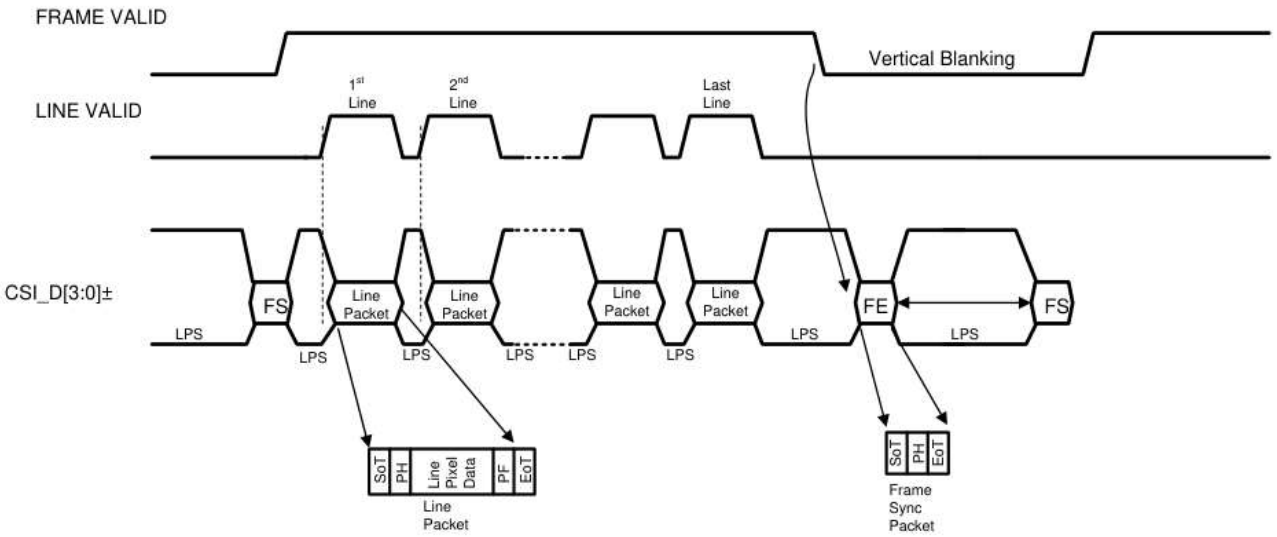

Figure 3-3. Long Line Packets and Short Frame Sync Packets

3.2 MIPI CSI-2 Overhead Introduction

Between long and short packets, and between different long packets, the CSI-2 transmitter must enter low-power state (LPS). The transmitter is also required to transition from Low-Power to High-Speed signaling mode. During the LPS and time associated with the transition, the transmitter is idle and no data packets that can be sent, which means the CSI-2 output bandwidth is reduced.

The minimum CSI-2 High-Speed data transmission overhead consists of T_{LPX}, $T_{HS-PREPARE}$, $T_{HS-ZERO}$, $T_{HS-SYNC}$, $T_{HS-TRAIL}$, and $T_{HS-EXIT}$ as shown in Figure 3-3. The bandwidth is further reduced when operating in discontinuous CSI-2 Clock mode as it brings more CSI-2 overhead since data also cannot be sent while the clock lane is either in LP mode or transiting to HS mode, as shown in Figure 3-4.

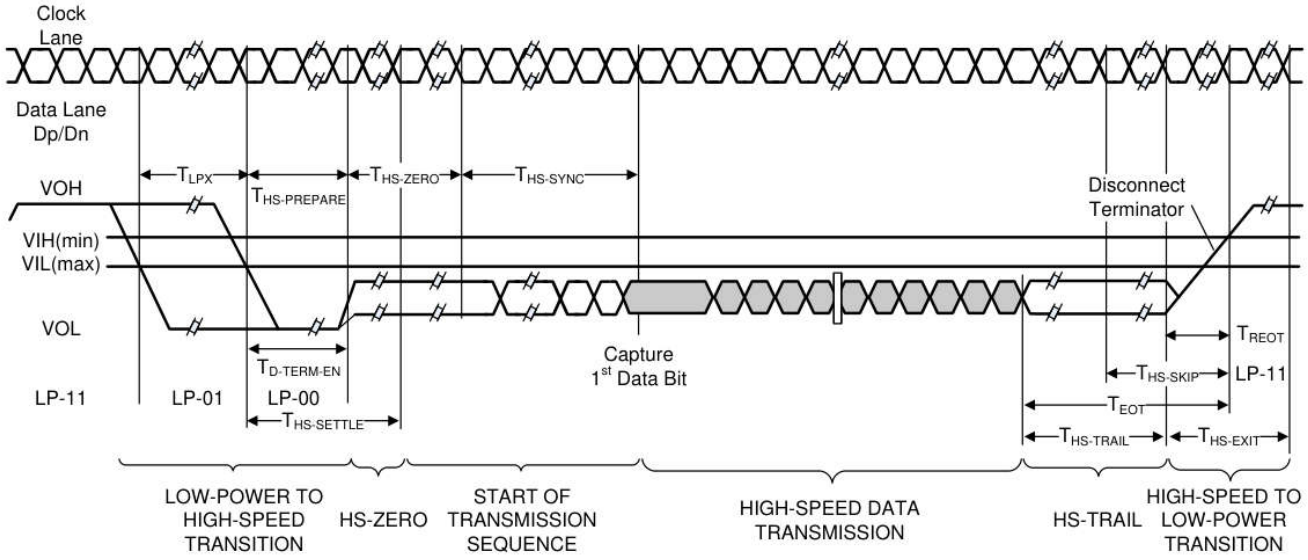

Figure 3-4. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

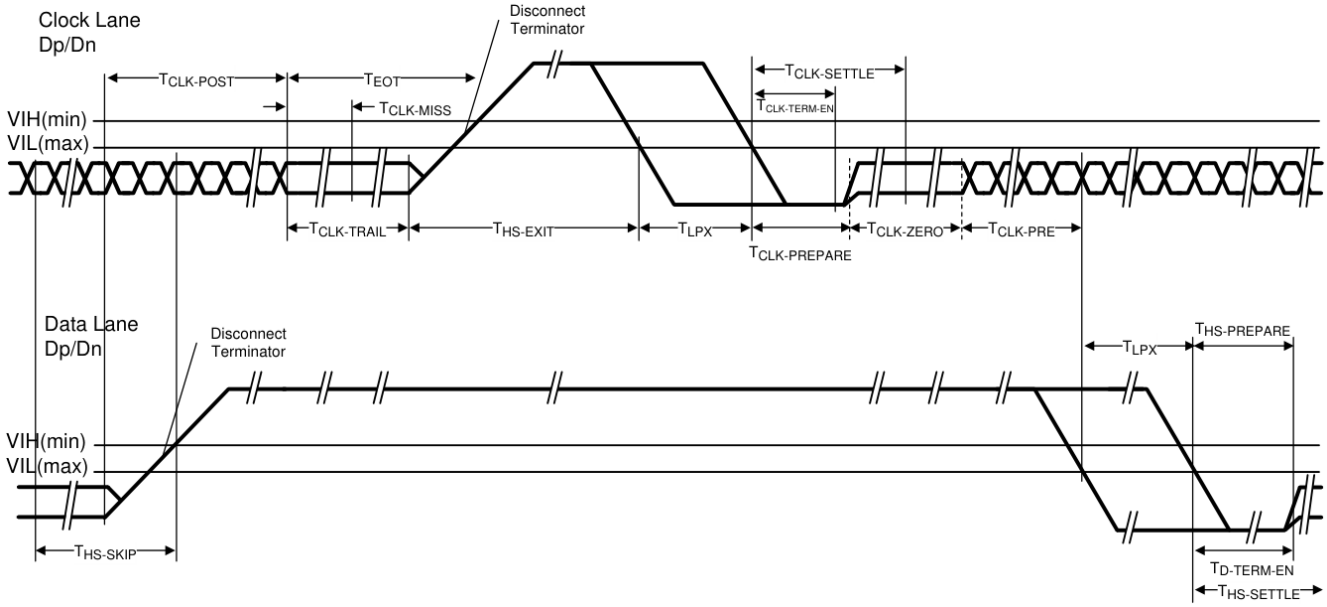

Figure 3-5. High Speed Data Transmission Burst

4 CSI-2 Input Bandwidth Calculation

When considering CSI-2 input bandwidths for the purposes of aggregation, it is necessary to evaluate the bandwidth required for each video line since CSI-2 packetization occurs on a packet level and overhead is introduced as the CSI-2 lanes transition in and out of LP mode. Therefore, Equation 1 represents the average input bandwidth, but it is not sufficient to determine how much bandwidth each input stream consumes at the deserialzier CSI-2 output.

$$\mathrm{InputBW} = \mathrm{H_{total}}{*}\mathrm{V_{total}}{*}\mathrm{F_{ps}}{*}\mathrm{Bitsperpixel} \quad (1)$$

Instead, the input bandwidth must be calculated as the following when evaluating aggregation use cases.

$$\mathrm{HorizontalLineTime} = \frac{1}{\mathrm{F_{ps}}{*}\mathrm{V_{total}}} \quad (2)$$

$$\mathrm{LineinputBW} = \frac{\mathrm{H_{active}}{*}\mathrm{Bitsperpixel}}{\mathrm{HorizontalLineTime}} \quad (3)$$

Where,

- H_{total} is the total horizontal line length in pixels
- V_{total} is the total number of lines
- Bits/pxl is the number of bits per pixel
- F_{ps} is the frame refresh rate

5 CSI-2 Output Bandwidth Calculation

5.1 CSI-2 Aggregation Overview

As shown in Figure 5-1, there are several steps to aggregate data from the FPD-Link receiver inputs onto the CSI-2 outputs:

- The FPD-Link inputs are decoded by each FPD-Link receiver (RX) and stored in the corresponding RX buffers
- The CSI aggregator rotates through the enabled video buffers if valid data is ready
- If ready, the CSI aggregator extracts the data and sends the data to the assigned CSI-2 port

The data in each RX buffer is only extracted by one CSI aggregator and is cleared automatically.

During the process of CSI aggregation, there are two major types of CSI-2 forwarding modes for FPD-Link hub devices: best-effort round robin forwarding and synchronized forwarding. The best-effort round robin forwarding is the most common and straightforward aggregation method. Compared to best-effort round robin forwarding mode, synchronized forwarding requires the enabled RX ports to be synchronized and can be divided into the following three kinds of forwarding modes based on different CSI-2 frame structures. For more details, users can refer to the corresponding deserializer data sheet to further explore the forwarding modes.

- Basic Synchronized forwarding
- Line-Interleave forwarding
- Line-Concatenated forwarding

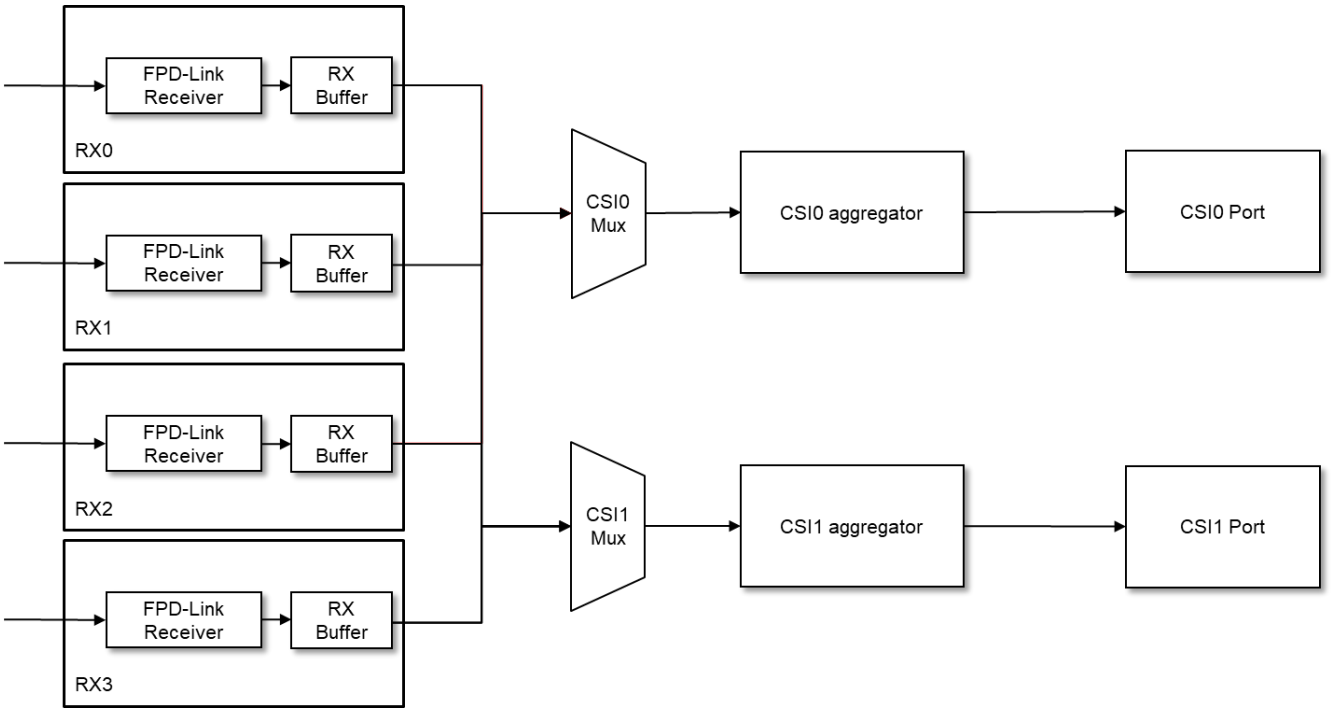

Figure 5-1. CSI-2 Aggregation Breakdown

5.2 CSI-2 Output Bandwidth Calculation

The CSI-2 overhead varies with different forwarding modes. For example, as shown in Figure 5-2 and Figure 5-3, Line-Interleave forwarding with four RX ports enabled includes one LP11 state between each long packet coming from each RX port. Line-Concatenated forwarding alternatively only includes one LP11 state for every four long packets from the receives (when four RX ports are enabled) since four symmetric video lines are combined into a single long packet on the CSI-2 output.

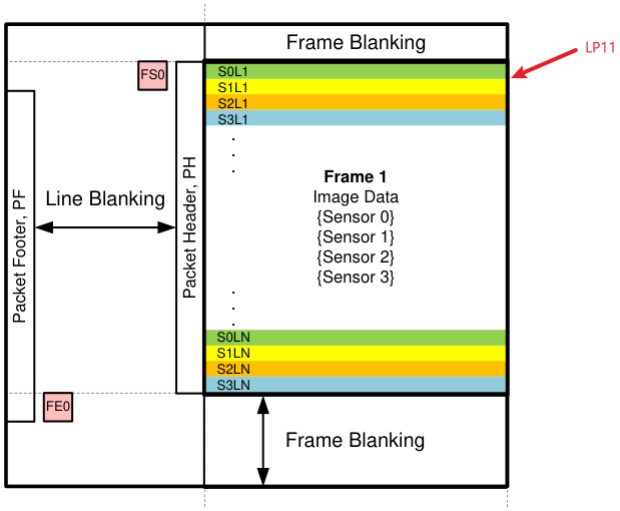

Figure 5-2. Line-Interleave CSI-2 Forwarding Format (LP11 Between Each One Long Packets)

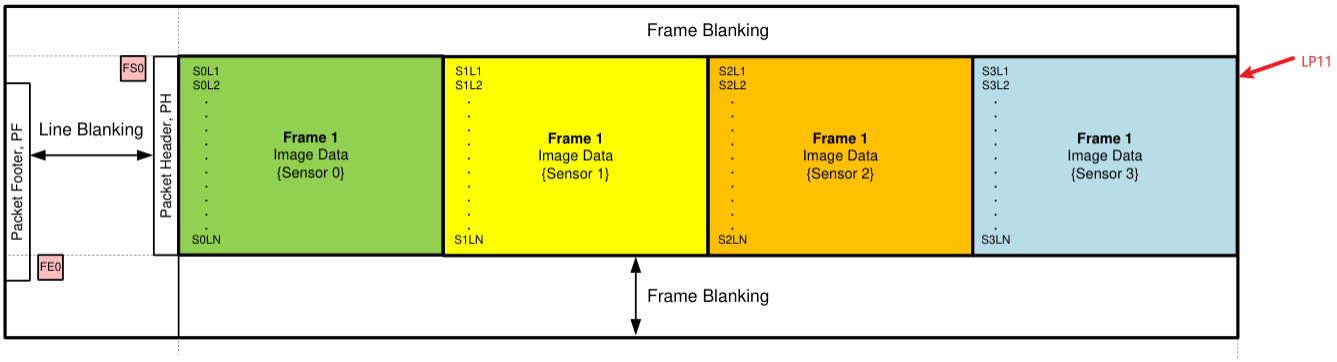

Figure 5-3. Line-Concatenated CSI-2 Forwarding Format (LP11 After Every Four Received Lines)

The bandwidth of Line-Concatenated forwarding can be calculated using the following equation:

$$\text{OuputBW} = \frac{N_{sensor}{}^{*}H_{active}{}^{*}\text{Bits/pxl}}{\frac{N_{sensor}{}^{*}H_{active}{}^{*}\text{Bits/pxl}}{N_{CSI}{}^{*}F_{csi}} + T_{csioverhead}} \quad (4)$$

For Best-Effort Round Robin (same Hactive for all RX ports), Basic Synchronized and Line-Interleaved forwarding:

$$\text{OuputBW} = \frac{H_{active}{}^{*}\text{Bits/pxl}}{\frac{H_{active}{}^{*}\text{Bits/pxl}}{N_{CSI}{}^{*}F_{csi}} + T_{csioverhaed}} \quad (5)$$

But if CSI forwarding mode is Best-Effort Round Robin and each RX port has different Hactive, the calculation is different.

$$\text{RepeatingTime} = \text{LCM}(\text{LineTime0}, \text{LineTime1}, \text{LineTime2}, \text{LineTime3}) \quad (6)$$

$$\text{SensorNLines} = \frac{\text{RepeatingTime}}{\text{SensorNLineTime}} \quad (7)$$

$$\text{TotalLines} = \text{Sensor0Lines} + \text{Sensor1Lines} + \text{Sensor2Lines} + \text{Sensor3Lines} \quad (8)$$

$$TotalRepeatingBits = Sensor0Lines*BitsPerLine + Sensor1Lines*BitsPerLine + Sensor2Lines*BitsPerLine + Sensor3Lines*BitsPerLine \quad (9)$$

$$\text{OutputBW} = \frac{\text{TotalRepeatingBits}}{\frac{\text{TotalRepeatingBits}}{\text{N}_{\text{CSI}}*\text{F}_{\text{csi}}} + \text{TotalLines}*\text{T}_{\text{csioverhaed}}} \quad (10)$$

Where,

- N_{sensor} is the number of sensors attached to the DS90UB960-Q1
- H_{active} is the horizontal line length of the active video frame in pixels
- Bits/pxl is the number of bits per pixel
- N_{CSI} is the number of CSI-2 Lanes
- f_{CSI} is the CSI-2 TX frequency per lane in Hz
- $T_{CSI\_Overhead}$ is the CSI-2 overhead

The default CSI overhead is given in Table 5-1.

Table 5-1. Deserializer CSI-2 Transmitter Default Overhead vs Data Rate

CSI-2 TX Data Rate	CSI-2 TX Overhead, $t_{CSI\_Overhead}$ [µs]	
	Continuous CSI-2 Clock (0x33[1]=1)	Discontinuous CSI-2 Clock (0x33[1]=0)
1.664 Gbps	0.73	1.68
1.6 Gbps	0.76	1.74
1.5Gbps	0.725	1.65
1.472 Gbps	0.83	1.89
1.2 Gbps	0.91	1.92
800 Mbps	0.93	2.06
400 Mbps	1.30	2.65

From the equation, in addition to data rate and forwarding modes, tuning the CSI-2 timing parameters T_{LPX}, $T_{HS\text{-}PREPARE}$, $T_{HS\text{-}ZERO}$, $T_{HS\text{-}SYNC}$, $T_{HS\text{-}TRAIL}$, and $T_{HS\text{-}EXIT}$ can also increase the efficiency of the CSI-2 output. Tune each parameter for a particular CSI-2 RX (such as SOC CSI-2 input) and then verify the SoC receives no CSI-2 errors during tuning. The timing parameters are port specific; below is example reference pseudo-code for the DS90UB960-Q1.

```
# Set CSI-2 timing parameters for CSI0
WriteI2C(0xB0,0x02) # set auto-increment, page 0
WriteI2C(0xB1,0x40) # CSI-2 Port 0
WriteI2C(0xB2,0x83) # TCK Prep
WriteI2C(0xB2,0x8D) # TCK Zero
WriteI2C(0xB2,0x87) # TCK Trail
WriteI2C(0xB2,0x87) # TCK Post
WriteI2C(0xB2,0x83) # THS Prep
WriteI2C(0xB2,0x86) # THS Zero
WriteI2C(0xB2,0x84) # THS Trail
WriteI2C(0xB2,0x86) # THS Exit
WriteI2C(0xB2,0x84) # TLPX
# Set CSI-2 timing parameters for CSI1
WriteI2C(0xB0,0x2) # set auto-increment, page 0
WriteI2C(0xB1,0x60) # CSI-2 Port 1
WriteI2C(0xB2,0x83) # TCK Prep
WriteI2C(0xB2,0x8D) # TCK Zero
WriteI2C(0xB2,0x87) # TCK Trail
WriteI2C(0xB2,0x87) # TCK Post
WriteI2C(0xB2,0x83) # THS Prep
WriteI2C(0xB2,0x86) # THS Zero
WriteI2C(0xB2,0x84) # THS Trail
WriteI2C(0xB2,0x86) # THS Exit
WriteI2C(0xB2,0x84) # TLPX
```

6 Summary

When considering CSI-2 input bandwidths for the purposes of aggregation, it is necessary to evaluate the bandwidth required for each video line since CSI-2 packetization occurs on a packet level and overhead is introduced as the CSI-2 lanes transition in and out of LP mode. From CSI-2 output bandwidth perspective, the output bandwidth is reduced from the nominal data rate because data cannot be transmitted during Low-Power states and the transition time between low-power and high-speed modes. This application note breaks down the FPD-Link deserializer internal CSI-2 aggregator process to calculate the accurate input and output bandwidth when using different CSI-2 forwarding modes.

7 References

1. Texas Instruments, *DS90UB960-Q1 Quad 4.16-Gbps FPD-Link III Deserializer Hub With Dual MIPI CSI-2 Ports*, datasheet.
2. Texas Instruments, *DS90UB954-Q1 Dual 4.16 Gbps FPD-Link III Deserializer Hub With MIPI CSI-2 Outputs for 2MP/60fps Cameras and RADAR* data sheet
3. Texas Instruments, *CSI-2 Aggregation Breakdown*, video.

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