Application Brief

Mitigate System Level Flex I/O Risks using LMKDB11xx-FS Fail Safe Output Devices

ABSTRACT

Flexible input or output (Flex I/O) signals or interfaces allows user to use interface pins flexibly for different type of interfaces such as PCIe differential clock inputs, side band signals or future evolving needs for high speed management interfaces. When using the Flex I/O interface pins, Flex I/O interface engagement goes through a set of required steps to negotiate the control. During the control negotiation, the Flex I/O signals connected to platform are tri-stated or high impedance with very low leakage. However, when the Flex I/O pins are used as PCIe differential clock pins through clock buffer devices, this condition of no bias or high impedance requirement is not fully satisfied due to low, low requirement on the clock buffer devices in power down mode. This presents a leakage path during the engagement phase if user plugs in a incompatible platform card, presenting a reliability concern. LMKDB11xx-FS devices solves this reliability concern by providing fail-safe outputs with very low leakage of <10µA, when outputs are pulled high to 3.3V during no supply power to the part.

Flexible Input / Output (Flex I/O) Interface

Flexible input / output (Flex I/O) allows users flexibility to re-purpose functionality of the interface pins after interface engagement requirements are satisfied as defined in PCIe Express Base Specification. Flex I/O interface provides system designers flexibility for an improved hardware interface utilization, evolving needs for future generation of high-speed management interfaces and value add of out-of-band functionality between different platforms[1].

Flex I/O interface requires following guidelines for engagement as described in PCIe Express Base Specification:

- Default State
- Discovery
- Compatibility Check
- Control Negotiation

Refer to PCIe Express Base Specification section 12.3.2.1 for details on each guideline during the engagement phase. This application note is concerned with permitted Default States as defined in PCIe Express Base Specification:

- **Unused:** Unconnected (electrical open) or with a specific termination as dictated by a specific form factor or connector/cable specification.
- **Pre-Wired/Inert:** This is where a pin or interface is wired with a predetermined circuit and connectivity but does not perform the intended functionality until after negotiation is complete. Voltage bias before negotiation is allowed. An example is a form factor specific required Flex I/O signal connected to platform logic that defaults to tristate or high impedance with a platform-side pullup resistor to the platform side's +3.3V auxiliary power rail. Then after negotiation is complete, the signal is allowed to be used for its intended purpose. Form factor specifications must ensure that any allowed default circuit conditions are electrically safe and do not impose logical domain constraints. An example is a cross power domain electrical stress or leakage condition.
- **Switchable Function:** This is where a pin/ interface defaults to a pre-defined function (often a legacy function), but then is electrically or logically switchable to an alternate function. An example is a form factor interface that defaults to JTAG functionality, with all the associated requirements such as default terminations and connectivity. Then following a positive discovery and compatibility check (defined below), a control disengages the default functionality and then engages the intended alternate functionality.

[1] See also, the References

Modular - Extensible IO (M-XIO) Base Specification

Open Compute Project (OCP) Modular - Extensible IO (M-XIO) defines the technical specification for DC-MHS Modular Extensible I/O connectors and products. The specification covers following elements for M-XIO source connectors:

- Requirements
- Signal List
- Addendums with specific pinouts for a selection of connector models.

Under the section 6.7 in Modular - Extensible IO (M-XIO), Flex I/O pin default initialization on the connector is defined with respect to PCIe Express Base Specification guidelines[2]. Following Table 1 shows the default initialization state for each FLEXIO pins.

Table 1. M-XIOs Flexible I/O Selection

Signal Name	Default Initialization	Comments
FLEXIO_0	No Function & No Bias	Single Ended Optimized From M-XIO Pinout Perspective
FLEXIO_1	SB_FLEX_1	Differentially Coupled to FLEXIO_2 From M-XIO Pinout Perspective
FLEXIO_2	SB_FLEX_2	Differentially Coupled to FLEXIO_1 From M-XIO Pinout Perspective
FLEXIO_3	No Function & No Bias	Differentially Coupled to FLEXIO_4 From M-XIO Pinout Perspective
FLEXIO_4	No Function & No Bias	Differentially Coupled to FLEXIO_3 From M-XIO Pinout Perspective
FLEXIO_5	No Function & No Bias	Differentially Coupled to FLEXIO_6 From M-XIO Pinout Perspective
FLEXIO_6	No Function & No Bias	Differentially Coupled to FLEXIO_5 From M-XIO Pinout Perspective

Flex I/O Interface Pins as High Speed Signals (Clock Inputs) Using Clock Devices

As noted earlier, Flex I/O interface pins can be re-purposed for various different use case. One of these use case is to distribute PCIe differential clock signals, if there is a need for additional clocks. The problem arises with specification of clock distribution devices and Flex I/O pins default state when using Flex I/O pins for clock signal routing. The default state requires no-bias or no function based on Modular - Extensible IO (M-XIO) specifications as shown in Section 2, while the clock buffer devices outputs are set to low, low in power down as per DB2000QL specification. This presents a leakage path when the outputs are pulled high through a pull up in power down state. The leakage values depends on different clock buffer vendor architectures. Different architectures can use diode clamps or resistors to ground.

Thus, whenever Flex I/O pins are used as high speed clock pins, if a user inserts an incompatible card which has side band signals defined other than clock signals. This poses a leakage risk or device reliability issue until the interface engagement determines the card is not compatible.

LMKDB11xx-FS Fail-Safe Clock Buffer for Flex I/O Use Case

LMKDB11xx-FS family of clock buffers are designed to minimize the leakage and reliability risks when using Flex I/O pins for differential clocks. The LMKDB11xx-FS features transistor switch to protect the outputs from any leakage when the device is power down towards the output driver side. To comply with output low, low requirement with DB2000QL, a high impedance value resistor to ground is used on the pad. With the addition of transistor switch and high impedance on the pad as shown in Section 4, leakage on the LMKDB11xx-FS devices is limited to <10µA worst case. The LMKDB11xx-FS minimizes the risk of any leakage or reliability issue during the discovery or prolonged exposure to incompatible adapters and cards on the platform. Thus, providing flexibility to system designers to use Flex I/O interface for various use cases.

In addition LMKDB11xx-FS device's all clock inputs and digital inputs are fail-safe which means if the part is powered down, any clock input or digital input can be held above the supply voltage or absolute maximum value defined in the data sheet. This allows flexible power sequence design as well in a system.

[2] See also, the References

Following are key points about the working of LMKDB11xx-FS devices as shown in Figure 1.

- When VDD = 3.3V or 1.8V OE# (output enable) / PWRGD/PWRDN# are used to inactive the outputs. The outputs are pulled down with a 50Ω / 42.5Ω impedance push pull driver output stage.
- When VDD = 0V, then there is weak pull down resistor to ground for low state providing less than 10µA of leakage or almost no-bias condition as shown in green. The transistor switch switch disconnects the output pads from the output driver and protects the outputs as well.
- LMKDB110x-FS behavior acts as high impedance when VDD=0V and also have a weak pull down to comply with DB2000QL specification. This allows low leakage path if incompatible cards are plugged into motherboard.
- LMKDB110x-FS opens up possibilities to use Flex I/O pins as clock inputs without any issue with the default state requirements.

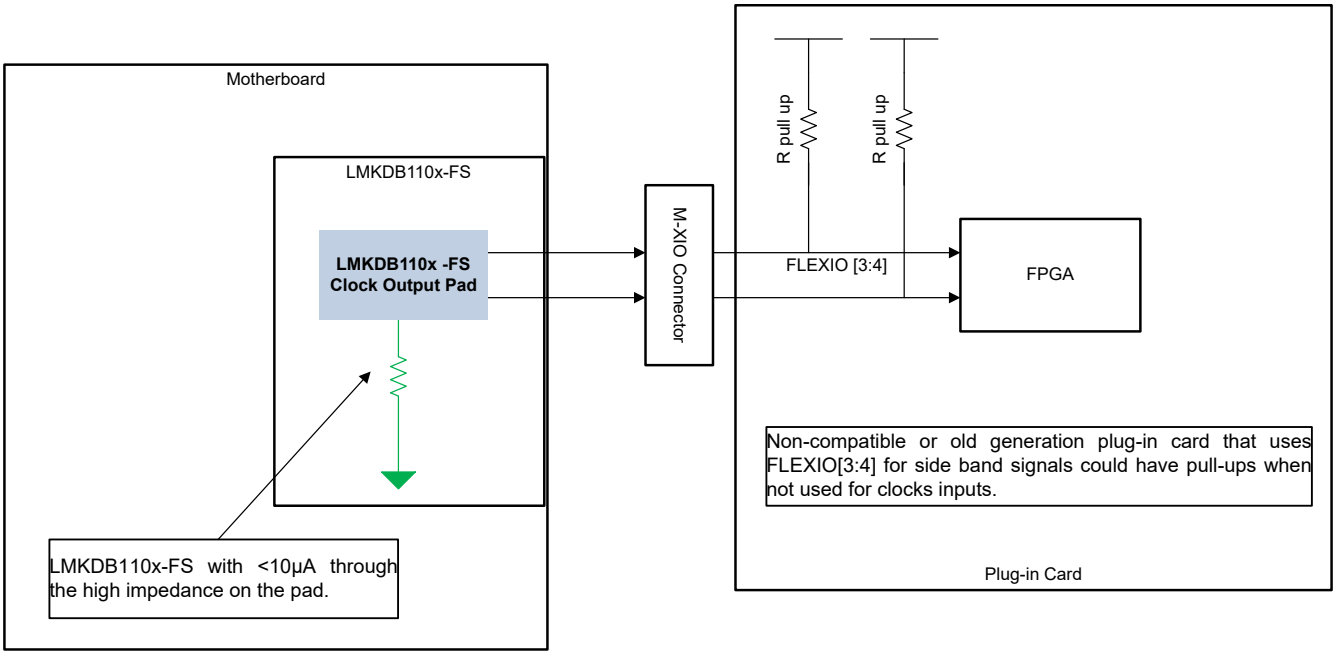

Figure 1. LMKDB11xx-FS Device Use Case for Flex I/O Default State Requirement

Summary

LMKDB11xx-FS clock buffer devices provide a pin to pin and software compatible design to existing family on PCIe clock buffer for Flex I/O interface use case. The devices gives flexibility to system designers for routing differential clock signals on Flex I/O pins without worrying about the leakage or compatibility issues. If a user plugs in a incompatible card with side-band signals during the discovery period or for prolonged times. The LMKDB11xx-FS devices have no reverse current or reliability issues. Furthermore, the LMKDB11xx-FS fail-safe capability on both the inputs and outputs gives system designers flexibility in power sequence design as well.

References

- PCI Express Specifications
- Modular - Extensible IO (M-XIO) Base Specification
- LMKDB11xx

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