Application Note

Seamless PWM Duty Cycle Updates Without Intermediate Artifacts

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ABSTRACT

Pulse Width Modulation (PWM) is a core technology used across many embedded applications including LED dimming control, motor control, and power regulation. When PWM duty cycle updates are made without proper synchronization, the PWM can introduce unintended PWM duty cycle causing unintended behaviors of corresponding devices such as unintended LED flicker or motor torque control. These effects are undesirable in both visual and functional applications, particularly where precision and smooth operation are required. This application note explains how undesirable duty cycle can occur and how to overcome this problem for seamless PWM duty cycle transitions using the Enhanced Pulse Width Modulation (EPWM) module on the Texas Instruments TDA4x platform by presenting LED dimming control example.

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Trademarks

1 Introduction

In the Texas Instruments TDA4x processor family, PWM generation is typically implemented using the EPWM module, which supports a range of flexible features such as configurable counter modes, compare registers, shadow loading, and event triggering. These features are essential for real-time, high-performance control systems.

Despite the versatility, PWM can produce undesirable output behavior if not configured carefully — especially during runtime updates of the duty cycle. A common issue is the appearance of intermediate or incorrect duty cycle when the compare register (CMPA/CMPB) is updated immediately, without proper synchronization to the PWM cycle. These can result in visual flicker (for example, in LEDs), sudden torque changes (for example, in motors), or EMI spikes in sensitive applications.

In real-world designs, this is essential to make sure that updates of the duty cycle occur smoothly and without unintended transients. This can be achieved through the use of shadow registers, which defer register updates until a safe point in the PWM cycle typically at the period boundary.

This application note focuses on two specific sources of PWM artifacts and presents reliable designs optimized for the TDA4x platform:

- Immediate update of registers related to the PWM duty cycle. The recommended design is to enable and use the shadow register mechanism, which makes sure that updates take effect synchronously with the PWM period.
- Use of center-aligned (up-down count mode) PWM mode in applications where edge-aligned timing is expected. This mismatch can cause inconsistent behavior, particularly in applications like LED dimming that rely on rising-edge or falling-edge alignment. The recommendation is to use up-count or down-count modes for edge-aligned applications.

This application note explains those issues in detail and provides a best practice to use EPWM module for LED dimming control as an example.

2 Understanding PWM Operation on TDA4x

The Texas Instruments TDA4x platform integrates advanced PWM generation capabilities through the EPWM (Enhanced Pulse Width Modulation) modules. These modules provide high-resolution and flexible PWM signal control, making them well-suited for a wide range of real-time control applications.

2.1 PWM Architecture Overview

Each EPWM module in TDA4x consists of a Time-Base (TB) module, Counter-Compare (CC) module, Action Qualifier (AQ) module, and event triggering mechanisms. The time-base counter defines frequency and period of the PWM waveform, while the counter-compare module determines when PWM signal transitions occur within each period.

The EPWM module supports several counter modes based on Time-Base Counter (TBCNT) and Time-Base Prriod (TBPRD):

- Up-count mode: TBCNT counts from zero to TBPRD, then resets.
- Down-count mode: TBCNT counts down from TBPRD to zero.
- Up-down-count mode: TBCNT counts up to TBPRD and then back down to zero, creating center-aligned waveforms.

Each mode affects the timing of the PWM and how count compare values map to output transitions.

2.2 Counter-Compare Register and Duty Cycle Control

The CMPA register holds the compare value that defines the duty cycle of the PWM output. For example, in up-count mode, an active-high PWM waveform can go high at zero and low when TBCNT matches CMPA. The same logic applies to CMPB for independent or complementary control of a second output.

Importantly, CMPA can be updated in two ways:

- Immediate mode: CMPA changes take effect as soon as written. This can cause mid-period glitches if written at the wrong time.
- Shadow mode: CMPA writes are held in a shadow register and transferred to the active register on a predefined event (for example, counter equals zero or period match), making sure of glitch-free updates.

Shadow loading is enabled through the CMPCTL register, and is essential for synchronizing updates with the PWM cycle.

2.3 Action Qualifier and Output Behavior

The Action Qualifier (AQ) module controls how the PWM output responds to events such as TBCNT = CMPA. Developers configure AQCTLA to define actions like set, clear, or toggle based on compare matches or counter zero events. This flexible mechanism enables precise waveform shaping.

2.4 Synchronization and Update Timing

TDA4x allows synchronization of PWM modules using sync inputs and outputs, enabling time-coordinated behavior across multiple channels. Additionally, features such as dead-band insertion, trip-zone logic, and event triggers provide safe and responsive control in critical applications.

To avoid artifacts during dynamic operation, this is essential to:

- Enable and correctly configure shadow registers.
- Choose an appropriate counter mode that matches the timing expectations of the application.
- Avoid direct writes to CMPA and CMPB when immediate mode is active unless precise timing is maintained.

Understanding these components is foundational for implementing reliable and artifact-free PWM behavior on the TDA4x platform.

3 Unintended PWM Duty Cycle from Immediate CMPA Update

To change PWM duty rate, write a new value into CMPA register is necessary. There is difficulty for software to update very deterministically, so CMPA register can be updated at incorrect instance and this can cause unintended PWM duty cycle, consequently results in incorrect brightness in LED control or incorrect motor speed and torque control within a short period. To prevent unpredictable update, shadow register update is used instead of immediate register update. Let us try to understand how immediate register update can cause this issue with up-count mode by changing PWM duty rate from 20% to 80%.

Consider an up-count mode PWM configured to go HIGH at TBCNT = 0 and LOW at TBCNT = CMPA. If the CMPA register is updated during the middle of a period, the PWM output can switch to LOW earlier or later than intended in the current cycle, depending on the new CMPA value. This causes a duty cycle distortion lasting for one or more PWM periods.

The following registers configuration can be used to generate 20% of PWM duty cycle in up count mode.

```
EPWM_TBPRD = 62500
EPWM_TBCTL.CTRMODE = 0 → Up count mode
EPWM_CMPA = 12500 (= 62500 x 20%)
EPWM_CMPCTL.SHDWAMODE = 1 → Immediate mode
```

Make 80% of PWM duty cycle by updating CMPA register as shown in the following.

```
EPWM_CMPA = 50000 (= 62500 × 80%)
```

Figure 3-1 is PWM signal probed through logic analyzer.

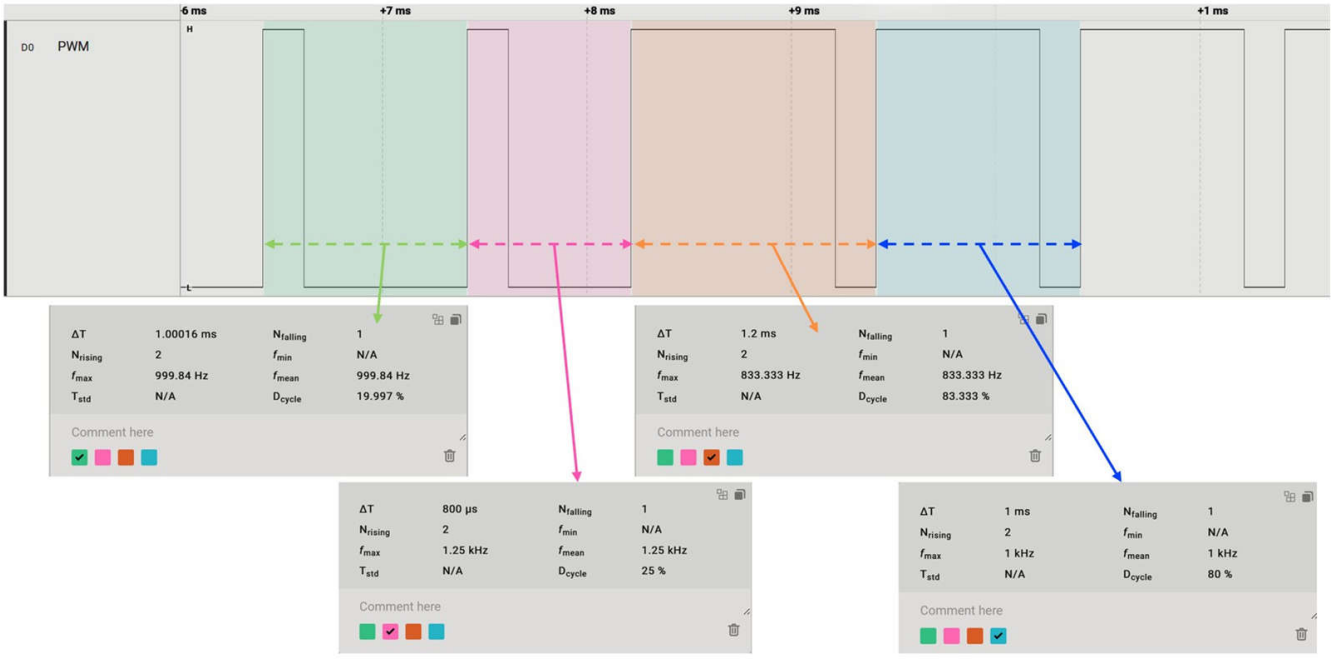

Figure 3-1. Probe PWM Changes During Updating CMPA Register in Up Count Mode

The expectation is that the duty cycle becomes from 20% to 80% directly but there are 25% duty and 83% duty which are not intended.

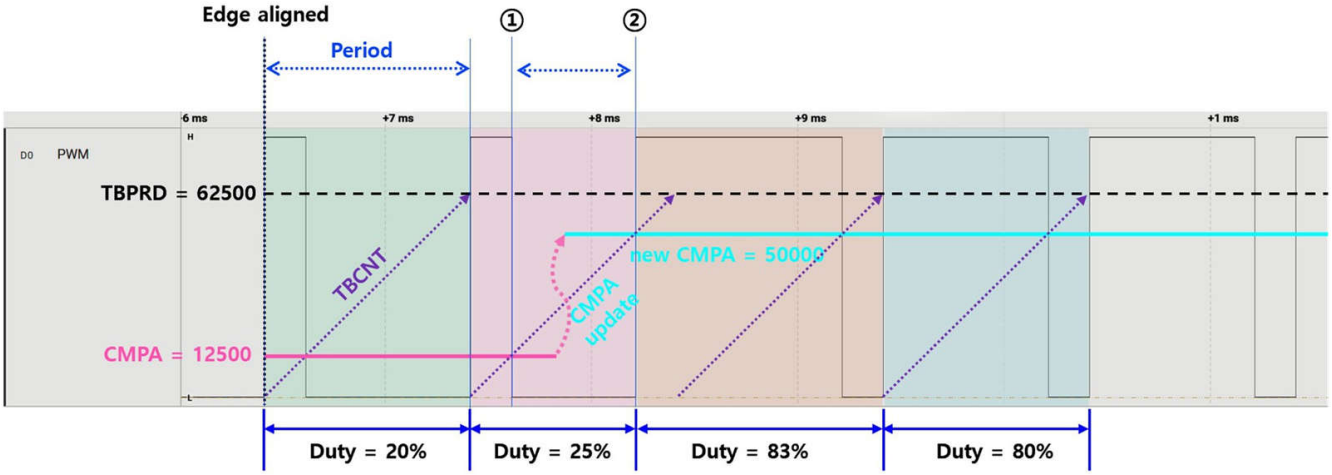

Figure 3-2. Analyze PWM Duty Cycle Change From 20% to 80% in Up Count Mode

This is analyzed in the following.

- Current duty cycle is 20%.

$$Duty = 100 \times \frac{12500}{12500 + 50000} = 20\,\% \quad (1)$$

- Software writes 50000 into CMPA register in between ① and ②.
- CMPA register value is updated immediately.
- PWM toggles at the instance of ②, and this makes duty cycle 25%.

$$Duty = 100 \times \frac{12500}{12500 + 37500} = 25\,\% \quad (2)$$

- In following PWM period, PWM duty cycle becomes 83%.

$$Duty = 100 \times \frac{62500}{62500 + 12500} = 83\,\% \quad (3)$$

- After two consecutive PWM periods, PWM duty cycle becomes stable with 80%.

$$Duty = 100 \times \frac{50000}{50000 + 62500} = 80\,\% \quad (4)$$

Note

Duty is calculated with following equation.

$$Duty = 100 \times \frac{High\ \ Period}{High\ \ Period + Low\ \ Period} \quad (5)$$

The root cause of this behavior lies in the immediate update mode of the CMPA register. In this mode, any new value written to CMPA is used immediately — even if this occurs mid-cycle. Since the PWM logic uses the current CMPA value for compare events, a mid-period change leads to incorrect output timing. This is not a hardware bug but rather a configuration oversight. Immediate updates are valid in some cases, but for dynamic duty cycle adjustment during operation, updates are not safe.

4 Unintended PWM Duty Cycle from Up-Down Count Mode

In LED dimming applications using PWM, maintaining intended brightness transitions is important. However, when using the up-down count mode to generate PWM, the PWM is center aligned and this causes unintended duty cycle, consequently unintended brightness flicker or glitches can appear during duty cycle changes. Let's try to understand and analyze how this issue can happen with up-down count mode by changing the duty cycle from 20% to 80%, and also applying shadowing register update as well.

Up-down count mode uses two events from Action Qualifier (AQ) module. PWM signal can toggle when TBCNT = CMPA but this event occurs two times in one PWM period, at up-counting and at down-counting.

The following registers configuration can be used to generate 20% of PWM duty cycle in up-down count mode.

```
EPWM_TBPRD = 62500
EPWM_TBCTL.CTRMODE = 0x2 → Up-down count mode
EPWM_CMPA = 12500 (= 62500 x 20%)
EPWM_CMPCTL.SHDWAMODE = 0 → Shadow mode
```

Make 80% of PWM duty cycle by updating CMPA register as shown in the following.

```
EPWM_CMPA = 50000 (= 62500 x 80%)
```

Figure 4-1 is a PWM waveform probed by logic analyzer.

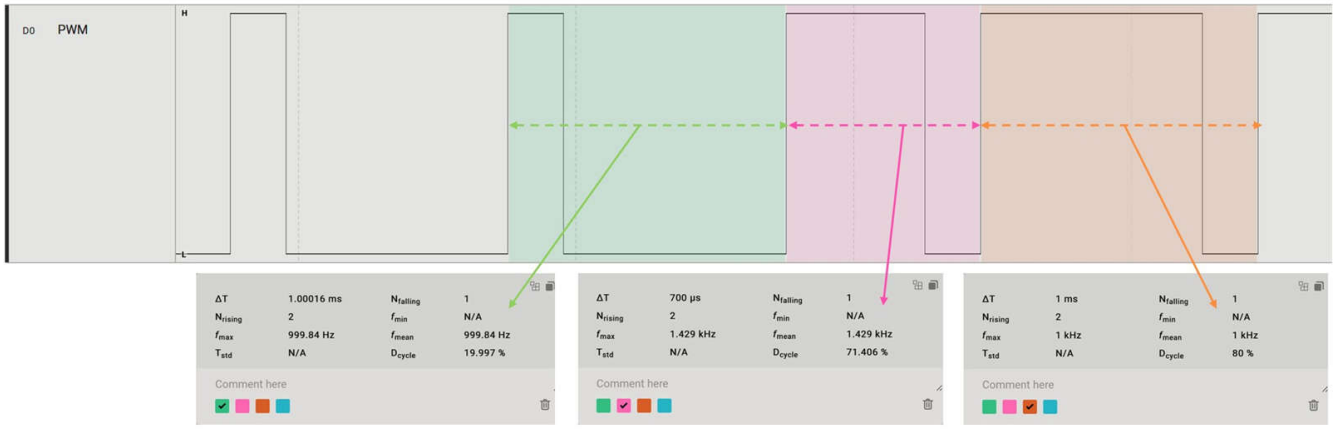

Figure 4-1. Probe PWM Changes During Updating CMPA Register in Up-Down Count Mode

The expectations is that duty cycle comes from 20% to 80% directly but there is 71% duty which is not intended.

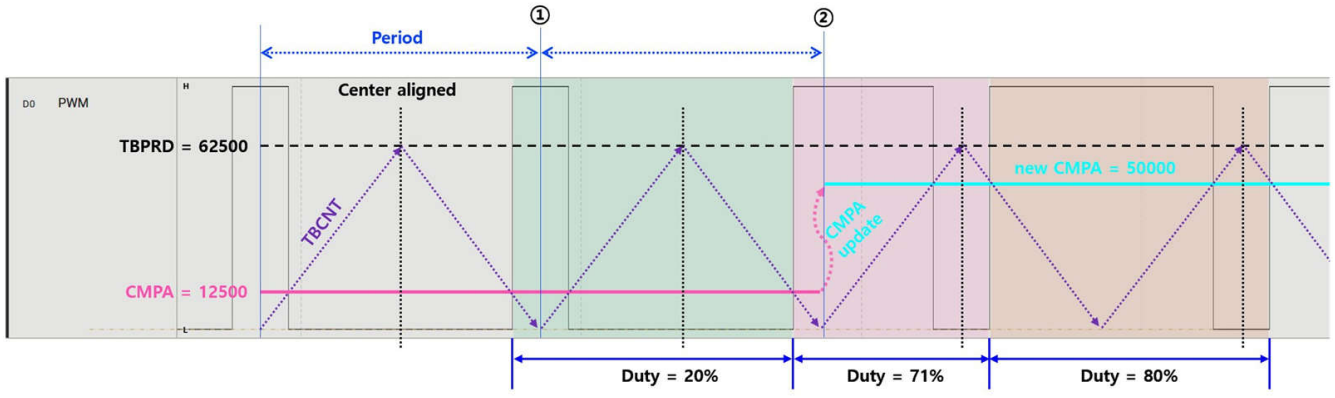

Figure 4-2. Analyze PWM Duty Cycle Change From 20% to 80% in Up-Down Count Mode

This is analyzed as in the following.

- Current duty cycle is 20%.

$$Duty = 100 \times \frac{25000}{25000 + 100000} = 20\,\% \quad (6)$$

- Software writes 50000 into CMPA register in between ① and ②.
- CMPA register is shadowed and is updated at TBCNT = 0.
- PWM toggles at the instance of ② when TBCNT = 0 and this makes duty cycle 71%.

$$Duty = 100 \times \frac{62500}{62500 + 25000} = 71\,\% \quad (7)$$

- From the following PWM periods, PWM duty cycle becomes 80%.

$$Duty = 100 \times \frac{100000}{100000 + 25000} = 80\,\% \quad (8)$$

In Figure 4-2, PWM duty cycle is being changed by updating CMPA register value, and CMPA register value is updated using shadowing technique accordingly. This means that CMPA register value is updated deterministically, and this happens at the event of TBCNT is zero.

Even though shadow mode is used, PWM duty cycle is transitioning from 20%, 25% and then 80%. This is inevitable and is the nature of center-aligned PWM generation and this can cause unintended result such as LED flicker in LED dimming control application.

5 Best Practice for Seamless PWM Updates for LED Dimming Control

Achieving artifact-free PWM duty cycle changes requires careful configurations and synchronization methods which are available on EPWM. The following best practice can assist developers understand PWM generation scheme better and how to configure EPWM module properly.

5.1 Use Shadow Registers for Duty Cycle Updates

Always enable shadow loading of CMPA compare register to defer updates until the start or end of the PWM period by configuring EPWM_CMPCTL.LOADAMODE = 0, and this makes sure the CMPA register is updated deterministically at a specific event such as TBCNT = 0 or TBCNT = TBPRD.

5.2 Select the Appropriate Counter Mode

As this application explained previously, shadow register update mode also can make the problem. So, depending on the application, this is necessary to select proper count mode. In LED dimming application, up count or down count mode is proper option to choose rather than up-down count mode (center aligned PWM).

5.3 Register Configurations for Up-count Mode Under Shadowing

The following registers configuration can be used to generate 20% of PWM duty cycle in up count mode.

```
EPWM_TBPRD = 62500
EPWM_TBCTL.CTRMODE = 0 → Up count mode
EPWM_TBCTL.CLKDIV = 1
EPWM_CMPA = 12500 (= 62500 x 20%)
EPWM_CMPCTL.SHDWAMODE = 0 → Shadow mode
EPWM_CMPCTL.LOADAMODE = 0 → Load on TBCNT = 0 when shadow mode is enabled.
EPWM_AQCTLA.CAU = 0x3 → Toggle EPWM output
EPWM_AQCTLA.ZRO = 0x2 → Force EPWM output HIGH
```

Then, there can be no unintended PWM duty cycle regardless the instance of writing a value into CMPA. Figure 5-1 is PWM signal probed when changing PWM duty cycle from 20% to 80%.

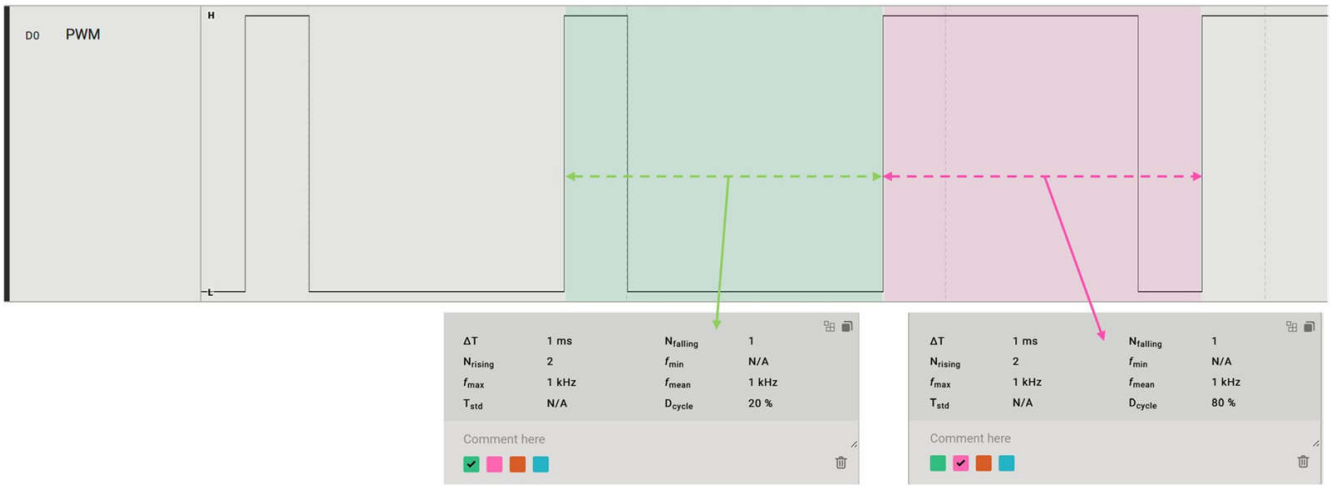

Figure 5-1. Probe PWM Changes With Shadow Mode in Up Count Mode

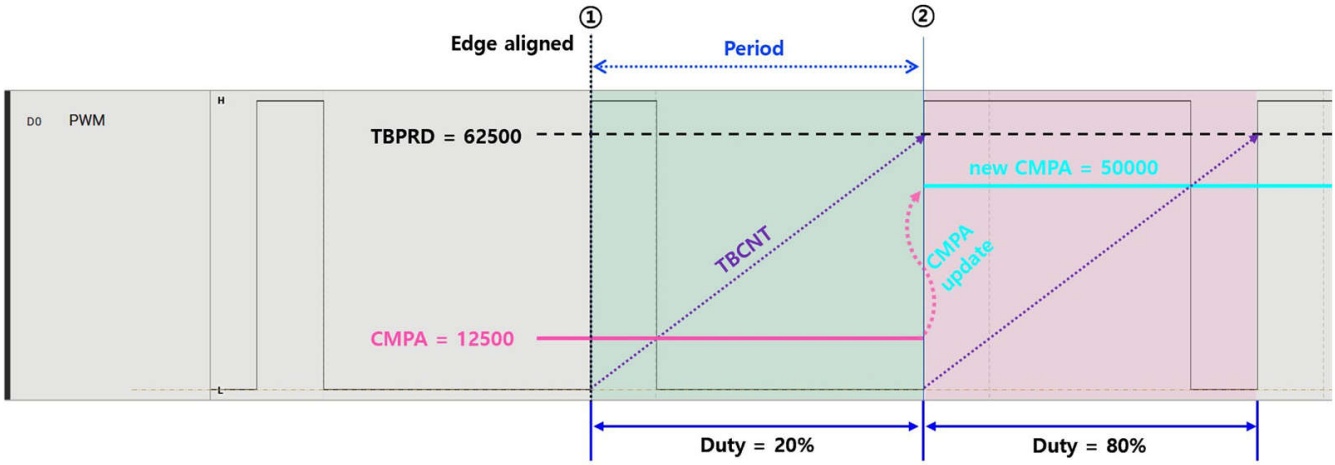

Figure 5-2. Analyze PWM Duty Cycle Change with Shadow Mode in Up Count Mode

This can be analyzed as in the following.

- Current duty cycle is 20%.

$$Duty = 100 \times \frac{12500}{12500 + 50000} = 20\,\% \quad (9)$$

- Software writes 50000 into CMPA register in between ① and ②
- CMPA register is shadowed and is updated at TBCNT = 0.
- PWM toggles at the instance of ② when TBCNT = 0 and this makes duty cycle 80%.

$$Duty = 100 \times \frac{50000}{50000 + 12500} = 80\,\% \quad (10)$$

- For the following PWM periods, PWM duty cycle stays at 80%.

This is just an example to show how to control PWM duty cycle especially for LED dimming without unintended brightness.

6 Summary

This application note described two important considerations for achieving seamless transitions of PWM duty cycle. Specifically, this application note explained in detail how immediate register updates such as CMPA and the use of up-down count mode (center-aligned PWM) can result in unintended PWM duty cycle depending on applications when changing PWM duty cycle at run time. To address these issues, shadow register update and up count mode were recommended by providing LED dimming control as a practical example.

By understanding and analyzing these behaviors, developers can gain deeper insight into how to configure the EPWM module appropriately based on the specific requirements of the application. This foundation enables more robust, glitch-free PWM control in real-time embedded systems.

7 References

1. Texas Instruments, *TDA4VM Product Page*
2. Texas Instruments, *J721E DRA829/TDA4VM Processors Silicon Revision 2.0, 1.1 Technical Reference Manual*
3. Texas Instruments, *PROCESSOR-SDK-RTOS-J721E: Software development kit for DRA829 and TDA4VM Jacinto™ processors*
4. Texas Instruments, *MCAL Documentation*

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