EVM User's Guide: ADS125H18EVM-PDK

ADS125H18EVM-PDK Evaluation Module

Description

The ADS125H18 evaluation module (EVM) is a platform for evaluating the performance of the ADS125H18, which is a 24-bit, 8-channel multiplexed delta-sigma (ΔΣ) analog-to-digital converter (ADC) designed to directly measure process-level (10V and 4mA to 20mA) inputs. The ADS125H18 provides sample rates up to 1MSPS, a flexible sequencer, a low noise voltage reference, and many diagnostic features to aid the design of high-reliability systems. The ADS125H18EVM-PDK eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface.

Get Started

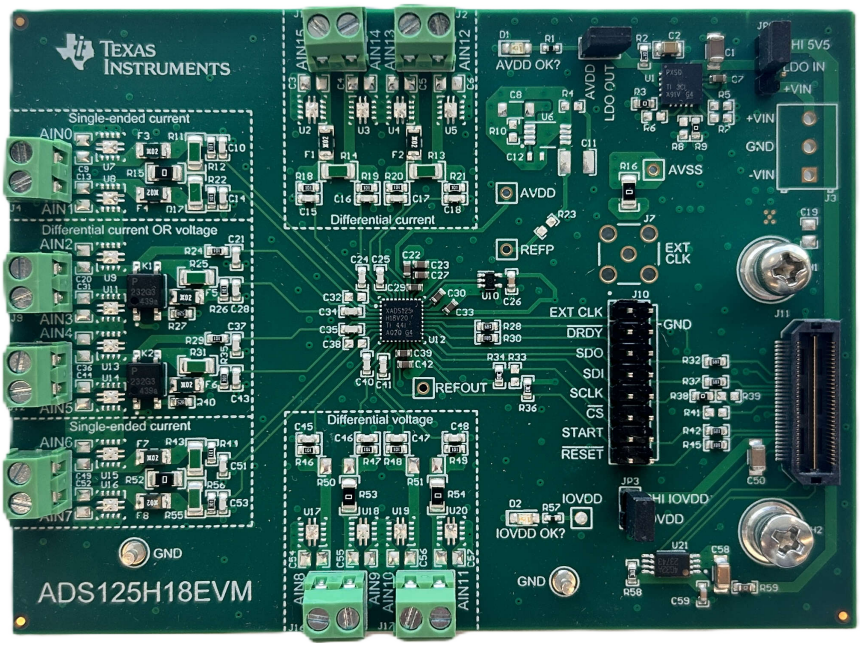
1. Order the EVM from ti.com
2. Download the latest software from the ADS125H18EVM-PDK tool folder
3. Launch the ADS125H18 EVM GUI from the start menu
4. Connect the ADS125H18 EVM to the PHI controller board and connect the PHI board to the computer running the ADS125H18 EVM GUI

Features

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS125H18
- The PHI controller provides a convenient communication interface to the ADS125H18 over USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft® Windows® 10 operating system
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing

Applications

- PLC analog input modules
- Industrial robot analog I/O module
- HVAC controller



1 Evaluation Module Overview

1.1 Introduction

The ADS125H18EVM-PDK is a platform for evaluating the performance of the ADS125H18, a 24-bit, 8-channel, multiplexed delta-sigma ADC designed to directly measure process-level (10V and 4-20mA) inputs. The evaluation kit includes the ADS125H18 EVM and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis. The ADS125H18 EVM includes the ADS125H18 and all the peripheral analog circuits and components required to evaluate the performance of the ADS125H18. The PHI board provides a communication interface from the ADS125H18 EVM to the computer through a USB port.

This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS125H18 EVM

1.2 Kit Contents

The ADS125H18EVM-PDK includes the following components, as shown in Figure 1-1:

1. The PHI controller board
2. The ADS125H18 EVM that includes the ADS125H18 and peripheral circuitry required for device operation and communication with the PHI board.
3. An A-to-Micro-B USB cable for communication between the PHI board and the EVM GUI.
4. The EVM GUI, which can be found online in the EVM tool folder

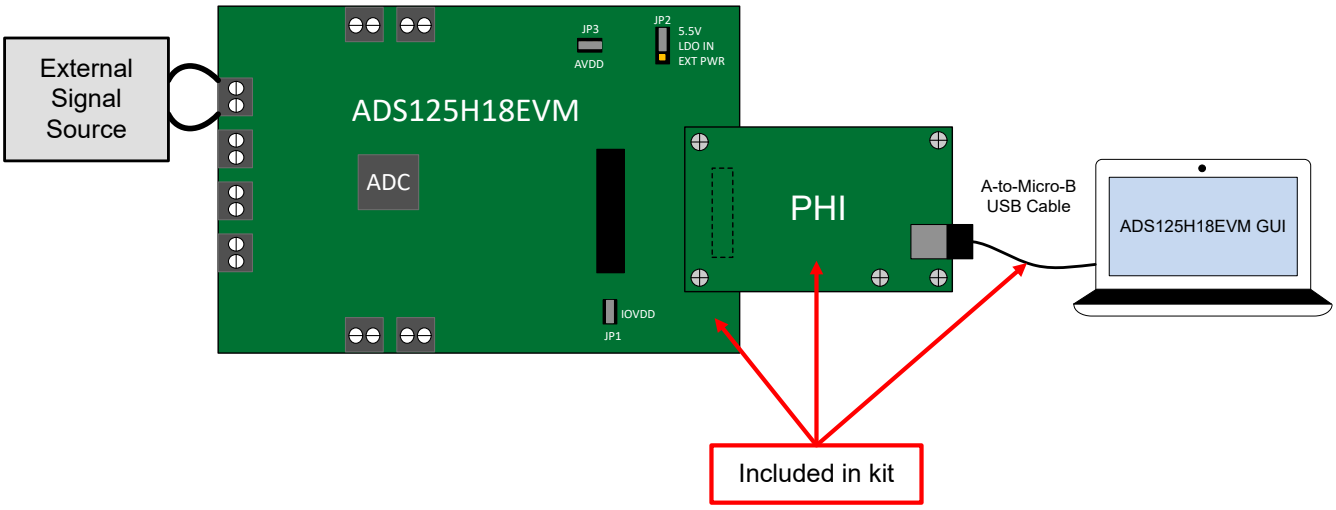


Figure 1-1. System Connection for Evaluation

1.3 Specifications

The following specifications are applicable to the ADS125H18 EVM board and the PHI board.

Table 1-1. Specifications

PARAMETER	CONDITIONS		VALUE
Temperature	Recommended operating free-air temperature range, T_A		15°C ≤ T_A ≤ 35°C
Power supply input range (unipolar)	Recommended voltage input range for J14-3 (+Vin) with respect to GND		5.5V ≤ +Vin ≤ 6.5V
	Supply current range $\|I_s\|$		0.25A ≤ $\|I_s\|$ ≤ 0.5A
Power supply input range (bipolar)	Recommended voltage input range for J14-1 (-Vin) with respect to GND		-6.5V ≤ -Vin ≤ -5.5V
	Supply current range $\|I_s\|$		0.25A ≤ $\|I_s\|$ ≤ 0.5A
Input voltage range	Absolute input voltage with respect to GND for AIN0 to AIN15 inputs	V12 device variant	-12.5V ≤ AINx ≤ 12.5V
		V20 device variant	-20.5V ≤ AINx ≤ 20.5V
		V40 device variant	-40.5V ≤ AINx ≤ 40.5V
EXT clock	Recommended frequency range (f_{CLK})		0.5MHz ≤ f_{CLK} ≤ 26.2MHz
External digital IO (including EXT clock)	Recommended logic levels (applied to header J12 or connector J13) with respect to GND	Logic Level Low ($V_{IOl)}$	0V ≤ V_{CLKl} ≤ 0.3*IOVDD
		Logic Level High ($V_{IOh)}$	0.7*IOVDD ≤ V_{CLKh} ≤ IOVDD
ADS125H18 AVDD to AVSS	Recommended voltage range (applied to JP3-2), external source	High-speed or Mid-speed mode	4.5V ≤ AVDD ≤ 5.5V
		Low-speed or Very-low-speed mode	3V ≤ AVDD ≤ 5.5V
ADS125H18 |AVSS/AVDD1| ratio to GND	Recommended absolute ratio range, external source, DGND = GND		|AVSS/AVDD1| ≤ 1.2V/V
ADS125H18 AVSS to GND	Recommended voltage range (JP2 2-3 position), DGND = GND		-2.75V ≤ AVSS ≤ 0V
ADS125H18 IOVDD to GND	Recommended voltage range (applied to JP1-1), external source, DGND = GND		1.65V ≤ IOVDD ≤ 5.5V
ADS125H18 Reference REFP to AVSS	Recommended voltage range (J9 installed, U20 not installed), external source	REFP buffer off	1V ≤ REFP ≤ AVDD + 0.05V
		REFP buffer on	1V ≤ REFP ≤ AVDD - 0.7V

1.4 Device Information

This section introduces important information about the ADS125H18 device family. Table 1-2 describes some of the parameters and features that are common among all ADCs in the ADS125H18 device family, while Table 1-3 lists the key differences among the ADCs in the ADS125H18 device family. Refer to the ADS125H18 data sheet for complete device specifications.

Table 1-2. ADS125H18 Device Family Key Features and Parameters

PARAMETER	VALUE
Maximum data rate	1.067MSPS
Input impedance	≥1MΩ
Integrated features	• Flexible channel sequencer • FIFO buffer • Voltage reference • Oscillator • Test DAC • Fault detection
Package	VQFN-36
Package size	5.00mm × 5.00mm
Specified temperature range	-40°C ≤ T_A ≤ 125°C

Table 1-3. ADC Options in the ADS125H18 Device Family

DEVICE	RESOLUTION	CHANNEL CONFIGURATION (INPUT VOLTAGE RANGE)	HIGH VOLTAGE INPUT RANGE
ADS125H18V12	24 bit	16x high voltage channels (see HIGH VOLTAGE INPUT RANGE column)	±12V
ADS125H18V20			±20V
ADS125H18V40			±40V
ADS115H18V12	16 bit		±12V
ADS115H18V20			±20V
ADS115H18V40			±40V
ADS125H14V12	24 bit	8x high voltage channels (see HIGH VOLTAGE INPUT RANGE column) 8x low voltage channels (≤AVDD)	±12V
ADS125H14V20			±20V
ADS125H14V40			±40V
ADS115H14V12	16 bit		±12V
ADS115H14V20			±20V
ADS115H14V40			±40V

The ADS125H18 EVM is provided with an ADS125H18V20 installed, while the ADS125H18 EVM GUI is intended to operate specifically with the ADS125H18V20. The user can replace the ADS125H18V20 with any device listed in Table 1-3; however, the user cannot use the ADS125H18 EVM GUI or PHI controller card if the user replaces the ADS125H18V20 already installed on the EVM. Refer to Section 2.7 for more information about using the ADS125H18 EVM with an external controller. The rest of this document assumes that the ADS125H18V20 is installed on the EVM, unless otherwise noted.

Figure 1-2 shows the block diagram for all input range options for the 16-bit ADS115H18 and 24-bit ADS125H18.

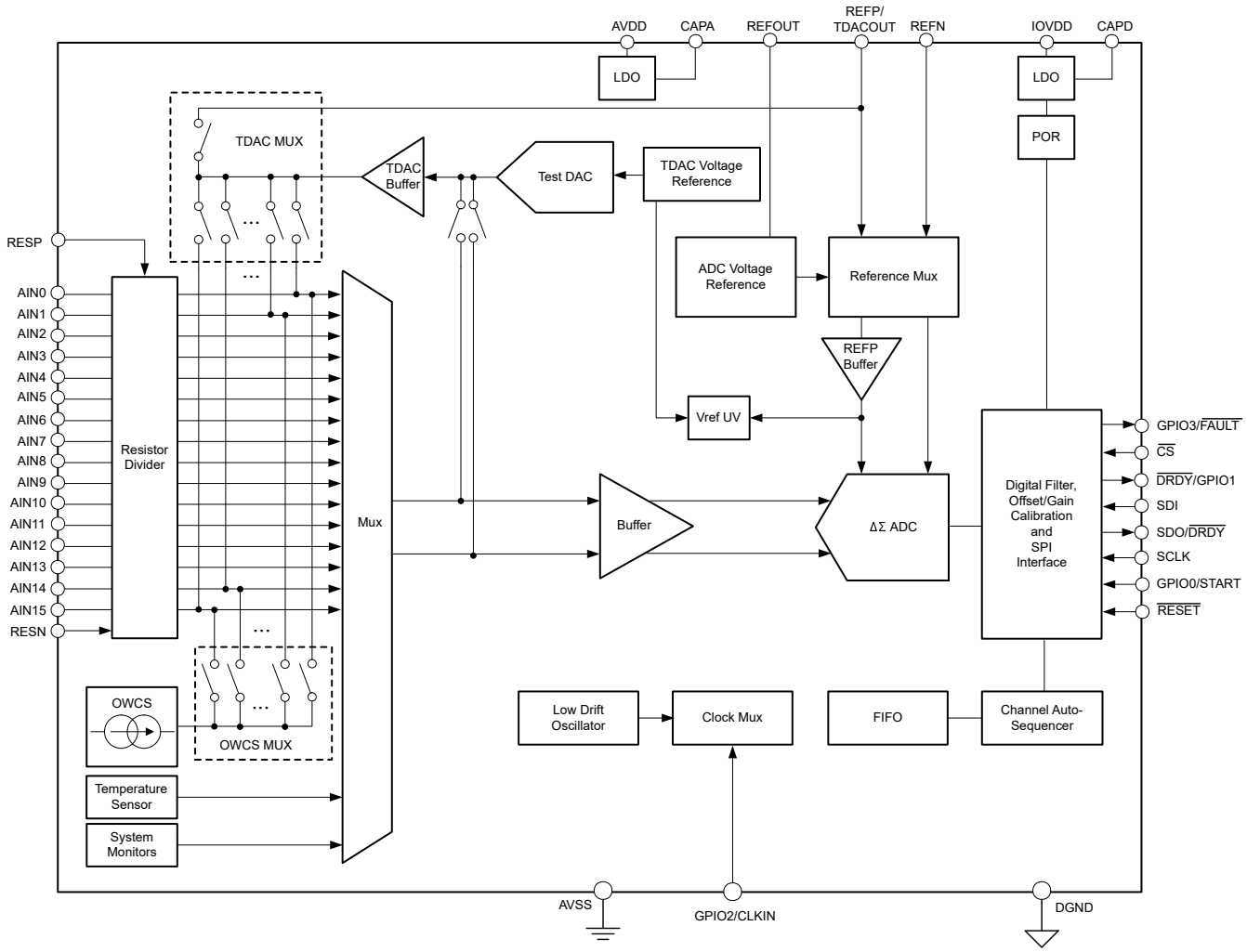


Figure 1-2. ADS115H18 and ADS125H18 Block Diagram

2 Hardware

2.1 Analog Inputs

The ADS125H18 EVM supports multiple configuration types. By default, the EVM includes input channels that support differential voltage measurements, differential current measurements, single-ended current measurements, or combined differential voltage or current measurements. Table 2-1 shows the default configuration for each ADC channel. Subsequent sections describe the input structure for each configuration type in more detail.

Table 2-1. Default Configuration for each ADC Channel Pair

ADC CHANNEL	DEFAULT CONFIGURATION
AIN0	Single-ended current
AIN1	Single-ended current
AIN2 / AIN3	Differential current OR voltage
AIN4 / AIN5	Differential current OR voltage
AIN6	Single-ended current
AIN7	Single-ended current
AIN8 / AIN9	Differential voltage
AIN10 / AIN11	Differential voltage
AIN12 / AIN13	Differential current
AIN14 / AIN15	Differential current

2.1.1 Differential Current Input Channels

Figure 2-1 shows the schematic for one input channel that, by default, measures differential current signals from -20mA to +20mA. This current flows through a PCB-mounted shunt that is converted to a voltage and then measured by the ADS125H18.Table 2-2 describes the function of each component in the differential current input channel schematic. Additionally, Table 2-2 references component designators specifically from Figure 2-1; however, the information in the table generally applies to all differential current input channels.

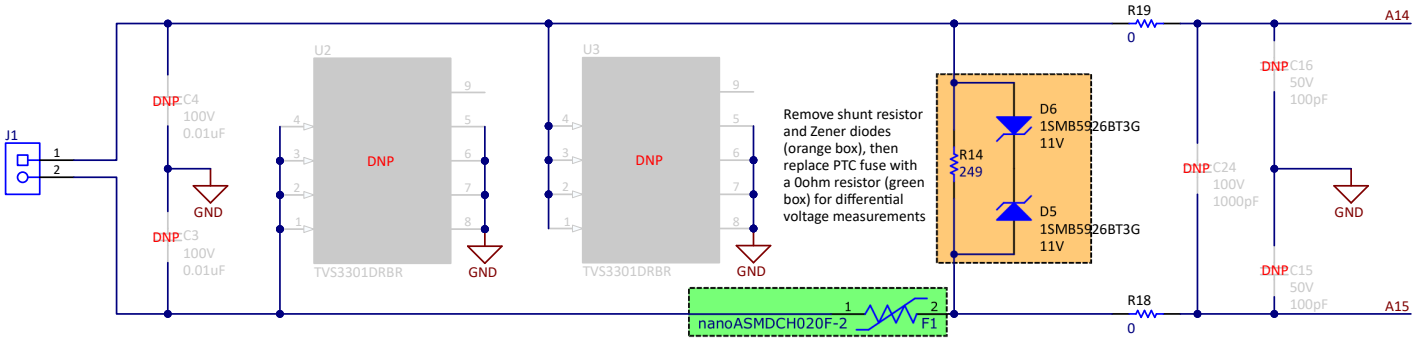


Figure 2-1. Differential Current Input Channel

Table 2-2. Important Components (Differential Current Input Channels)

COMPONENT	FUNCTION
Terminal block (J1)	Apply one differential current signal per terminal block
TVS diode (U2 and U3)	• Protection device that limits transient voltage into the ADC • The recommended component (TVS3301) offers bidirectional voltage suppression at a typical breakdown voltage of 37.5V The TVS diodes are not installed by default on this channel
Shunt (R14)	Converts the current signal to a voltage to be read by the ADC
Zener diodes (D5 and D6)	Protection device that limits the current through the shunt in case of a sustained positive or negative overvoltage event
PTC fuse (F1)	Protection device whose resistance increases with temperature, thereby increasing the total circuit resistance. This increased resistance limits the current through the shunt in the case of a sustained overvoltage event
Filter components (R18, R19, C15, C16, and C24)	Provides additional input filtering if desired The capacitors are not installed by default on this channel. The installed resistors are 0Ω

Figure 2-1 shows that the default current input channel configuration is differential-ended. As a result, the EVM supports measurement of current inputs that are at different common-mode voltages. However, verify that the absolute voltage on any input pin does not exceed the values specified in the ADS125H18 datasheet.

A differential current input channel can also be configured as a differential voltage input channel by removing the PCB-mounted shunt and Zener diodes, as well as replacing the PTC fuse with a 0Ω resistor.

2.1.2 Differential Voltage Inputs Channels

Figure 2-2 shows the schematic for one input channel that, by default, measures differential voltage signals from -10V to +10V. This voltage is measured directly by the ADS125H18 without the need for external attenuation. Table 2-3 describes the function of each component in the differential voltage input channel schematic. Additionally, Table 2-3 references component designators specifically from Figure 2-2; however, the information in the table generally applies to all differential voltage input channels.

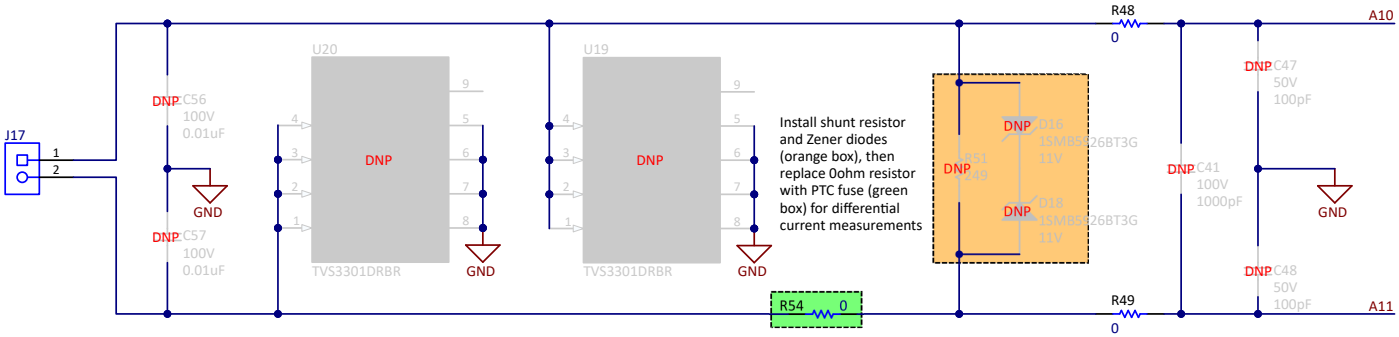


Figure 2-2. Differential Voltage Input Channel

Table 2-3. Important Components (Differential Voltage Input Channels)

COMPONENT	FUNCTION
Terminal block (17)	Apply one differential voltage signal per terminal block
TVS diode (U19 and U20)	• Protection device that limits transient voltage into the ADC • The recommended component (TVS3301) offers bidirectional voltage suppression at a typical breakdown voltage of 37.5V The TVS diodes are not installed by default on this channel
Shunt (R51)	Converts the current signal to a voltage to be read by the ADC The shunt is not installed by default on this channel
Zener diodes (D16 and D18)	Protection device that limits the current through the shunt in case of a sustained positive or negative overvoltage event The Zener diodes are not installed by default on this channel
0Ω resistor (R54)	Placeholder for a PTC fuse that must only be installed when the user reconfigures this channel for differential current measurements
Filter components (R48, R49, C41, C47, and C48)	Provides additional input filtering if desired The capacitors are not installed by default on this channel. The installed resistors are 0Ω

Figure 2-2 shows that the default voltage input channel configuration is differential-ended. As a result, the EVM supports measurement of voltage inputs that are at different common-mode voltages. However, verify that the absolute voltage on any input pin does not exceed the values specified in the ADS125H18 datasheet.

A differential voltage input channel can also be configured as a differential current input channel by installing the PCB-mounted shunt and Zener diodes, as well as replacing the 0Ω resistor with a PTC fuse.

2.1.3 Combined Differential Current and Voltage Input Channels

Figure 2-3 shows the schematic for one input channel that, by default, measures differential voltage signals from -10V to +10V. However, the user can also configure this channel to measure differential current signals from -20mA to +20mA. An isolated switch selects between the two modes by connecting or disconnecting a PCB-mounted shunt between the input terminals. This channel enables differential voltage measurements by default such that the PCB-mounted shunt is removed from the circuit. An ADC GPIO pin controls the isolated switch and is toggled by the GUI. The current or voltage is then measured directly by the ADS125H18 without the need for external attenuation.

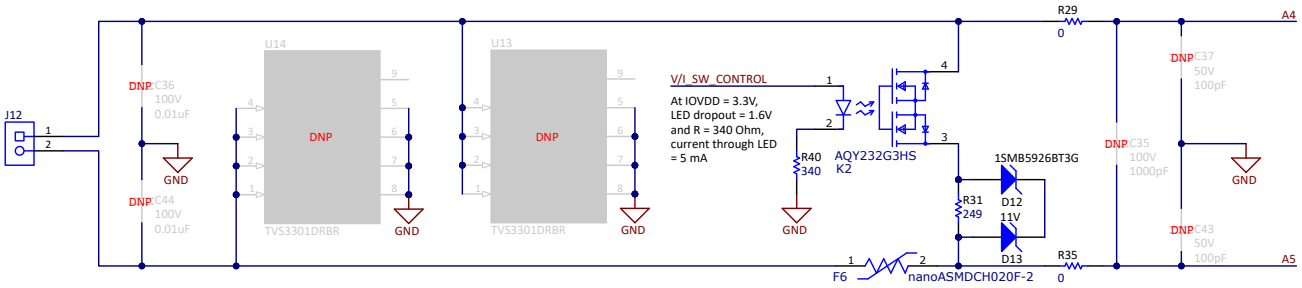


Figure 2-3. Combined Differential Current and Voltage Input Channel

Table 2-4 describes the function of each component in the combined differential current and voltage input channel schematic. Additionally, Table 2-4 references component designators specifically from Figure 2-3; however, the information in the table generally applies to all combined differential current and voltage input channels.

Table 2-4. Important Components (Combined Differential Current and Voltage Input Channels)

COMPONENT	FUNCTION
Terminal block (J12)	Apply one differential current or voltage signal per terminal block
TVS diode (U13 and U14)	• Protection device that limits transient voltage into the ADC • The recommended component (TVS3301) offers bidirectional voltage suppression at a typical breakdown voltage of 37.5V The TVS diodes are not installed by default on this channel
Isolated switch (K2)	• Low-ohm (0.35Ω max) switch controlled by ADC GPIO3 • Enable this switch in current mode and disable this switch in voltage mode • Both switches (K1 [not shown] and K2) are controlled by the same GPIO and are therefore always in the same mode • The default measurement mode is differential voltage
Shunt (R31)	Converts the current signal to a voltage to be read by the ADC
Zener diodes (D12 and D13)	Protection device that limits the current through the shunt in case of a sustained positive or negative overvoltage event
PTC fuse (F6)	Protection device whose resistance increases with temperature, thereby increasing the total circuit resistance. This increased resistance limits the current through the shunt in the case of a sustained overvoltage event
Filter components (R29, R35, C35, C37, and C43)	Provides additional input filtering if desired The capacitors are not installed by default on this channel. The installed resistors are 0Ω

Figure 2-3 shows that the default input channel configuration is differential-ended. As a result, the EVM supports measurement of current and voltage inputs that are at different common-mode voltages. However, verify that the absolute voltage on any input pin does not exceed the values specified in the ADS125H18 datasheet.

2.1.4 Single-Ended Current Input Channels

Figure 2-4 shows the schematic for two input channels that each, by default, measure single-ended current signals from 0mA to +20mA. This current flows through a PCB-mounted shunt that is converted to a voltage and then measured by the ADS125H18. Table 2-5 describes the function of each component in the single-ended current input channel schematic. Additionally, Table 2-5 references component designators specifically from Figure 2-4; however, the information in the table generally applies to all single-ended current input channels.

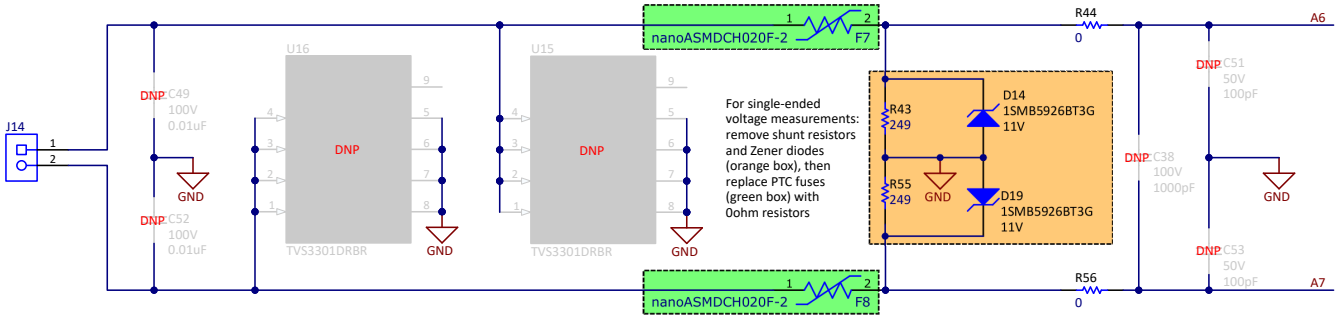


Figure 2-4. Single-Ended Current Input Channels

Table 2-5. Important Components (Single-Ended Current Input Channels)

COMPONENT	FUNCTION
Terminal block (J14)	Apply one or two single-ended current signals per terminal block
TVS diode (U15 and U16)	• Protection device that limits transient voltage into the ADC • The recommended component (TVS3301) offers bidirectional voltage suppression at a typical breakdown voltage of 37.5V The TVS diodes are not installed by default on this channel
Shunt (R43 and R55)	Converts the current signal to a voltage to be read by the ADC
Zener diodes (D5 and D6)	Protection device that limits the current through the shunt in case of a sustained positive overvoltage event. In the case of a sustained negative overvoltage event, the diode is forward biased and the user measures the diode forward voltage drop
PTC fuse (F7 and F8)	Protection device whose resistance increases with temperature, thereby increasing the total circuit resistance. This increased resistance limits the current through the shunt in the case of a sustained overvoltage event
Filter components (R44, R56, C38, C51, and C53)	Provides additional input filtering if desired The capacitors are not installed by default on this channel. The installed resistors are 0Ω

Figure 2-4 shows that the default current input channel configuration is single-ended. As a result, no common-mode voltage difference between input signals is allowed. Additionally, verify that the absolute voltage on any input pin does not exceed the values specified in the ADS125H18 datasheet.

A single-ended current input channel can also be configured as a single-ended voltage input channel by removing the PCB-mounted shunt and Zener diode, as well as replacing the PTC fuse with a 0Ω resistor.

2.2 ADC Connections and Decoupling

Figure 2-5 shows all connections to the ADS125H18 data converter. Each power supply connection has a 1µF decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the ground plane. Each digital pin has a 49.9Ω series resistor near the driving source. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. Although not strictly required, these components can be included in the final design to improve digital signal integrity. Also, digital inputs $\overline{\text{RESET}}$ and START each have 10kΩ pullup or pulldown resistors to verify that the ADC powers up in a known state.

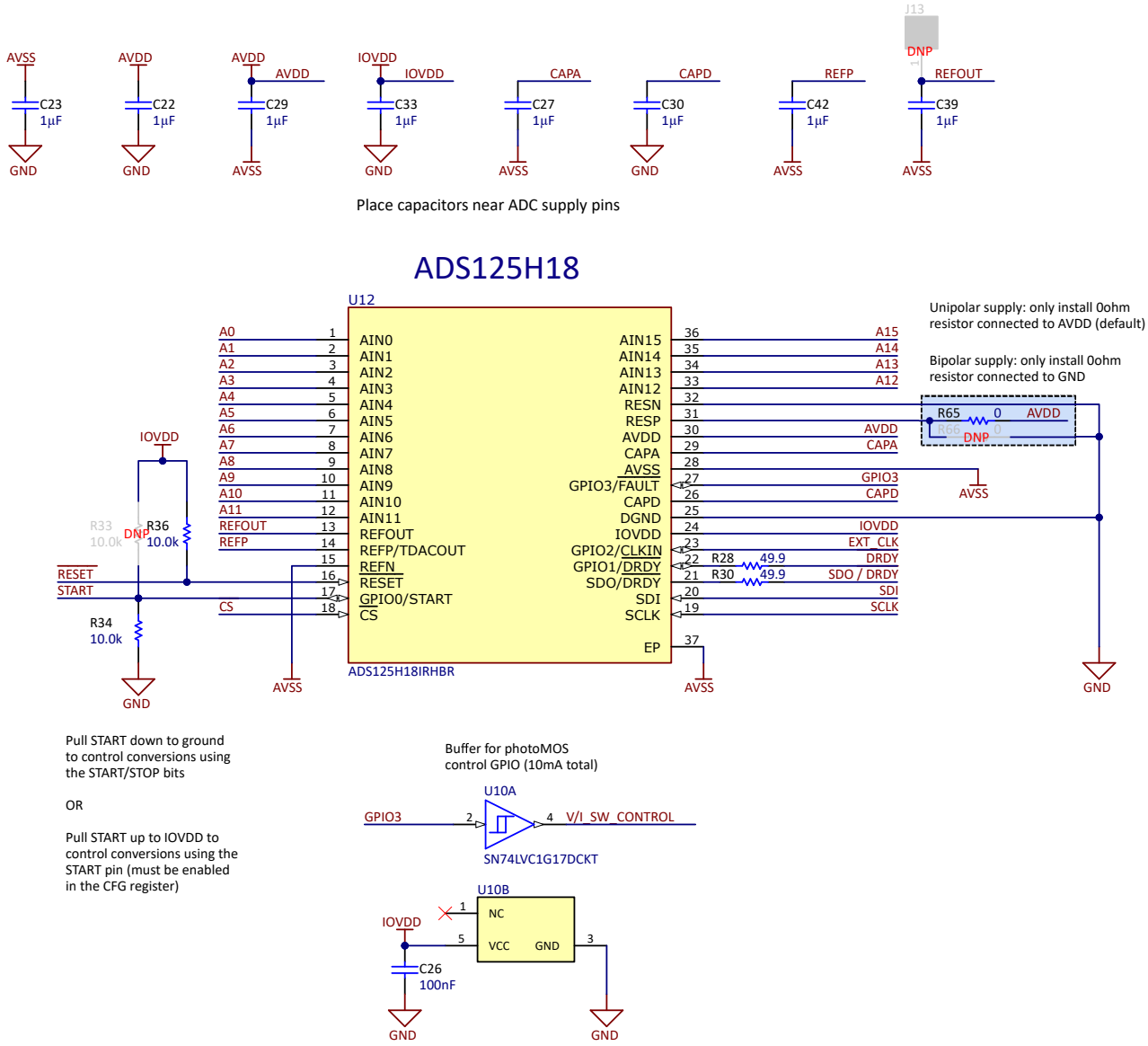


Figure 2-5. ADC Connections and Decoupling

Figure 2-5 also shows two different configurations for the RESP pin. The RESP pin sets the voltage level for floating inputs, which depends on the power supply configuration for AVDD. The default EVM AVDD supply configuration is unipolar. This configuration requires installing R65 such that RESP connects to AVDD. For bipolar supplies, remove R65 and install a 0Ω resistor at R66. See Section 2.4 for more information about the EVM power supply options.

Finally, Figure 2-5 includes a buffer for the ADC GPIO3 output pin. The GPIO3 pin does not have sufficient drive strength to turn on both isolated switches (see Figure 2-3). Instead, the buffer provides additional current to allow the user to enable both switches simultaneously.

2.3 Digital Interface

As noted in Section 1.1, the EVM interfaces with the PHI and communicates with the computer over the USB. The PHI communicates with two devices on the EVM: the ADS125H18 (over SPI) and the EEPROM (over I2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS125H18 platform. The EEPROM is no longer used after the hardware is initialized.

The ADS125H18 requires SPI serial communication such that CPOL = 0 and CPHA = 1. Header J10, shown in Figure 2-6, provides test points to probe the digital signals with a logic analyzer. Additionally, header J10 can be used to connect communication signals from an external controller. Remove the PHI controller card from connector J11 before applying external signals to header J10.

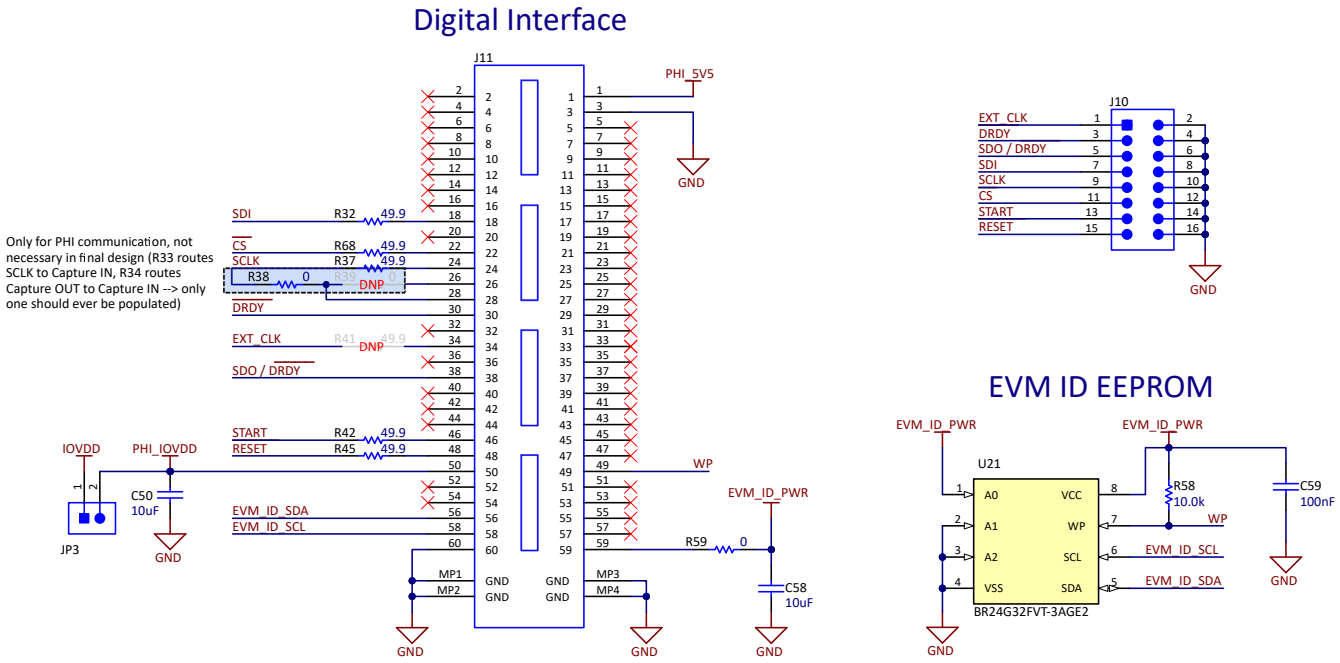


Figure 2-6. EVM Digital Interface and EEPROM

Similar to Figure 2-5, each digital pin has a 49.9Ω series resistor near the driving source. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. Although not strictly required, these components can be included in the final design to improve digital signal integrity.

Figure 2-6 also shows that jumper JP3 connects the PHI_DVDD and IOVDD nets. By default, the PHI_DVDD net provides 3.3V to the ADC digital supply (IOVDD) pin through jumper JP3. Remove the shunt on JP3 and apply a current meter (ammeter) to measure the digital current consumed by the ADC. If desired, removing the shunt on jumper JP3 also enables connection of an external IOVDD power source to pin 1 of jumper JP3. Verify that the IOVDD voltage applied to pin 1 of jumper JP3 is the same as the I/O voltage used by the external controller.

2.4 Power Supplies

Figure 2-7 shows the analog supply circuitry included on the ADS125H18 EVM. The default configuration applies a unipolar, 5V voltage to the ADC analog supply (AVDD) pin. Options are provided for external supplies as well as ±2.5V, bipolar supplies. LEDs indicate if the supply voltages are valid. Important power supply components and the functions are described in Table 2-6.

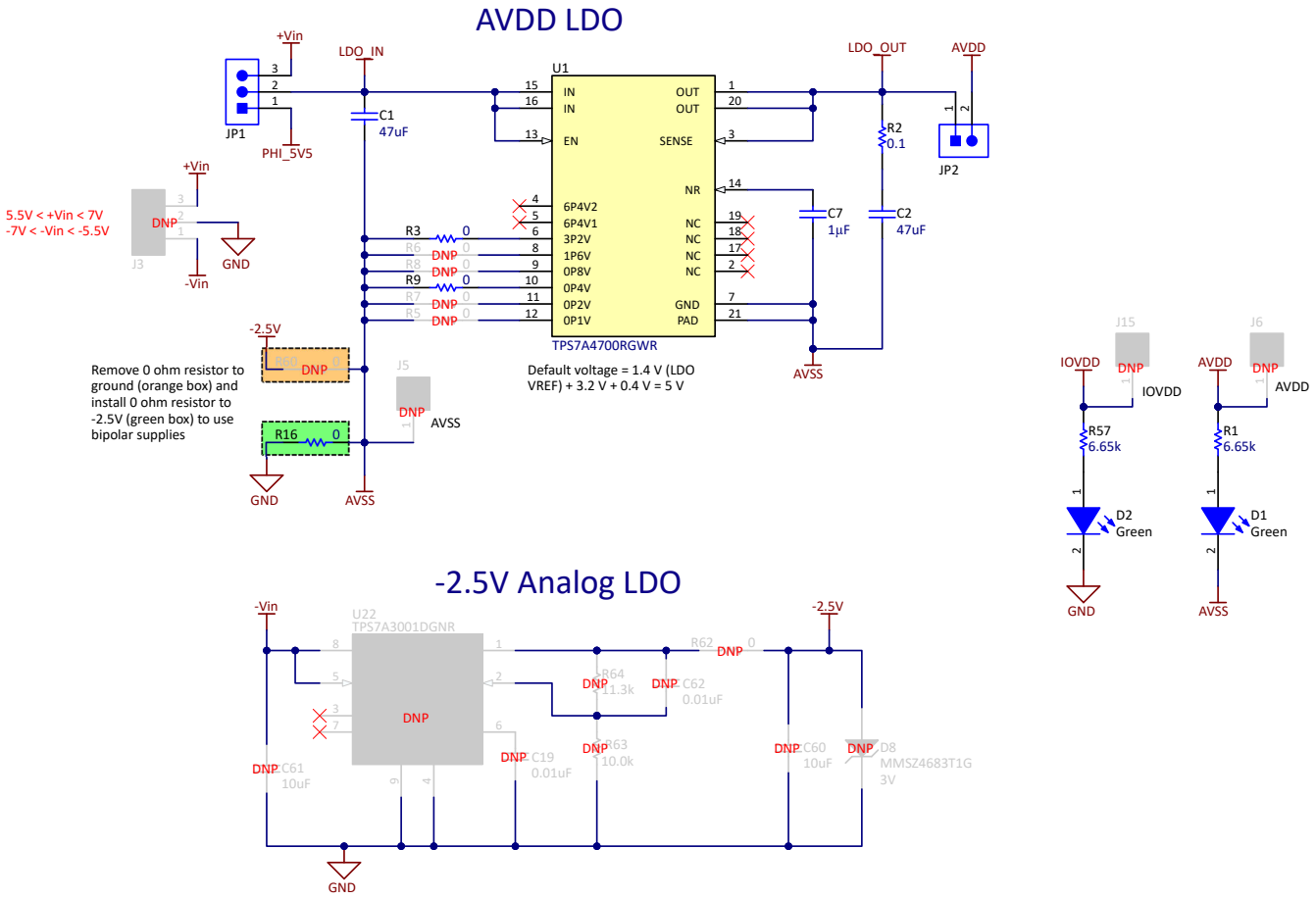


Figure 2-7. EVM Power Supplies

Table 2-6. Important Components (Power Supplies)

COMPONENT	FUNCTION
Input voltage jumper (JP1)	Selects the LDO power source: onboard 5.5V from the PHI (pin 1) or external power (pin 3)
Terminal block (J3)	Apply a positive supply voltage to pin 3 and a negative supply voltage to pin 1 (if applicable) when pin 3 is selected on jumper JP1. Verify that the external power supply inputs are within the limits specified in Figure 2-7 Terminal block J3 is not installed by default
TPS7A4700: adjustable, positive output LDO (U1)	Uses PHI 5.5V voltage as the input voltage and outputs 5V to AVDD by default If necessary, adjust the LDO output voltage using resistors R3 to R9, excluding R4
AVDD jumper (JP2)	Remove the shunt and apply a current meter (ammeter) to measure the analog current consumed by the ADC If desired, apply an external voltage directly to the ADC AVDD pin using pin 2. Ensure that the input voltage is within the range specified by the ADS125H18 datasheet
TPS7A300: fixed, negative output LDO (U22)	Provides a low-noise, clean -2.5V signal to the ADC analog ground (AVSS) pin. Requires the user to provide an external negative input as indicated in the description for "Terminal block (J3)" TPS7A300 is not installed by default

Table 2-6. Important Components (Power Supplies) (continued)

COMPONENT	FUNCTION
0Ω resistors (R16 and R60)	Selects the connection for the AVSS plane. By default, the EVM is configured for unipolar supplies such that AVSS is shorted to GND. For bipolar supplies, remove resistor R60 and install a 0Ω resistor at location R61 Resistor R60 is not installed by default
LEDs (D1 and D2)	Indicates if AVDD (D1) and IOVDD (D2) power supplies are valid

By default, the ADS125H18 EVM is configured to use a unipolar supply voltage that is supplied by a 5.5V voltage from the PHI controller card. However, several different power supply configurations are also possible, as described in Table 2-7:

Table 2-7. Configuring Different Power Supply Options on the ADS125H18 EVM

CONFIGURATION	IMPLEMENTATION STEPS
Change the adjustable LDO (11) output voltage	Remove and replace resistors R3 to R9, excluding R4, as needed. For example, set the LDO output voltage to 3V by removing 0Ω resistors R3 and R9, then installing 0Ω resistor R6 (1.6V). Since the LDO VREF = 1.4V, the total voltage is 1.4V + 1.6V = 3V Note that the LDO output voltage is with respect to AVSS
Apply an external, unipolar supply voltage to the LDO input	1. Remove the shunt on jumper JP1 2. Connect the external power supply ground to one of the GND test points on the EVM 3. Apply a voltage between 5.5V and 7V to pin 2 (LDO_IN) jumper JP1
Apply an external, unipolar supply voltage to AVDD	1. Remove the shunt on jumper JP2 2. Connect the external power supply ground to one of the GND test points on the EVM 3. Apply an external voltage directly to the ADC AVDD input using pin 2 of jumper JP2. Verify that the input voltage is within the range specified by the ADC datasheet
Use an external, ±2.5V bipolar supply voltage	1. Install terminal block J3 2. Install negative LDO (U22) and all surrounding passive components (see Figure 2-7) 3. Remove 0Ω resistors R16 and R65 4. Install 0Ω resistors R60 and R66 a. Refer to Figure 2-5 for the location of R16 and R60 5. Connect the external power supply ground to pin 2 (GND) on terminal block J3 6. Apply a voltage between -5.5V and -7V to pin 1 (-Vin) on terminal block J3 7. Apply a voltage between 5.5V and 7V to pin 3 (+Vin) on terminal block J3

2.5 Voltage Reference

Figure 2-8 shows an optional external voltage reference circuit included on the ADS125H18 EVM. The ADS125H18 integrates a low-noise, low-drift voltage reference that is sufficient for most applications. Alternatively, the EVM supports two external voltage reference options if desired. First, install header pin J11 and apply an external voltage source to this pin. Second, the EVM includes the 2.5V voltage reference REF6025 and its surrounding circuitry. However, these components are not included on the EVM by default and therefore must be installed by the user. Verify that any external reference voltage applied to the ADC meets the voltage requirements as described in Table 1-1. Additionally, configure the ADC registers as needed to use an external reference. Refer to the ADC datasheet for more information.

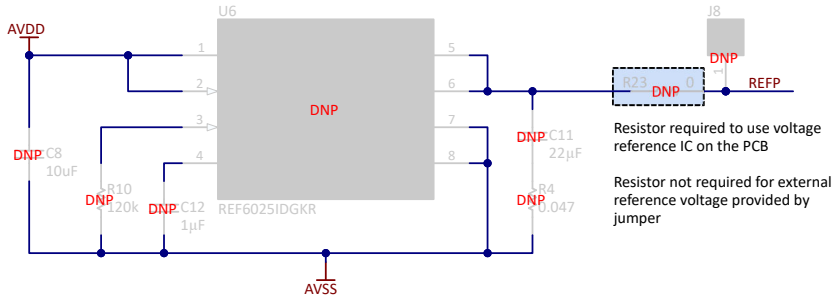


Figure 2-8. Optional External Reference Voltage Circuit

2.6 Clocking

Figure 2-9 shows an optional external clock connection on the ADS125H18 EVM using an SMA connector. The ADS125H18 integrates a high-accuracy oscillator that is sufficient for most applications. If necessary, the EVM includes component footprints to enable an external clock. By default, the SMA connector and series resistance are not installed, and therefore must be added to the EVM by the user. Verify that any external clock signal applied to the ADC meets the clocking requirements as described in Table 1-1. Additionally, configure the ADC registers as needed to use an external clock. Refer to the ADC datasheet for more information.

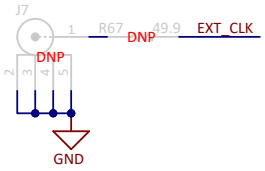


Figure 2-9. Optional External Clock Connection

2.7 Using the ADS125H18 EVM With an External Controller

The ADS125H18 EVM is designed for easy connection to an external controller. This design enables the user to test application code and firmware on the ADS125H18 without having to develop a custom PCB. This section describes the specific connections required to use the ADS125H18 EVM with an external controller. Figure 2-10 shows the location of various headers, connectors, and terminal blocks described in this section.

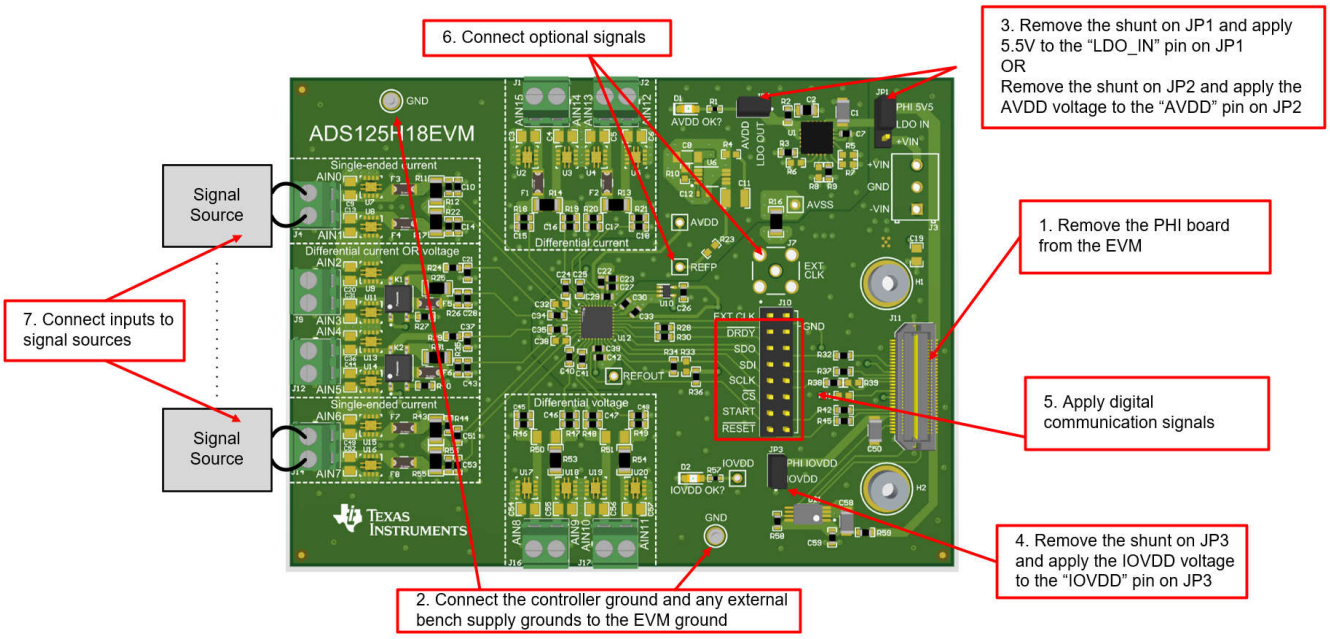


Figure 2-10. Connecting an External Controller to the ADS125H18 EVM

Complete the following steps to prepare the ADS125H18 EVM for use with an external controller:

1. Remove the PHI board if still connected to the EVM
2. Connect the external controller ground and bench supply ground to the GND pins on the EVM
3. Connect an external bench supply to the ADC AVDD pin by performing only one of the following two options:
   a. Remove the shunt on JP1 and apply 5.5V to the "LDO_IN" pin on JP1
   b. Remove the shunt on JP2 and apply the AVDD voltage to the "AVDD" pin on JP2
4. Connect an external bench supply to the ADC IOVDD pin by removing the shunt on JP3 and applying the IOVDD voltage to the "IOVDD" pin on JP3
5. Apply digital communication signals to header J10 on the EVM:
   a. Connect POCI (peripheral out, controller in) from the controller to the SDO pin
   b. Connect PICO (peripheral in, controller out) from the controller to the SDI pin
   c. Connect SCLK from the controller to the SCLK pin
   d. Connect $\overline{CS}$ from the controller to the $\overline{CS}$ pin
   e. Connect an I/O pin from the controller to the $\overline{DRDY}$ pin. $\overline{DRDY}$ is an output from the ADC that indicates when new data are ready to be clocked out of the ADC. Write a user-defined data collection routine that monitors this pin (polling or interrupt) and only transfers data after a falling edge
   f. (Optional) Connect I/O pins from the controller to the START and $\overline{RESET}$ pins to control conversions and reset the device, respectively
6. (Optional) Connect an external Clock or Voltage Reference
7. Connect the signal source to the terminal blocks

Verify that the external power supply voltages, communication signal levels, and applied input signals meet the specifications listed in Table 1-1

3 Software

3.1 Software Description

The ADS125H18EVM-PDK-GUI software suite includes graphical tools for data capture, full ADS125H18 register configuration, time domain analysis, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

3.2 ADS125H18 GUI Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* section of the ADS125H18 EVM tool folder. Then, run the GUI installer to install the EVM GUI software on your computer.

> Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer.exe file can be deleted.

Figure 3-1 through Figure 3-4 show the prompts seen by the user during the GUI installation process. Accept the license agreement and follow the on-screen instructions to complete the installation.

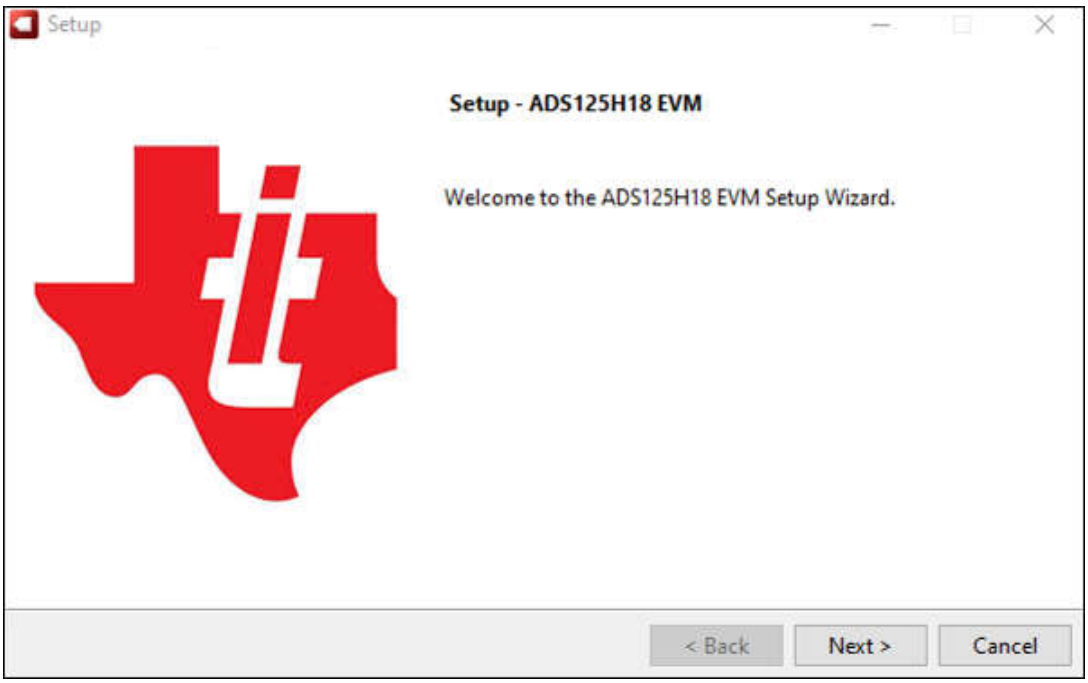


Figure 3-1. ADS125H18 EVM GUI Install Welcome Screen

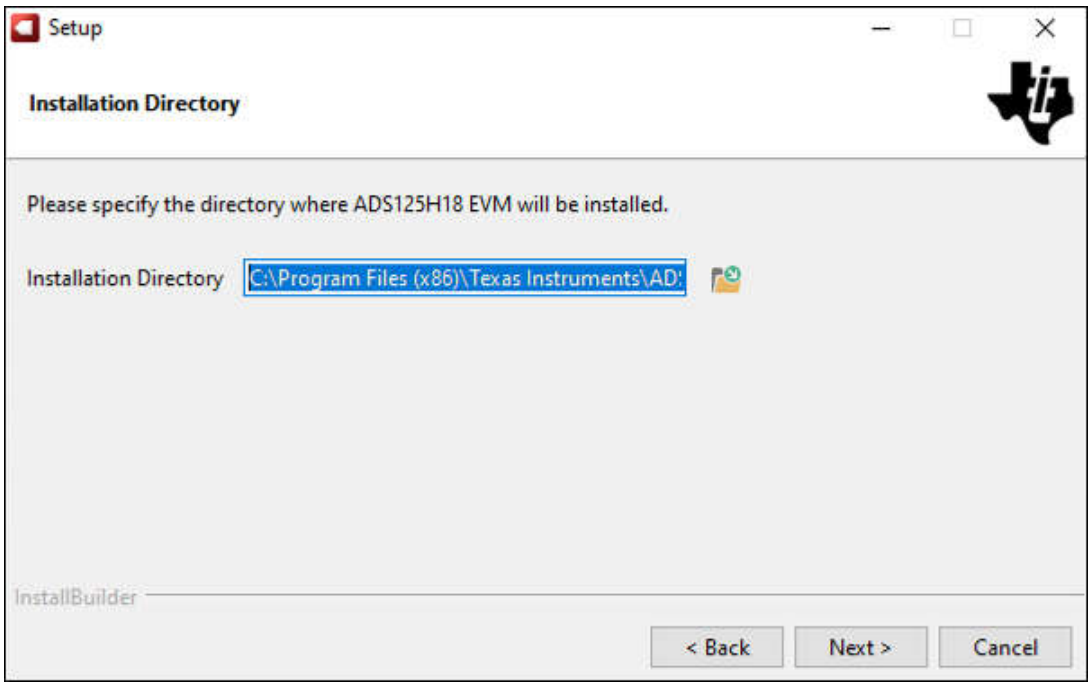


Figure 3-2. ADS125H18 EVM GUI Select Install Directory

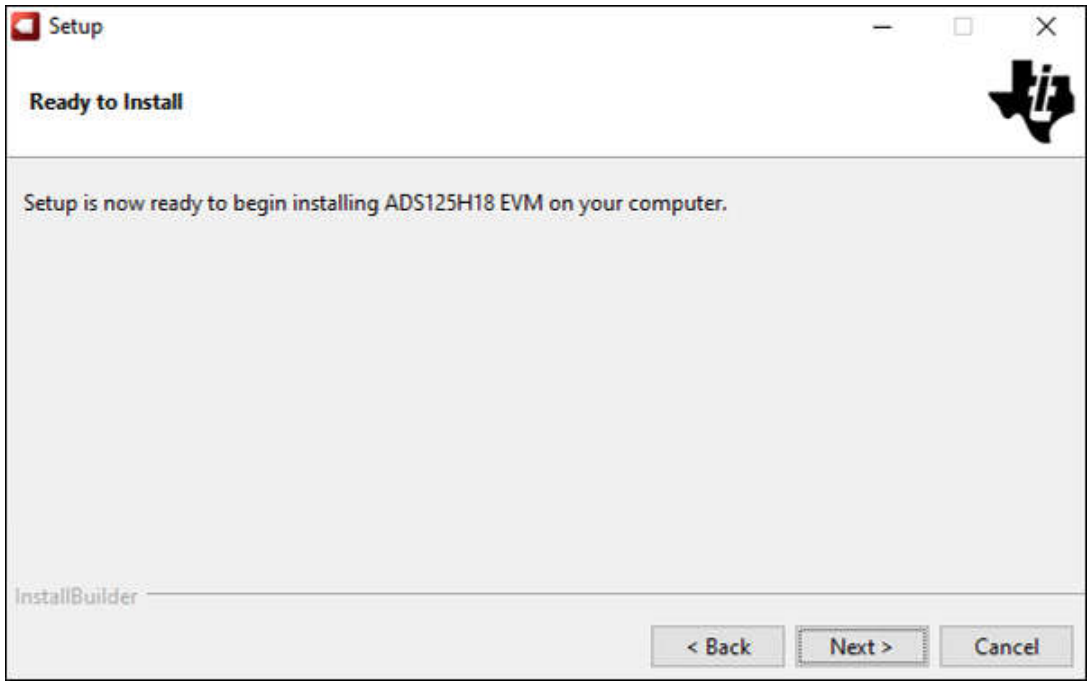


Figure 3-3. ADS125H18 EVM GUI Ready to Install

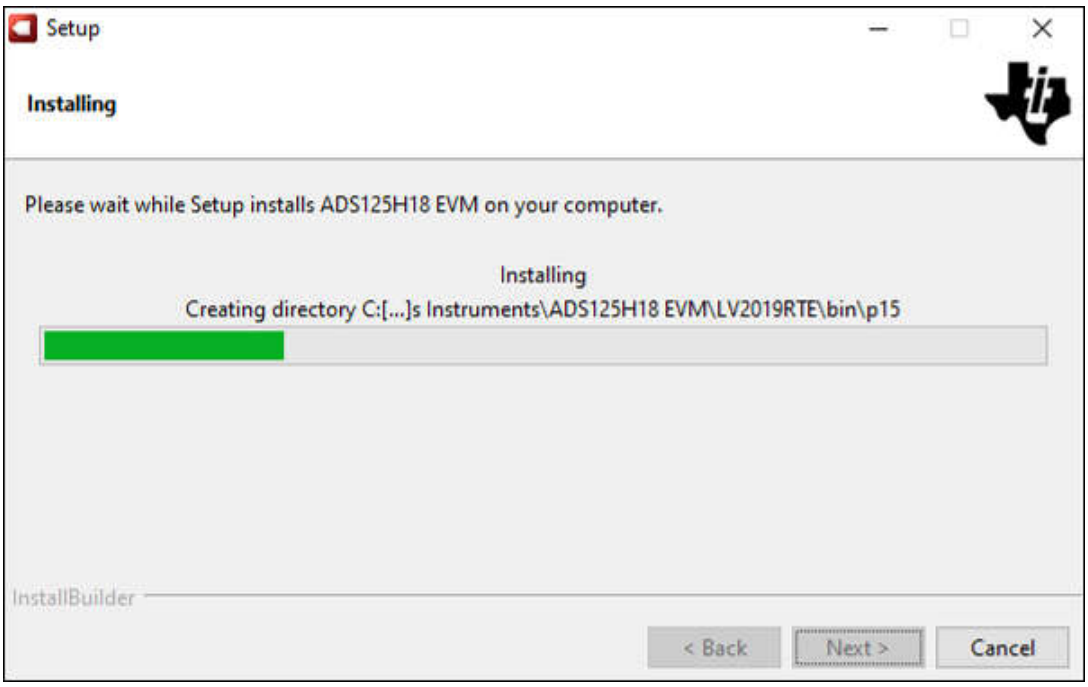


Figure 3-4. ADS125H18 EVM GUI Installing

The ADS125H18 EVM requires the LabVIEW™ run-time engine and can prompt for the installation of this software if not already installed. If applicable, this prompt occurs during the actual GUI installation (see Figure 3-4). However, the LabVIEW™ install prompt is not shown in this document.

Figure 3-5 shows the final prompt after the installation process completes. Click the *Finish* button to exit the installer.

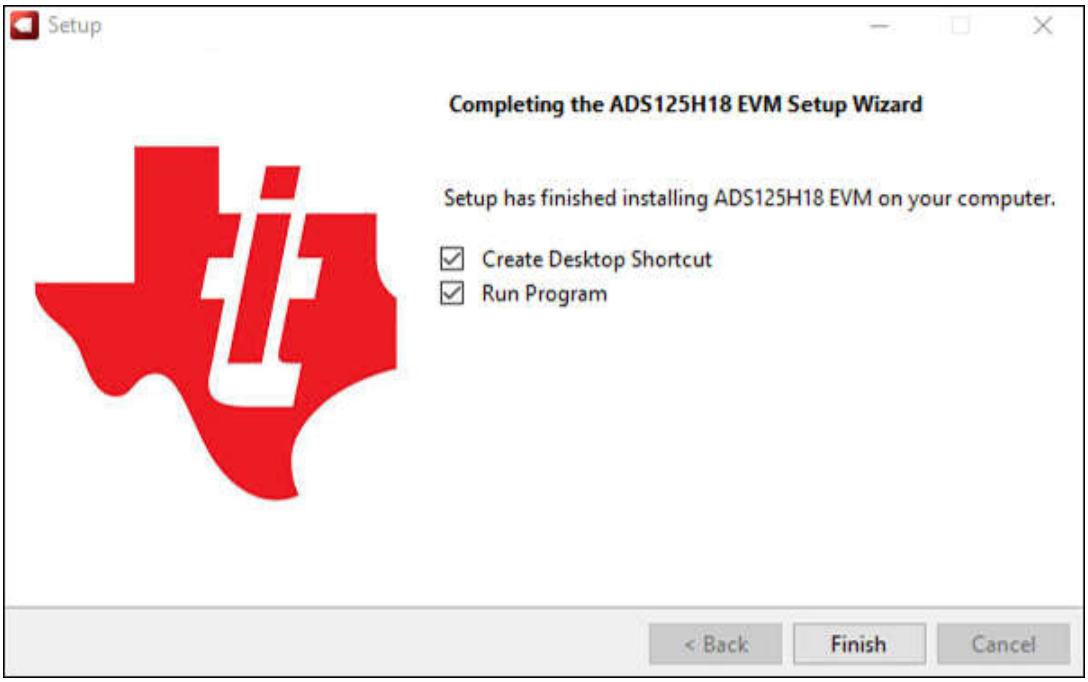


Figure 3-5. ADS125H18 EVM GUI Install Complete

4 Implementation Results

4.1 Hardware Connections

Connect the EVM as shown in Figure 4-1 after installing the software

1. Physically connect P2 of the PHI to J11 of the ADS125H18 EVM. Install the included screws to provide a robust connection.
2. (Optional) Connect an external Power Supply, Clock, or Voltage Reference
3. Verify the default jumper positions: JP2 and JP3 have shunts installed, and the shunt for JP1 is connected to the *PHI 5V5* net
4. Connect a USB cable between the PHI and the computer
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 4-1 shows the resulting LED indicators
5. Start the software GUI as shown in Figure 4-2. Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds.
6. Connect the signal source to the terminal blocks. Verify that the signal source voltage and current levels meet the specifications listed in Table 1-1

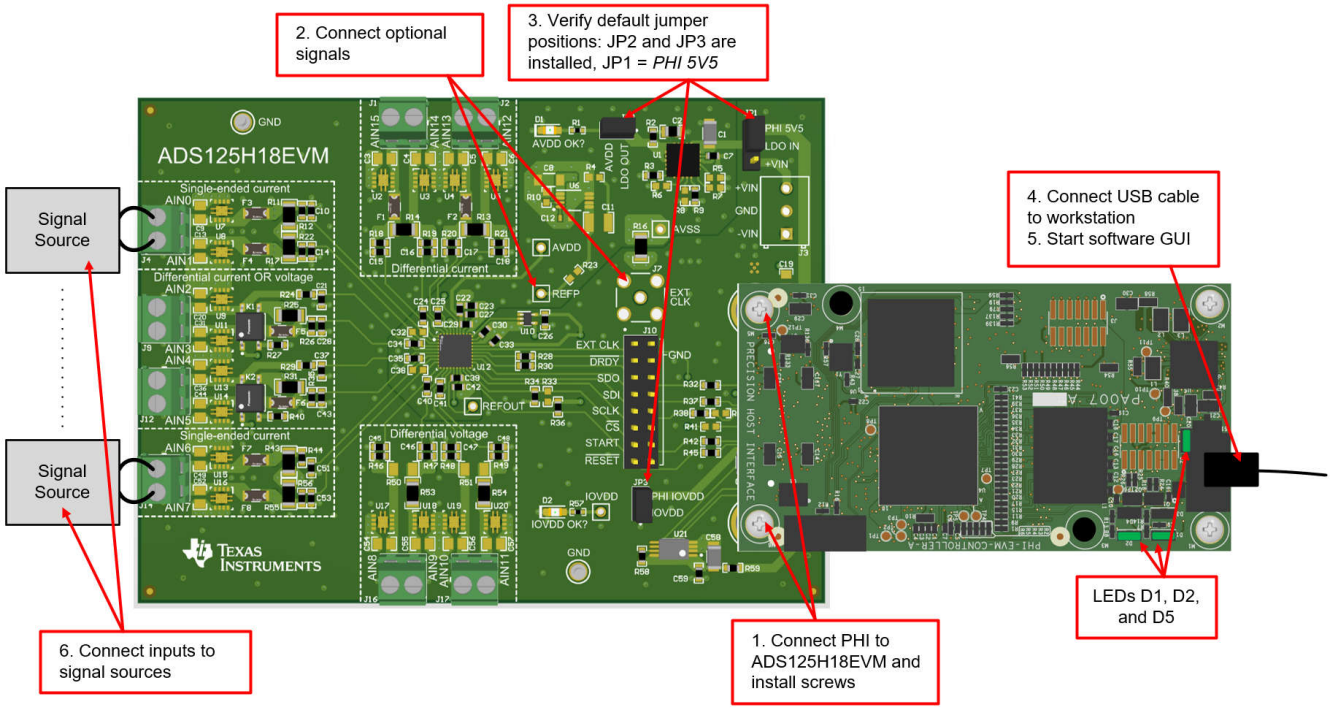


Figure 4-1. Connecting the Hardware to the ADS125H18 EVM

Figure 4-2. Launch the EVM GUI Software

4.2 GUI Operation

The following sections describe the operation and behavior of the ADS125H18 EVM GUI.

4.2.1 ADC Capture Settings and Sequencer Configuration

Figure 4-3 shows how the *Pages* control in the upper-left corner allows access to the other pages in the GUI. Navigate to any of the GUI pages using these controls. Figure 4-3 also shows the *ADC Capture* page. Use this page to easily configure the most important ADC settings, including the General Configuration and Step Configuration parameters, the sequencer mode, and the number of samples or sequences to capture.

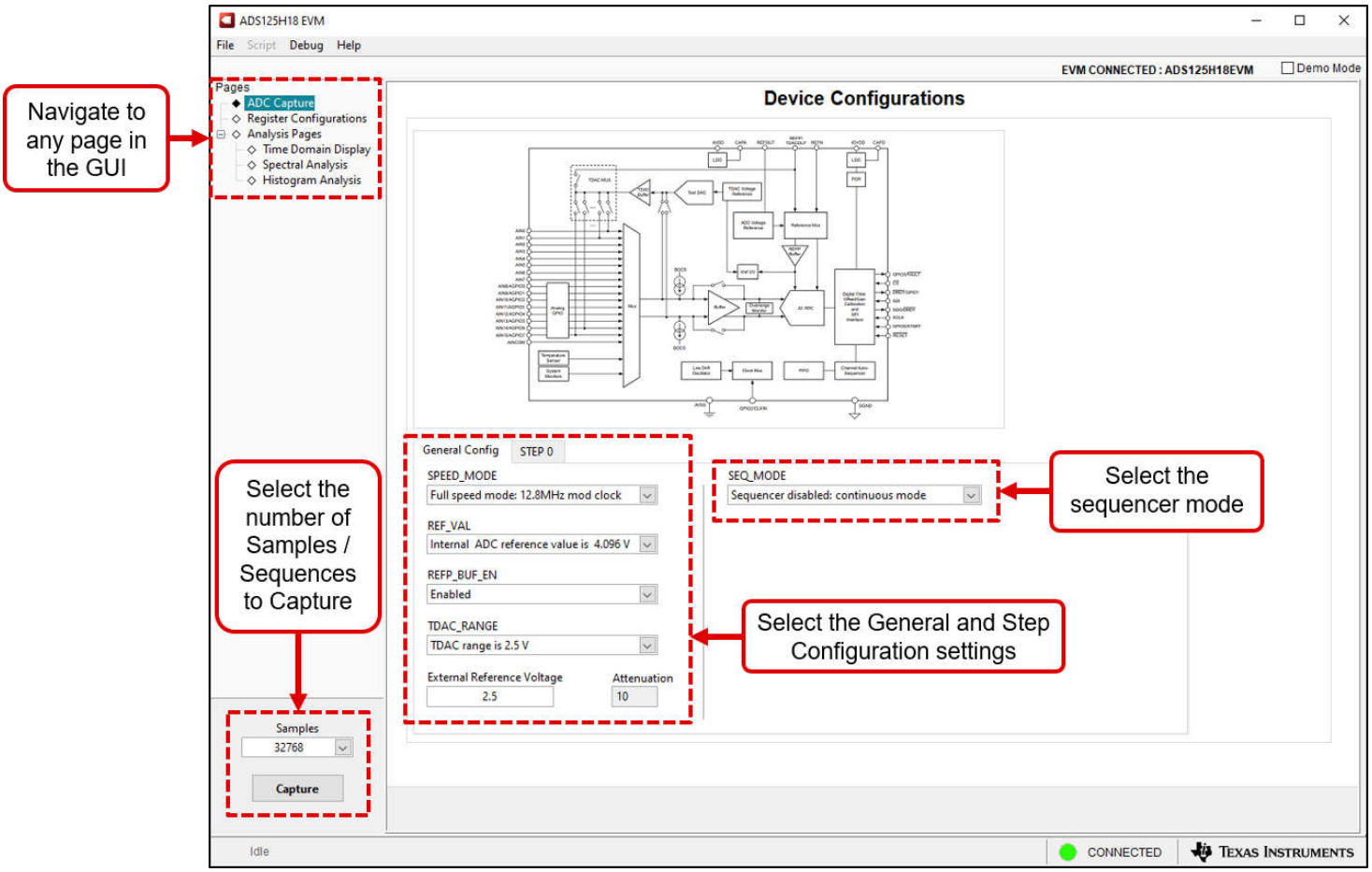


Figure 4-3. ADS125H18 EVM GUI ADC Capture Page - General Configuration

The General Configuration tab allows to user to set certain parameters that are used for all steps, including the speed mode, the internal reference voltage, the state of the reference buffer, and the Test DAC range. Additionally, the user can enter the *External Reference Voltage* if applicable. Finally, the ADC Capture page reports the device attenuation by reading the ADC DEVICE_ID register.

The default option in the sequencer mode dropdown in Figure 4-3 allows the user to capture *n* conversions of a single step, where *n* is the number entered in the box in the lower left of the GUI. Alternatively, enable the sequencer to capture *n* complete sequences of all enabled steps.

Figure 4-4 shows the *Step Configuration* tab. Use these controls to configure the settings for each individual step. When the sequencer is disabled, only Step 0 is shown.

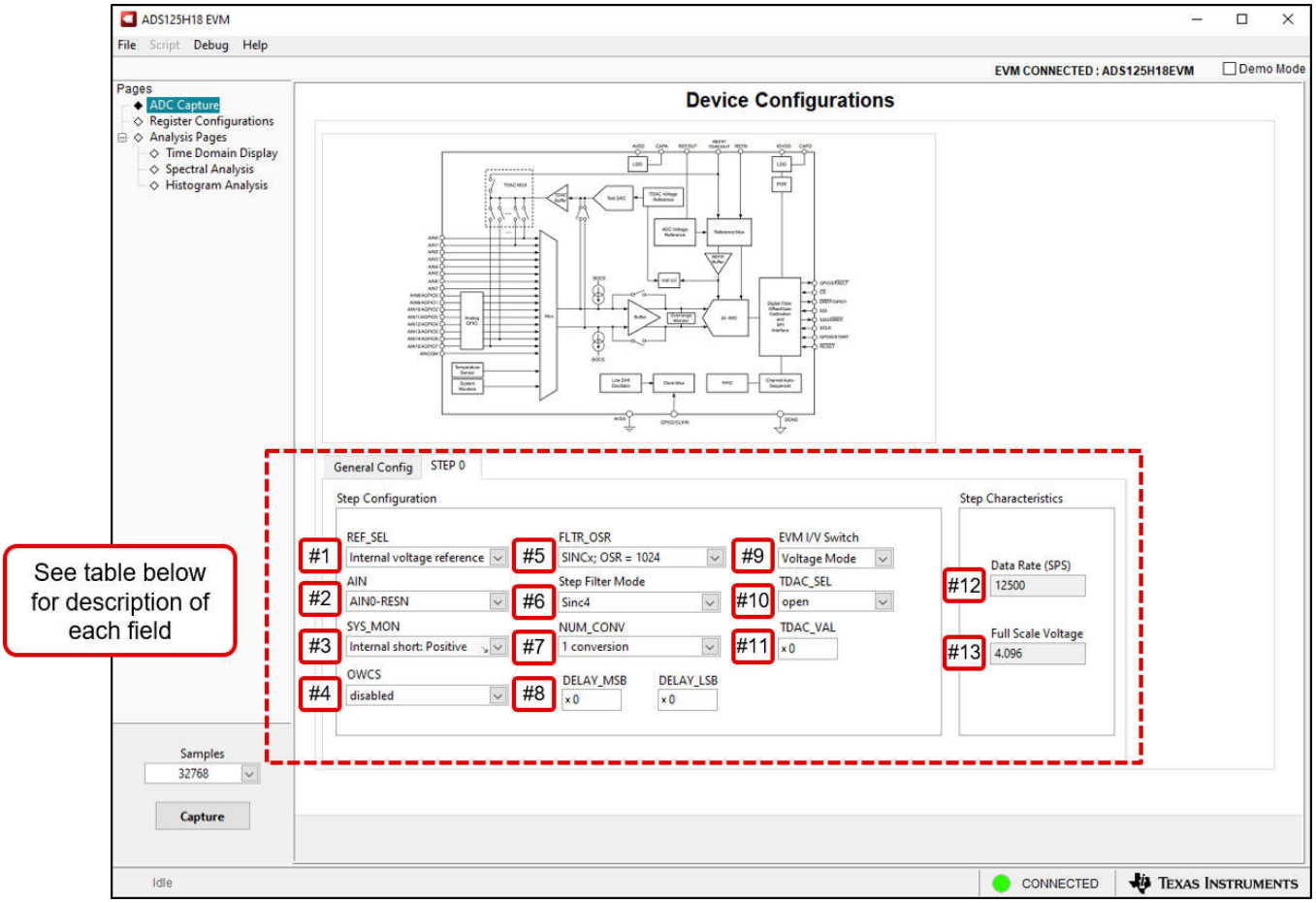


Figure 4-4. ADS125H18 EVM GUI ADC Capture Page - Step Configuration

Table 4-1 explains in more detail each field shown in Figure 4-4:

Table 4-1. Understanding the Step Configuration Page Parameters

ITEM #	PARAMETER	DESCRIPTION
1	REF_SEL	Select the reference voltage source to be used with this step
2	AIN	Select the measurement channel for this step
3	SYS_MON	Select the system monitor option to be measured in this step NOTE: the system monitor takes precedence over the AIN selection (see #2 above), and also uses the internal reference regardless of the selection in REF_SEL
4	OWCS	Enable or disable the open-wire current sources for this step
5	FLTR_OSR	Select the OSR for this step NOTE: the data rate corresponding to this OSR is shown on the right (see #12 below)
6	FLTR_MODE	Select the filter mode for this step
7	NUM_CONV	Enter the number of conversions for this step
8	DELAY	Enter the programmable delay to be used for this step NOTE: the delay value is measured in modulator clock periods (t_{MOD}), is a 16-bit field, and is entered in hex
9	EVM I/V SWITCH	Select the state of the I/V switch on the EVM for this step NOTE: this is a feature of the EVM, not the ADC. These switches are only installed on the EVM on differential channels AIN2/AIN3 and AIN4/AIN5, so this selection only affects those channels
10	TDAC_SEL	Select the location where the Test DAC voltage is output to in this step

Table 4-1. Understanding the Step Configuration Page Parameters (continued)

ITEM #	PARAMETER	DESCRIPTION
11	TDAC_VAL	Enter the value of the Test DAC voltage to be used for this step NOTE: the Test DAC value is some the reference voltage, is a 5-bit field, and must be entered in hex
12	Data Rate (SPS)	Data rate relative to the selected OSR (see #5 above), the clock frequency, and the clock mode NOTE: the clock mode is selected on the *General Config* tab
13	Full Scale Voltage	Calculates the full-scale voltage (FSV) for this step, where FSV = Reference Voltage * Attenuation NOTE: the reference voltage is set on the *General Config* tab, and the Attenuation factor is determined by reading the DEVICE_ID register

Enable the ADC sequencer by selecting "Sequencer enabled: continuous mode" from the SEQ_MODE dropdown. Multiple step options appear after selecting this configuration. Additionally, the *Capture* parameter changes from "Samples" to "Sequences". As a result, the GUI captures and displays the data for the desired number of sequences defined by the user. Figure 4-5 shows how the GUI changes after enabling the sequencer.

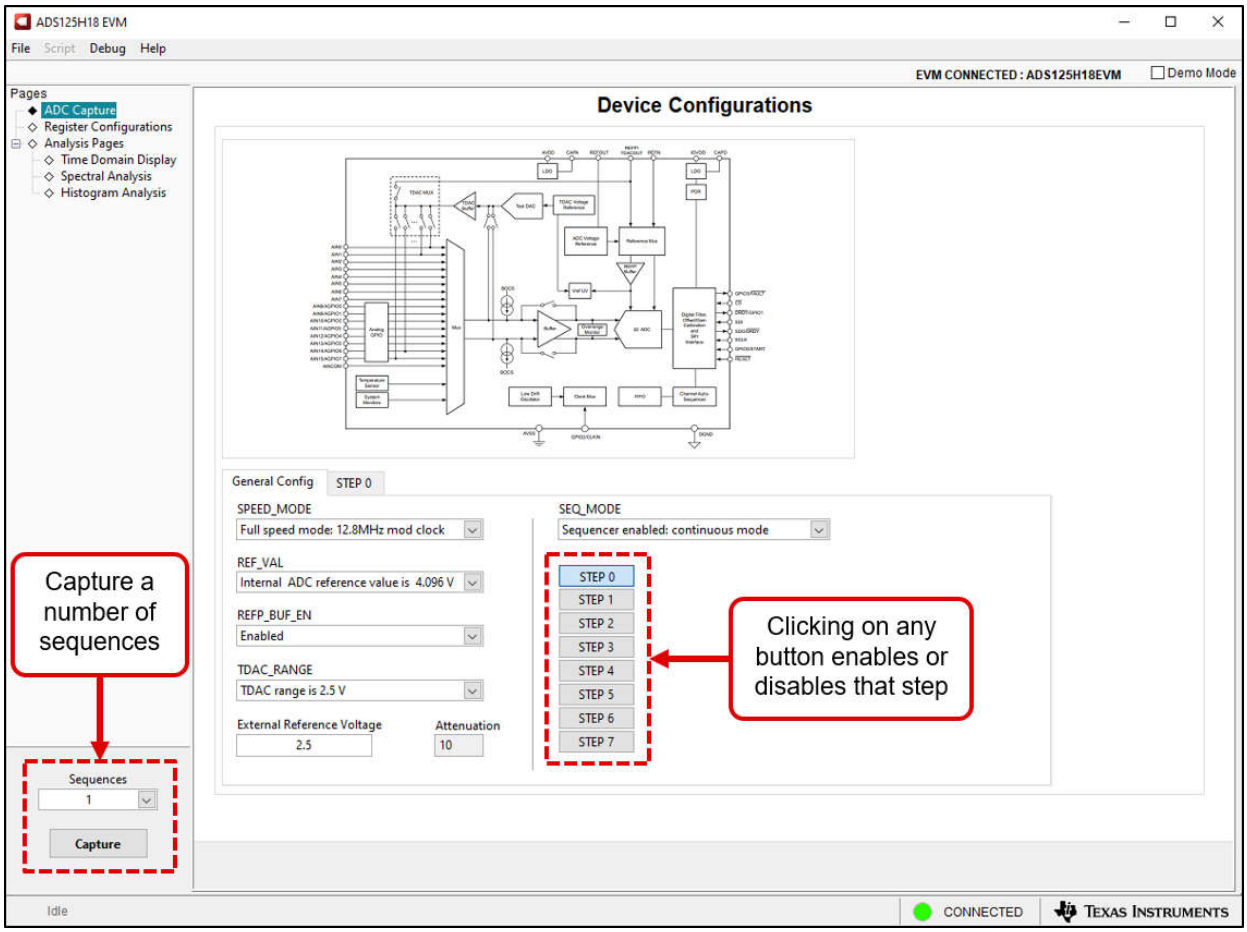


Figure 4-5. ADS125H18 EVM GUI ADC Capture Page - Enable Sequencer

After enabling the sequencer, Figure 4-6 shows how clicking on each individual step opens up a new *Step* tab. Clicking on the same step again closes that step tab. This is true for all steps except Step 0, which cannot be disabled.

Configure each enabled step as shown in Figure 4-4 and described in Table 4-1.

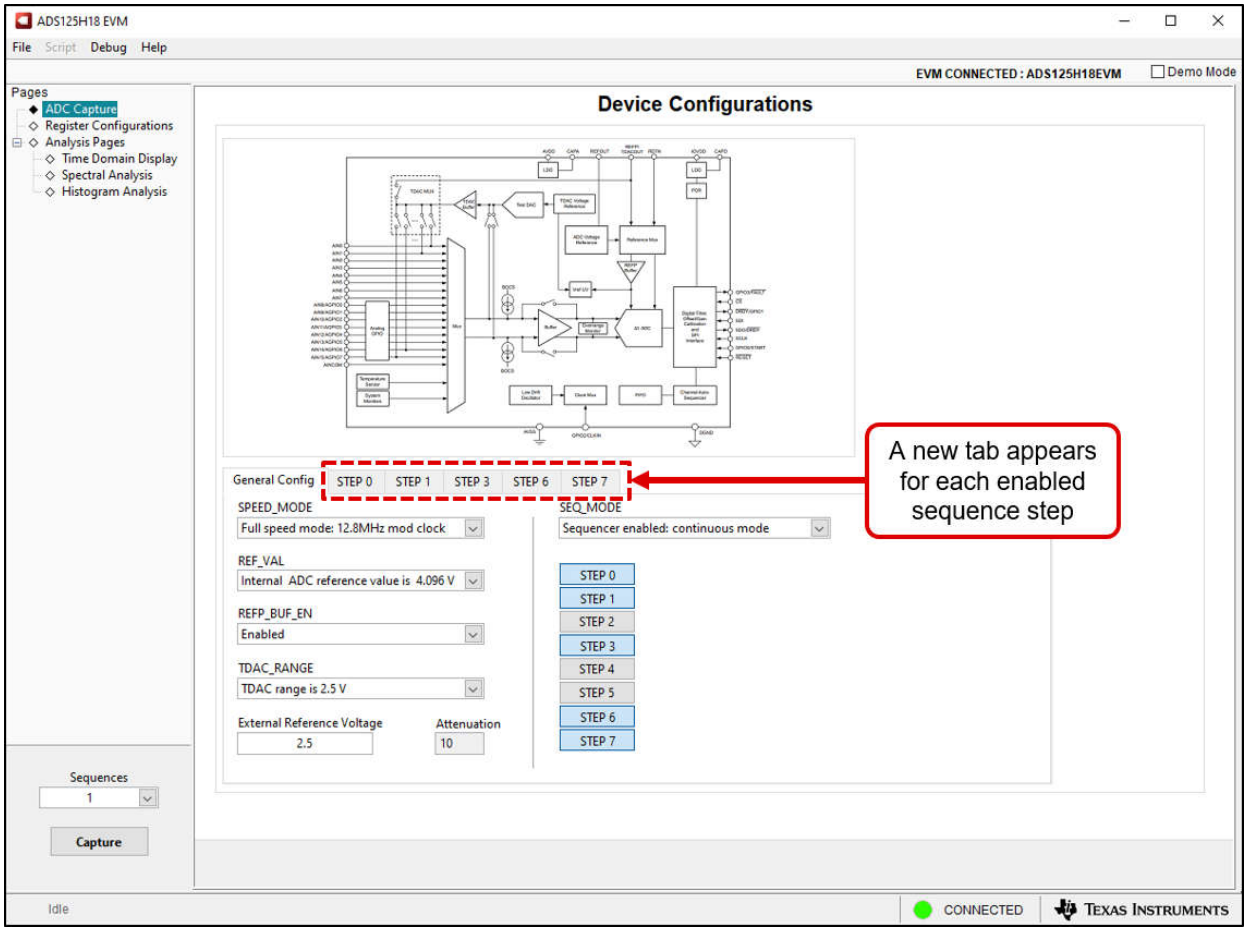


Figure 4-6. ADS125H18 EVM GUI ADC Capture Page - Enabling Multiple Sequence Steps

4.2.2 EVM Register Settings

Figure 4-7 shows a portion of the ADS125H18 register map. The registers can be used to configure any ADC register to change functions such as the data rate, setup the channel sequencer, or enable integrated features. Change the register settings by clicking on each bit, typing a value directly into the *Value* column, or by selecting from the drop-down menus in the *Field View* control.

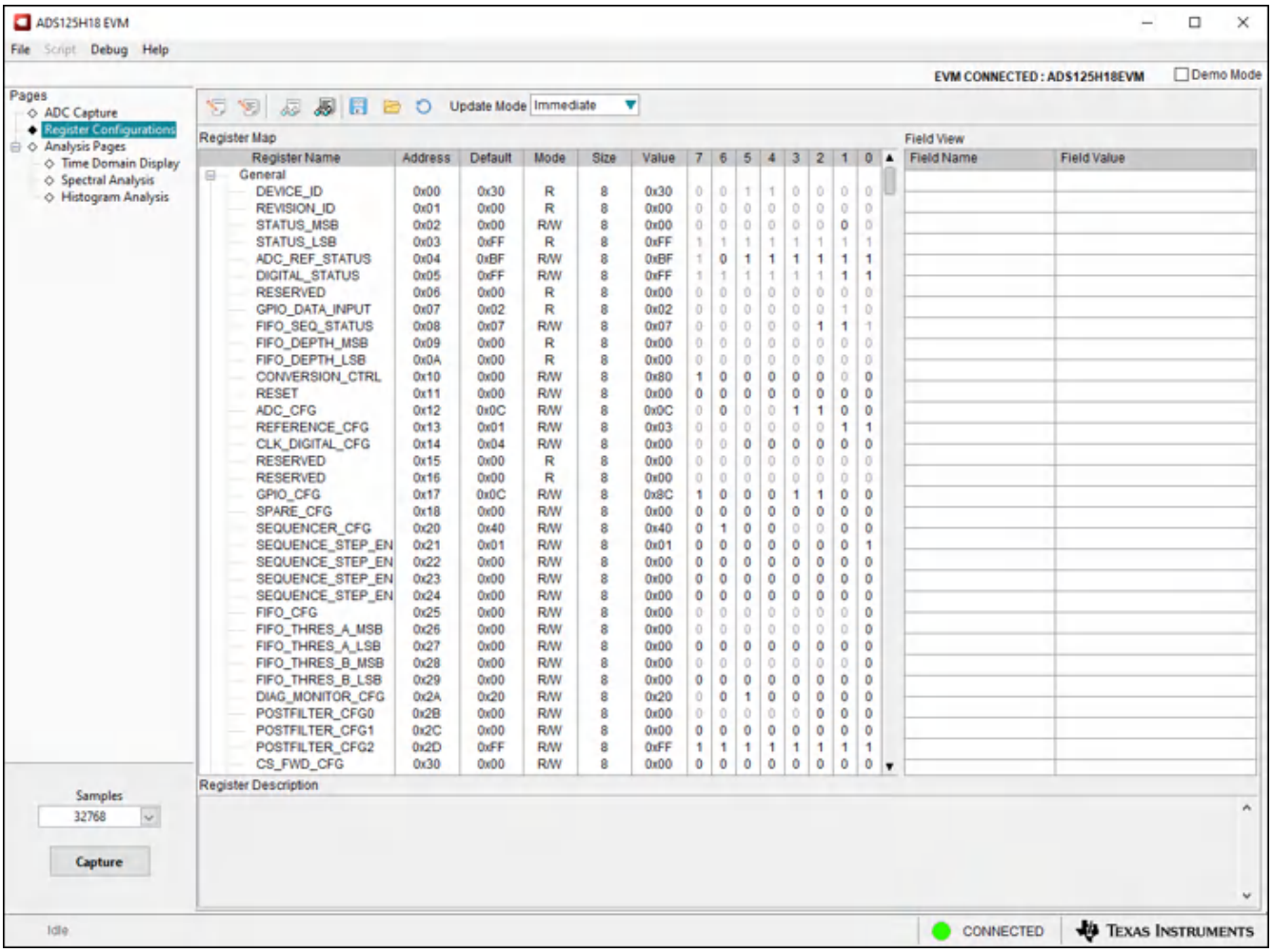


Figure 4-7. ADS125H18 EVM GUI Navigation and Register Map

Figure 4-8 shows a consolidated view of the entire ADS125H18 register map, which includes the *General* page as well as all 32 *Step* pages. Navigate to a specific register within a specific step using the scroll bar between the *Register Map* and *Field View* sections.

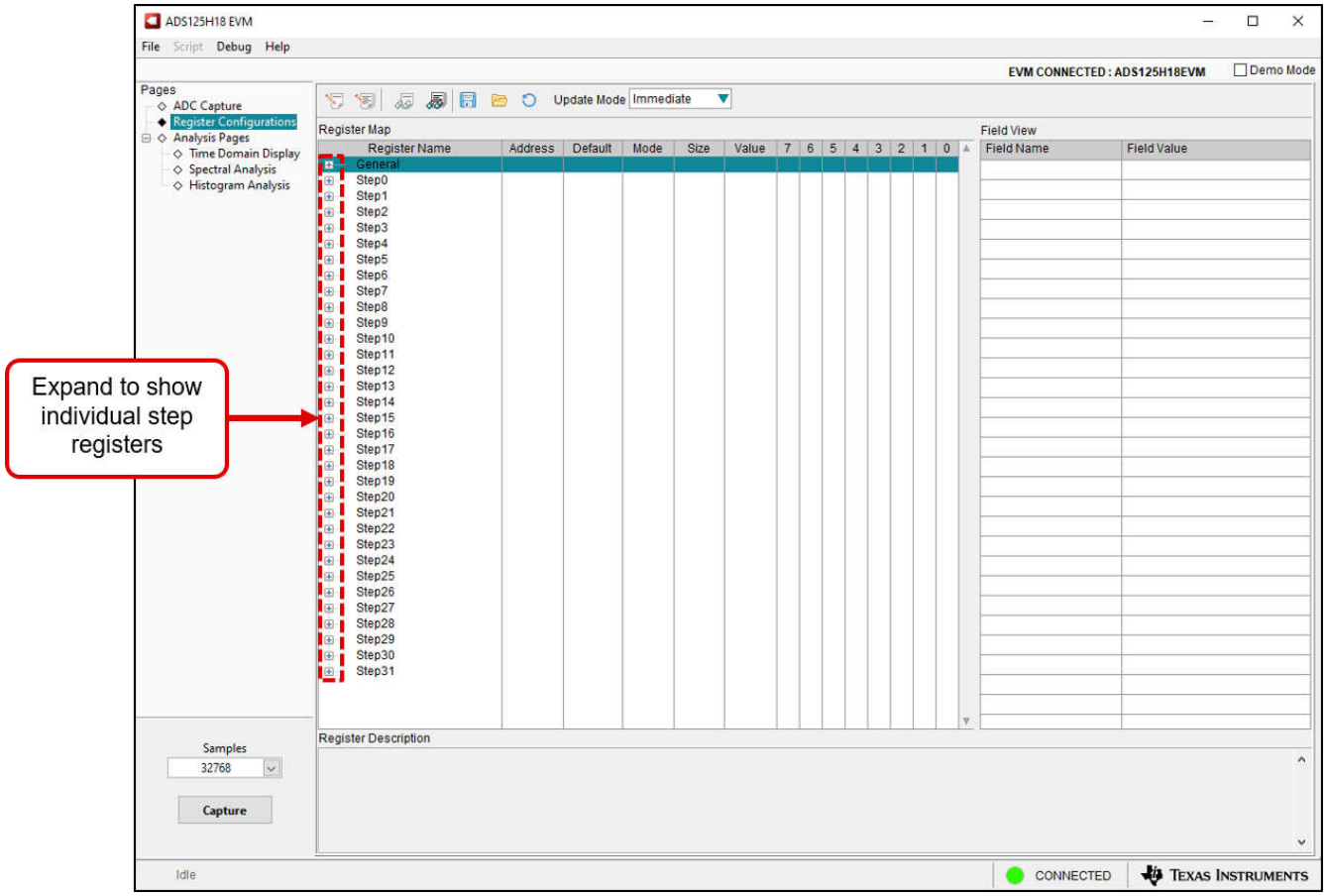


Figure 4-8. ADS125H18 EVM GUI Register Configurations Page - All Steps

4.2.3 Time-Domain Display

The time-domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for studying the behavior of and debugging any gross problems with the ADC or drive circuits. Trigger a data capture of the selected number of samples from the ADS125H18 EVM by using the *Capture* button in Figure 4-9. The time-domain plot has *Time* on the x-axis and by default shows the corresponding *Voltage* on the y-axis relative to the specified reference voltage.

The *Measurements* control on the bottom of Figure 4-9 calculates the code range, the mean code, and the code standard deviation. Switching pages to any of the *Analysis* tools described in the subsequent sections causes calculations to be performed on the same set of data.

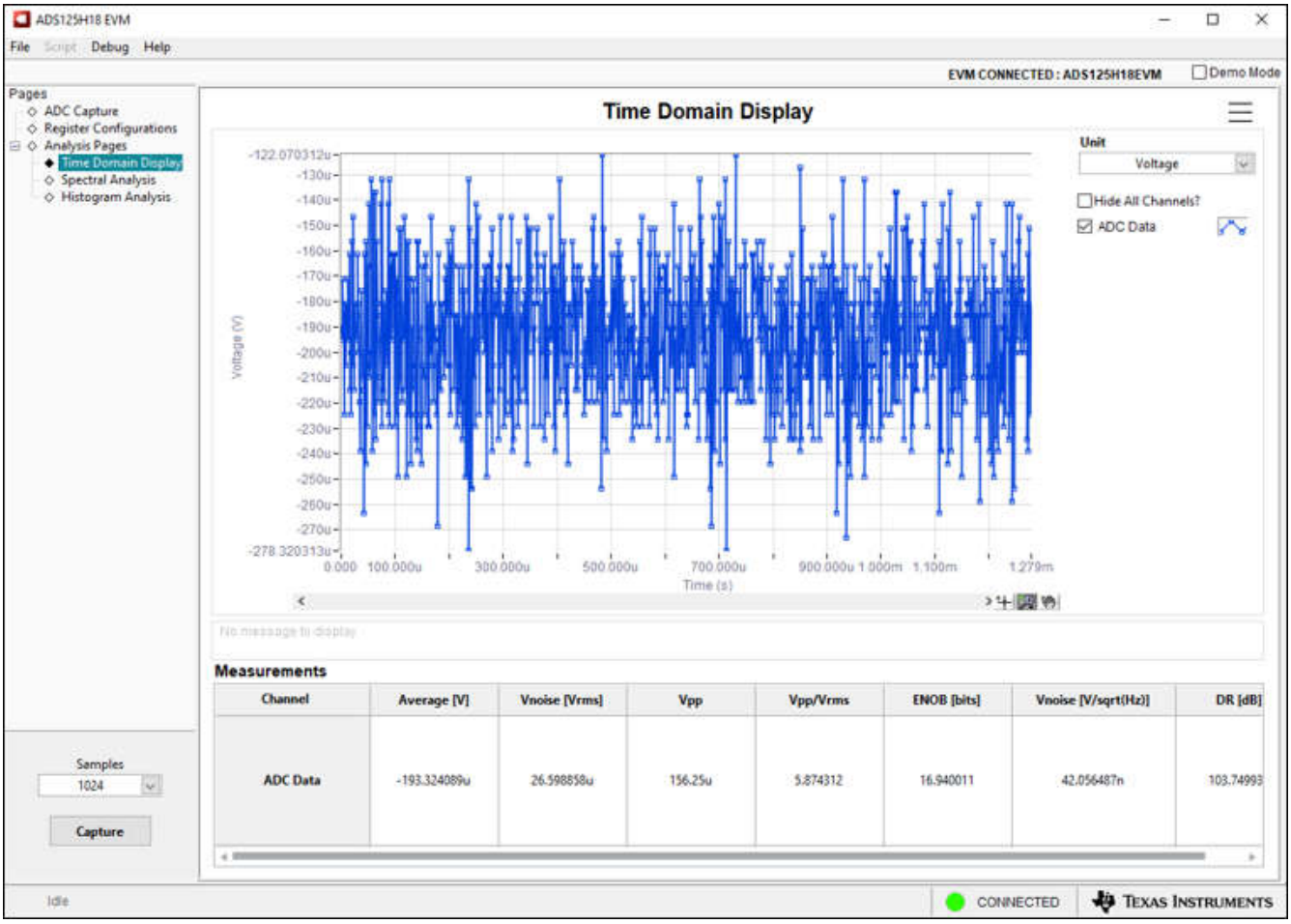


Figure 4-9. ADS125H18 EVM GUI Time-Domain Display Page

4.2.4 Frequency-Domain Display

Figure 4-10 shows the spectral analysis tool that evaluates the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS125H18. This dynamic performance is calculated by single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

Figure 4-10. ADS125H18 EVM GUI Frequency-Domain Display Page

4.2.5 Histogram Display

Noise degrades ADC resolution and the histogram tool shown in Figure 4-11 can be used to estimate effective resolution. Effective resolution is a metric describing the ADC resolution loss resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

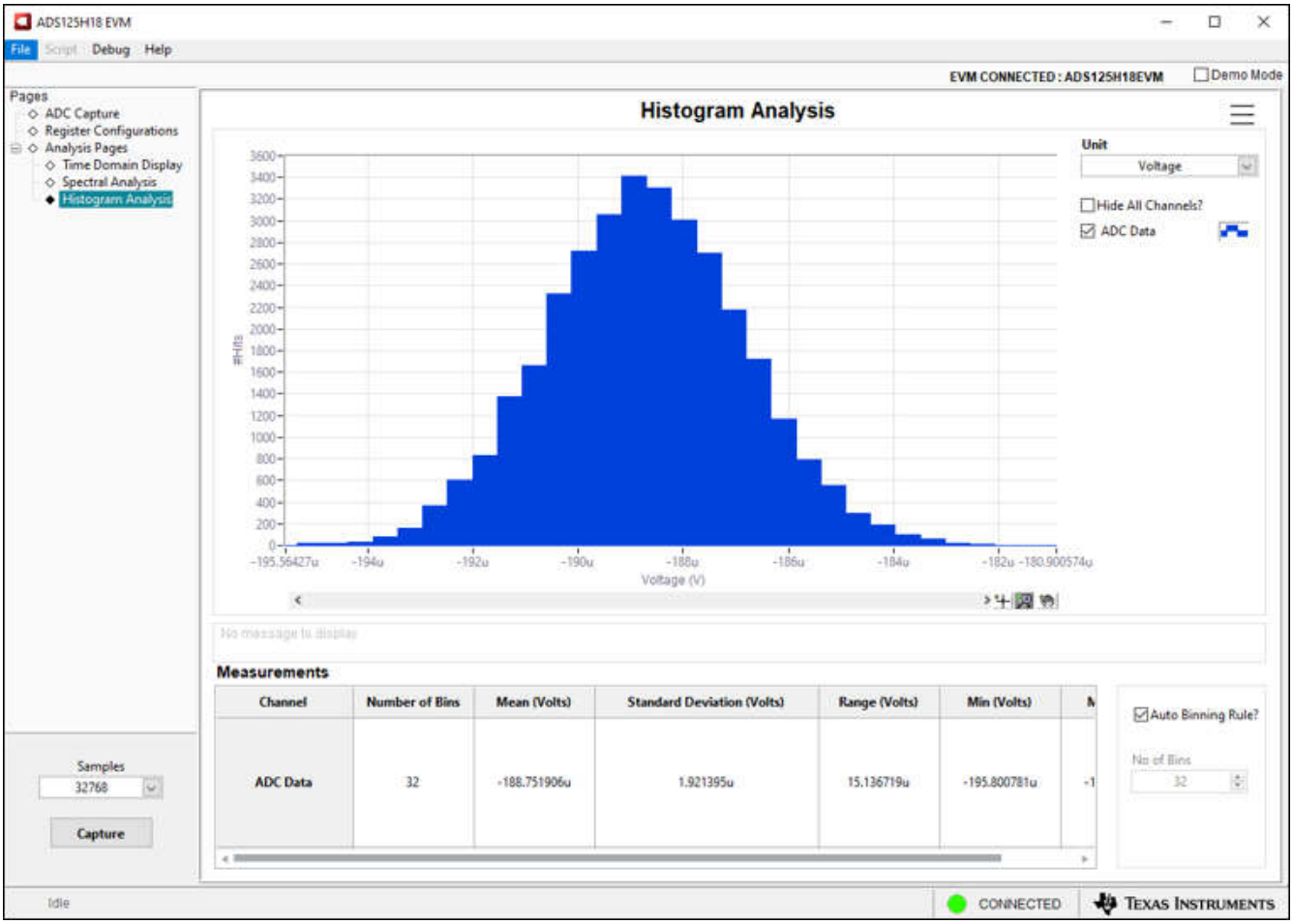


Figure 4-11. ADS125H18 EVM GUI Histogram Display Page

5 Hardware Design Files

This section contains the ADS125H18 EVM schematics, PCB layout, and bill of materials (BOM)

5.1 Schematics

Figure 5-1 to Figure 5-4 show the complete ADS125H18 EVM schematic

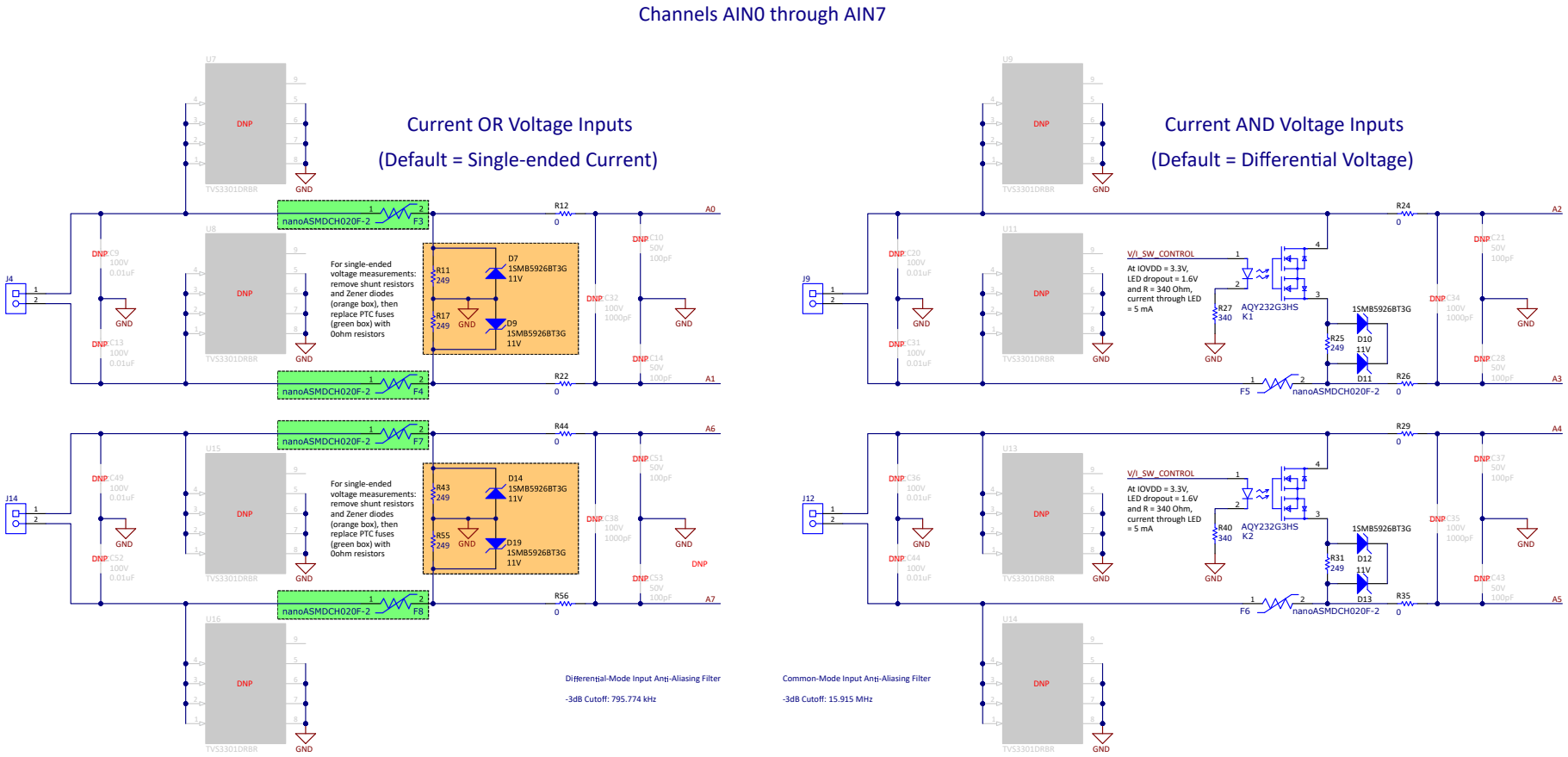


Figure 5-1. EVM Analog Inputs AIN0 to AIN7

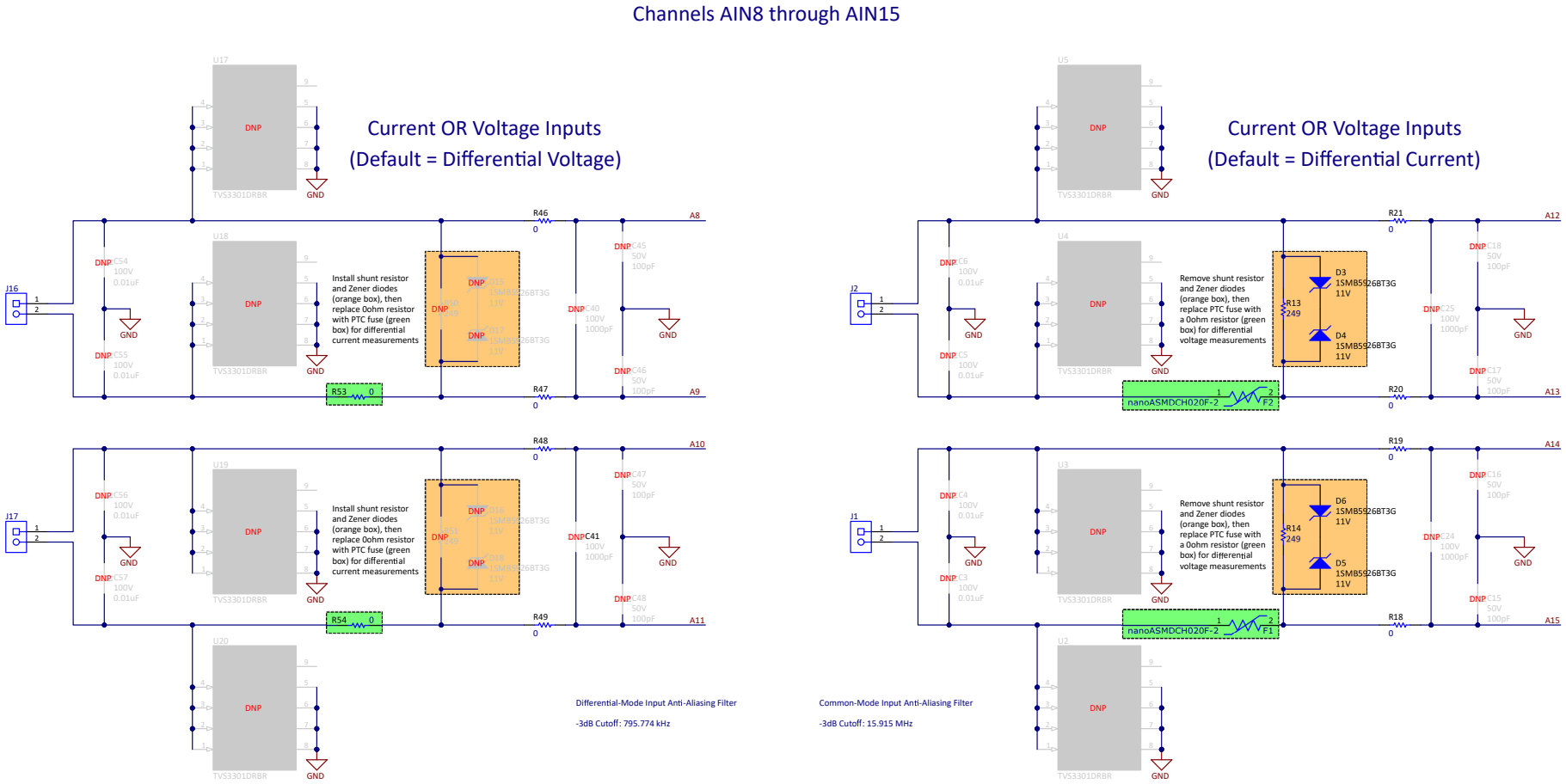


Figure 5-2. EVM Analog Inputs AIN8 to AIN15

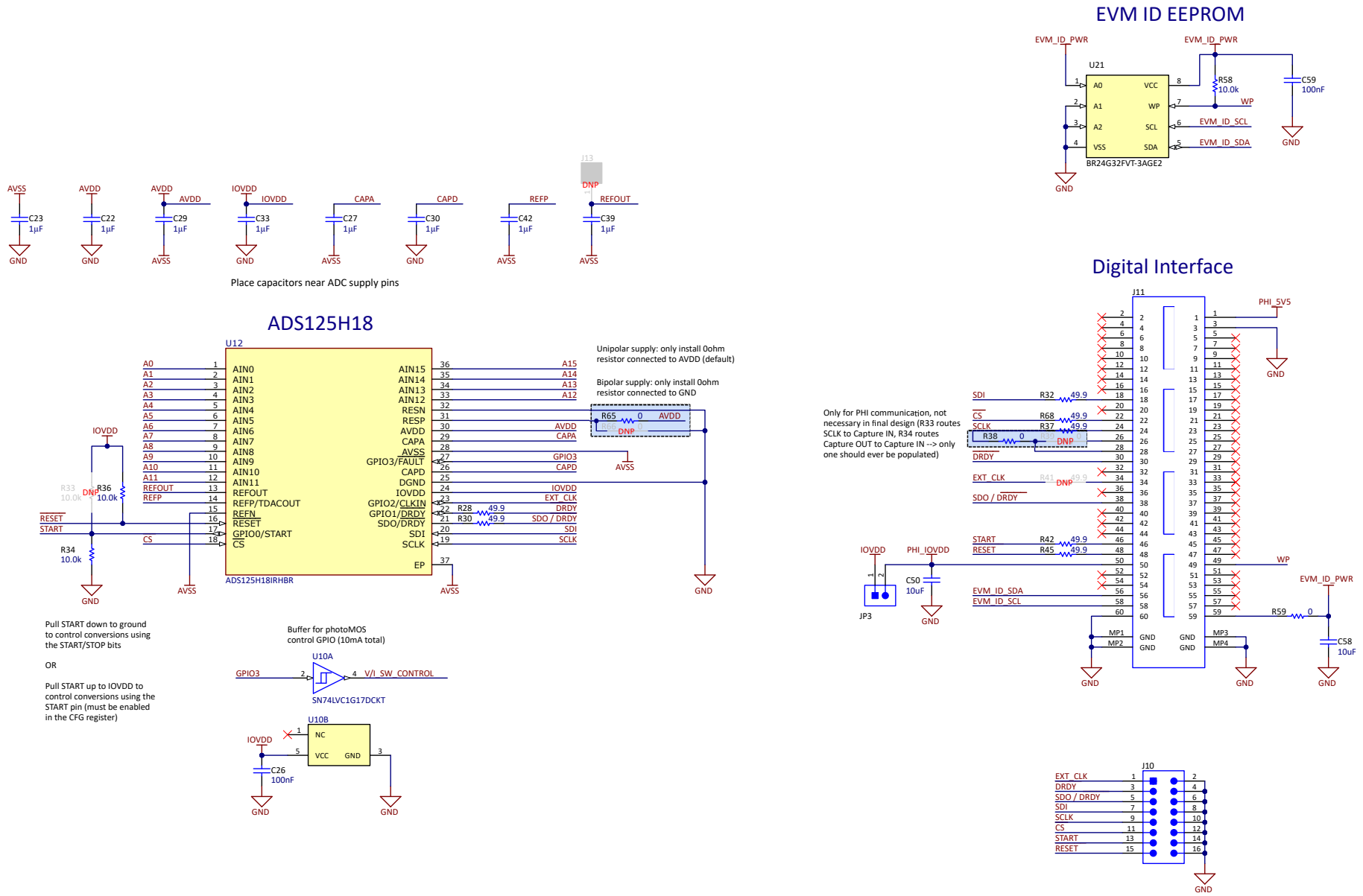


Figure 5-3. EVM ADC and Digital Communication Schematic

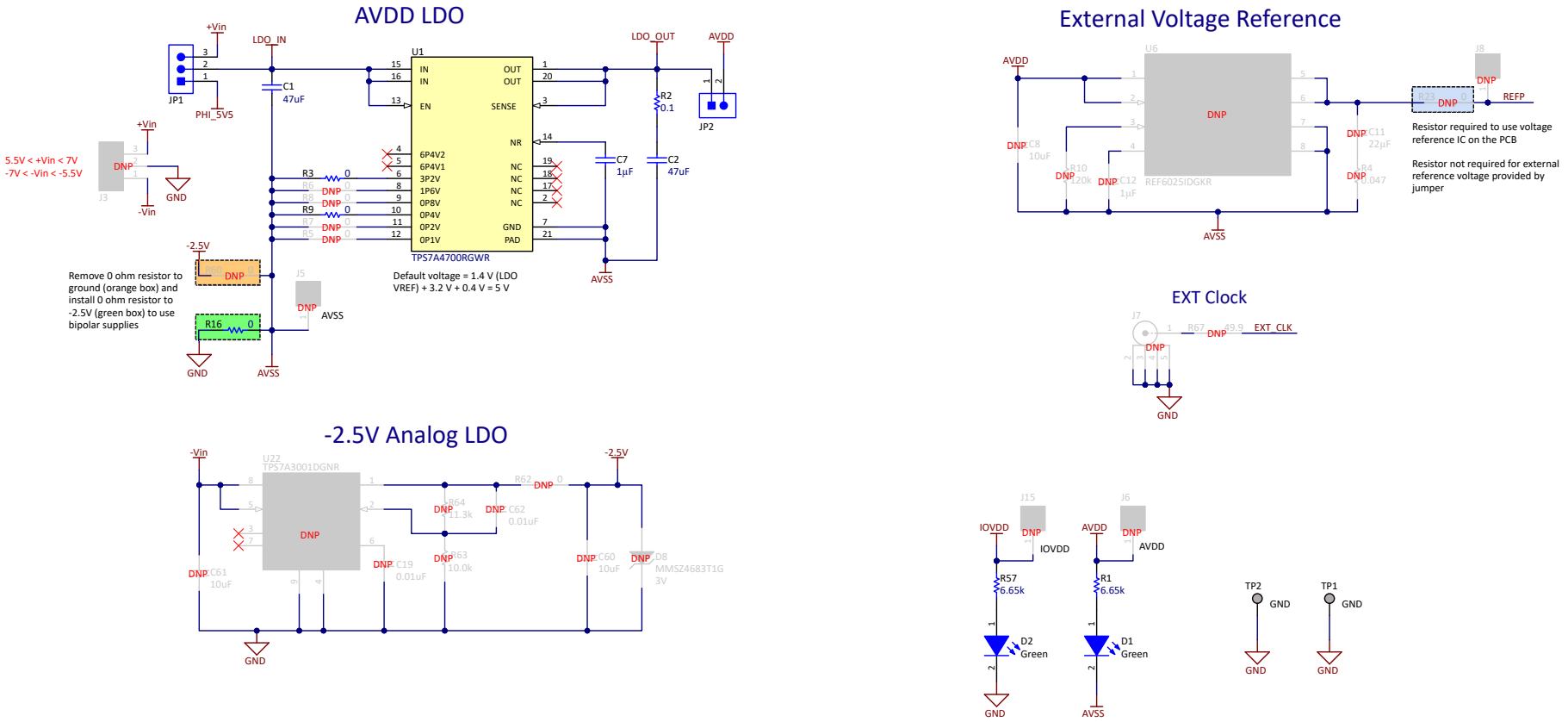


Figure 5-4. EVM Power, Voltage Reference, and External Clock Schematic

5.2 PCB Layouts

Figure 5-5 to Figure 5-8 show the layout drawings for all ADS125H18 EVM PCB layers

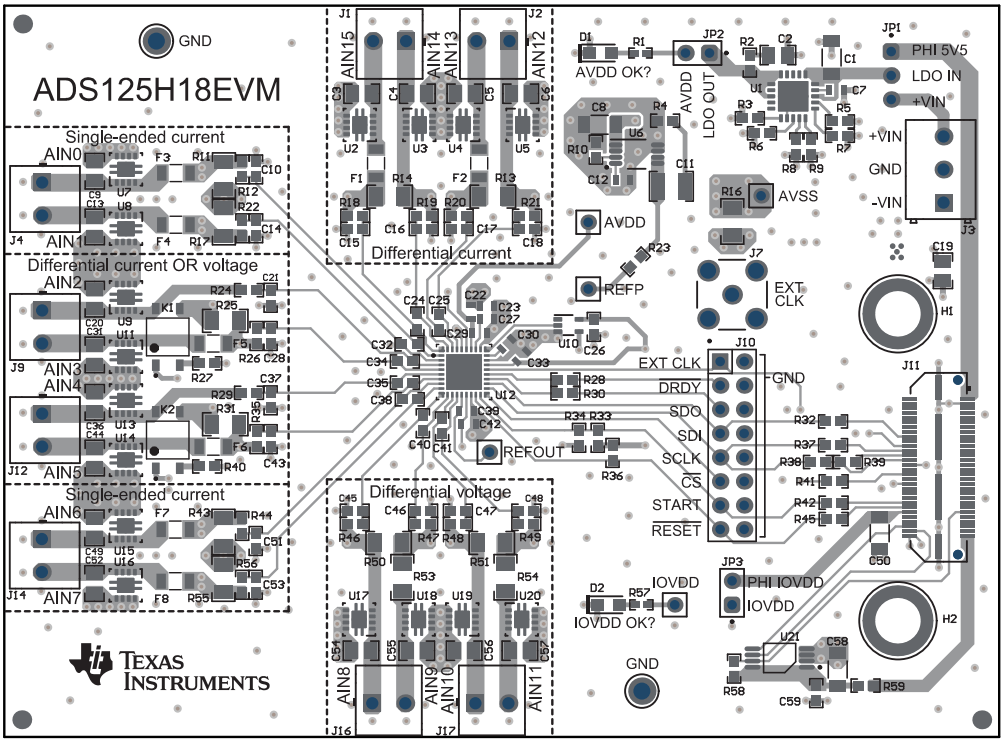


Figure 5-5. ADS125H18 EVM PCB Layout - Top Layer

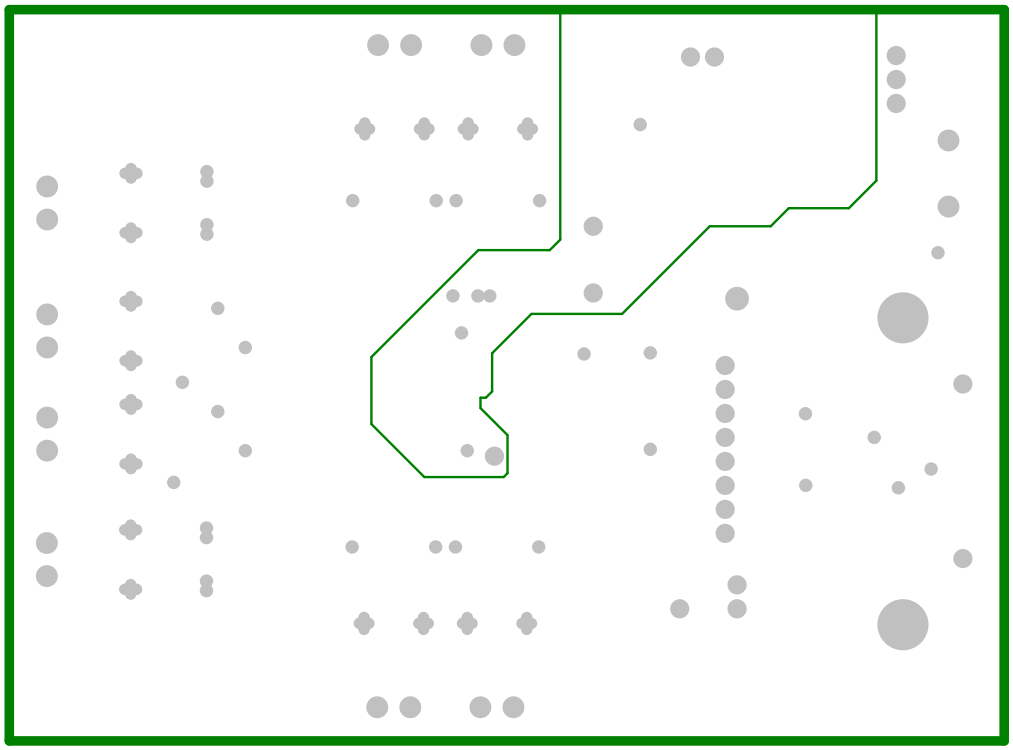


Figure 5-6. ADS125H18 EVM PCB Layout - Ground Layer 1

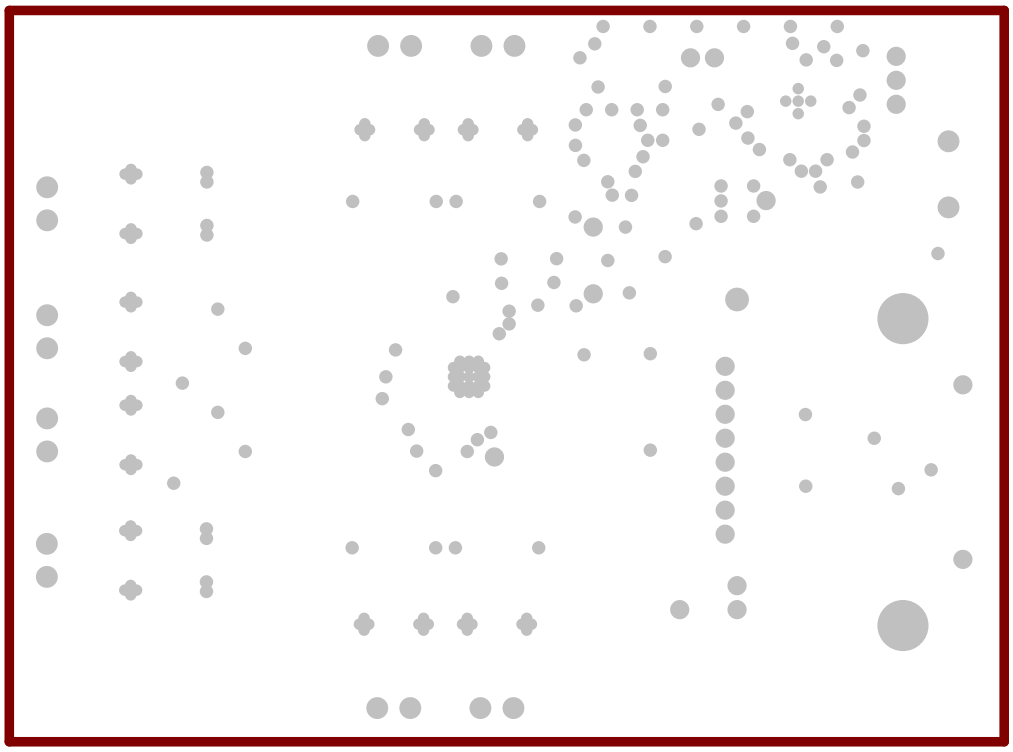


Figure 5-7. ADS125H18 EVM PCB Layout - Ground Layer 2

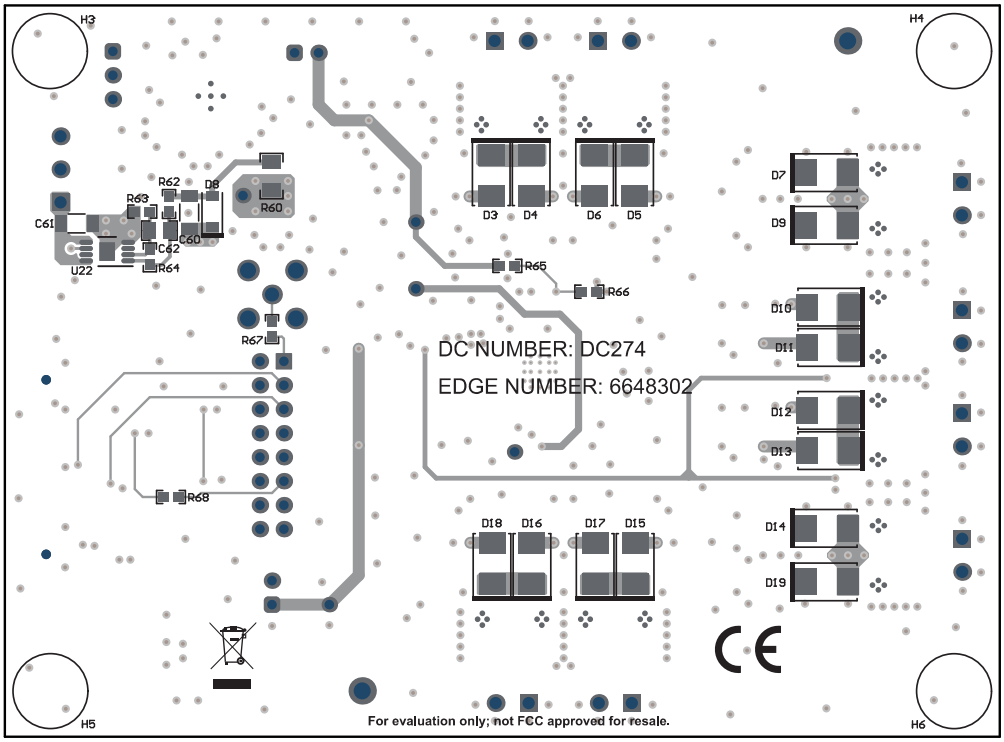


Figure 5-8. ADS125H18 EVM PCB Layout - Bottom Layer

5.3 Bill of Materials (BOM)

Table 5-1 lists the bill of materials (BOM) for the ADS125H18 EVM

Table 5-1. ADS125H18 EVM BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	47uF	CAP, CERM, 47uF, 25V, +/- 20%, X5R, 1206_190	1206_190	C3216X5R1E476M160AC	TDK
C2	1	47uF	CAP, CERM, 47uF, 10V, +/- 20%, X5R, 0805	805	C2012X5R1A476M125AC	TDK
C7, C22, C23, C27, C29, C30, C33, C39, C42	9	1uF	CAP, CERM, 1 µF, 25V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105K080AC	TDK
C10, C14, C15, C16, C17, C18, C21, C28, C37, C43, C45, C46, C47, C48, C51, C53	16	100pF	CAP, CERM, 100pF, 50V, +/- 5%, C0G/NP0, 0603	603	C0603C101J5GAC	Kemet
C24, C25, C34, C35, C40, C41	6	1000pF	CAP, CERM, 1000pF, 100V, +/- 5%, C0G/NP0, 0603	603	GRM1885C2A102JA01D	MuRata
C26, C59	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
C50, C58	2	10uF	CAP, CERM, 10uF, 25V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
D1, D2	2	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D3, D4, D5, D6, D7, D9, D10, D11, D12, D13, D14, D19	12	11V	Diode, Zener, 11V, 550 mW, SMB	SMB	1SMB5926BT3G	ON Semiconductor
F1, F2, F3, F4, F5, F6, F7, F8	8		Polymeric PTC Resettable Fuse 30V 200mA Ih Surface Mount 1206 (3216 Metric), Concave	1206	nanoASMDCH020F-2	Littelfuse
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H3, H4, H5, H6	4		Bumpon, Cylindrical, 0.312X 0.200, Black	Black Bumpon	SJ61A1	3M
H7, H8	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
J1, J2, J4, J9, J12, J14, J16, J17	8		Terminal Block, 3.5mm, 2x1, Tin, TH	Receptacle, 3.5mm, 2x1, TH	6.91214E+11	Wurth Elektronik
J10	1		Header, 100mil, 8x2, Gold, TH	8x2 Header	TSW-108-07G-D	Samtec

Table 5-1. ADS125H18 EVM BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J11	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01L-D-A	Samtec
JP1	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07G-S	Samtec
JP2, JP3	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07G-S	Samtec
K1, K2	2		Relay SSR 1mA 1.75V DC-IN 2A 60V AC/DC-OUT 4-Pin SOP Tube	SOP4	AQY232G3HS	Panasonic
R1, R57	2	6.65k	RES, 6.65k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	402	CRCW04026K65FKED	Vishay-Dale
R2	1	0.1	RES, 0.1, 1%, 0.1W, AEC-Q200 Grade 0, 0603	603	ERJ-3RSFR10V	Panasonic
R3, R9, R38, R59, R65	5	0	RES, 0, 5%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale
R11, R13, R14, R17, R25, R31, R43, R55	8	249	RES, 249, 0.1%, 0.25W, 1206	1206	TNPW1206249RBEEA	Vishay-Dale
R12, R18, R19, R20, R21, R22, R24, R26, R29, R35, R44, R46, R47, R48, R49, R56	16	100	RES, 100, 0.1%, 0.1W, 0603	603	RG1608P-101B-T5	Susumu Co Ltd
R16, R53, R54	3	0	RES, 0, 5%, 0.25W, AEC-Q200 Grade 0, 1206	1206	ERJ-8GEY0R00V	Panasonic
R27, R40	2	340	RES, 340, 0.1%, 0.1W, 0603	603	RT0603BRD07340RL	Yageo America
R28, R30, R32, R37, R42, R45, R68	7	49.9	RES, 49.9, 0.5%, 0.1W, 0603	603	RT0603DRE0749R9L	Yageo America
R34, R36, R58	3	10.0k	RES, 10.0k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0FKEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2	2		Terminal, Turret, TH, Double	Keystone1593-2	1593-2	Keystone
U1	1		36V, 1A, 4.17µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U10	1		Single Schmitt-Trigger Buffer, DCK0005A, SMALL T&R	DCK0005A	SN74LVC1G17DCKT	Texas Instruments
U12	1		ADS125H18IRHBR	VQFN36	ADS125H18IRHBR	Texas Instruments
U21	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm

Table 5-1. ADS125H18 EVM BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C3, C4, C5, C6, C9, C13, C19, C20, C31, C36, C44, C49, C52, C54, C55, C56, C57, C62	0	0.01uF	CAP, CERM, 0.01uF, 100V, +/- 1%, C0G/NP0, 0805	805	C0805C103F1GACTU	Kemet
C8, C60, C61	0	10uF	CAP, CERM, 10uF, 25V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C11	0	22uF	CAP, CERM, 22 µF, 25V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C12	0	1uF	CAP, CERM, 1 µF, 25V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105K080AC	TDK
C32, C38	0	1000pF	CAP, CERM, 1000pF, 100V, +/- 5%, C0G/NP0, 0603	603	GRM1885C2A102JA01D	MuRata
D8	0	3V	Diode, Zener, 3V, 500 mW, SOD-123	SOD-123	MMSZ4683T1G	ON Semiconductor
D15, D16, D17, D18	0	11V	Diode, Zener, 11V, 550 mW, SMB	SMB	1SMB5926BT3G	ON Semiconductor
J3	0		Terminal Block, 3.5mm, 3x1, Tin, TH	Terminal Block, 3.5mm, 3x1, Tin, TH	6.91214E+11	Wurth Elektronik
J5, J6, J8, J13, J15	0		Header, 100mil, 1x1, Gold, TH	Header, 1x1, 2.54mm, TH	HTSW-101-09G-S	Samtec
J7	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
R4	0	0.047	RES, 0.047, 1%, 0.1W, AEC-Q200 Grade 1, 0603	603	ERJ-L03KF47MV	Panasonic
R5, R6, R7, R8, R23, R39, R62, R66	0	0	RES, 0, 5%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale
R10	0	120k	RES, 120k, 0.1%, 0.1W, 0603	603	RG1608P-124B-T5	Susumu Co Ltd
R33, R63	0	10.0k	RES, 10.0k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0FKEA	Vishay-Dale
R41, R67	0	49.9	RES, 49.9, 0.5%, 0.1W, 0603	603	RT0603DRE0749R9L	Yageo America
R50, R51	0	249	RES, 249, 0.1%, 0.25W, 1206	1206	TNPW1206249RBEEA	Vishay-Dale
R60	0	0	RES, 0, 5%, 0.25W, AEC-Q200 Grade 0, 1206	1206	ERJ-8GEY0R00V	Panasonic
R64	0	11.3k	RES, 11.3k, 1%, 0.1W, 0603	603	RC0603FR-0711K3L	Yageo
U2, U3, U4, U5, U7, U8, U9, U11, U13, U14, U15, U16, U17, U18, U19, U20	0		33V Bidirectional Flat-Clamp Surge Protection Device, DRB0008A (VSON-8)	DRB0008A	TVS3301DRBR	Texas Instruments

Table 5-1. ADS125H18 EVM BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U6	0		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6025IDGKR	Texas Instruments
U22	0		Single Output High PSRR LDO, 200mA, Adjustable -1.18 to -33V Output, -3 to -36V Input, with Ultra-Low Noise, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	DGN0008D	TPS7A3001DGNR	Texas Instruments

6 Additional Information

6.1 Trademarks

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STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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