Application Note

Minimum system and test of isolated signal modulator AMC1305M25 and F28377S

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ABSTRACT

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In the field of high electrical isolation motor control, the solution combining SIGMA-DELTA modulators with MCU or FPGA has been increasingly prevalent. Compared to traditional analog isolated op-amp solutions: Higher current sampling accuracy is suitable for servo drives requiring high precision; simpler design eliminates the need for differential-to-single-ended signal conditioning and bias circuits between ADC and MCU; in multi-axis robotic arm applications requiring simultaneous control of 4-8 motors, FPGA can directly implement digital filtering function to obtain sampled signals without additional ADC device. This article introduces the fundamental principles of SIGMA-DELTA modulator scheme and SINC filter. Furthermore, it implements analog signal sampling and computation using TI's latest reinforced isolation SIGMA-DELTA modulator AMC1305M25 in conjunction with F28377S MCU.

Table of Contents

List of Figures

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1 Introduction to sampling solution of the high electrical isolation motor drive current

In high voltage motor drive systems (as shown in Figure 1-1), the closed-loop current control requires phase current information to complete current closed-loop control. Current sampling in practical applications is typically achieved through three methods: Hall sensor; shunt paired with the isolated amplifier; and shunt paired with SIGMA-DELTA modulators. There are advantages and disadvantages to each of the three sampling methods.

Three high-voltage isolated phase current sampling methods are briefly analyzed in Table 1-1. Hall sensor senses the magnetic field generated by the current. This solution features extremely low impedance, minimal losses, and strong immunity to interference, making it common in high power applications (e.g., 380V, 100A and above). Meanwhile, due to limitations in sensor output amplitude and type, signal conditioning is typically required in the post-output stage to meet the input range of the MCU's built-in ADC. The second method to sense current involves connecting shunts in series in the motor drive power stage and sensing the voltage drop across the shunt through an isolated operational amplifier or an isolated SIGMA-DELTA modulator. The primary difference between them is that the isolated operational amplifier output is a voltage signal, typically a differential signal, requiring an additional operational amplifier for amplitude adjustment to meet ADC input range. At this aspect, it is similar to Hall sensor. SIGMA-DELTA modulator outputs a digital bit stream, necessitating digital filtering in the back end. This requires MCU to possess digital filtering capabilities (e.g., TMS320F28x7x series and FPGA). The most prominent feature of this method is the elimination of operational amplifiers and ADC, making it suitable for MCU and FPGA equipped with digital filtering functionality.

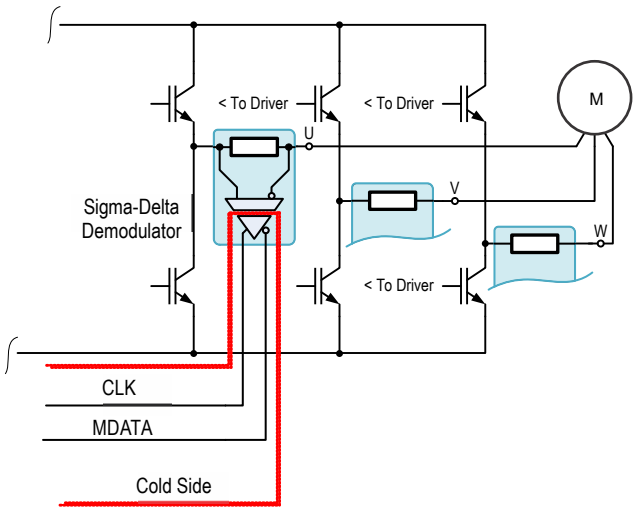

Figure 1-1. Current sampling and drive stage circuit in motor control

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Table 1-1. Comparison of three popular sampling methods for high voltage isolated phase current

Current sampling type	Hall sensor	Isolated operational amplifier	Isolated SIGMA-DELTA modulator
Power supply requirements	Power supply on the low voltage side	Power supply on the high voltage side and the low voltage side	Power supply on the high voltage side and the low voltage side
Sampling needs for the main controller	ADC required	ADC required	SINC filter required
External resistor/shunt	Not required	Required	Required
Isolation ratings	Enable reinforced isolation	Enable reinforced isolation	Enable reinforced isolation
Output mode	Single-ended (current/voltage)/ differential	Differential	Digital
Delay	Small	Medium	Medium/High
On-resistance/shunt range	Magnetic field loss (Microohm)	Milliohm	Milliohm
Application power	Small/Medium/High	Small/Medium	Small/Medium
Solution costs	High	Medium	Low

This article uses SDFM (Sigma-Delta Filter Module) integrated in TMS320F28x7x family, pairing with TI's SIGMA-DELTA modulator AMC1305M25 with the reinforced isolation rating. Additionally, it describes how to build a minimum signal chain to complete the basic testing of AMC1305M25.

1. It describes the basic principles and implementation methods of SINC filter for SIGMA-DELTA modulator.
2. Analog signal sampling is implemented using F28377S control board and AMC1305M25 EVM.

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2 Essence and implementation of SINC filter

SIGMA-DELTA modulator shifts the input noise to the high-frequency domain, and the frequency response of AMC1305M25 is shown in Figure 2-1, with an exponential increase in noise above 10KHz. Therefore, when using SIGMA-DELTA modulator solution, MCU or FPGA must provide a digital low-pass filter to complete the filtering of the bit stream in order to restore the detected active signal. The most common digital low-pass filter is SINC filter, and the multi-order SINC filter is also known as CIC (Cascaded-Integrator-Comb) filter[5] [6]. SINC filter is the most frequently used in practical applications because it achieves effective low-pass filtering in the most "economical" manner while maintaining excellent performance. This section will discuss the essence of the SINC filter and its most simplified implementation.

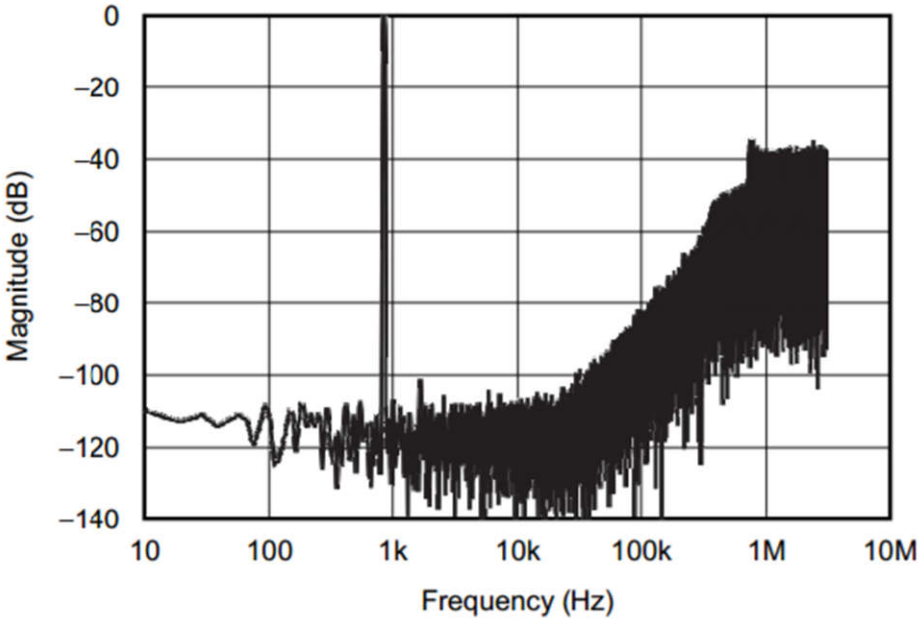

Figure 2-1. 1KHz signal output spectrum and quantization noise of SIGMA-DELTA modulator AMC1305

FIR filter is most commonly used in sampling systems due to its phase linear response. SINC filter expression can be derived by transforming the general-purpose FIR filter[5]. Based on a linear time-invariant system, FIR filter output is:

$$y(n) = \sum_{k=0}^{M-1} h(k)x(n-k)$$

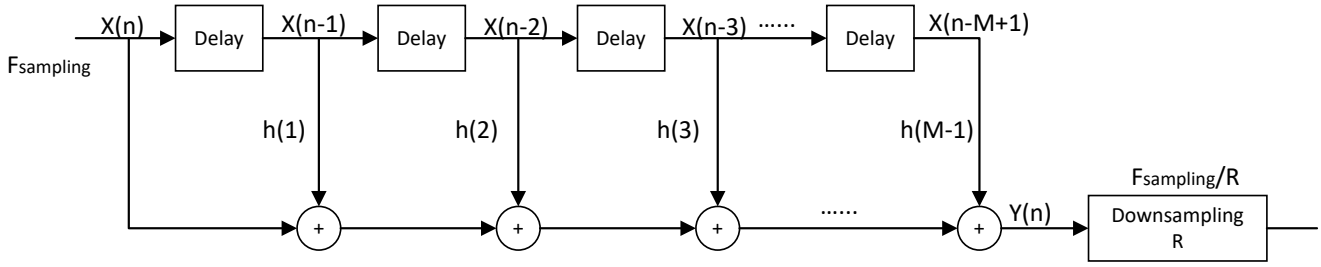

Figure 2-2. FIR filter standard expression

$$y(n) = x(n) + x(n-1)h(1) + x(n-2)h(2) + x(n-3)h(3) + \cdots + x(n-M+1)h(M-1)$$

$$y(n-1) = x(n-1)h(1) + x(n-2)h(2) + x(n-3)(h3) + x(n-4)h(4) + \cdots + x(n-M)h(M))$$

h(n) is Moving Average filter of "1", h(0) = h(1) … = h(m) = 1:

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$$y(n) - y(n-1) = x(n) - x(n-M)$$

$$y(n) = x(n) - x(n-M) + y(n-1)$$

Using the Z transform, a single-cycle delay is equal to Z−1:

$$y(z) = x(z) + x(z)z^{-1} + x(z)z^{-2} + x(z)z^{-3} + \cdots + x(z)z^{-(M-1)}$$

$$y(z)z^{-1} = x(z)z^{-1} + x(z)z^{-2} + x(z)z^{-3} + x(z)z^{-4} + \cdots + x(z)z^{-M}$$

$$y(z) = x(z) - x(z)z^{-M} + y(z)z^{-1}$$

$$y(z) = \frac{x(z) - x(z)z^{-M}}{1 - z^{-1}}$$

$$H(z) = \frac{1 - z^{-M}}{1 - z^{-1}} \quad (1)$$

From the most basic FIR filter, the Z-change expression shown in (1) can be derived, which is the recursive expression of the moving average filter in Figure 2-3.Figure 2-2 comparing with Figure 2-3 reveals that recursive expressions significantly reduce computing resources, requiring only one subtractor, one adder, and M+1 cache on hardware.

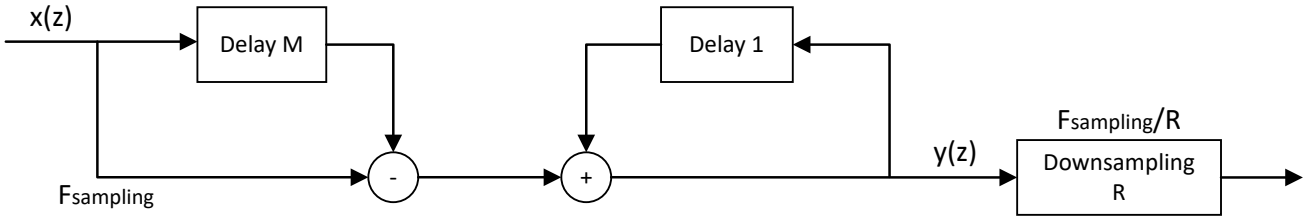

Figure 2-3. Iterative expression of FIR moving average filter-SINC first-order filter

Calculating the frequency response requires using = :

$$H\left(e^{jw}\right) = e^{\frac{-jw(M-1)}{2}} \frac{\sin\left(\frac{wM}{2}\right)}{\sin\left(\frac{M}{2}\right)}$$

$$\left|H\left(e^{jw}\right)\right| = \frac{\left|\sin\left(\frac{wM}{2}\right)\right|}{\left|\sin\left(\frac{w}{2}\right)\right|} \quad (2)$$

(2) is approximated to SINC function (SINx/x), so it is also referred to as a SINC filter. Rearranging (1) yields formula (3) and Figure 2-4:

$$y(z) = \frac{x(z) - x(z)z^{-M}}{1 - z^{-1}}$$

$$W(z) = \frac{x(z)}{1 - z^{-1}}$$

$$y(z) = W(z) - W(z)z^{-M} \quad (3)$$

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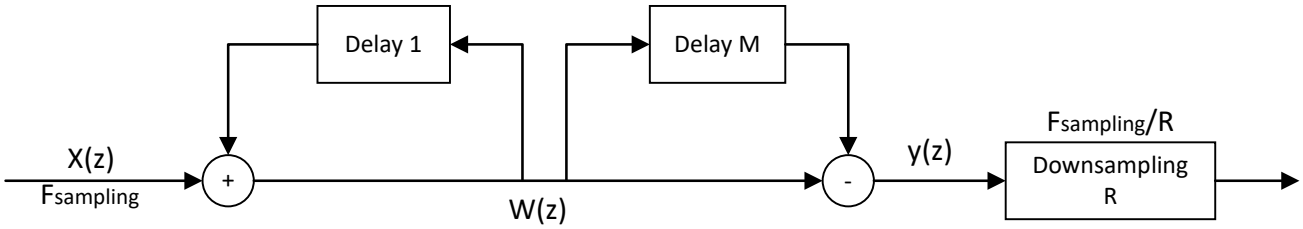

Figure 2-4. The first-order filter of SINC filter after rearranging

The number of delay period M is combined with the down sampling rate R in formula (3). Delay W(n) sampling points by M periods, subtracting them is equivalent to sampling the signal every R period, then applying M/R delay. The output OUT yields the same result. Finally, you can get what is shown in Figure 2-5. If R=M, that constitutes the final SINC filter form. The output is a signal down sampled by a factor of M, where M also represents the number of pulses in the filter.

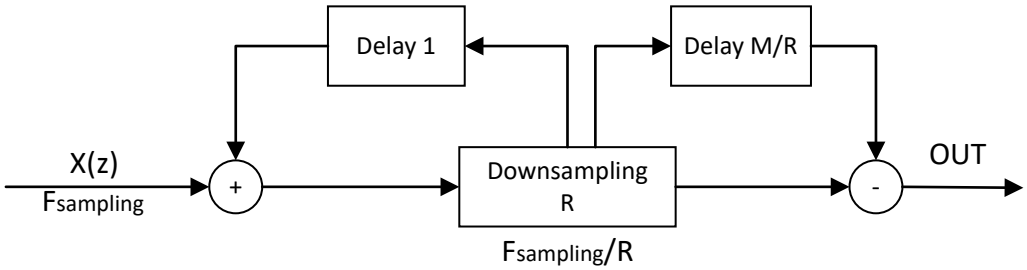

Figure 2-5. Hardware-optimized expression for SINC first-order filter combining down sampling and delay buffering

(1) expression is recursive representation of FIR filter that is a first-order SINC filter. Therefore, Z expression for SINC3 filter, which is a third-order filter SINC, is shown as:

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{3} \tag{4}$$

For a SINC filter, the most important design parameters are the sampling rate f_{data}, SINC filter order O (The first-order, second-order and third-order correspond to 1, 2 and 3 respectively) and delay M. Typically, for hardware optimization, M equals the down sampling rate R.

From above, the main design parameters can be derived as:

R: Oversampling ratio/down sampling ratio; f_{data} data clock frequency (sampling frequency); O: SINC filter order

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{O} \tag{5}$$

Sampling frequency of output signal:

$$f_{sampling} = \frac{f_{data}}{R} \tag{6}$$

SINC filter step response sampling delay is shown as:

$$Td = \frac{R \times O}{f_{data}} \tag{7}$$

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3 Configuration and calculation of SIGMA-DELTA filter module based on integration of AMC1305M25 and F28377S

SINC filter is flexible to configure and the output result is closely related to the oversampling rate and SINC filter order. This chapter describes how to complete the voltage sampling function using the F28377SSDFM module and the AMC1305M25. The input analog signal amplitude for AMC1305M25 is acquired by reading F28377S SDFM register.

3.1 Hardware configuration

Evaluation board:

1. AMC1305M25 evaluation module: SBAU237
2. TMS320F28377S LaunchPad: http://www.ti.com/tool/LAUNCHXL-F28377S

AMC1305M25 works in conjunction with F28377S. The following hardware configuration must be completed at the interface, as shown in Figure 3-1 the simplified diagram:

1. AMC1305M25 digital-side DVDD uses an external 5V. The evaluation board provides an isolated power supply design, and AVDD power supply at the analog detection side is provided by the built-in isolated power supply on the evaluation board[1].
2. AMC1305M25 requires one data clock, f_{data}, with a frequency range of 5MHz-20.1MHz (CLK_IN). This clock can be generated by using F28337D EPWM module. GPIO4/PWM3A is selected for this test according to TMS320F28377S specification[7] Table4-1.
3. According to[7], F28377S SDFM requires data clock SDx_Cx and data stream SDx_Dx for data sampling. Since F28377S captures data on the rising or falling edge of the clock, it is possible to ensure that DOUT and CLK_RETURN are close to the AMC1305M25 chip pins so that the data and clock delays returning to the host controller are the same. At this time, GPIO16 and GPIO17 of F28377S are used as modulator data and clock inputs.
4. AMC1305M25 data output DOUT links SDx_Dx pins of the SDFM module, providing the data source.

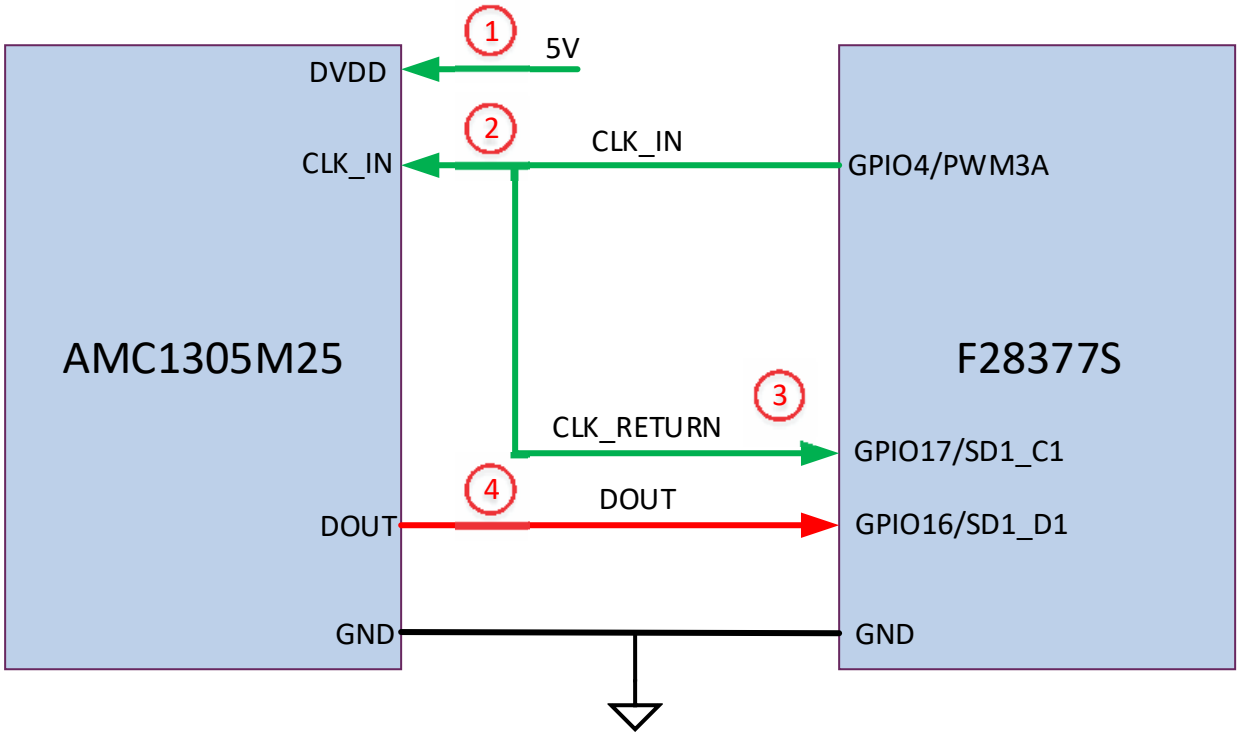

Figure 3-1. AMC1305EVM connects with the F28377S control board hardware

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3.2 F28377S software configuration

TI provides SDFM module development sample code in F2837 family in the ControSUITE software development package. Please refer to the ControlSUITE installation path:

C:\ti\controlSUITE\device_support\F2837xD\v210\F2837xD_examples_Cpu1\sdfm_pwm_sync_cpu\cpu01sdfm_pwm_sync_cpu_cpu01.c

The default sample code does not work and requires EPWM module configuration and SDFM module configuration before minimal system of AMC1305M25 and F28377S can work.

The configuration steps are shown as follows:

1. F28377S can use EPWM module to generate the clock signal required by AMC1305M25. In this example, the clock configuration is shown in Figure 3-2. In this way, EPWMCLK in EPWM3A (GPIO4) module, is divided down to 100MHz, and the counting mode UP_DOWN is used. The final GPIO4 output clock is 10MHz.

```
#ifdef CPU1
    GPIO_SetupPinOptions(4, GPIO_OUTPUT, GPIO_ASYNC);
    GPIO_SetupPinMux(4,GPIO_MUX_CPU1,1);
#endif

    EALLOW;

    //
    // Allows all users to globally synchronize all enabled ePWM modules to
    // the time-base clock (TBCLK)
    //
    CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    //
    // Setup TBCLK
    //
    (*EPWM[gPWM_number]).TBFHS.bit.TBPHS = 0x0000;    // Phase is 0
    (*EPWM[gPWM_number]).TBCTR = 0x0000;              // Clear counter
    (*EPWM[gPWM_number]).TBFRD = 5;                   // Set timer period PLLSYSCLK = 200MHz, EPWMCLK = 100MHz

    //
    // Setup counter mode
    //
    (*EPWM[gPWM_number]).TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up Use up count mode
    (*EPWM[gPWM_number]).TBCTL.bit.HSPCLKDIV = TB_DIV1; // TBCLK = EPWMCLK/(HSPCLKDIV*CLKDIV)
    (*EPWM[gPWM_number]).TBCTL.bit.CLKDIV = TB_DIV1; // HSPCLKDIV = 1, CLKDIV = 1;
    //
    // Set Actions
    //
    (*EPWM[gPWM_number]).AQCTLA.bit.PRD = SET;      // Set PWM1A on event A, TBPRD = 5, PWMA = 1;
    (*EPWM[gPWM_number]).AQCTLA.bit.ZRO = CLEAR;     // count TBPRD = 0, PWMA = 0;
```

Figure 3-2. Using GPIO4 - Configuring clock frequency to 10MHz

2. Configure SIGMA-DELTA filter

   The sdfm_configureData_filter() function is available in F28377S library to directly configure SDFM filter type, oversampling ratio and output data bit length. In the next input short-circuit noise test, the main modified filter type is SINC1, SINC2 and SINC3; the oversampling ratio is OSR=64, OSR=128 and OSR=256.

```
Sdfm_configureData_filter(gPeripheralNumber, FILTER1, FILTER_ENABLE, SINC2, OSR_64, DATA_32_BIT, SHIFT_0_BITS);
```

The software configuration is complete and the minimal system functionality of AMC1305M25 and F28377S needs to be verified. Short the input terminal J2 of AMC1305M25 evaluation module to power GND as shown in Figure 3-3.

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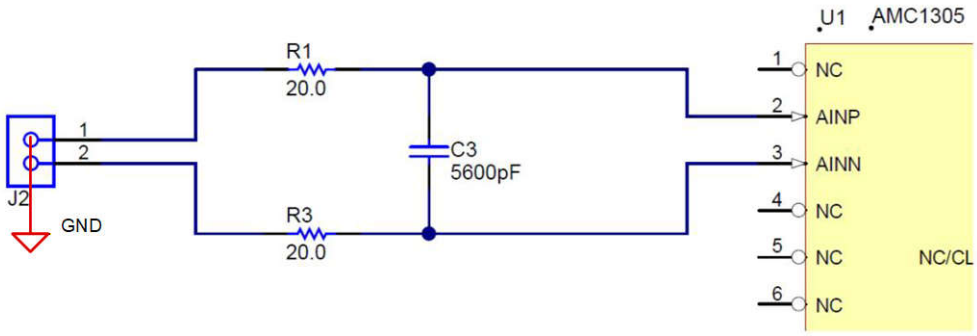

Figure 3-3. Short circuit in analog front ends 1&2 based on AMC1305M25 EVM

Observe CLK_IN and DOUT pins with an oscilloscope probe. At this point, CLK_IN data clock frequency should be 10MHz. DOUT outputs digital signals “1” and “0” since the input differential signal is 0V, as shown in Figure 3-4. DOUT output may encounter a situation where two consecutive clock data are both “1”. In this case, the data for the next two clock cycles will be “0”, and the output clock will maintain a 50% duty cycle state. This waveform indicates that the minimal system hardware is properly connected and that AMC1305M25 is correctly getting 0V input data.

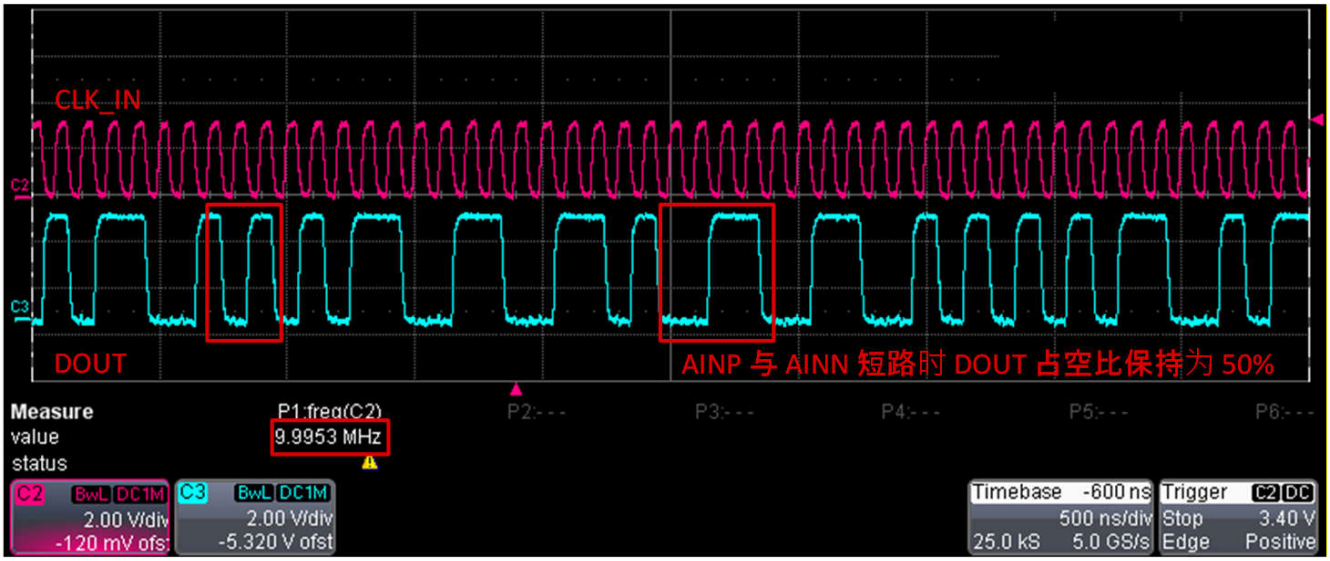

Figure 3-4. CLK_IN pin channel 1 (red) clock signal; DOUT channel 2 (blue) data signal

3.3 AMC1305M25 sense voltage versus F28377S digital expression

According to the specification, AMC1305M25 has an input range of ±312.5mV. When the input reaches 312.5mV, the output is nearly 100% “1” bit stream; when the input is -312.5mV, the output is nearly 100% “0” bit stream. Additionally, according to F28377S specification, SDFM module supports two data formats: The first is a 32-bit binary signed-complement code and the second is a signed 16-bit binary signed-complement code. In SINC3 filter mode, the final data needs to be shifted if 16 bits are used to represent the data due to the data bits being too wide. Incorrect shifts and conversions can result in a mismatch between the final digital result and the analog input amplitude. In this chapter, SINC3 filter is used as an example to calculate the input voltage from a 32-bit data format and a 16-bit data format, respectively.

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DOSR	Sinc1	Sinc2	Sinc3	Sincfast
x	x	x^2	x^3	$2x^2$
4	–4 to 4	–16 to 16	–64 to 64	–32 to 32
8	–8 to 8	–64 to 64	–512 to 512	–128 to 128
16	–16 to 16	–256 to 256	–4096 to 4096	–512 to 512
32	–32 to 32	–1024 to 1024	–32,768 to 32,768	–2048 to 2048
64	–64 to 64	–4096 to 4096	–262,144 to 262,144	–8192 to 8192
128	–128 to 128	–16,384 to 16,384	–2,097,152 to 2,097,152	–32,768 to 32,768
256	–256 to 256	–65,536 to 65,536	–16,777,216 to 16,777,215	–131,072 to 131,072

Figure 3-5. SDFM output range for different combinations of filter order and oversampling rate corresponds to formula (8)

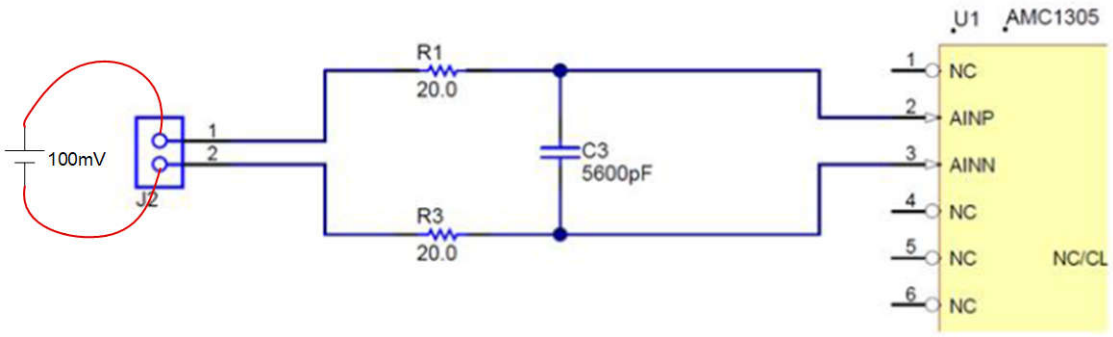

Figure 3-6. AMC1305 sampling front end connects to 100mV voltage

To verify the input analog magnitude versus digital magnitude, a 100mV voltage source is connected at the input of the AMC1305M25 for reference. The actual input voltage magnitude is measured to be 100.12mV using a six-digit half-voltmeter.

Use 32 BIT binary signed-complement code (SDDPARMx.DR = 1):

In the sample code, SDFM filter output value can be obtained by reading the SDFM1_READ_FILTER1_DATA_32BIT register. When calculating the input voltage, first convert the data obtained by the register from the binary complement code to decimal, and then use the formulas (8) and Figure 3-5 to obtain corresponding analog input amplitude of AMC1305M25. The results calculated using formula (8) at different oversampling rates are compared in Table 3-1. The input amplitude is 100mV ±2% in all cases, consistent with the voltmeter test results.

R/OSR: oversampling ratio; $OUT_{Decimal}$: Decimal expression of filtered data, binary signed bit complement code, MSB is a sign bit; O: SINC filter order; $V_{Clipping}$: Maximum analog front-end dynamic range

It can be known from AMC1305M25 specifications that $V_{Clipping}$ = 312.5mV;

$$V_{in} = V_{Clipping} \times \frac{OUT_{Decimal}}{R^O} \quad (8)$$

The following data is obtained by averaging 1024 samples of the digital signal using SINC3 filters with different oversampling rates:

Table 3-1. Test results for a 32-bit SINC3 filter with a 100mV input voltage under different oversampling configurations

Filter Type	Convert binary complement code to decimal		Vin calculation
SINC3 R/OSR64	84024	262144	100.16mV
SINC3 R/OSR100	319780	1000000	99.77mV
SINC3 R/OSR128	673092	2097152	100.14mV

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Table 3-1. Test results for a 32-bit SINC3 filter with a 100mV input voltage under different oversampling configurations (continued)

Filter Type	Convert binary complement code to decimal		Vin calculation
SINC3 R/OSR256	5361067	16777215	99.86mV

Use 16 BIT binary signed-complement code (SDDPARMx.DR = 0):

When 16 BIT data is used, the filter output data is stored in register SDFM1_READ_FILTER1_DATA_16BIT. Due to data overflow, F28377S automatically performs a right shift on the filtered results. Figure 3-7 gives the corresponding number of shifts for different SINC filters and oversampling rates.

OSR	SINC1	SINC2	SINCFAST	SINC3
1 to 31	0	0	0	0
32 to 40	0	0	0	1
41 to 50	0	0	0	2
51 to 63	0	0	0	3
64 to 80	0	0	0	4
81 to 101	0	0	0	5
102 to 127	0	0	0	6
128 to 161	0	0	1	7
162 to 181	0	0	1	8
182 to 203	0	1	2	8
204 to 255	0	1	2	9
256	0	2	3	9

Figure 3-7. Number of shifts when SINC filter supports 16BIT output at different oversampling rates

Combining Figure 3-7 and the formula (8) yields the formula (9), which corresponds the filter output result to the input analog magnitude using the 16 BIT signed-bit configuration.Table 3-2 shows the correspondence between the digital output of F28377S and the analog input amplitude during actual test, with an input of 100mV.

S: The number of register shifts corresponding to different OSRs in Figure 3-8

$$V_{in} = V_{Clipping} \times \frac{OUT_{Decimal}}{R^{O}} \tag{9}$$

Table 3-2. Test results for a 16-bit SINC3 filter with a 100mV input voltage under different oversampling configurations

Filter setting	Convert binary complement code to decimal	2		Vin calculation
SINC3 R/OSR 64	5244	16	262144	100.02mV
SINC3 R/OSR 100	10003	32	1000000	100.03mV
SINC3 R/OSR 128	5244	128	2097152	100.02mV
SINC3 R/OSR 256	10495	512	1677216	100.09mV

3.4 AMC1305M25 and F28377S zero drift and noise measurements

Based on the Figure 3-3 hardware circuits, the direct measurement of zero drift and noise in the input of AMC1305M25 and F28377S system can be performed. In this test, the output noise peak-to-peak is evaluated in comparison to different filter types and oversampling ratio multiples. In this test, SDFM output data uses a 32-bit signed-bit binary output and formula (8) for equivalent noise calculations. For complete data, please refer to Figure 5-1, Figure 5-2 and Figure 5-3. Table 4 Zero drift and noise results and equivalent Noise-Free Bit with different filter types and oversampling rate configurations and Figure 3-8 are summarized with the above data.

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			中低精度1%~0.1%			高精度0.1%			
Filter Mode	SINC1 OSR64	SINC1 OSR128	SINC1 OSR256	SINC2 OSR64	SINC2 OSR128	SINC2 OSR256	SINC3 OSR64	SINC3 OSR128	SINC3 OSR256
Pk-Pk Codes(LSB)	4	4	4	8	8	14	122	528	2278
Pk-Pk Noise(mV)	19.53	9.77	4.88	0.61	0.15	0.07	0.15	0.08	0.04
Noise Free-Bit(Bits)	5.00	6.00	7.00	10.00	12.00	13.19	12.07	12.96	13.85

Table 4 Zero drift and noise results and equivalent Noise-Free Bit with different filter types and oversampling rate configurations

It can be seen from the test results that higher SINC filter orders or higher oversampling rates yield data with higher resolution and lower noise. Correspondingly, according to formula (7), the system delay increases accordingly. When accurate current and voltage sampling is required, such as 0.1% resolution and precision, at least SINC2 type filter must be selected with an oversampling rate of at least 64. SINC1 or SINC2 filter is a better choice in scenarios that require a fast response and relatively low-precision, such as 1% resolution and precision.

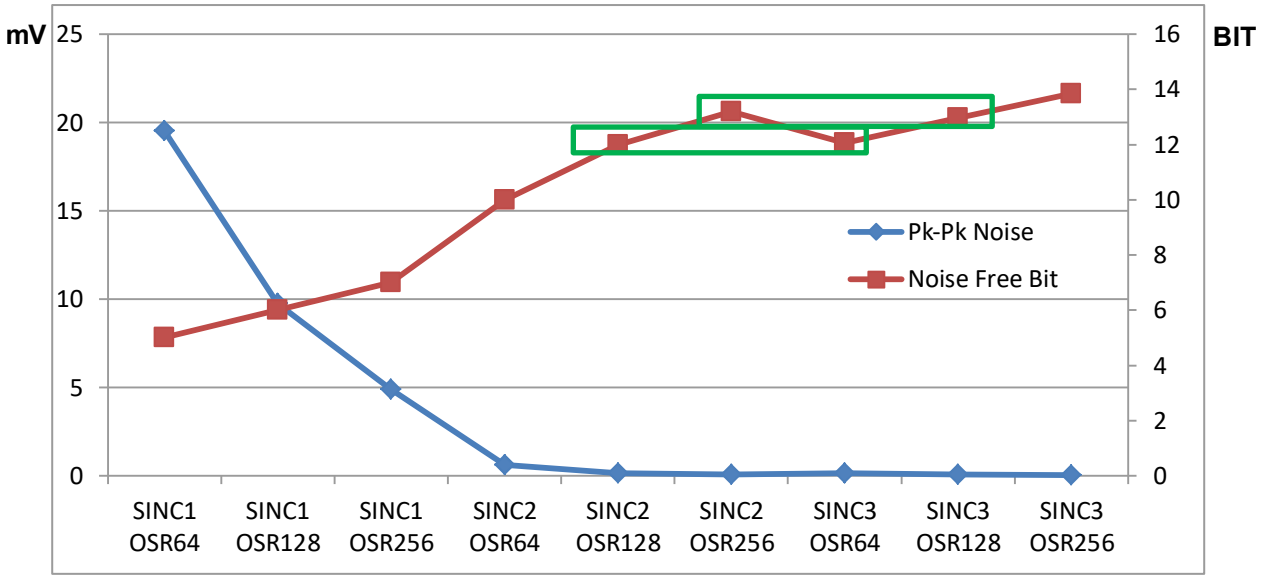

Figure 3-8. Filter mode and sample rate setting vs. zero drift and noise

In addition, the combination of different SINC filter orders and oversampling rates yields similar zero drift and noise. Using higher-order filters at this stage results in shorter data latency while maintaining the same resolution and precision. For example, SINC2 OSR128 has a noise level comparable to that of the SINC3 OSR64, but it incurs an additional 64 clock cycles of latency.

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5 Appendix:

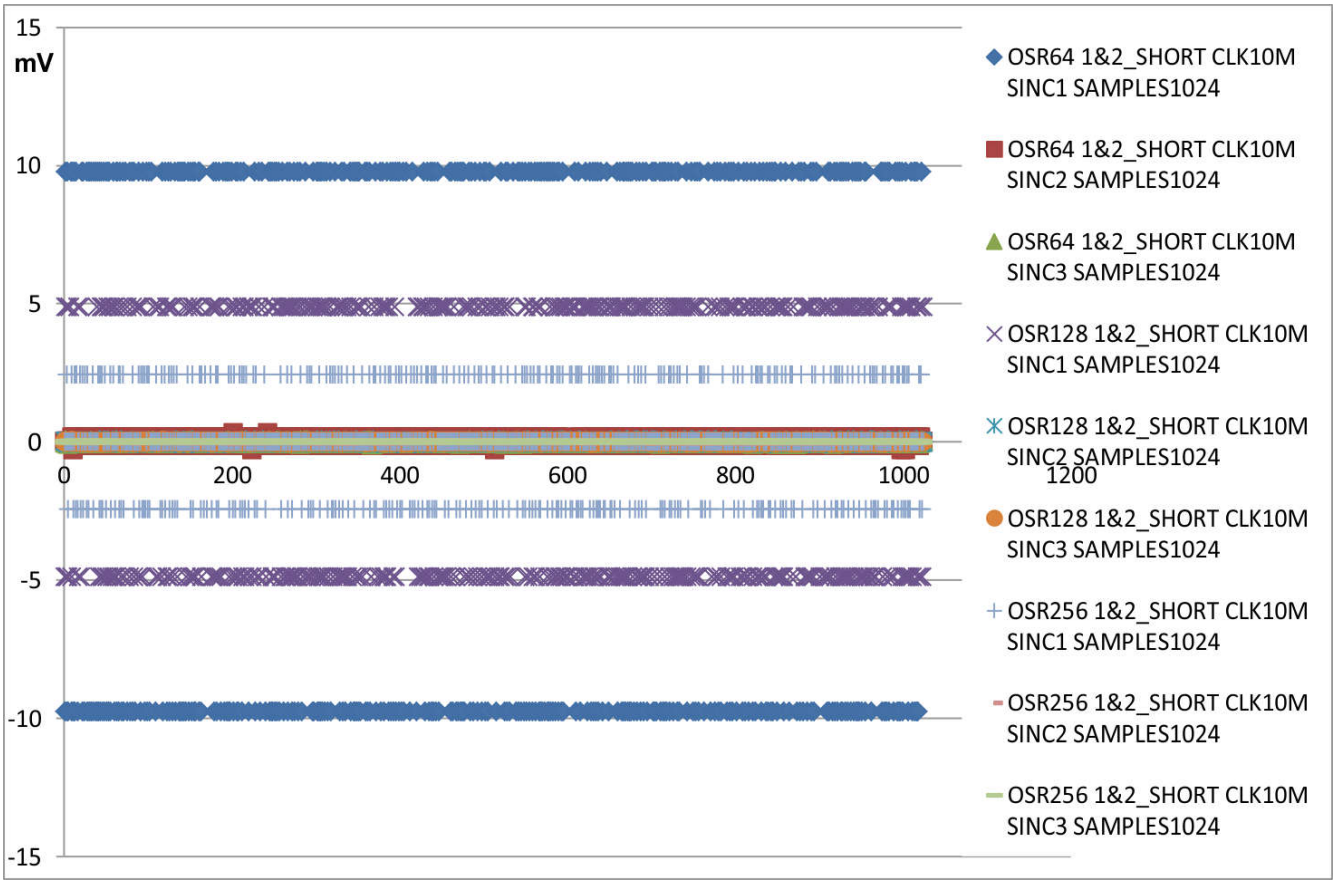

Figure 5-1. Based on SINC1/2/3 OSR64/128/256 input short-circuit noise and zero drift test

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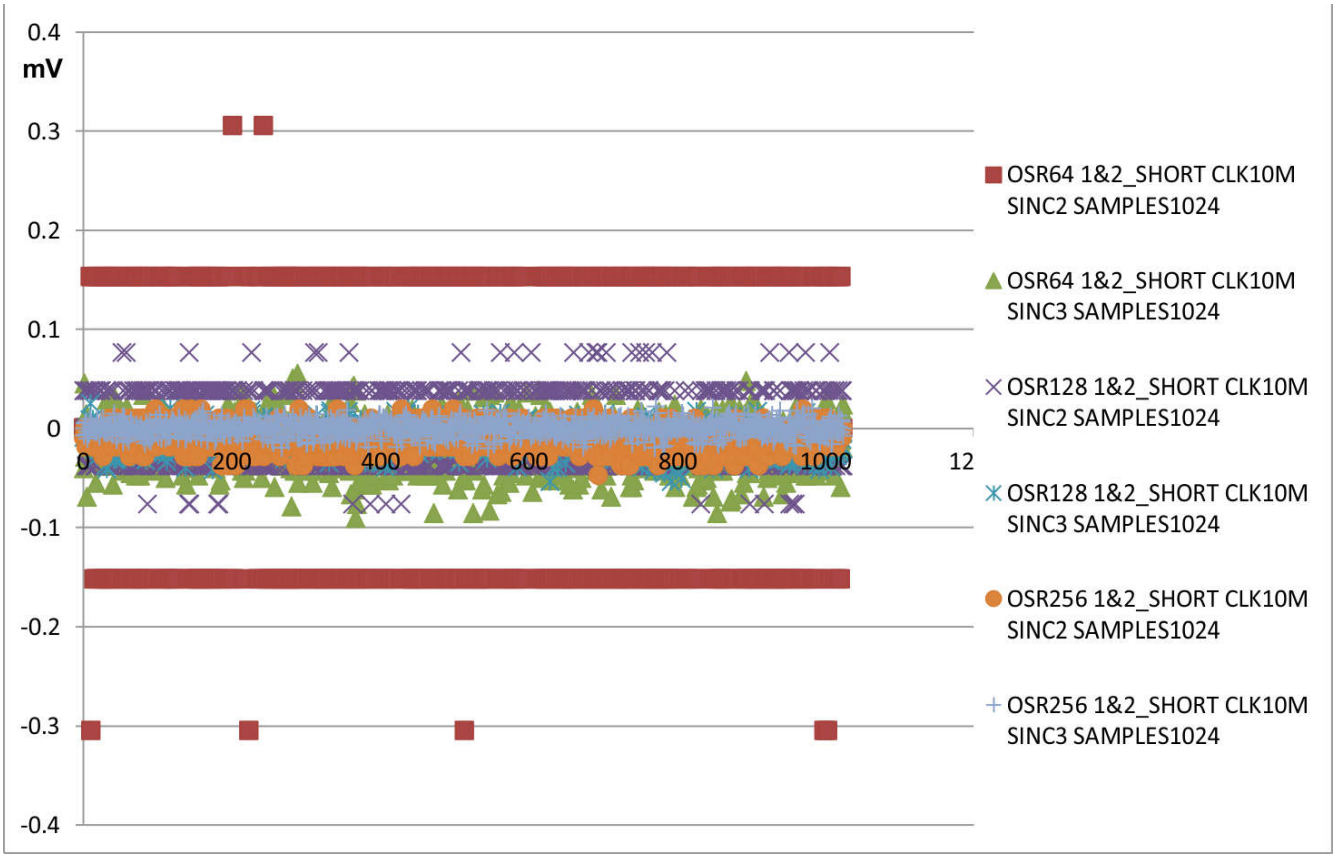

Figure 5-2. Based on SINC2/3 OSR64/128/256 input short-circuit noise and zero drift test

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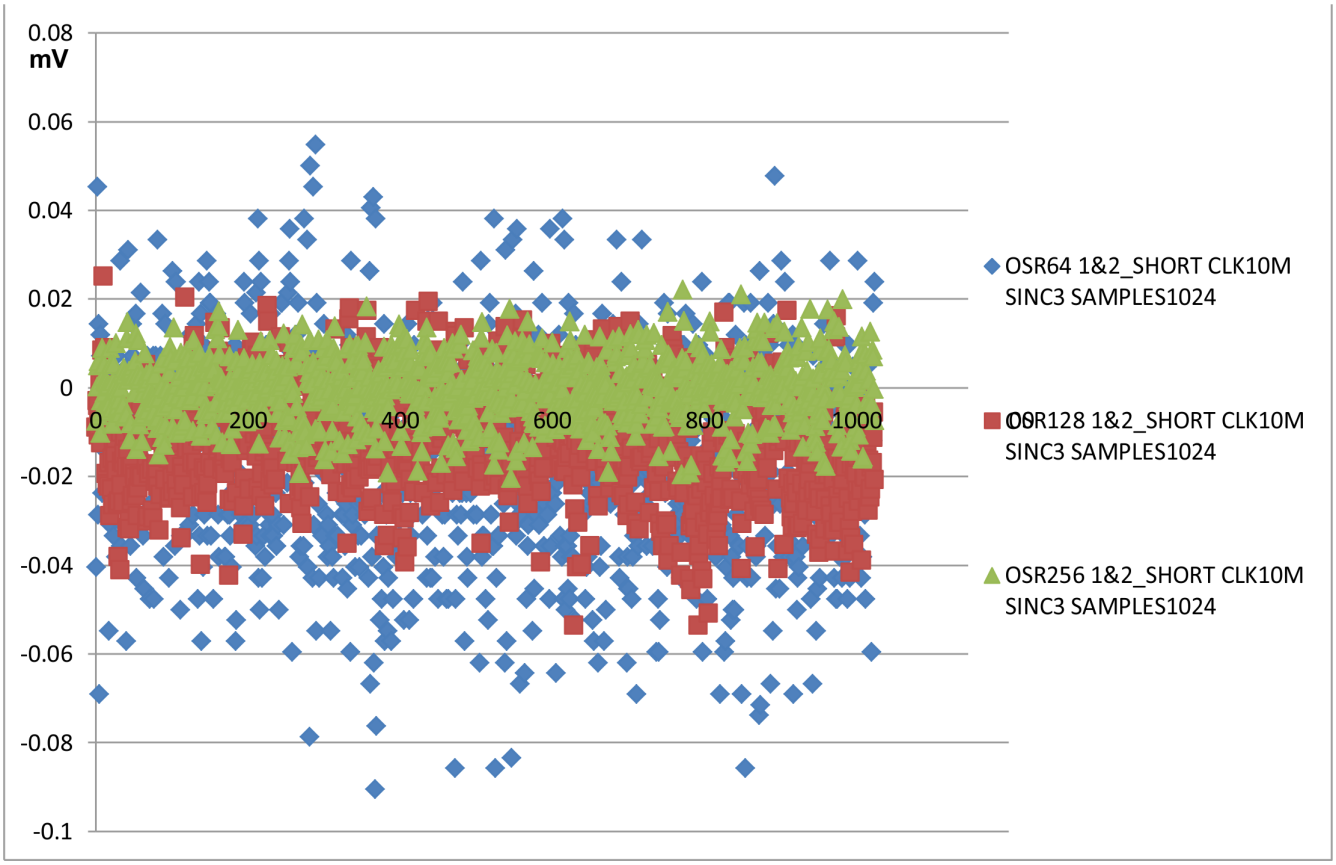

Figure 5-3. Based on SINC3 OSR64/128/256 input short-circuit noise and zero drift test

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