Application Brief

Biasing an APD With OPA596

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Introduction

An Avalanche Photodiode (APD) is an optical detector that converts photons (light) to current. APDs are frequently used in high-speed optical detection circuits because of fast response times and ability to offer increased gain versus a conventional photodiode. One challenge with APDs is the requirement for high-voltage bias circuits, some requiring voltages up to 150V. For many solutions, a conventional switching converter (for example, a boost converter) can provide this high voltage directly to the APD. For some systems, however, the biasing needs to be dynamic, where the bias rail may change either for calibration purposes or to change the gain of the circuit. For these cases, a high-voltage amplifier in addition to the switching converter can create a high-voltage, high-accuracy solution ideal for dynamic photodiode adjustments. The OPA596 is a great choice for dynamic APD biasing up to 80V because of the low quiescent current (420µA) and fast slew rate (100V/µs). This application brief gives two circuit examples using OPA596 for precision control with a DAC, and a fast transition example with a basic resistor-divider scheme along with a MOSFET switch.

Using a DAC With OPA596 for High-Capacitive Drive

To dynamically control the APD bias with precision, a DAC can be used to create a low-voltage bias, which then is gained up to provide the high-voltage necessary to bias node. A basic example of how this can be configured is shown in Figure 1. In this example, the output of the DAC63204W is connected to OPA596, with the OPA596 configured as an inverting amplifier with a gain of –15. Since the DAC63204W is a voltage-mode DAC, this outputs a voltage with 12 bits of accuracy from 0 to 4.8V (using the internal reference, with GAIN = 4). The DAC signal is then gained by OPA596 to –15×DAC output voltage. Since APD biasing also requires a decoupling capacitor to minimize bias transient excursions, the OPA596 is configured in a high-capacitive drive Dual-feedback circuit (for information on how to design a dual-feedback circuit, see *Three Ways to Stabalize Op Amp Capacitive Loads* and *TI Precision Labs*).

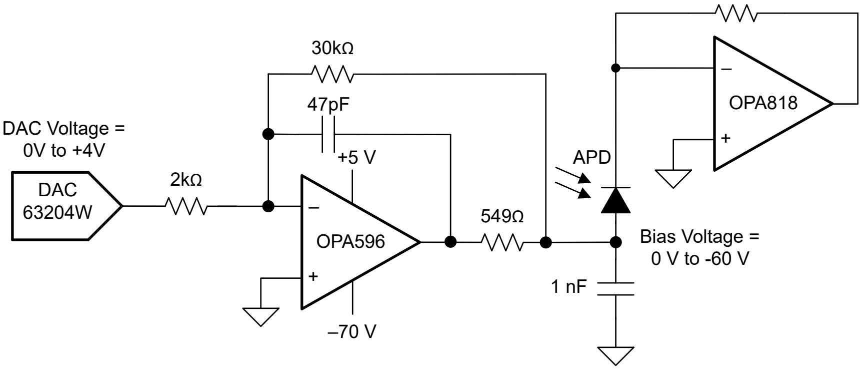


Figure 1. APD Bias Control Using OPA596 for a High-Voltage Gain Stage (Circuit 1)

Fast Dual-Level Switching With OPA596 and Resistor and MOSFET Control

While the DAC circuit is implemented because of a low-voltage control signal, the use of an inverting configuration in a gain of –15 on the OPA596 limits the bandwidth of the system. In an inverting gain of –15, the *noise gain* of the circuit is 16 (see *Operational Amplifier Stability Theory and Compensation*), which means the closed loop bandwidth is divided by a factor of 16 from the gain-bandwidth product of the amplifier. In this case, the rise/fall times of the output of the amplifier is limited to approximately 0.35 divided by the closed loop bandwidth (see *Op Amp Slew Rate Precision Labs Video*). If faster switching is required, then the amplifier needs to be configured in a lower gain.

Figure 2 shows a circuit that can be used to switch between two different bias voltage levels with the amplifier configured in unity gain. The resistors are used to set the two different levels, with the modulation of the reference voltage implemented with a small-signal PMOS device such as BSS84. In this configuration, the voltage provided by the resistor divider circuit can transition quickly due to minimal capacitive loading. Since the OPA596 is configured in a unity-gain dual feedback circuit, the amplifier can still provide fast transient responses, using the fast slew rate of the OPA596 to transition to each voltage level.

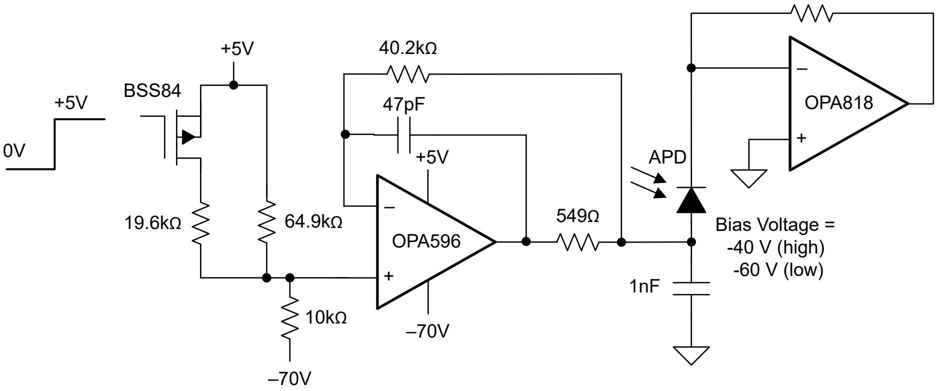


Figure 2. APD Bias Dual-Level Switching (Circuit 2)

A simulation of each circuit shows 5.3µs 0.1% settling on the faster circuit from a –60V to –40V transient, versus 13.4µs on the circuit in Figure 1.

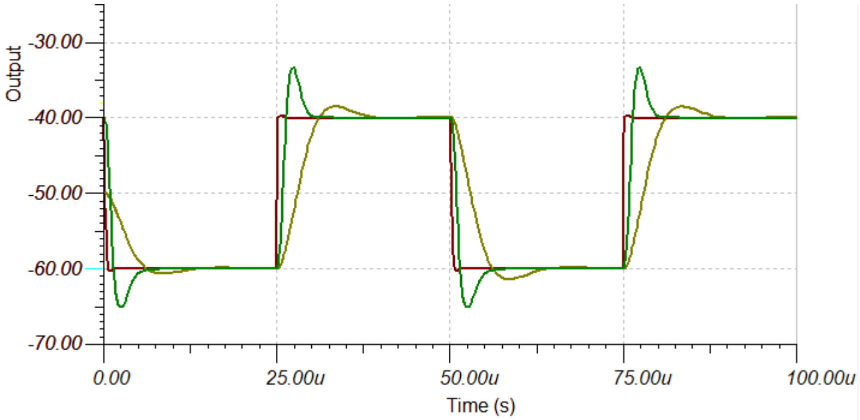


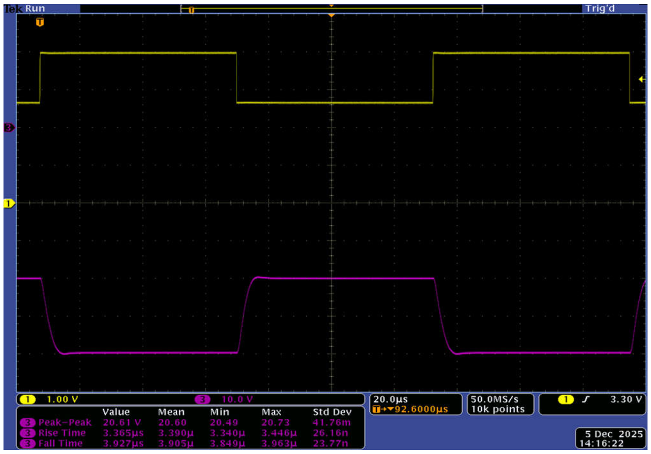
Figure 3. Simulation Results APD Bias Voltage in TINA

Yellow: OPA596 output (Circuit 1)

Red: Non-inverting input (Circuit 2)

Green: OPA596 output (Circuit 2)

Results of both circuits were also measured on the bench, see Figure 4 and Figure 5.



	Value	Mean	Min	Max	Std Dev
3 Peak−Peak	20.61 V	20.60	20.49	20.73	41.76m
3 Rise Time	3.365µs	3.390µ	3.340µ	3.446µ	26.16n
3 Fall Time	3.927µs	3.905µ	3.849µ	3.963µ	23.77n

Figure 4. Measured Results: Circuit 1

Yellow: Simulated DAC output voltage generated with waveform generator

Purple: OPA596 Output Voltage

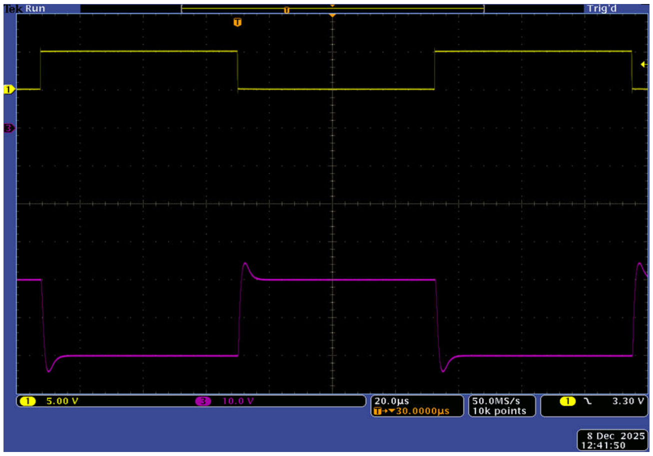


Figure 5. Measured Results: Circuit 2

Yellow: Gate Voltage at BSS84

Purple: OPA596 Output Voltage

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