

## TPS720 350 mA, Ultra-Low $V_{IN}$ , RF Low-Dropout Linear Regulator With Bias Pin

### 1 Features

- 350-mA High-Performance LDO
- Low Quiescent Current: 38  $\mu$ A
- Excellent Load Transient Response:  
 $\pm 15$  mV for  $I_{LOAD} = 0$  mA to 350 mA in 1  $\mu$ s
- Excellent Line Transient Response:  
 $\Delta V_{OUT} = \pm 2$  mV for  $\Delta V_{BIAS} = \pm 600$  mV in 1  $\mu$ s  
 $\Delta V_{OUT} = \pm 200$   $\mu$ V for  $\Delta V_{IN} = \pm 400$  mV in 1  $\mu$ s
- Low Noise: 48  $\mu$ V<sub>RMS</sub> (10 Hz to 100 kHz)
- 80 dB  $V_{IN}$  PSRR (10 Hz to 10 kHz)
- 70 dB  $V_{BIAS}$  PSRR (10 Hz to 10 kHz)
- Fast Start-Up Time: 140  $\mu$ s
- Built-In Soft-Start With Monotonic  $V_{OUT}$  Rise and Start-Up Current Limited to 100 mA +  $I_{LOAD}$
- Overcurrent and Thermal Protection
- Low Dropout: 110 mV at  $I_{LOAD} = 350$  mA
- Stable with 2.2- $\mu$ F Output Capacitor
- Available in 1.33 mm  $\times$  0.96 mm DSBGA-5 and 2 mm  $\times$  2 mm SON-6 Packages

### 2 Applications

- Digital Cameras
- Cellular Camera Phones
- Wireless LAN
- Handheld Products

### 3 Description

The TPS720 family of dual rail, low-dropout linear regulators (LDOs) offers outstanding ac performance (PSRR, load and line transient response), while consuming a very low quiescent current of 38  $\mu$ A.

The  $V_{BIAS}$  rail that powers the control circuit of the LDO draws very low current (on the order of the quiescent current of the LDO) and can be connected to any power supply that is equal to or greater than 1.4 V above the output voltage. The main power path is through  $V_{IN}$ , which can be a lower voltage than  $V_{BIAS}$ ; it can be as low as  $V_{OUT} + V_{DO}$ , increasing the efficiency of the solution in many power-sensitive applications. For example,  $V_{IN}$  can be an output of a high-efficiency, DC-DC step-down regulator.

The TPS720 supports a novel feature in which the output of the LDO regulates under light loads when the IN pin is left floating. The light-load drive current is sourced from  $V_{BIAS}$  under this condition. This feature is particularly useful in power-saving applications where the DC-DC converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load.

The TPS720 is stable with ceramic capacitors and uses an advanced BICMOS fabrication process that yields a dropout of 110 mV at a 350-mA output load. The TPS720 has the unique feature of providing a monotonic  $V_{OUT}$  rise (overshoot limited to 3%) with  $V_{IN}$  inrush current limited to 100 mA +  $I_{LOAD}$  with an output capacitor of 2.2  $\mu$ F.

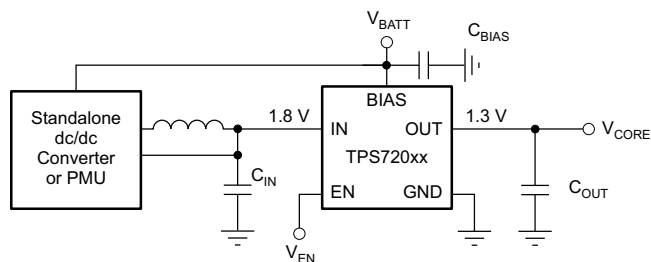
The TPS720 uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over load, line, process, and temperature extremes. An ultra-small DSBGA package makes the TPS720 ideal for handheld applications. The TPS720 is also available in a SON-8 package. This family of devices is fully specified over the temperature range of  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ .

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)          |
|-------------|-----------|--------------------------|
| TPS720      | DSBGA (5) | 1.36 mm $\times$ 0.96 mm |
|             | SON (6)   | 2.00 mm $\times$ 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



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## 4 Revision History

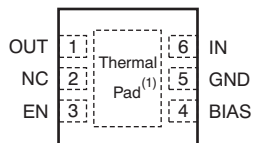
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (August 2009) to Revision E   | Page |
|---|------|
| <ul style="list-style-type: none"> <li>• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul> | 1    |

| Changes from Revision C (September, 2008) to Revision D  | Page   |
|--|--------|
| <ul style="list-style-type: none"> <li>• Added electrical specifications for DRV package .....</li> <li>• Noted electrical specifications for YZU package .....</li> </ul> | 5<br>5 |

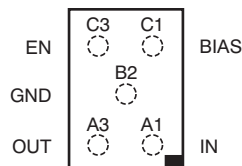
## 5 Pin Configuration and Functions

**DRV Package**  
6-Pin SON With Exposed Thermal Pad  
Top View



- (1) TI recommends connecting the SON (DRV) package thermal pad to ground.

**YZU Package**  
5-Pin DSBGA  
Top View



### Pin Functions

| PIN  |     |     | I/O | DESCRIPTION  |
|------|-----|-----|-----|--|
| NAME | DRV | YZU |     |  |
| OUT  | 1   | A3  | O   | Output pin. A 2.2- $\mu$ F ceramic capacitor is connected from this pin to ground, for stability and to provide load transients. See <a href="#">Input and Output Capacitor Requirements</a> .           |
| NC   | 2   | —   | —   | No connection.   |
| EN   | 3   | C3  | I   | Enable pin. A logic high signal on this pin turns the device on and regulates the voltage from IN to OUT. A logic low on this pin turns off the device.  |
| BIAS | 4   | C1  | I   | Bias supply pin. TI recommends bypassing this input with a ceramic capacitor to ground for better transient performance. See <a href="#">Input and Output Capacitor Requirements</a> .                   |
| GND  | 5   | B2  | —   | Ground pin.  |
| IN   | 6   | A1  | I   | Input pin. This pin can be a maximum of 4.5 V; $V_{IN}$ must not exceed $V_{BIAS}$ . Bypass this input with a ceramic capacitor to ground. See <a href="#">Input and Output Capacitor Requirements</a> . |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

At  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted). All voltages are with respect to GND. <sup>(1)</sup>

|                      |                                    | MIN                                     | MAX                            | UNIT               |
|----------------------|------------------------------------|---|--------------------------------|--------------------|
| $V_{IN}^{(2)}$       | Input voltage (steady-state)       | -0.3                                    | $V_{BIAS}$ or 5 <sup>(3)</sup> | V                  |
| $V_{IN\_PEAK}^{(4)}$ | Peak transient input               |   | 5.5                            | V                  |
| $V_{BIAS}$           | Bias voltage                       | -0.3                                    | 6                              | V                  |
| $V_{EN}$             | Enable voltage                     | -0.3                                    | 6                              | V                  |
| $V_{OUT}$            | Output voltage                     | -0.3                                    | 5                              | V                  |
| $I_{OUT}$            | Peak output current                | Internally limited                      |                                |                    |
|                      | Output short circuit duration      | Indefinite                              |                                |                    |
| $P_{DISS}$           | Total continuous power dissipation | See <a href="#">Thermal Information</a> |                                |                    |
| $T_J$                | Operating junction temperature     | -55                                     | 125                            | $^{\circ}\text{C}$ |
| $T_{stg}$            | Storage temperature                | -55                                     | 150                            | $^{\circ}\text{C}$ |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) To ensure proper operation of the device it is necessary that  $V_{IN} \leq V_{BIAS}$  under all conditions.
- (3) Whichever is less.
- (4) For durations no longer than 1ms each, for a total of no more than 1000 occurrences over the lifetime of the device.

## 6.2 ESD Ratings

|                                     |  | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |
|                                     | Machine model (MM)   | ±100  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction-air temperature range (unless otherwise noted)

|                          |                              | MIN                                      | NOM | MAX                              | UNIT |
|--------------------------|------------------------------|--|-----|----------------------------------|------|
| $V_{IN}$                 | Input voltage (steady-state) | 1.1                                      |     | $V_{BIAS}$ or 4.5 <sup>(1)</sup> | V    |
| $V_{BIAS}$               | Bias voltage                 | 2.5 or or $V_{OUT} + 1.4$ <sup>(2)</sup> |     | 5.5                              | V    |
| $V_{OUT}$                | Output voltage               | 0.9                                      |     | 3.6                              | V    |
| $I_{OUT}$                | Peak output current          | 0  |     | 350                              | mA   |
| $C_{IN}$                 | Input capacitance            |  | 1   |                                  | μF   |
| $C_{BIAS}$               | Bias capacitance             |  | 0.1 |                                  | μF   |
| $C_{OUT}$ <sup>(3)</sup> | Output capacitance           | 2.2                                      |     |                                  | μF   |

- (1) Whichever is less  
 (2) Whichever is greater  
 (3) Maximum ESR should be less than 250 mΩ.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | TPS720                                       |            | UNIT  |      |
|-------------------------------|--|------------|-------|------|
|                               | DRV (SON)                                    | YZU (WSCP) |       |      |
|                               | 6 PINS                                       | 5 PINS     |       |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 66.5       | 144.9 | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 86.2       | 1.1   | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 36.1       | 27.5  | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 1.7        | 4.1   | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 36.6       | 27.4  | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 7.4        | N/A   | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$  or  $2.5 \text{ V}$  (whichever is greater);  $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$ ,  $I_{\text{OUT}} = 1 \text{ mA}$ ,  $V_{\text{EN}} = 1.1 \text{ V}$ ,  $C_{\text{OUT}} = 2.2 \mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^\circ\text{C}$ .

| PARAMETER                                      |  | TEST CONDITIONS   | MIN  | TYP       | MAX                                     | UNIT                    |    |
|--|--|---|--|-----------|---|-------------------------|----|
| $V_{\text{IN}}$                                | Input voltage  |   | 1.1 <sup>(1)</sup>   |           | $V_{\text{BIAS}}$ or 4.5 <sup>(2)</sup> | V                       |    |
| $V_{\text{BIAS}}$                              | Bias voltage   |   | 2.5  |           | 5.5                                     | V                       |    |
| $V_{\text{OUT}}$ <sup>(3)</sup>                | Output voltage <sup>(4)</sup>  |   | 0.9  |           | 3.6                                     | V                       |    |
|  | Output accuracy  | Nominal   | $T_J = 25^\circ\text{C}$   | -3        |   | 3                       | mV |
|  |  | Over $V_{\text{BIAS}}$ , $V_{\text{IN}}$ , $I_{\text{OUT}}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$  | $V_{\text{OUT}} + 1.4 \text{ V} \leq V_{\text{BIAS}} \leq 5.5 \text{ V}$ ,<br>$V_{\text{OUT}} + 0.5 \text{ V} \leq V_{\text{IN}} \leq 4.5 \text{ V}$ ,<br>$0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$   | -2%       |   | 2%                      |    |
|  |  | Over $V_{\text{BIAS}}$ , $V_{\text{IN}}$ , $I_{\text{OUT}}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$  | <b>DRV package only:</b><br>$V_{\text{OUT}} + 1.4 \text{ V} \leq V_{\text{BIAS}} \leq 5.5 \text{ V}$ ,<br>$V_{\text{OUT}} + 0.5 \text{ V} \leq V_{\text{IN}} \leq 4.5 \text{ V}$ ,<br>$0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$ ,<br>$V_{\text{OUT}} < 1.2 \text{ V}$                       | -25       |   | 25                      | mV |
|  |  | Over $V_{\text{BIAS}}$ , $V_{\text{IN}}$ , $I_{\text{OUT}}$ , $T_J = -10^\circ\text{C}$ to $85^\circ\text{C}$   | <b>YZU package only:</b><br>$V_{\text{OUT}} + 1.4 \text{ V} \leq V_{\text{BIAS}} \leq 5.5 \text{ V}$ ,<br>$V_{\text{OUT}} + 0.5 \text{ V} \leq V_{\text{IN}} \leq 4.5 \text{ V}$ ,<br>$0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$ ,<br>$1.6 \text{ V} \leq V_{\text{OUT}} \leq 3.3 \text{ V}$ | -1%       |   | 1%                      |    |
| $V_{\text{IN}}$ floating                       | $V_{\text{OUT}} + 1.4 \text{ V} \leq V_{\text{BIAS}} \leq 5.5 \text{ V}$ ,<br>$0 \mu\text{A} \leq I_{\text{OUT}} \leq 500 \mu\text{A}$ |   | $\pm 1\%$  |           |   |                         |    |
| $\Delta V_{\text{OUT}}/\Delta V_{\text{IN}}$   | $V_{\text{IN}}$ line regulation  | $V_{\text{IN}} = (V_{\text{OUT}} + 0.5 \text{ V})$ to $4.5 \text{ V}$ , $I_{\text{OUT}} = 1 \text{ mA}$   |  | 16        |   | $\mu\text{V}/\text{V}$  |    |
| $\Delta V_{\text{OUT}}/\Delta V_{\text{BIAS}}$ | $V_{\text{BIAS}}$ line regulation  | $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$ or $2.5 \text{ V}$ (whichever is greater) to $5.5 \text{ V}$ , $I_{\text{OUT}} = 1 \text{ mA}$         |  | 16        |   | $\mu\text{V}/\text{V}$  |    |
|  | $V_{\text{IN}}$ line transient   | $\Delta V_{\text{IN}} = 400 \text{ mV}$ , $t_{\text{RISE}} = t_{\text{FALL}} = 1 \mu\text{s}$   |  | $\pm 200$ |   | $\mu\text{V}$           |    |
|  | $V_{\text{BIAS}}$ line transient   | $\Delta V_{\text{BIAS}} = 600 \text{ mV}$ , $t_{\text{RISE}} = t_{\text{FALL}} = 1 \mu\text{s}$   |  | $\pm 0.8$ |   | mV                      |    |
| $\Delta V_{\text{OUT}}/\Delta I_{\text{OUT}}$  | Load regulation  | $0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$ (no load to full load)   |  | -15       |   | $\mu\text{V}/\text{mA}$ |    |
|  | Load transient   | $0 \text{ mA} \leq I_{\text{OUT}} \leq 350 \text{ mA}$ , $t_{\text{RISE}} = t_{\text{FALL}} = 1 \mu\text{s}$  |  | $\pm 15$  |   | mV                      |    |
| $V_{\text{DO\_IN}}$                            | $V_{\text{IN}}$ dropout voltage <sup>(5)</sup>   | $V_{\text{IN}} = V_{\text{OUT(NOM)}} - 0.1 \text{ V}$ ,<br>$(V_{\text{BIAS}} - V_{\text{OUT(NOM)}}) = 1.4 \text{ V}$ ,<br>$I_{\text{OUT}} = 350 \text{ mA}$ |  | 110       | 200                                     | mV                      |    |
| $V_{\text{DO\_BIAS}}$                          | $V_{\text{BIAS}}$ dropout voltage <sup>(6)</sup>   | $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3 \text{ V}$ , $I_{\text{OUT}} = 350 \text{ mA}$   |  | 1.09      | 1.4                                     | V                       |    |
| $I_{\text{CL}}$                                | Output current limit   | $V_{\text{OUT}} = 0.9 \times V_{\text{OUT(NOM)}}$   | 420  | 525       | 800                                     | mA                      |    |
| $I_{\text{GND}}$                               | Ground pin current   | $I_{\text{OUT}} = 100 \mu\text{A}$  |  | 38        |   | $\mu\text{A}$           |    |
|  |  | $I_{\text{OUT}} = 0 \text{ mA}$ to $350 \text{ mA}$   |  | 54        | 80                                      |                         |    |
| $I_{\text{SHDN}}$                              | Shutdown current ( $I_{\text{GND}}$ )  | $V_{\text{EN}} \leq 0.4 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$  |  | 0.5       | 2                                       | $\mu\text{A}$           |    |
| PSRR   | $V_{\text{IN}}$ power-supply rejection ratio   | $V_{\text{IN}} - V_{\text{OUT}} \geq 0.5 \text{ V}$ ,<br>$V_{\text{BIAS}} = V_{\text{OUT}} + 1.4 \text{ V}$ ,<br>$I_{\text{OUT}} = 350 \text{ mA}$          | $f = 10 \text{ Hz}$  |           | 85                                      | dB                      |    |
|  |  |   | $f = 100 \text{ Hz}$   |           | 85                                      |                         |    |
|  |  |   | $f = 1 \text{ kHz}$  |           | 85                                      |                         |    |
|  |  |   | $f = 10 \text{ kHz}$   |           | 80                                      |                         |    |
|  |  |   | $f = 100 \text{ kHz}$  |           | 70                                      |                         |    |
|  |  |   | $f = 1 \text{ MHz}$  |           | 50                                      |                         |    |

(1) Performance specifications are ensured up to a minimum  $V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$ .

(2) Whichever is less.

(3) Minimum  $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$  or  $2.5 \text{ V}$  (whichever is greater) and  $V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$ .

(4)  $V_{\text{O}}$  nominal value is factory programmable through the onchip EEPROM.

(5) Measured for devices with  $V_{\text{OUT(NOM)}} \geq 1.2 \text{ V}$ .

(6)  $V_{\text{BIAS}} - V_{\text{OUT}}$  with  $V_{\text{OUT}} = V_{\text{OUT(NOM)}} - 0.1 \text{ V}$ . Measured for devices with  $V_{\text{OUT(NOM)}} \geq 1.8 \text{ V}$ .

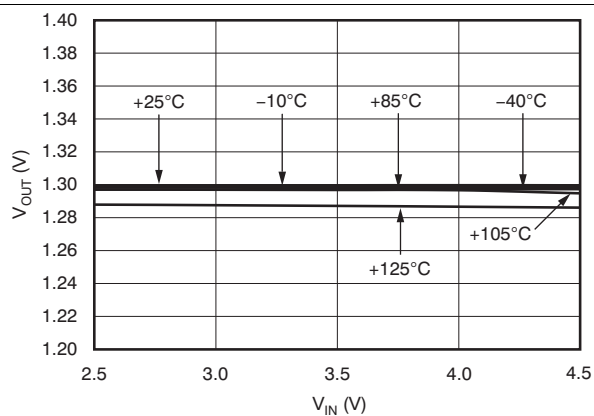
**Electrical Characteristics (continued)**

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$  or  $2.5 \text{ V}$  (whichever is greater);  $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$ ,  $I_{\text{OUT}} = 1 \text{ mA}$ ,  $V_{\text{EN}} = 1.1 \text{ V}$ ,  $C_{\text{OUT}} = 2.2 \mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

| PARAMETER                |  | TEST CONDITIONS  | MIN                   | TYP                     | MAX  | UNIT                       |
|--------------------------|--|--|-----------------------|-------------------------|------|----------------------------|
| PSRR                     | $V_{\text{BIAS}}$ power-supply rejection ratio | $V_{\text{IN}} - V_{\text{OUT}} \geq 0.5 \text{ V}$ ,<br>$V_{\text{BIAS}} = V_{\text{OUT}} + 1.4 \text{ V}$ ,<br>$I_{\text{OUT}} = 350 \text{ mA}$ | $f = 10 \text{ Hz}$   | 80                      |      | dB                         |
|                          |  |  | $f = 100 \text{ Hz}$  | 80                      |      |                            |
|                          |  |  | $f = 1 \text{ kHz}$   | 75                      |      |                            |
|                          |  |  | $f = 10 \text{ kHz}$  | 65                      |      |                            |
|                          |  |  | $f = 100 \text{ kHz}$ | 55                      |      |                            |
|                          |  |  | $f = 1 \text{ MHz}$   | 35                      |      |                            |
| $V_{\text{N}}$           | Output noise voltage                           | $\text{BW} = 10 \text{ Hz to } 100 \text{ kHz}$ , $V_{\text{BIAS}} \geq 2.5 \text{ V}$ ,<br>$V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$       |                       | 48                      |      | $\mu\text{V}_{\text{RMS}}$ |
| $I_{\text{VIN\_INRUSH}}$ | Inrush current on $V_{\text{IN}}$              | $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$ or $2.5 \text{ V}$ (whichever is greater), $V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$   |                       | $100 + I_{\text{LOAD}}$ |      | mA                         |
| $t_{\text{STR}}$         | Start-up time                                  | $V_{\text{OUT}} = 95\% V_{\text{OUT(NOM)}}$ , $I_{\text{OUT}} = 350 \text{ mA}$ ,<br>$C_{\text{OUT}} = 2.2 \mu\text{F}$                            |                       | 140                     |      | $\mu\text{s}$              |
| $V_{\text{EN(HI)}}$      | Enable pin high (enabled)                      |  | 1.1                   |                         |      | V                          |
| $V_{\text{EN(LO)}}$      | Enable pin low (disabled)                      |  | 0                     |                         | 0.4  | V                          |
| $I_{\text{EN}}$          | Enable pin current                             | $V_{\text{EN}} = 5.5 \text{ V}$ , $V_{\text{IN}} = 4.5 \text{ V}$ , $V_{\text{BIAS}} = 5.5 \text{ V}$  |                       |                         | 1    | $\mu\text{A}$              |
| UVLO                     | Undervoltage lockout                           | $V_{\text{BIAS}}$ rising   | 2.41                  | 2.45                    | 2.49 | V                          |
|                          | Hysteresis                                     | $V_{\text{BIAS}}$ falling  |                       | 150                     |      | mV                         |
| $T_{\text{SD}}$          | Thermal shutdown temperature                   | Shutdown, temperature increasing   |                       | 160                     |      | $^{\circ}\text{C}$         |
|                          |  | Reset, temperature decreasing  |                       | 140                     |      |                            |
| $T_J$                    | Operating junction temperature                 |  | -40                   |                         | 125  | $^{\circ}\text{C}$         |

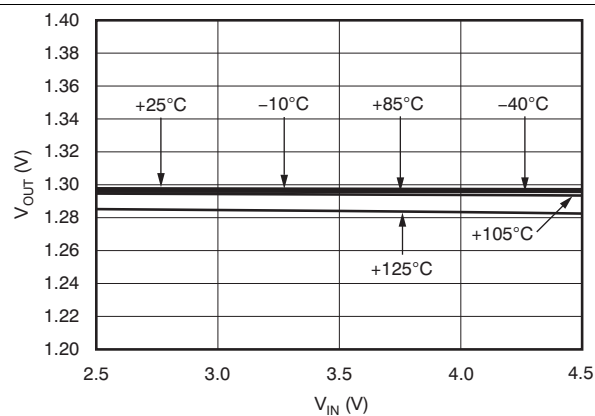
## 6.6 Typical Characteristics

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4 \text{ V})$  or  $2.5 \text{ V}$  (whichever is greater);  $V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$ ,  $I_{\text{OUT}} = 1 \text{ mA}$ ,  $V_{\text{EN}} = 1.1 \text{ V}$ ,  $C_{\text{OUT}} = 2.2 \mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^\circ\text{C}$ .



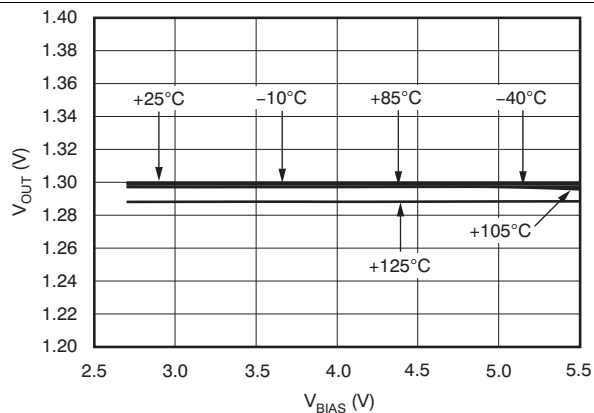
$I_{\text{OUT}} = 0 \text{ mA}$

Figure 1.  $V_{\text{IN}}$  Line Regulation (TPS72013YZU)



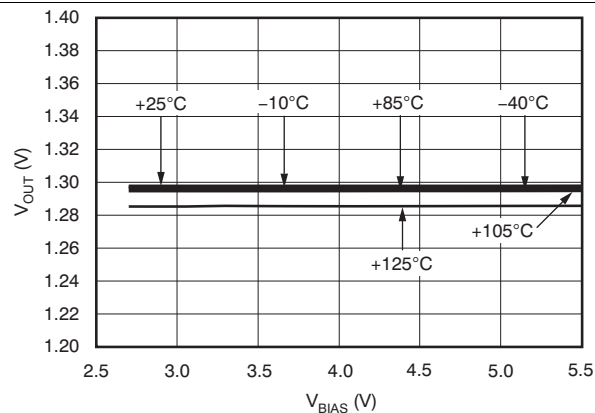
$I_{\text{OUT}} = 350 \text{ mA}$

Figure 2.  $V_{\text{IN}}$  Line Regulation (TPS72013YZU)



$I_{\text{OUT}} = 0 \text{ mA}$

Figure 3.  $V_{\text{BIAS}}$  Line Regulation (TPS72013YZU)



$I_{\text{OUT}} = 350 \text{ mA}$

Figure 4.  $V_{\text{BIAS}}$  Line Regulation (TPS72013YZU)

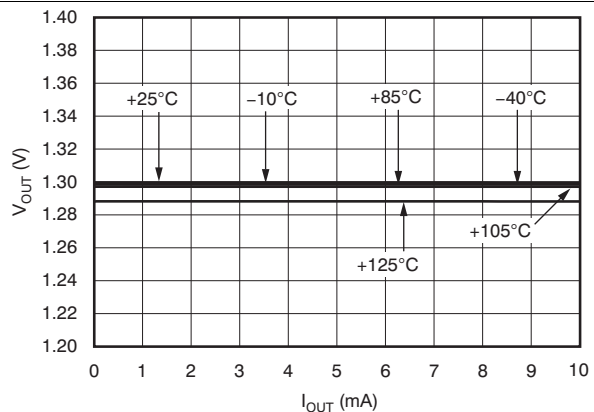


Figure 5. Load Regulation Under Light Loads (TPS72013YZU)

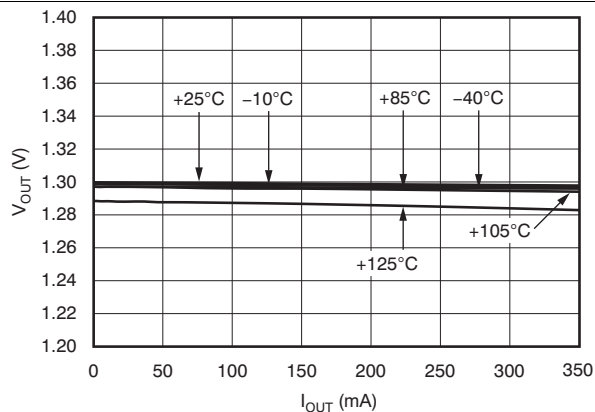


Figure 6. Load Regulation (TPS72013YZU)

Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.5\text{ V}$  (whichever is greater);  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

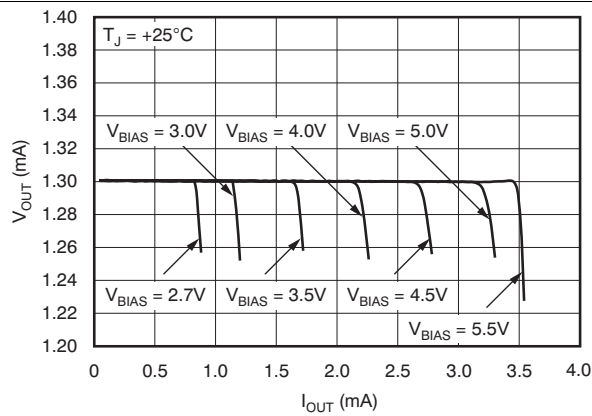


Figure 7. Load Regulation With  $V_{IN}$  Floating (TPS72013YZU)

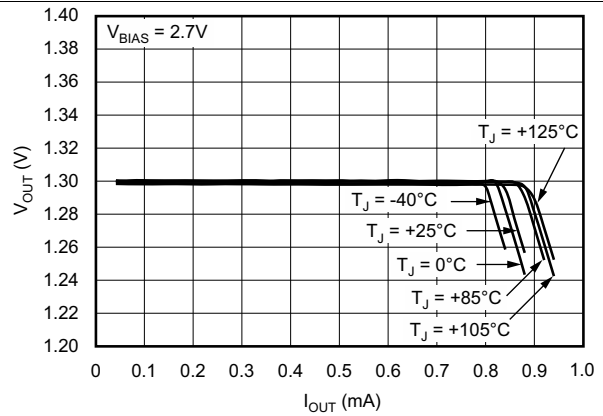


Figure 8. Load Regulation With  $V_{IN}$  Floating (TPS72013YZU)

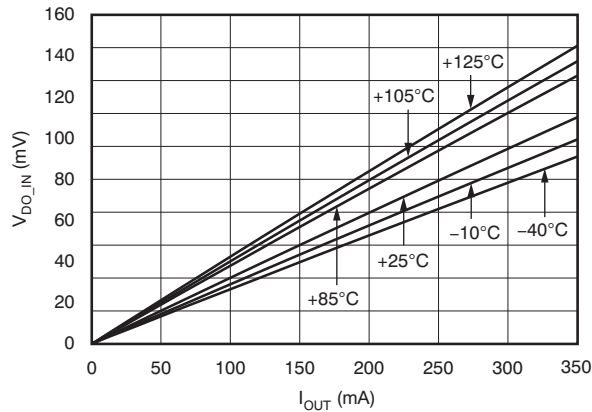


Figure 9.  $V_{IN}$  Dropout Voltage vs Output Current (TPS72013YZU)

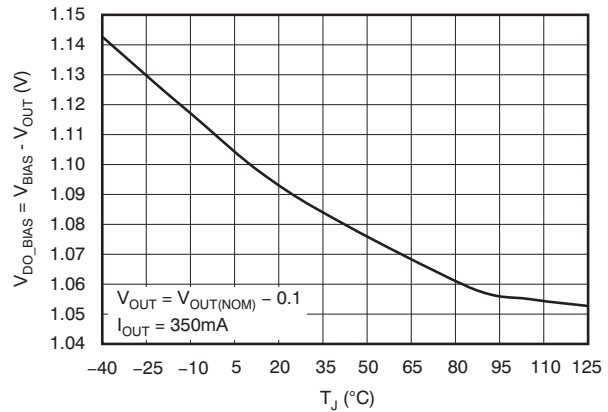


Figure 10.  $V_{BIAS}$  Dropout Voltage vs Temperature (TPS72033YZU)

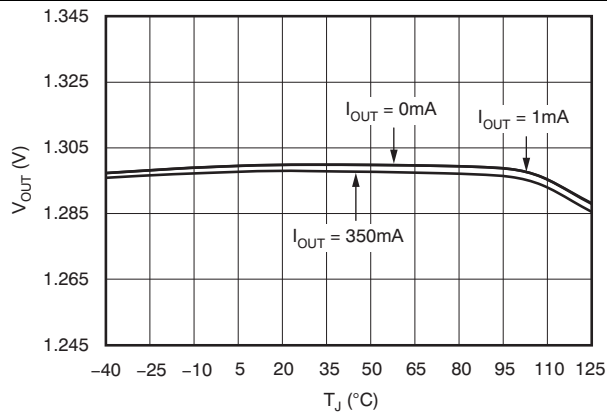


Figure 11. Output Voltage vs Temperature (TPS72013YZU)

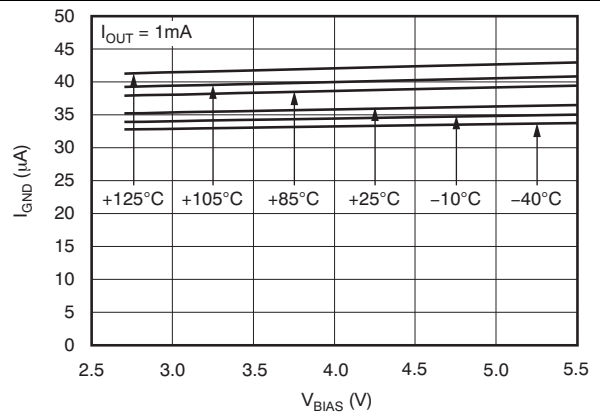


Figure 12. Ground Pin Current vs  $V_{BIAS}$  Input Voltage (TPS72013YZU)



Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_{\text{BIAS}} = (V_{\text{OUT}} + 1.4\text{ V})$  or  $2.5\text{ V}$  (whichever is greater);  $V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{ V}$ ,  $I_{\text{OUT}} = 1\text{ mA}$ ,  $V_{\text{EN}} = 1.1\text{ V}$ ,  $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^\circ\text{C}$ .

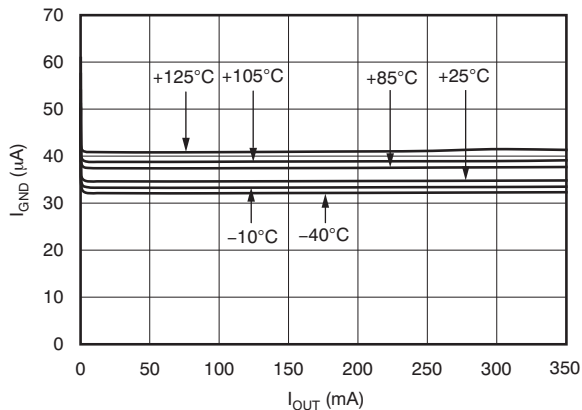


Figure 13. Ground Pin Current vs Output Current (TPS72013YZU)

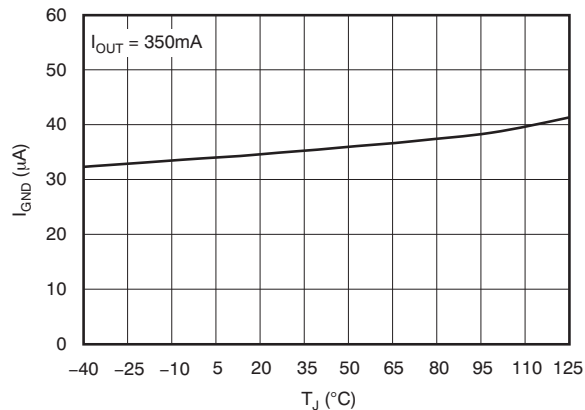


Figure 14. Ground Pin Current vs Temperature (TPS72013YZU)

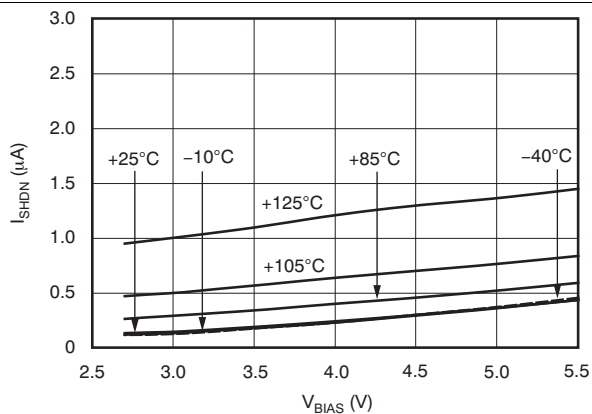


Figure 15. Shutdown Current vs VBIAS Input Voltage (TPS72013YZU)

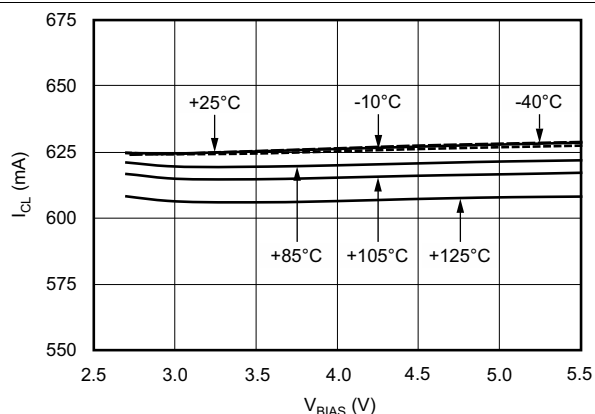


Figure 16. Current Limit vs VBIAS Input Voltage (TPS72013YZU)

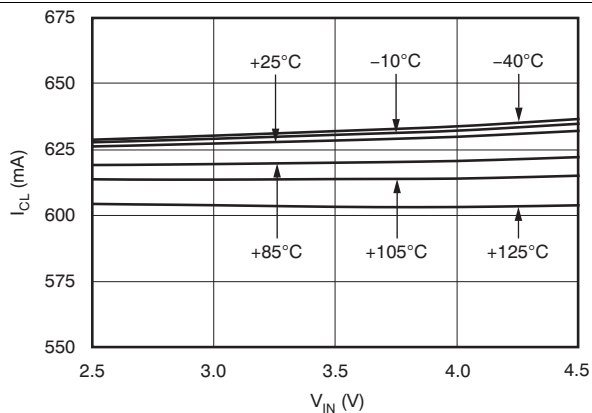


Figure 17. Current Limit vs VIN Input Voltage (TPS72013YZU)

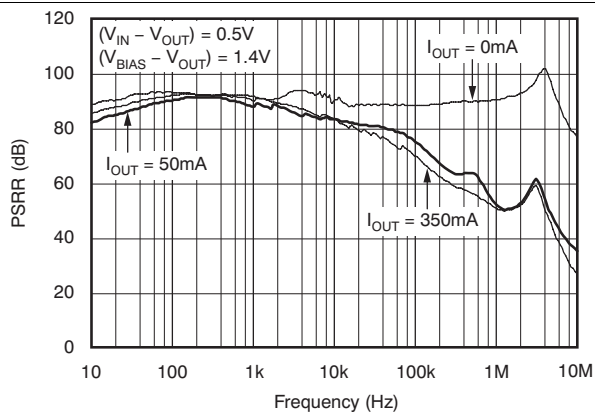


Figure 18. VIN Power-Supply Ripple Rejection vs Frequency (TPS72015YZU)

Typical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.5\text{ V}$  (whichever is greater);  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

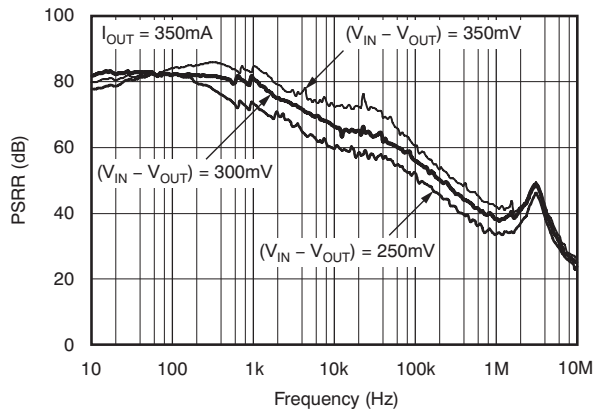


Figure 19.  $V_{IN}$  Power-Supply Ripple Rejection vs Frequency (TPS72015YZU)

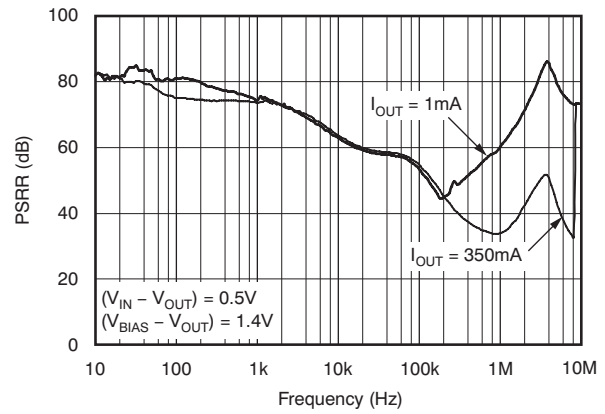


Figure 20.  $V_{BIAS}$  Power-Supply Ripple Rejection vs Frequency (TPS72015YZU)

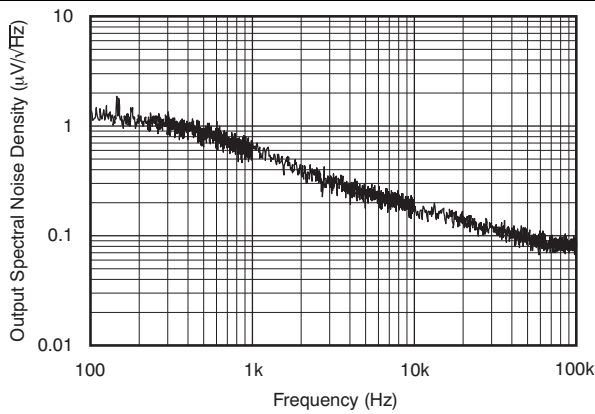


Figure 21. Output Spectral Noise Density vs Frequency (TPS72015YZU)

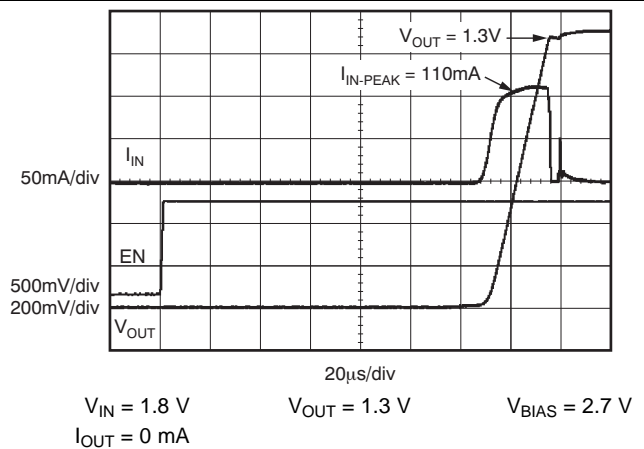


Figure 22.  $V_{IN}$  Inrush Current

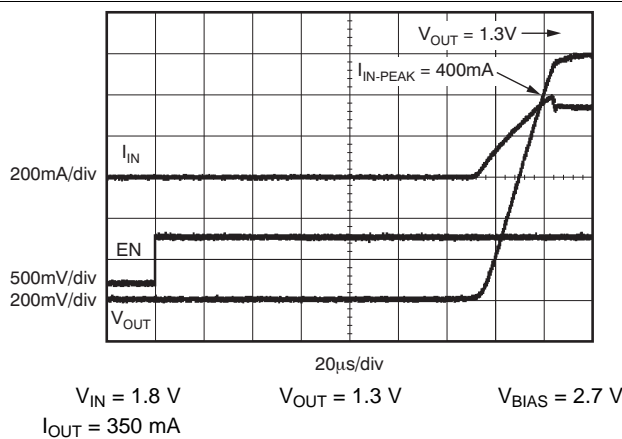


Figure 23.  $V_{IN}$  Inrush Current

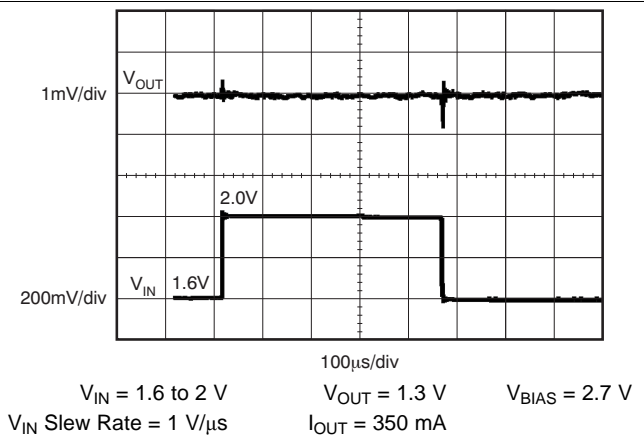
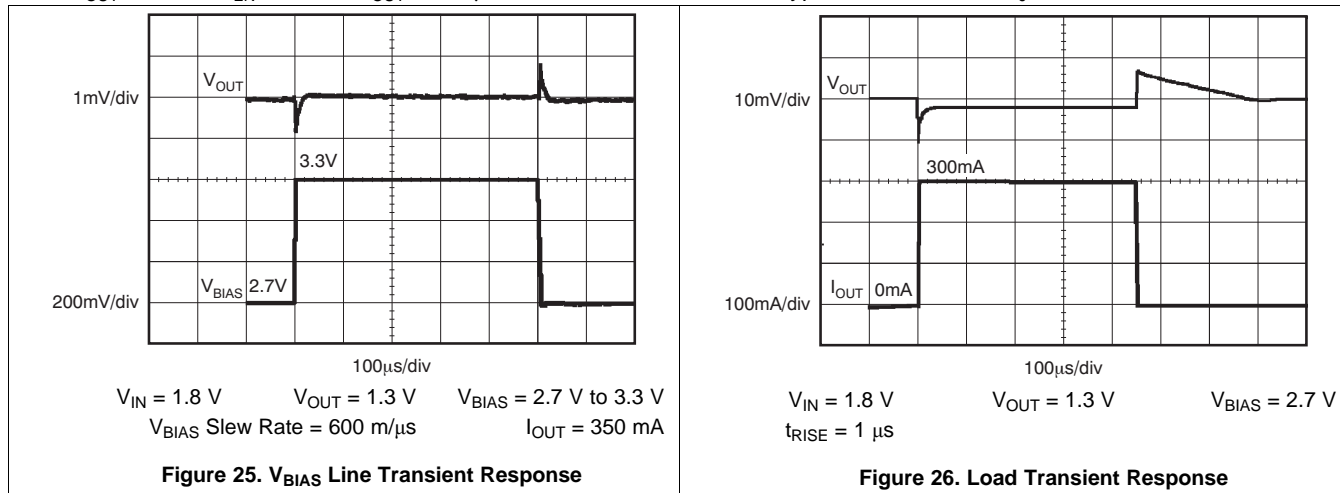


Figure 24.  $V_{IN}$  Line Transient Response

**Typical Characteristics (continued)**

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.5\text{ V}$  (whichever is greater);  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

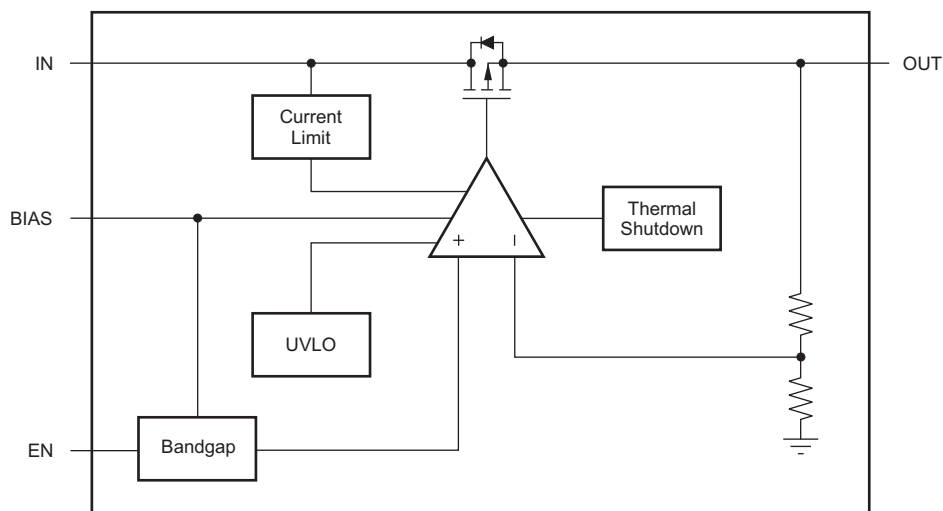


## 7 Detailed Description

### 7.1 Overview

The TPS720 belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1 MHz) at very low headroom ( $V_{IN} - V_{OUT}$ ). The implementation of the BIAS pin on the TPS720 vastly improves efficiency of low  $V_{OUT}$  applications by allowing the use of a preregulated, low-voltage input supply. The TPS720 supports a novel feature in which the output of the LDO regulates under light loads (<500  $\mu$ A) when the IN pin is left floating. The light-load drive current is sourced from  $V_{BIAS}$  under this condition. This feature is particularly useful in power-saving applications where the DC-DC converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load. These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Internal Current Limit

The TPS720 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is  $V_{OUT} = I_{LIMIT} \times R_{LOAD}$ . The NMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{LIMIT}$  until thermal shut down is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Considerations](#) section for more details.

The NMOS pass element in the TPS720 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

#### 7.3.2 Inrush Current Limit

The TPS720 family of LDO regulators implement a novel inrush current limit circuit architecture: the current drawn through the IN pin is limited to a finite value. This  $I_{INRUSHLIMIT}$  charges the output to its final voltage. All the current drawn through  $V_{IN}$  goes to charge the output capacitance when the load is disconnected. The following equation shows the inrush current limit performed by the circuit:

$$I_{INRUSHLIMIT}(A) = C_{OUT}(\mu F) \times 0.0454545 (V/\mu s) + I_{LOAD}(A) \quad (1)$$

## Feature Description (continued)

Assuming a  $C_{OUT}$  of 2.2  $\mu\text{F}$  with the load disconnected (that is,  $I_{LOAD} = 0$ ) the  $I_{INRUSHLIMIT}$  is calculated to be 100 mA. The inrush current charges the LDO output capacitor. If the output of the LDO regulates to 1.3 V, then the LDO charges the output capacitor to the final output value in approximately 28.6  $\mu\text{s}$ .

Another consideration is when a load is connected to the output of an LDO. The connected load tries to steer a portion of the current away from  $V_{OUT}$ . The TPS720 inrush current limit circuit employs a new technique that supplies not only the  $I_{INRUSHLIMIT}$ , but also the additional current needed by the load. If  $I_{LOAD} = 350$  mA, then the  $I_{INRUSHLIMIT}$  calculates to be approximately 450 mA (from [Equation 1](#)).

### 7.3.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

### 7.3.4 Undervoltage Lockout (UVLO)

The TPS720 uses an undervoltage lock-out circuit on the BIAS pin to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50- $\mu\text{s}$  duration.

## 7.4 Device Functional Modes

Driving the EN pin over 1.1 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 500 nA, typically.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability on the IN pin, it is good analog design practice to connect a 0.1- $\mu\text{F}$  to 1- $\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located close to the power source. If source impedance is not sufficiently low, a 0.1- $\mu\text{F}$  input capacitor may be necessary to ensure stability.

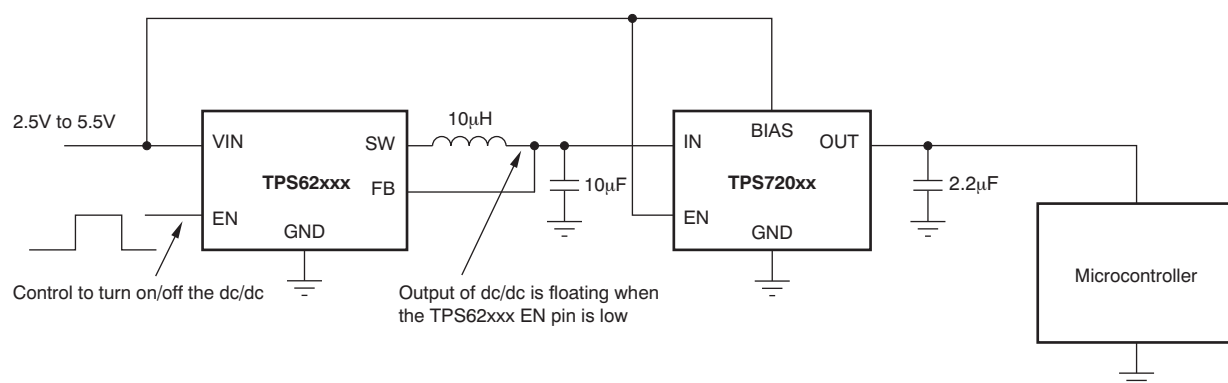
The BIAS pin does not require an input capacitor because it does not source high currents. However, if source impedance is not sufficiently low, then TI recommends a small 0.1- $\mu\text{F}$  bypass capacitor.

The TPS720 is designed to be stable with standard ceramic capacitors with values of 2.2  $\mu\text{F}$  or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 250 m $\Omega$ .

#### 8.1.2 Output Regulation With IN Pin Floating

The TPS720 supports a novel feature in which the output of the LDO regulates under light loads when the IN pin is left floating. Under normal conditions, when the IN pin is connected to a power source, the BIAS pin draws only tens of milliamperes. However, when the IN pin is floating, an innovative circuit is used that allows a maximum current of 500  $\mu\text{A}$  to be drawn by the load through the BIAS pin, while maintaining the output in regulation. This feature is particularly useful in power-saving applications where a DC-DC converter connected to the IN pin is disabled, but the LDO is required to regulate the output voltage to a light load.

Figure 27 shows an application example where a microcontroller is not turned off (to maintain the state of the internal memory), but where the regulated supply (shown as the TPS62xxx) is turned off to reduce power. In this case, the TPS720 BIAS pin provides sufficient load current to maintain a regulated voltage to the microcontroller.



**Figure 27. Example of Floating IN Pin Regulation**

## Application Information (continued)

### 8.1.3 Dropout Voltage

The TPS720 uses a NMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the NMOS pass element.  $V_{DO}$  approximately scales with output current because the NMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in [Figure 19](#).

### 8.1.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

### 8.1.5 Minimum Load

The TPS720 is stable with no output load. Traditional LDOs suffer from low loop gain at very light output loads. The TPS720 employs an innovative, low-current mode circuit under very light or no-load conditions, resulting in improved output voltage regulation performance reduced to zero output current.

## 8.2 Typical Application

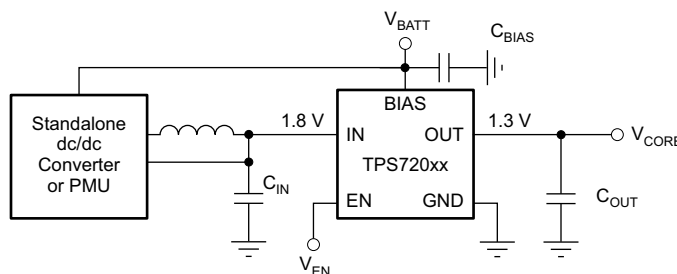


Figure 28. Typical Application Schematic

### 8.2.1 Design Requirements

[Table 1](#) shows the parameters for this design example.

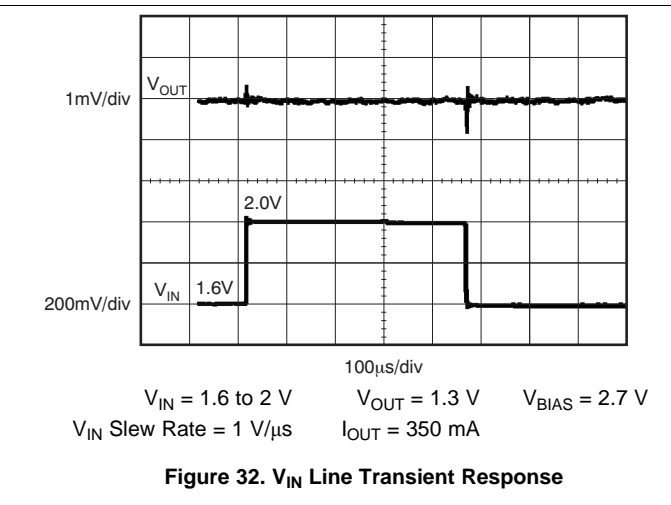
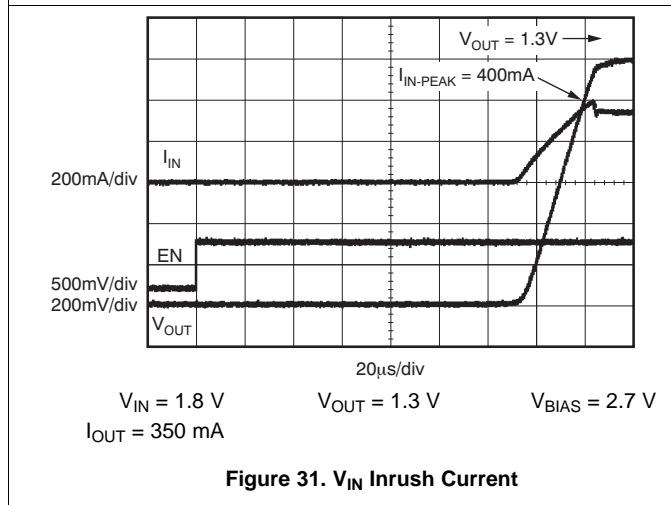
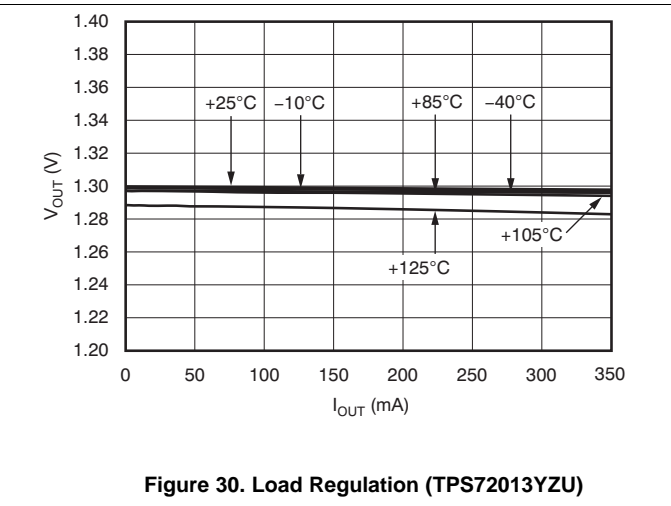
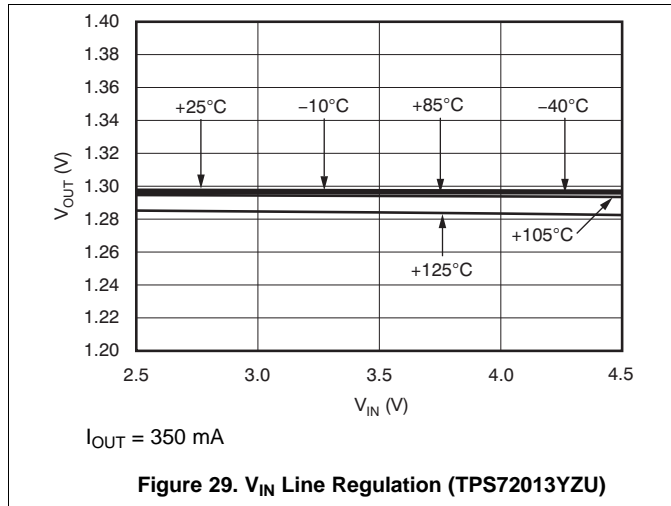
Table 1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE              |
|------------------|----------------------------|
| $V_{IN}$         | 1.8 V                      |
| $V_{BIAS}$       | 2.7 V                      |
| $V_{OUT}$        | 1.3 V                      |
| $I_{OUT}$        | 10-mA typical, 350-mA peak |

### 8.2.2 Detailed Design Procedures

A small-size solution is desired, so select the minimum recommended component size. Set  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 100 \text{ nF}$ ,  $C_{OUT} = 2.2 \mu\text{F}$ .

### 8.2.3 Application Curves





## 9 Power Supply Recommendations

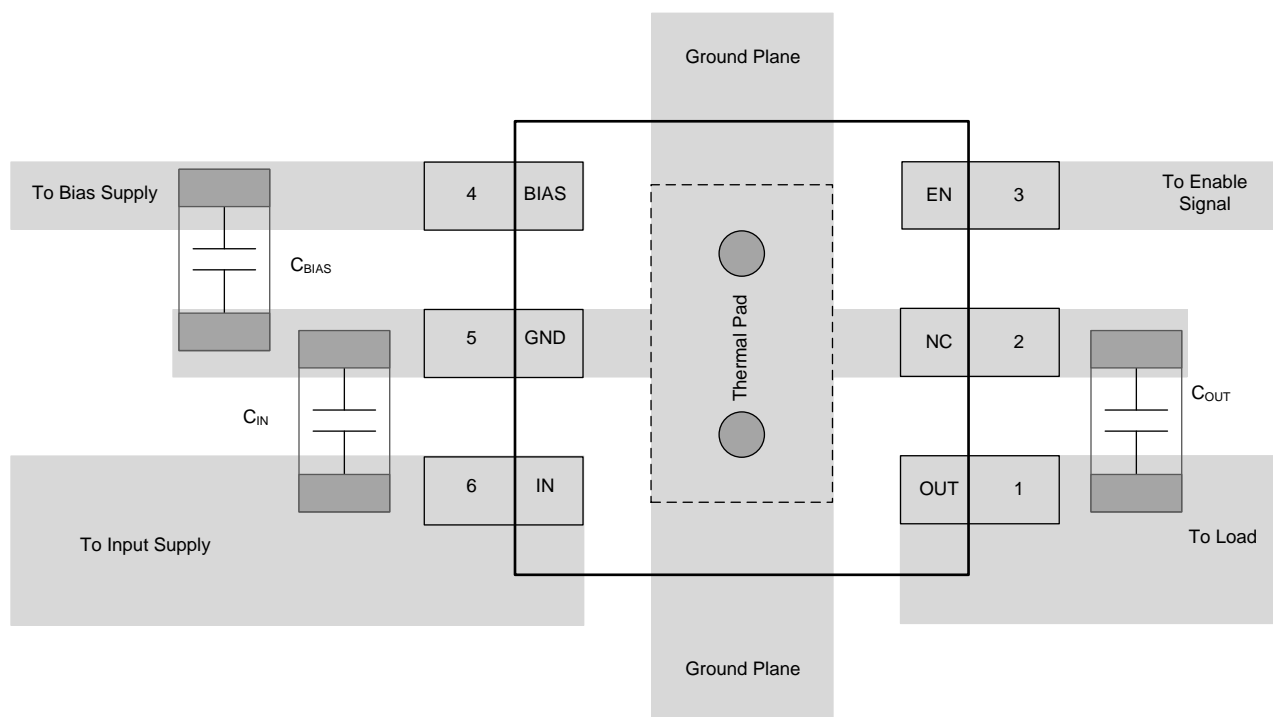
The input supply and bias supply for the LDO must be within its recommended operating conditions and provide adequate headroom for the device to have a regulated output. The minimum capacitor requirements must be met, and if the input supply is noisy, then additional input capacitors with low ESR can help improve transient performance.

## 10 Layout

### 10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High equivalent series resistance (ESR) capacitors may degrade PSRR. The BIAS pin draws very little current and can be routed as a signal (make sure to shield it from high-frequency coupling).

### 10.2 Layout Example



**Figure 33. Recommended Layout**

### 10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

## Thermal Considerations (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS720 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS720 into thermal shutdown degrades device reliability.

### 10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element ( $V_{IN}$  to  $V_{OUT}$ ), as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS720. The [TPS720xxDRVEVM evaluation module](#) (and [related user guide](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

#### 11.1.2 Device Nomenclature

**Table 2. Device Nomenclature<sup>(1)(2)</sup>**

| PRODUCT     | V <sub>OUT</sub>  |
|-------------|---|
| TPS720xx(x) | <p><b>xx(x)</b> is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V).</p> <p><b>yy</b> is the package designator.</p> <p><b>z</b> is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).</p> |

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).
- (2) Output voltages from 0.9 V to 3.6 V in 50-mV increments are available. Contact the factory for details and availability.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [TPS720xxDRVEVM Evaluation Module, SBVU024](#)
- [Using New Thermal Metrics, SBVA025](#)

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

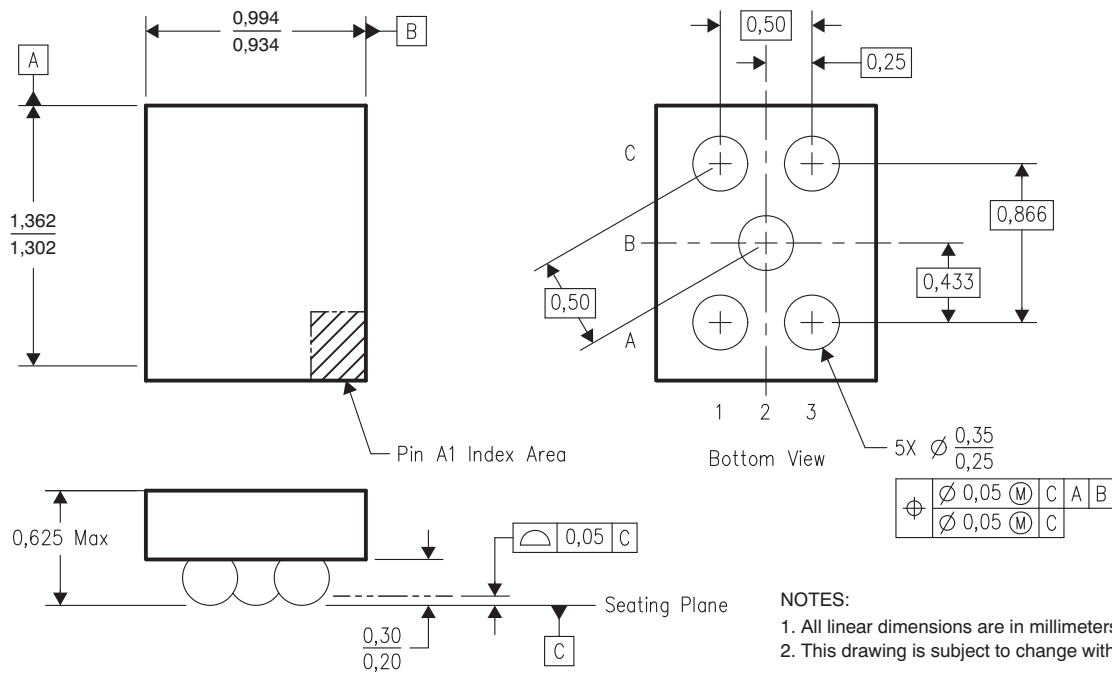
This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 12.1 Package Mounting

Solder pad footprint recommendations for the TPS720 are available from the Texas Instruments website at [www.ti.com](http://www.ti.com).



**Figure 34. YZU Wafer Chip-Scale Package Dimensions (in mm)**

**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS72009YZUR</a>  | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | G3                  |
| TPS72009YZUR.B                | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | G3                  |
| <a href="#">TPS72009YZUT</a>  | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | G3                  |
| TPS72009YZUT.B                | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | G3                  |
| <a href="#">TPS720102YZUR</a> | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | DI                  |
| TPS720102YZUR.B               | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | DI                  |
| <a href="#">TPS720102YZUT</a> | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | DI                  |
| TPS720102YZUT.B               | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | DI                  |
| <a href="#">TPS720105DRVR</a> | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | ODC                 |
| TPS720105DRVR.B               | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | ODC                 |
| <a href="#">TPS720105DRVT</a> | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | ODC                 |
| TPS720105DRVT.B               | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | ODC                 |
| <a href="#">TPS720105YZUR</a> | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NM                  |
| TPS720105YZUR.B               | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NM                  |
| <a href="#">TPS720105YZUT</a> | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NM                  |
| TPS720105YZUT.B               | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NM                  |
| <a href="#">TPS72010DRVR</a>  | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAA                 |
| TPS72010DRVR.B                | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAA                 |
| <a href="#">TPS72010DRVT</a>  | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAA                 |
| TPS72010DRVT.B                | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAA                 |
| <a href="#">TPS720115DRVR</a> | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | SHP                 |
| TPS720115DRVR.B               | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | SHP                 |
| <a href="#">TPS720115DRVT</a> | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | SHP                 |
| TPS720115DRVT.B               | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | SHP                 |
| <a href="#">TPS72011DRVR</a>  | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | PAR                 |
| TPS72011DRVR.B                | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | PAR                 |
| <a href="#">TPS72011DRVT</a>  | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | PAR                 |
| TPS72011DRVT.B                | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | PAR                 |
| <a href="#">TPS72011YZUR</a>  | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | BQ                  |

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS72011YZUR.B                | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | BQ                  |
| <a href="#">TPS72011YZUT</a>  | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | BQ                  |
| TPS72011YZUT.B                | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | BQ                  |
| <a href="#">TPS72012DRVR</a>  | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAB                 |
| TPS72012DRVR.B                | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAB                 |
| <a href="#">TPS72012DRVT</a>  | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAB                 |
| TPS72012DRVT.B                | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAB                 |
| <a href="#">TPS72012YZUR</a>  | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NN                  |
| TPS72012YZUR.B                | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NN                  |
| <a href="#">TPS72012YZUT</a>  | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NN                  |
| TPS72012YZUT.B                | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | NN                  |
| <a href="#">TPS720132YZUR</a> | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 7J                  |
| TPS720132YZUR.B               | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 7J                  |
| <a href="#">TPS720132YZUT</a> | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 7J                  |
| TPS720132YZUT.B               | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 7J                  |
| <a href="#">TPS72013YZUR</a>  | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FS                  |
| TPS72013YZUR.B                | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FS                  |
| <a href="#">TPS72013YZUT</a>  | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FS                  |
| TPS72013YZUT.B                | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FS                  |
| <a href="#">TPS72015DRVR</a>  | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAC                 |
| TPS72015DRVR.B                | Active        | Production           | WSON (DRV)   6  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAC                 |
| <a href="#">TPS72015DRVT</a>  | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAC                 |
| TPS72015DRVT.B                | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAC                 |
| TPS72015DRVTG4                | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAC                 |
| TPS72015DRVTG4.B              | Active        | Production           | WSON (DRV)   6  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | DAC                 |
| <a href="#">TPS72015YZUR</a>  | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FT                  |
| TPS72015YZUR.B                | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FT                  |
| <a href="#">TPS72015YZUT</a>  | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FT                  |
| TPS72015YZUT.B                | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | FT                  |
| <a href="#">TPS72017YZUR</a>  | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GC                  |
| TPS72017YZUR.B                | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GC                  |

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS72017YZUT</a> | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GC                  |
| TPS72017YZUT.B               | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GC                  |
| <a href="#">TPS72018DRVR</a> | Active        | Production           | WSO (DRV)   6   | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAD                 |
| TPS72018DRVR.B               | Active        | Production           | WSO (DRV)   6   | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAD                 |
| <a href="#">TPS72018DRVT</a> | Active        | Production           | WSO (DRV)   6   | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAD                 |
| TPS72018DRVT.B               | Active        | Production           | WSO (DRV)   6   | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | DAD                 |
| <a href="#">TPS72018YZUR</a> | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GD                  |
| TPS72018YZUR.B               | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GD                  |
| <a href="#">TPS72018YZUT</a> | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GD                  |
| TPS72018YZUT.B               | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | GD                  |
| <a href="#">TPS72023YZUR</a> | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 6F                  |
| TPS72023YZUR.B               | Active        | Production           | DSBGA (YZU)   5 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 6F                  |
| <a href="#">TPS72023YZUT</a> | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 6F                  |
| TPS72023YZUT.B               | Active        | Production           | DSBGA (YZU)   5 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 125   | 6F                  |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF TPS720 :**

- Automotive : [TPS720-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS72009YZUR  | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72009YZUT  | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS720102YZUR | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS720102YZUT | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS720105DRVR | WSO          | DRV             | 6    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS720105DRVT | WSO          | DRV             | 6    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS720105YZUR | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS720105YZUT | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72010DRVR  | WSO          | DRV             | 6    | 3000 | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72010DRVT  | WSO          | DRV             | 6    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS720115DRVR | WSO          | DRV             | 6    | 3000 | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS720115DRVT | WSO          | DRV             | 6    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72011DRVR  | WSO          | DRV             | 6    | 3000 | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72011DRVT  | WSO          | DRV             | 6    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72011YZUR  | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72011YZUT  | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS72012DRVR   | WSO          | DRV             | 6    | 3000 | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72012DRVT   | WSO          | DRV             | 6    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72012YZUR   | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72012YZUT   | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS720132YZUR  | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS720132YZUT  | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72013YZUR   | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72013YZUT   | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72015DRVR   | WSO          | DRV             | 6    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS72015DRVT   | WSO          | DRV             | 6    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72015DRVT   | WSO          | DRV             | 6    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS72015DRVTG4 | WSO          | DRV             | 6    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS72015YZUR   | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72015YZUT   | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72017YZUR   | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72017YZUT   | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72018DRVR   | WSO          | DRV             | 6    | 3000 | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72018DRVT   | WSO          | DRV             | 6    | 250  | 179.0              | 8.4                | 2.2     | 2.2     | 1.2     | 4.0     | 8.0    | Q2            |
| TPS72018YZUR   | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72018YZUT   | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72023YZUR   | DSBGA        | YZU             | 5    | 3000 | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |
| TPS72023YZUT   | DSBGA        | YZU             | 5    | 250  | 180.0              | 8.4                | 1.07    | 1.42    | 0.74    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

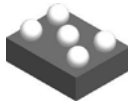


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS72009YZUR  | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72009YZUT  | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS720102YZUR | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS720102YZUT | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS720105DRVR | WSON         | DRV             | 6    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS720105DRVT | WSON         | DRV             | 6    | 250  | 182.0       | 182.0      | 20.0        |
| TPS720105YZUR | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS720105YZUT | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72010DRVR  | WSON         | DRV             | 6    | 3000 | 200.0       | 183.0      | 25.0        |
| TPS72010DRVT  | WSON         | DRV             | 6    | 250  | 200.0       | 183.0      | 25.0        |
| TPS720115DRVR | WSON         | DRV             | 6    | 3000 | 203.0       | 203.0      | 35.0        |
| TPS720115DRVT | WSON         | DRV             | 6    | 250  | 203.0       | 203.0      | 35.0        |
| TPS72011DRVR  | WSON         | DRV             | 6    | 3000 | 200.0       | 183.0      | 25.0        |
| TPS72011DRVT  | WSON         | DRV             | 6    | 250  | 200.0       | 183.0      | 25.0        |
| TPS72011YZUR  | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72011YZUT  | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72012DRVR  | WSON         | DRV             | 6    | 3000 | 200.0       | 183.0      | 25.0        |
| TPS72012DRVT  | WSON         | DRV             | 6    | 250  | 200.0       | 183.0      | 25.0        |

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS72012YZUR   | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72012YZUT   | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS720132YZUR  | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS720132YZUT  | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72013YZUR   | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72013YZUT   | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72015DRVR   | WSON         | DRV             | 6    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72015DRVT   | WSON         | DRV             | 6    | 250  | 203.0       | 203.0      | 35.0        |
| TPS72015DRVT   | WSON         | DRV             | 6    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72015DRVTG4 | WSON         | DRV             | 6    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72015YZUR   | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72015YZUT   | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72017YZUR   | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72017YZUT   | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72018DRVR   | WSON         | DRV             | 6    | 3000 | 200.0       | 183.0      | 25.0        |
| TPS72018DRVT   | WSON         | DRV             | 6    | 250  | 203.0       | 203.0      | 35.0        |
| TPS72018YZUR   | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72018YZUT   | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TPS72023YZUR   | DSBGA        | YZU             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS72023YZUT   | DSBGA        | YZU             | 5    | 250  | 182.0       | 182.0      | 20.0        |

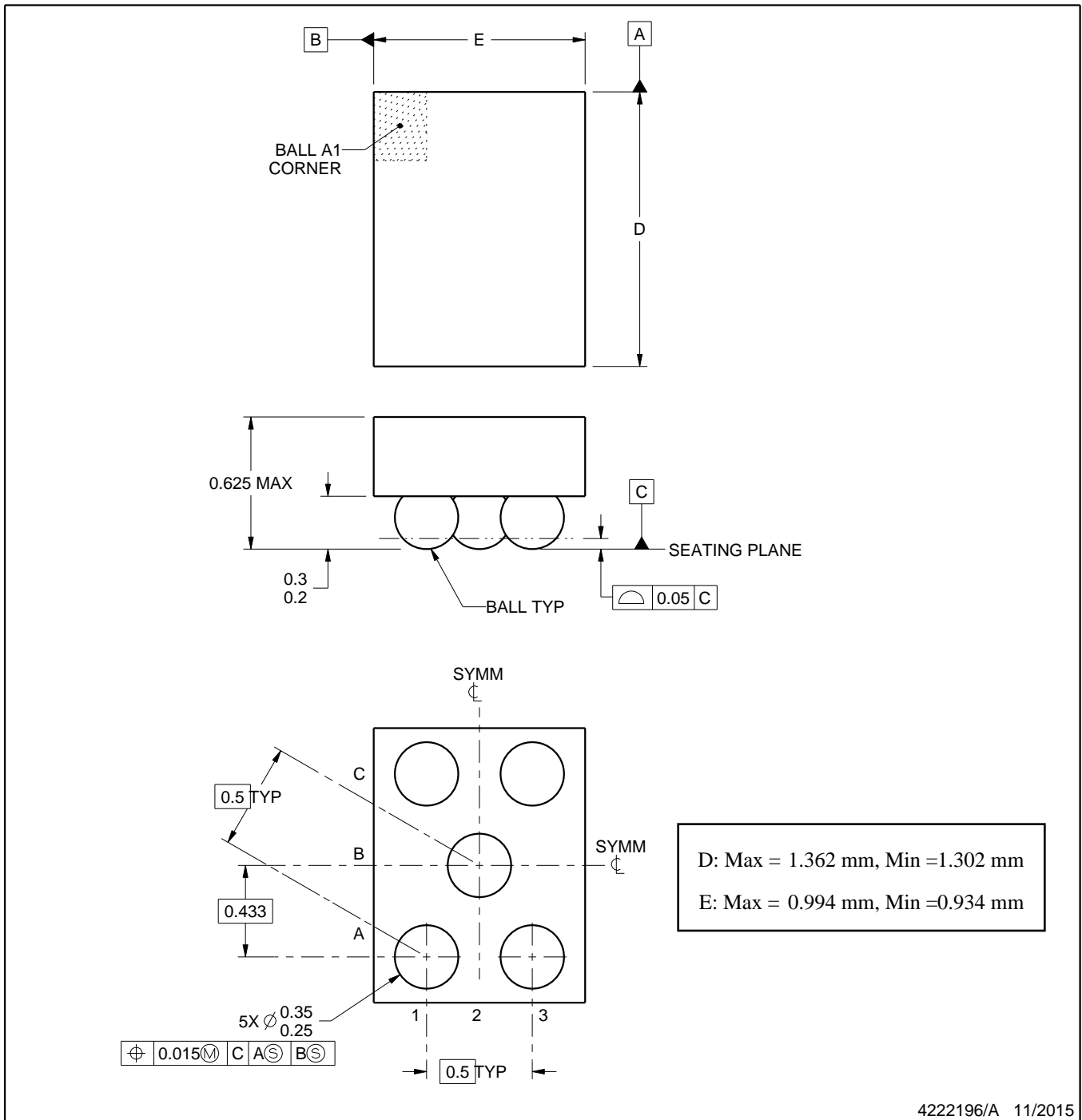
YZU0005



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4222196/A 11/2015

NOTES:

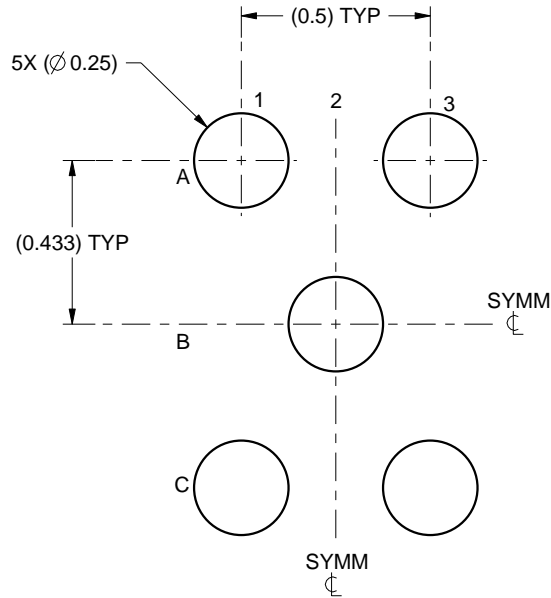
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

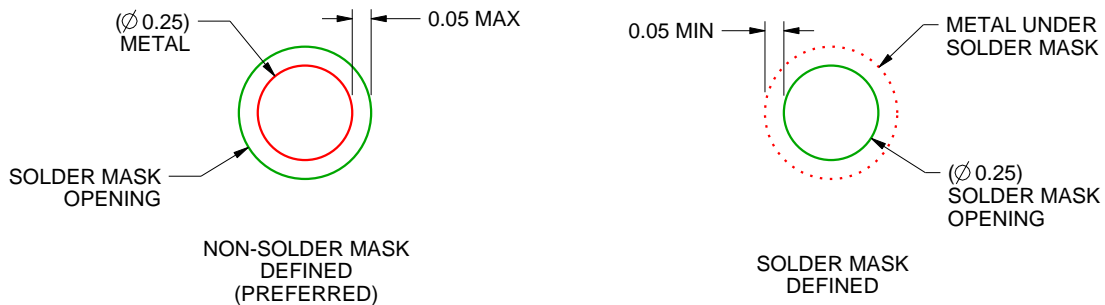
YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:50X



SOLDER MASK DETAILS  
NOT TO SCALE

4222196/A 11/2015

NOTES: (continued)

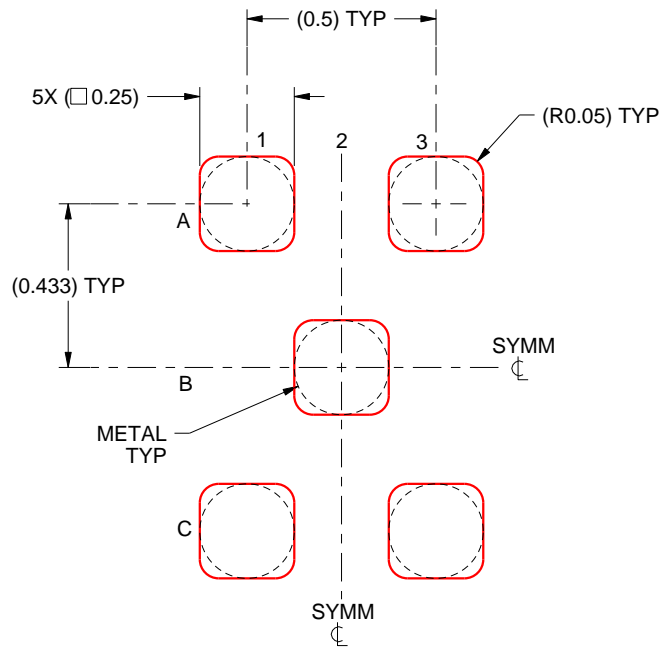
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZU0005

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

4222196/A 11/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## GENERIC PACKAGE VIEW

DRV 6

WSO - 0.8 mm max height

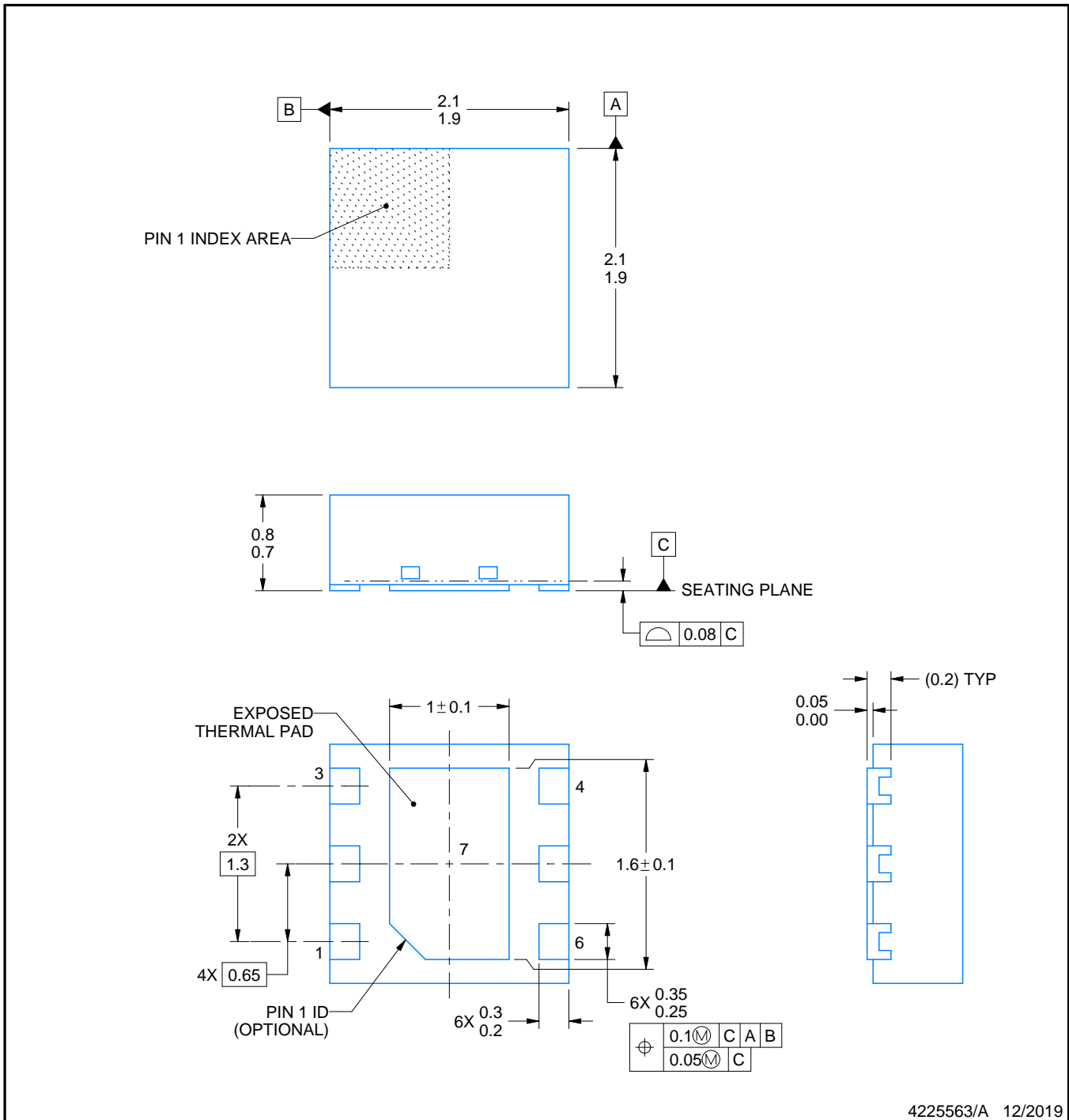
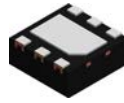
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F





4225563/A 12/2019

NOTES:

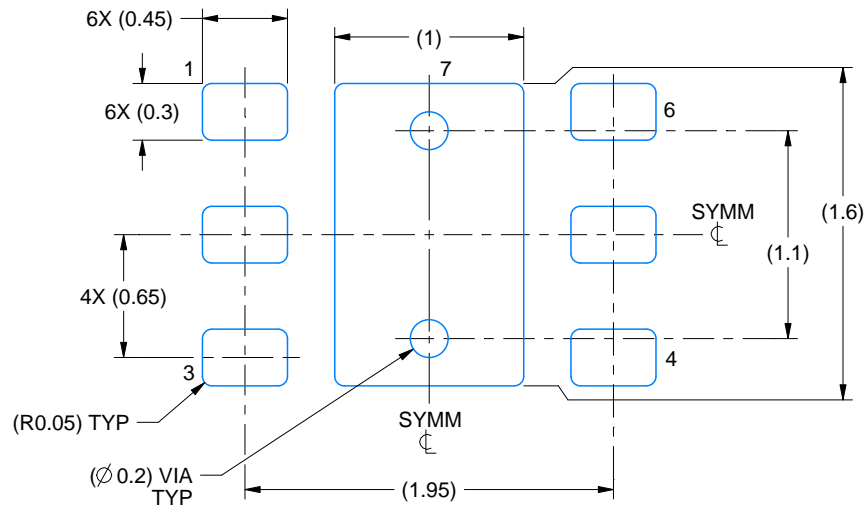
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DRV0006D

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



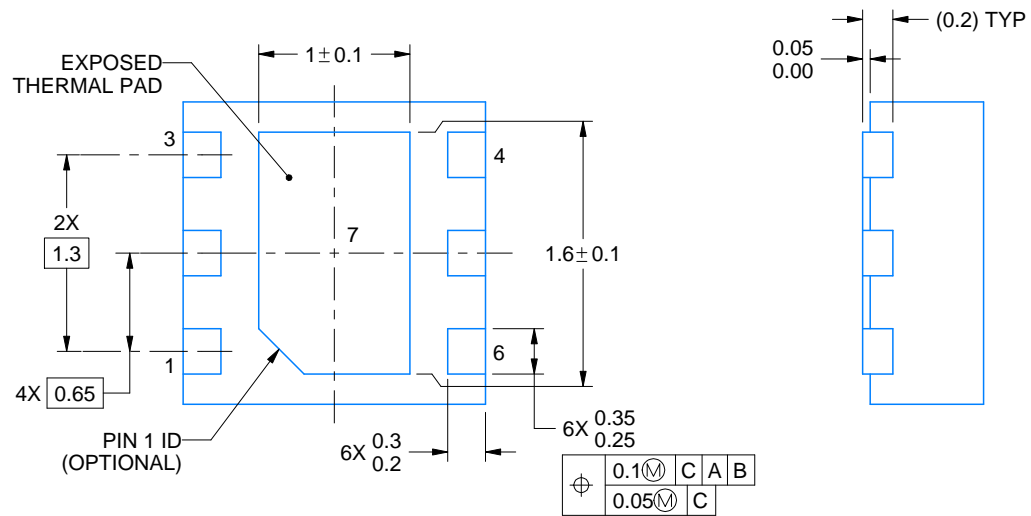
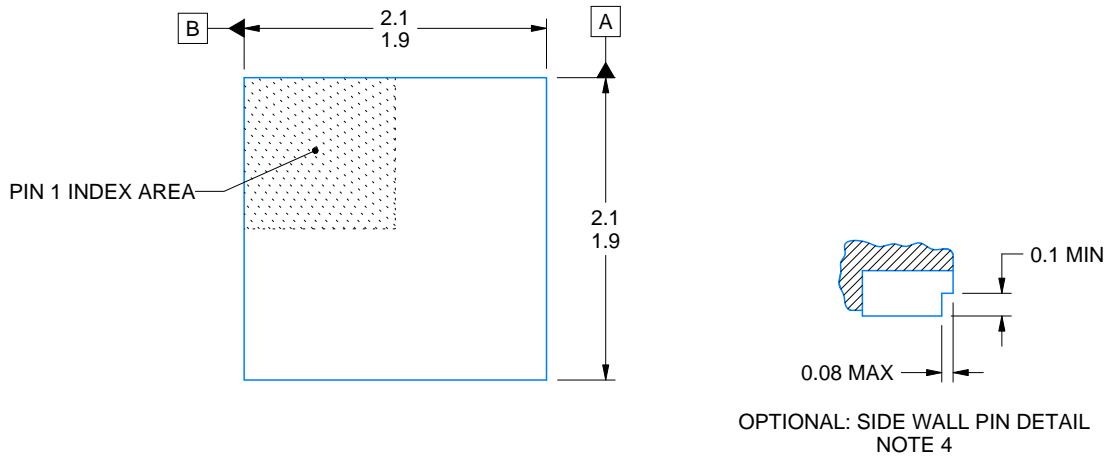
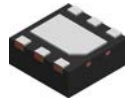
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4222173/C 11/2025

NOTES:

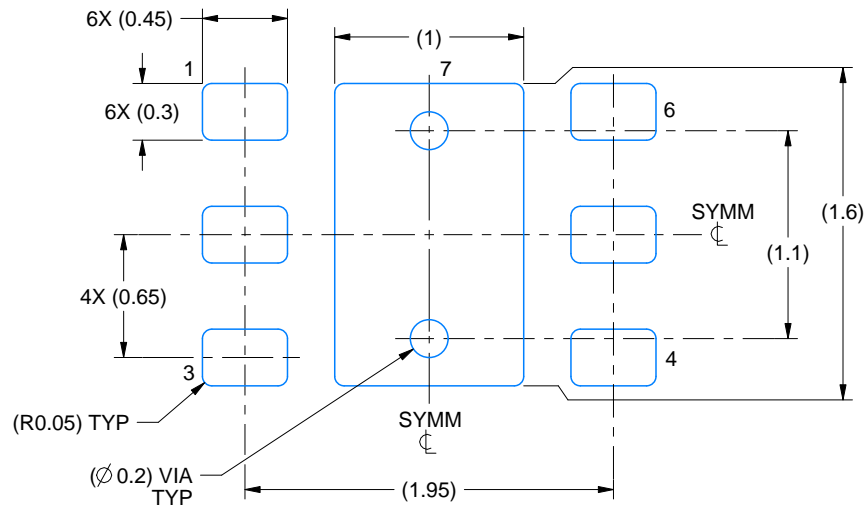
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

# EXAMPLE BOARD LAYOUT

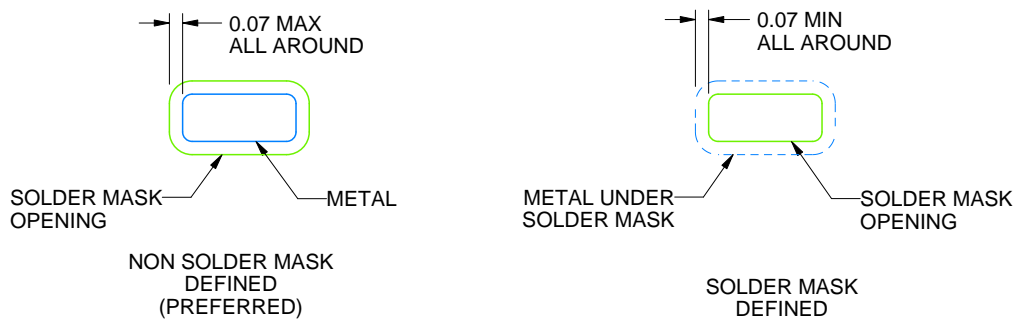
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

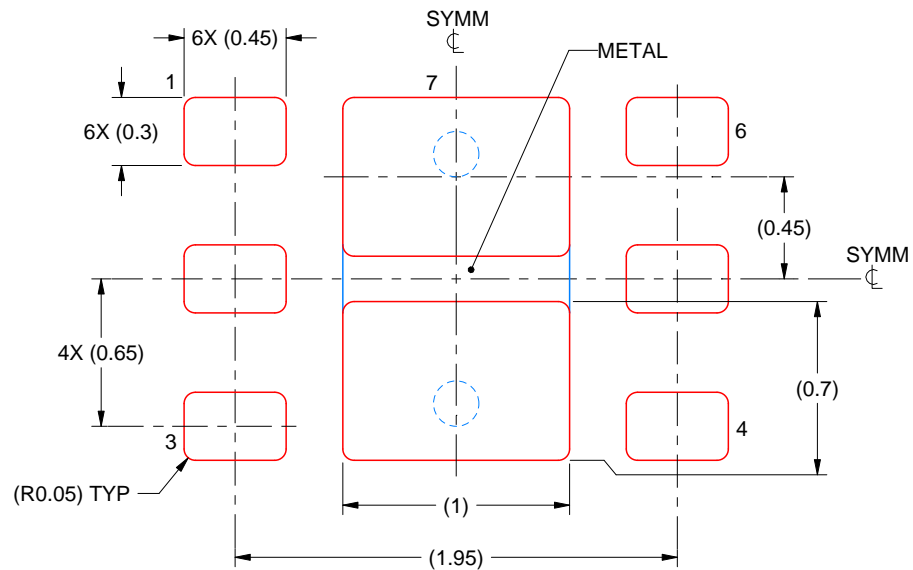
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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