TPS650842 PMIC for Intel™ Braswell Platform

1 Device Overview

1.1 Features

- Wide V_{IN} Range From 5.6 V to 21 V
- Three Variable-Output Voltage Synchronous Step-Down Controllers With D-CAP2™ Topology
  - Up to 7-A Output Current for BUCK1 (VCC) and BUCK6 (VDDQ), and 11 A for BUCK2 (VGG) Using External FETs
  - I^2C Dynamic Voltage Scaling (DVS) Control (0.5 V to 1.45 V in 10-mV Steps) for BUCK1 BUCK2, and BUCK3
  - Pin-Selectable Dual Output Voltages (1.2 V or 1.35 V) for BUCK6 (VDDQ)
- Three Variable-Output Voltage Synchronous Step-Down Converters With DCS-Control Topology
  - V_{IN} Range From 4.5 V to 5.5 V
  - Up to 3.5 A of Output Current for BUCK3 (VNN) With I^2C DVS Control (0.65 V to 1.45 V in 25-mV Steps)
  - Up to 3 A of Output Current for BUCK4 (V1P05A) and up to 1.5 A of Output Current for BUCK5 (V1P8A)
- Three LDO Regulators With Adjustable Output Voltage
  - LDOA1: I^2C-Selectable Output Voltage From 1.35 V to 3.3 V for up to 200 mA of Output Current
  - LDOA2: I^2C-Selectable Output Voltage From 1.05 V, 1.1 V, 1.15 V, and 1.2 V
  - LDOA3: I^2C-Selectable Output Voltage From 1.1 V, 1.15 V, 1.2 V, and 1.24 V
- VTT LDO for DDR Memory Termination
- Three Load Switches With Slew Rate Control
  - Up to 300 mA of Output Current With Voltage Drop Less Than 1.5% of Nominal Input Voltage
  - R_{DSON} < 96 mΩ at Input Voltage of 1.8 V
- I^2C Interface (Device Address 0x5E) Supports:
  - Standard Mode (100 kHz)
  - Fast Mode (400 kHz)
  - Fast Mode Plus (1 MHz)

1.2 Applications

- 2-, 3-, or 4-Series Cell Li-Ion Battery-Powered Products (NVDC or Non-NVDC)
- Wall-Powered Designs, Particularly From 12-V Supply
- Tablets, Ultrabook™, and Notebook Computers
- Mobile PCs and Mobile Internet Devices

1.3 Description

The TPS650842 device is a single-chip solution, power-management integrated chip (PMIC) designed specifically for the latest Intel™ processors targeted for tablets, ultrabooks, notebooks, industrial PCs, and Internet-of-Things (IOT) applications using 2S, 3S, or 4S Li-Ion battery packs (NVDC or non-NVDC power architectures), as well as wall-powered applications. The TPS650842 device is used for essential systems with low-voltage rails merged for the smallest footprint and lowest-cost system-power solution. The TPS650842 device provides the complete power solution based on the Intel Reference Designs. Six highly efficient step-down voltage regulators (VRs), a sink or source LDO (VTT), two LDOs, and three load switches are controlled by power-up sequence logic to provide the proper power rails, sequencing, and protection—including DDR3 and DDR4 memory power. The three regulators (BUCK–BUCK3) support dynamic voltage scaling (DVS) for maximum efficiency—including support for Connected Standby. The high-frequency VRs use small inductors and capacitors to achieve a small solution size. An I^2C interface allows simple control by an embedded controller (EC) or by a system on chip (SoC). The PMIC comes in an 8-mm × 8-mm single-row VQFN package with a thermal pad for good thermal dissipation and ease of board routing.

Use the following email address to request the full version of this data sheet: ipgmkt@list.ti.com.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS650842	VQFN (64)	8.00 mm × 8.00 mm

(1) For more information, see the *Mechanical Packaging and Orderable Information* section.

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1.4 Functional Block Diagram

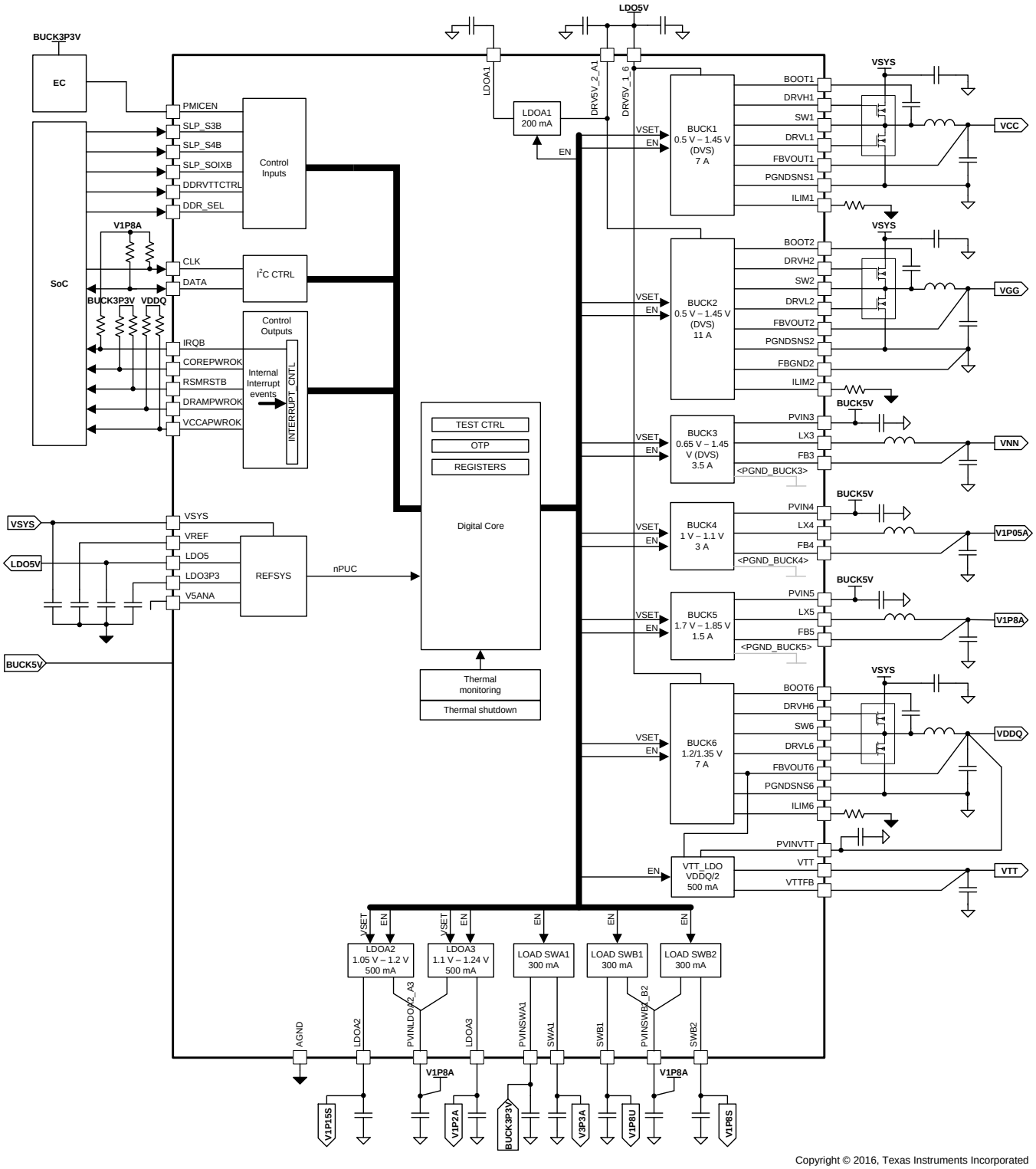

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Figure 1-1. PMIC Functional Block Diagram

2 Device and Documentation Support

2.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-ro-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

2.2 Trademarks

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2.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

2.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

3 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS650842A0RSKT	Active	Production	VQFN (RSK) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T650842A0 PG1.0

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Last updated 10/2025