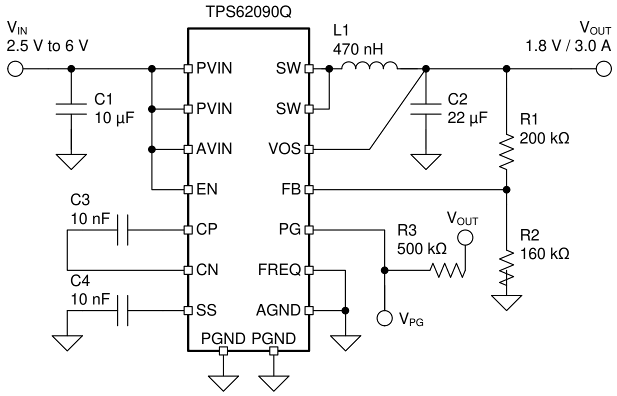
TPS62090-Q1 3A, High-Efficiency, Automotive, Synchronous Step-Down Converter With DCS-Control

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C junction operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C6
- 2.5V to 6V input voltage range
- DCS-Control
- 95% converter efficiency
- Power save mode
- 20μA operating quiescent current
- 100% duty cycle for lowest dropout
- 2.8MHz and 1.4MHz typical switching frequency
- 0.8V to V_{IN} adjustable output voltage
- Output discharge function
- Adjustable soft start
- Hiccup short-circuit protection
- Output voltage tracking
- Wide output capacitance selection
- Available in 3mm × 3mm, 16-pin QFN package
- New product available: TPS62813-Q1, 6V step-down converter in 2mm × 3mm QFN package with wettable flanks

2 Applications

- Automotive applications
- Distributed power supplies
- Processor supply
- Battery-powered applications



Typical Application

3 Description

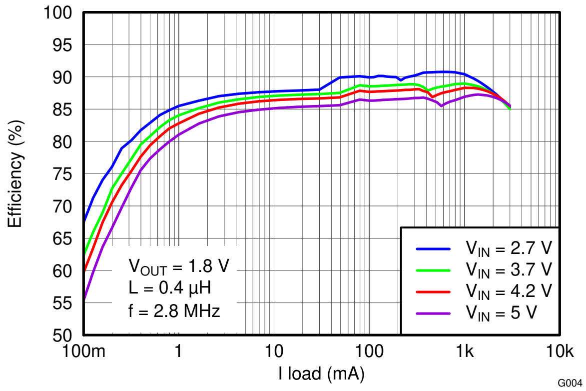
The TPS62090-Q1 devices are a family of high-frequency, synchronous, step-down converters optimized for small design size, high efficiency, and are designed for battery-powered applications. To maximize efficiency, the converters operate in pulse width modulation (PWM) mode with a nominal switching frequency of 2.8MHz to 1.4MHz and automatically enter power save mode operation at light load currents. When used in distributed power supplies and point-of-load regulation, the devices allow voltage tracking to other voltage rails and tolerate output capacitors ranging from 10μF up to 150μF and beyond. Using the DCS-Control topology, the devices achieve excellent load transient performance and accurate output voltage regulation.

The output voltage start-up ramp is controlled by the SS pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable and power good pins. In power save mode, the devices operate at typically 20μA quiescent current. Power save mode is entered automatically and seamlessly maintaining high efficiency over the entire load current range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS62090-Q1	RGT (QFN, 16)	3.00mm × 3.00mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency

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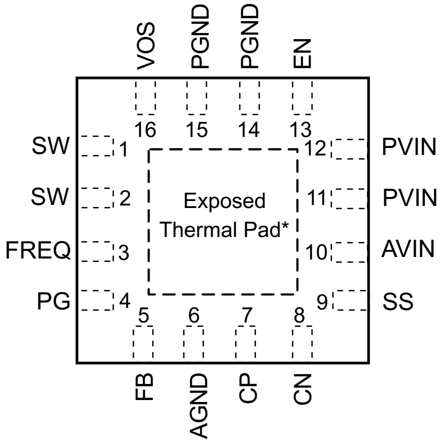
4 Pin Configuration and Functions



The exposed thermal pad is connected to AGND.

Figure 4-1. RGT Package 16-Pin QFN With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	6	—	Analog ground
AVIN	10	I	Bias supply input voltage pin
CN	8	I/O	Internal charge-pump flying capacitor. Connect a 10-nF capacitor between CP and CN.
CP	7	I/O	Internal charge-pump flying capacitor. Connect a 10-nF capacitor between CP and CN.
EN	13	I	Device enable. To enable the device this pin must be pulled high. Pulling this pin low disables the device. This pin has a pulldown resistor of typically 400 kΩ, which is active when EN is low.
Exposed Thermal Pad	—	—	The exposed thermal pad is connected to AGND. This pin must be soldered for mechanical reliability.
FB	5	I	Feedback pin of the device. For the adjustable version, connect a resistor divider to set the output voltage.
FREQ	3	I	This pin selects the switching frequency of the device. FREQ = Low sets the typical switching frequency to 2.8 MHz. FREQ = High sets the typical switching frequency to 1.4 MHz. This pin has an active pulldown resistor of typically 400 kΩ and can be left floating for 2.8-MHz operation.
PG	4	O	Power good open-drain output. This pin is high impedance if the output voltage is within regulation. This pin is pulled low if the output is below the nominal value. The pullup resistor can not be connected to any voltage higher than the input voltage of the device.
PGND	14, 15	—	Power ground connection
PVIN	11, 12	I	Power supply input voltage pin
SS	9	I	Soft-start control pin. A capacitor is connected to this pin and sets the soft-start time. Leaving this pin floating sets the minimum start-up time.
SW	1, 2	I/O	Switch pin of the power stage
VOS	16	I	Output voltage sense pin. This pin must be connected to the output voltage.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	PVIN, AVIN, FB, SS, EN, FREQ, VOS	–0.3	7	V
	SW, PG	–0.3	V_{IN} + 0.3	
	CN, CP	-0.3	V_{IN} + 7	
Power Good sink current, PG			1	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

For additional information, see *Section 7.1*.

		MIN	MAX	UNIT
V_{IN}	Input voltage	2.5	6	V
T_J	Operating junction temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS62090-Q1	UNIT
		RGT (QFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

V_{IN} = 3.6 V, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.5		6	V
I_{QIN}	Quiescent current	Not switching, FB = FB +5 %, Into PVIN and AVIN			20		μA
I_{sd}	Shutdown current	Into PVIN and AVIN			0.6	5	μA
UVLO	Undervoltage lockout threshold	V_{IN} falling		2.1	2.2	2.3	V
	Undervoltage lockout hysteresis				200		mV
	Thermal shutdown	Temperature rising			150		°C
	Thermal shutdown hysteresis				20		°C
CONTROL SIGNALS EN, FREQ							
V_H	High level input voltage	V_{IN} = 2.5 to 6 V		1	0.65		V
V_L	Low level input voltage	V_{IN} = 2.5 to 6 V			0.6	0.4	V
I_{lkg}	Input leakage current	EN, FREQ = GND or V_{IN}			10	100	nA
R_{PD}	Pulldown resistance				400		kΩ
SOFT START							
I_{SS}	Soft-start current			6.3	7.5	8.7	μA
POWER GOOD							
V_{th}	Power good threshold	Output voltage rising			95%		
		Output voltage falling			90%		
V_L	Low level voltage	$I_{(sink)}$ = 1 mA				0.4	V
I_{PG}	PG sinking current					1	mA
I_{lkg}	Leakage current	V_{PG} = 3.6 V			10	200	nA
POWER SWITCH							
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500 mA			50		mΩ
	Low-side FET on-resistance	I_{SW} = 500 mA			40		mΩ
I_{LIM}	High-side FET switch current limit			3.7	4.6	5.5	A
f_s	Switching frequency	FREQ = GND, I_{OUT} = 3 A			2.8		MHz
		FREQ = VIN, I_{OUT} = 3 A			1.4		MHz
OUTPUT							
V_s	Output voltage			0.8		V_{IN}	V
R_{od}	Output discharge resistor	EN = GND, V_{OUT} = 1.8 V			200		Ω
V_{FB}	Feedback regulation voltage				0.8		V
V_{FB}	Feedback voltage accuracy(1) (2)	$V_{IN} \geq V_{OUT}$ + 1 V	I_{OUT} = 1 A, PWM mode	–1.4%		1.4%	
			I_{OUT} = 0 mA, FREQ = 2.8 MHz, $V_{OUT} \geq$ 0.8 V, PFM mode	–1.4%		3%	
			I_{OUT} = 0 mA, FREQ = 1.4 MHz, $V_{OUT} \geq$ 1.2 V, PFM mode	–1.4%		3%	
			I_{OUT} = 0 mA, FREQ = 1.4 MHz, V_{OUT} < 1.2 V, PFM mode	–1.4%		3.7%	
I_{FB}	Feedback input bias current	V_{FB} = 0.8 V			10	100	nA
V_{OUT}	Output voltage accuracy(2)	$V_{IN} \geq V_{OUT}$ + 1 V, fixed output voltage, f = 2.8 MHz, L = 0.47 μH, C_{OUT} = 22 μF or f = 1.4 MHz, L = 1 μH, C_{OUT} = 22 μF	I_{OUT} = 1 A, PWM mode	–1.4%		1.4%	
			I_{OUT} = 0 mA, FREQ = high and low, PFM mode	–1.4%		2.5%	
	Line regulation	V_{OUT} = 1.8 V, PWM operation			0.016%		V
	Load regulation	V_{OUT} = 1.8 V, PWM operation			0.04%		A

(1) For output voltages < 1.2 V, use a 2 × 22 μF output capacitance to achieve 3% output voltage accuracy.
(2) For more information, see *Section 6.4.2*.

5.6 Typical Characteristics

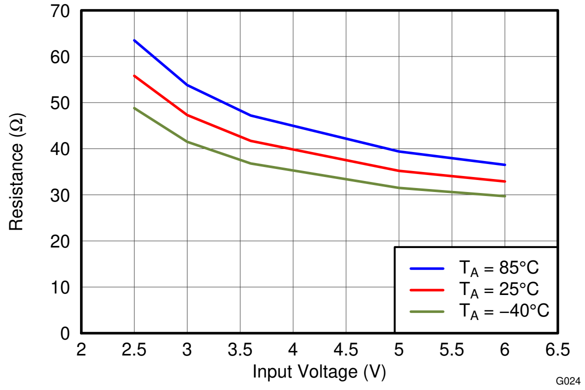


Figure 5-1. High-Side FET ON-Resistance vs Input Voltage

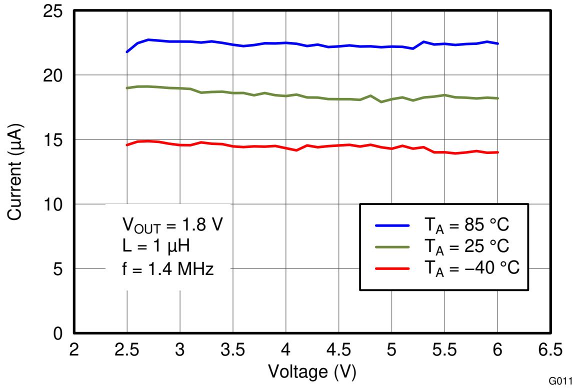
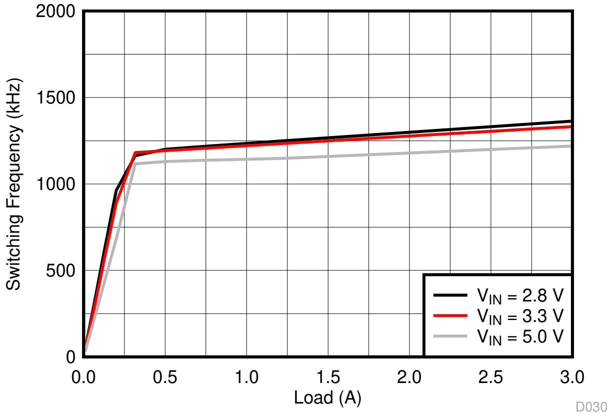
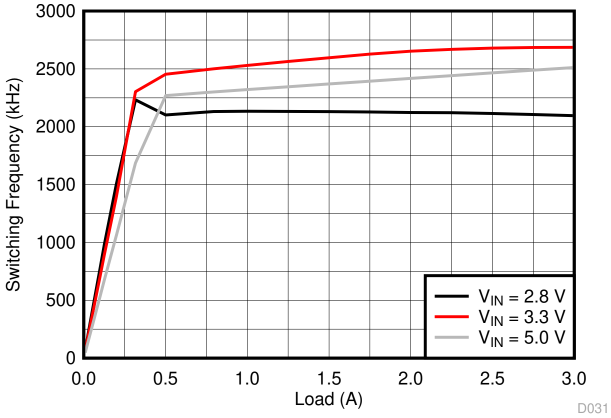


Figure 5-2. Quiescent Current vs Input Voltage



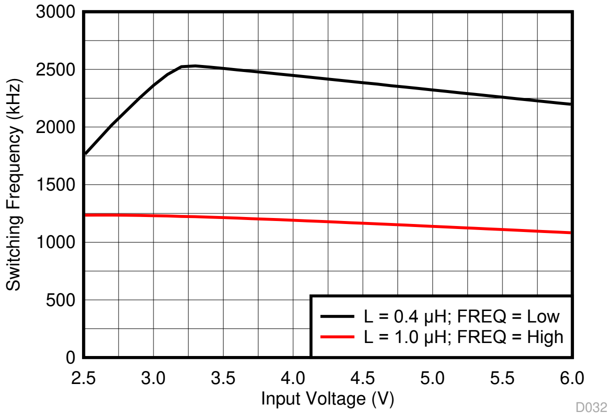
V_{OUT} = 1 V L = 1 µH FREQ = High

Figure 5-3. Switching Frequency vs Load Current



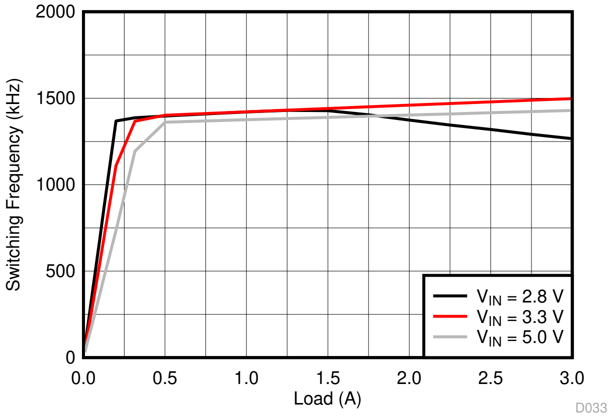
V_{OUT} = 1 V L = 0.4 µH FREQ = Low

Figure 5-4. Switching Frequency vs Load Current



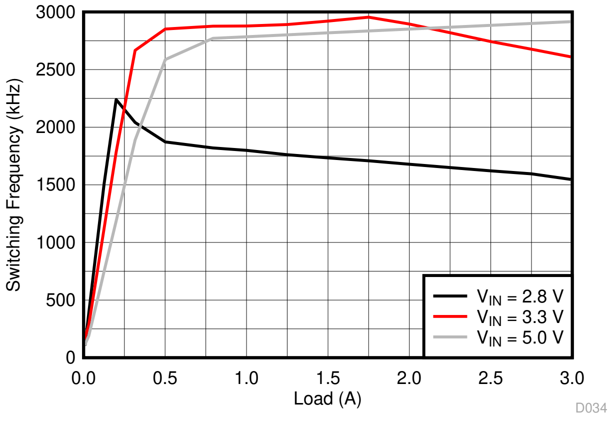
V_{OUT} = 1 V I_{OUT} = 1 A

Figure 5-5. Frequency vs Input Voltage



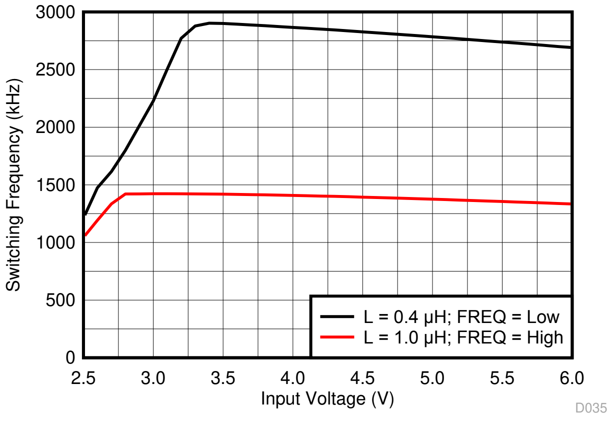
V_{OUT} = 1.8 V L = 1 µH FREQ = High

Figure 5-6. Frequency vs Load Current



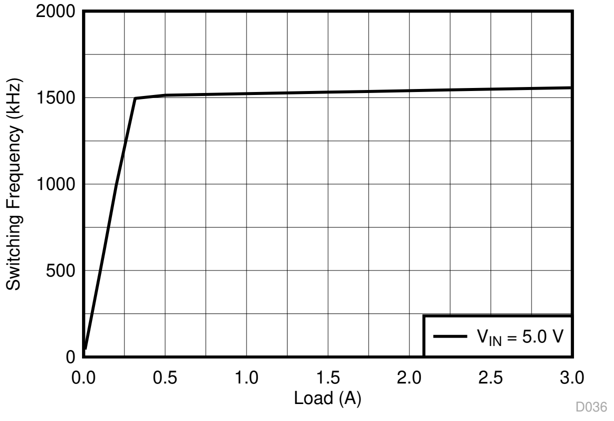
V_{OUT} = 1.8 V L = 0.4 µH FREQ = Low

Figure 5-7. Frequency vs Load Current



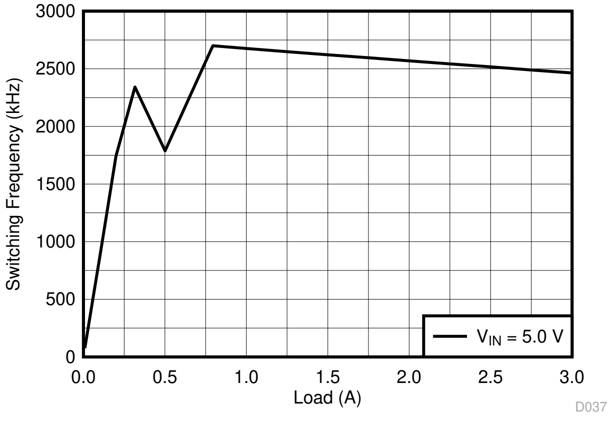
V_{OUT} = 1.8 V I_{OUT} = 1 A

Figure 5-8. Frequency vs Input Voltage



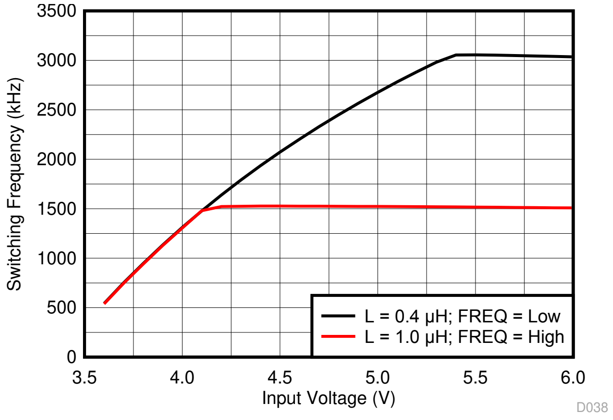
V_{OUT} = 3.3 V L = 1 µH FREQ = High

Figure 5-9. Frequency vs Load Current



V_{OUT} = 3.3 V L = 0.4 µH FREQ = Low

Figure 5-10. Frequency vs Load Current



V_{OUT} = 3.3 V I_{OUT} = 1 A

Figure 5-11. Frequency vs Input Voltage

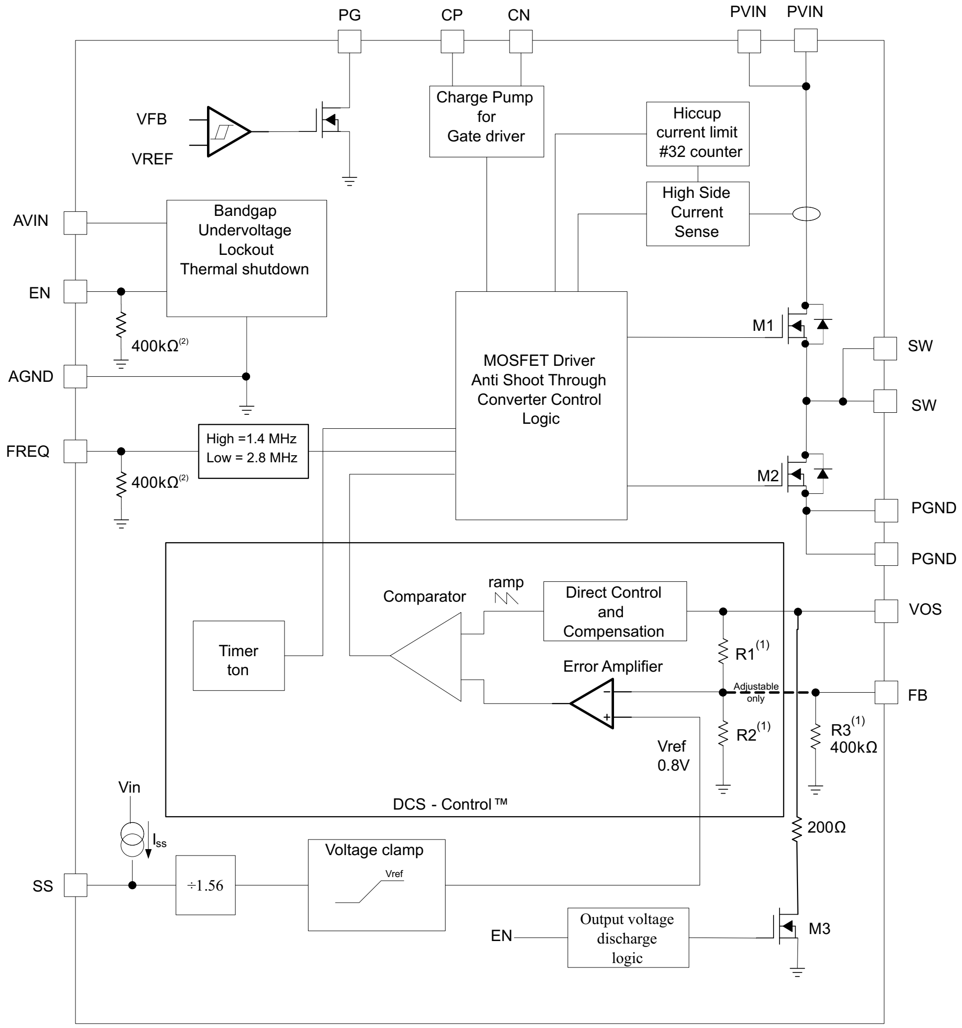
6 Detailed Description

6.1 Overview

The TPS62090Q synchronous switched mode converter is based on DCS-Control (Direct Control with Seamless transition into power save mode). DCS-Control is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control topology operates in Pulse Width Modulation (PWM) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM, the converter operates with nominal switching frequency of 2.8 MHz or 1.4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes (PWM and PFM) using a single building block with a seamless transition from PWM to power save mode without effecting the output voltage. The TPS62090Q device offers excellent DC-voltage regulation and load transient regulation, combined with low output voltage ripple, to minimize interference with RF circuits.

6.2 Functional Block Diagram



(2) The resistors are disconnected when the pins are high.

6.3 Feature Description

6.3.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 0.6 µA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 200 Ω discharges the output through the VOS pin smoothly. An internal pulldown resistor of 400 kΩ is connected to the EN pin when the EN pin is low. The pulldown resistor is disconnected when the EN pin is high.

6.3.2 Soft Start (SS) and Hiccup Current Limit During Start-Up

To minimize inrush current during start-up, the device has an adjustable soft start depending on the capacitor value connected to the SS pin. The device charges the soft-start capacitor with a constant current of typically 7.5 µA. The feedback voltage follows this voltage with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The soft-start operation is complete when the voltage at the soft-start capacitor has reached typically 1.25 V. The soft-start time is calculated using Equation 1. The larger the soft-start capacitor, the longer the soft-start time. The relation between soft-start voltage and feedback voltage is estimated using Equation 2.

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \tag{1}$$

$$V_{FB} = \frac{V_{SS}}{1.56} \tag{2}$$

During start-up, the switch current limit is reduced to 1/3 (approximately 1.5 A) of the typical current limit of 4.6 A. After the output voltage exceeds typically 0.6 V, the current limit is released to the nominal value. The device provides a reduced load current of approximately 1.5 A when the output voltage is below typically 0.6 V. Due to this, a small or no soft-start time can trigger the short-circuit protection during start-up especially for larger output capacitors. This is avoided by using a larger soft-start capacitance to extend the soft-start time. See *Section 6.3.4* for details of the reduced current limit during start-up. Leaving the soft-start pin floating sets the minimum start-up time (around 50 µs).

6.3.3 Voltage Tracking (SS)

The SS pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in Figure 6-1. The internal reference voltage follows the voltage at the SS pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in Figure 6-2.

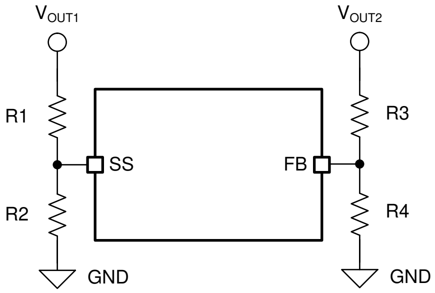
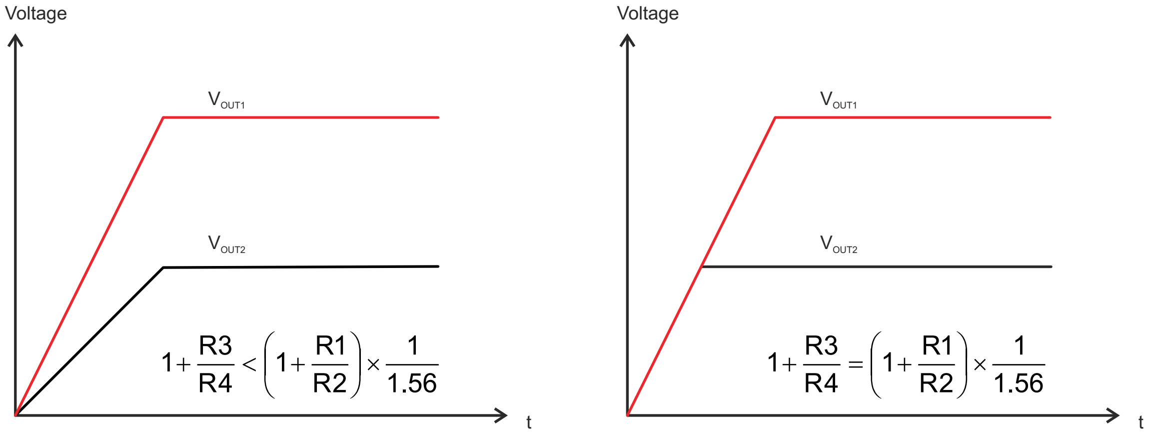


Figure 6-1. Output Voltage Tracking



a) Ratiometric Tracking

b) Coincidental Tracking

Figure 6-2. Voltage Tracking Options

The R2 value must be set properly to achieve accurate voltage tracking by taking 7.5-µA soft start-up current into account. 1 kΩ or smaller is a sufficient value for R2.

For decreasing the SS pin voltage, the device does not sink current from the output when the device is in power save mode. So the resulting decreases of the output voltage can be slower than the SS pin voltage if the load is light. When driving the SS pin with an external voltage, do not exceed the voltage rating of the SS pin which is 7 V.

6.3.4 Short-Circuit Protection (Hiccup Mode)

The device is protected against hard short circuits to GND and overcurrent events. This protection is implemented by a two-level short-circuit protection. During start-up and when the output is shorted to GND, the switch current limit is reduced to 1/3 of the typical current limit of 4.6 A. When the output voltage exceeds typically 0.6 V, the current limit is released to the nominal value. The full current limit is implemented as a hiccup current limit. After the internal current limits are triggered 32 times, the device stops switching and starts a new start-up sequence after a typical delay time of 66 µS passed by. The device continues in this cycle until the high current condition is released.

6.3.5 Output Discharge Function

To make sure the device starts up under the defined conditions, the output discharges through the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This discharge happens when the device is disabled or if thermal shutdown, undervoltage lockout or short-circuit hiccup mode is triggered.

6.3.6 Power Good Output (PG)

The power good output is low when the output voltage is below the nominal value. The power good becomes high impedance after the output is within 5% of regulation. The PG pin is an open-drain output and is specified to typically sink up to 1 mA. This output requires a pullup resistor to be monitored properly. The pullup resistor cannot be connected to any voltage higher than the input voltage of the device. The PG output is low when the device is disabled, in thermal shutdown, or in UVLO. The PG output can be left floating if unused.

6.3.7 Frequency Set Pin (FREQ)

The FREQ pin is a digital logic input which sets the nominal switching frequency. Pulling this pin to GND sets the nominal switching frequency to 2.8 MHz and pulling this pin high sets the nominal switching frequency to 1.4 MHz. Because this pin changes the switching frequency, it also changes the on-time during PFM mode. At 1.4 MHz the on-time is twice the on-time as operating at 2.8 MHz. This pin has an active pulldown resistor of typically 400 kΩ. For applications where efficiency is of highest importance, a lower switching frequency must be selected. A higher switching frequency allows the use of smaller external components, faster load transient response, and lower output voltage ripple when using same L-C values.

6.3.8 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200-mV hysteresis.

6.3.9 Thermal Shutdown

The device enters thermal shutdown after the junction temperature exceeds typically 150°C with a 20°C hysteresis.

6.3.10 Charge Pump (CP, CN)

The CP and CN pins must attach to an external 10-nF capacitor to complete a charge pump for the gate driver. This capacitor must be rated for the input voltage. TI does not recommend connecting any other circuits to the CP or CN pins.

6.4 Device Functional Modes

6.4.1 Pulse Width Modulation Operation

At medium to heavy load currents, the device operates with PWM at a nominal switching frequency of 2.8 MHz or 1.4 MHz depending on the setting of the FREQ pin. As the load current decreases, the converter enters the power save mode operation reducing the switching frequency. The device enters power save mode at the boundary to discontinuous conduction mode (DCM).

6.4.2 Power Save Mode Operation

As the load current decreases, the converter enters power save mode operation. During power save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current while maintaining high efficiency. The power save mode is based on a fixed on-time architecture following Equation 3. When operating at 1.4 MHz, the on-time is twice as long as the on-time for 2.8-MHz operation, resulting in larger output voltage ripple, as shown in Figure 7-11 and Figure 7-12, and slightly higher output voltage at no load, as shown in Figure 7-8 and Figure 7-9. To have the same output voltage ripple at 1.4 MHz during PFM mode, either the output capacitor or the inductor value must be increased. As an example, operating at 2.8 MHz using 0.47-μH inductor gives the same output voltage ripple as operating with 1.4 MHz using 1-μH inductor.

$$ton_{2.8MHz} = \frac{V_{OUT}}{V_{IN}} \times 360ns$$

$$ton_{1.4MHz} = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{ton^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}}\right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (3)$$

In power save mode the output voltage rises slightly above the nominal output voltage in PWM mode, as shown in Figure 7-8 and Figure 7-9. This effect is reduced by increasing the output capacitance or the inductor value. This effect is also reduced by programming the output voltage of the TPS62090Q lower than the target value. As an example, if the target output voltage is 3.3 V, then the TPS62090Q is programmed to 3.3 V – 0.8%. As a result the output voltage accuracy is now –2.2% to +2.2% instead of –1.4% to 3%. The output voltage accuracy in PFM operation is reflected in the *Section 5.5* table and given for a 22-μF output capacitance.

6.4.3 Low-Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high-side MOSFET switch is constantly turned on which is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below the nominal regulation value is given by Equation 4.

$$V_{IN\,(min)} = V_{OUT} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (4)$$

Where

- $R_{DS(on)}$ = High side FET on-resistance
- R_L = DC resistance of the inductor

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS62090-Q1 device is a high-frequency, synchronous, step-down converter optimized for small solution size, high efficiency, and is suitable for battery-powered applications.

7.2 Typical Application

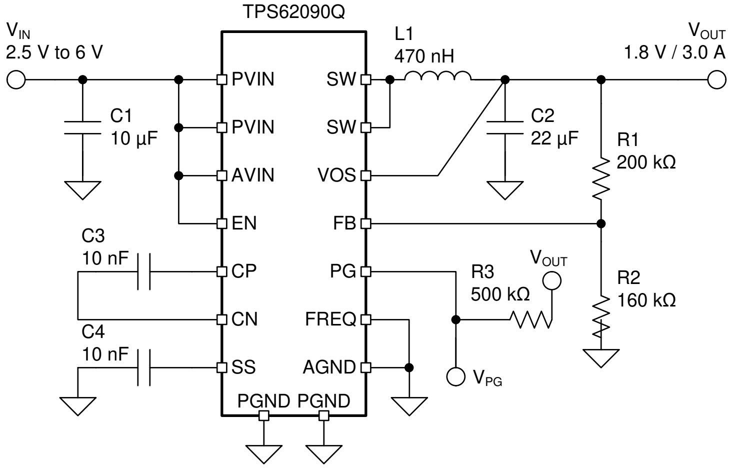


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Figure 7-1. Test Circuit

7.2.1 Design Requirements

Table 7-1 is a recommended list of components for the test circuit in Figure 7-1.

Table 7-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
TPS62090Q	High efficiency step-down converter	Texas Instruments
L1	Inductor: 1 µH, 0.47 µH, 0.4 µH	Coilcraft XFL4020-102, XAL4020-401, TOKO DEF252012-R47
C1	Ceramic capacitor: 10 µF, 22 µF	(6.3-V, X5R, 0603), (6.3-V, X5R, 0805)
C2	Ceramic capacitor: 22 µF	(6.3-V, X5R, 0805)
C3, C4	Ceramic capacitor	Standard
R1, R2, R3	Resistor	Standard

7.2.2 Detailed Design Procedure

The first step in the design procedure is the selection of the output filter components. To simplify this process, Table 7-2 and Table 7-3 list possible inductor and capacitor value combinations.

Table 7-2. Output Filter Selection (2.8-MHz Operation, FREQ = GND)

INDUCTOR VALUE (µH)(3)	OUTPUT CAPACITOR VALUE (µF)(2)				
	10	**22**	**47**	**100**	**150**
0.47	—	√(1)	√	√	√
1	√	√	√	√	√
2.2	—	—	—	—	—
3.3	—	—	—	—	—

(1) Typical application configuration. Other check marks indicate alternative filter combinations.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
(3) Inductor tolerance and current de-rating is anticipated. The effective inductance varies by +20% and –30%.

Table 7-3. Output Filter Selection (1.4-MHz Operation, FREQ = V_{IN})

INDUCTOR VALUE (µH)(3)	OUTPUT CAPACITOR VALUE (µF)(2)				
	10	**22**	**47**	**100**	**150**
0.47	—	√	√	√	√
1	√	√(1)	√	√	√
2.2	√	√	√	√	√
3.3	—	—	—	—	—

(1) Typical application configuration. Other check marks indicate alternative filter combinations.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
(3) Inductor tolerance and current de-rating is anticipated. The effective inductance varies by +20% and –30%.

7.2.2.1 Inductor Selection

The inductor selection is affected by several parameters such as inductor-ripple current, output-voltage ripple, transition point into power save mode, and efficiency. See Table 7-4 for typical inductors.

Table 7-4. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (L × W × H mm)	Isat / DCR
0.6 µH	Coilcraft XAL4012-601	4 × 4 × 2.1	7.1 A / 9.5 mΩ
1 µH	Coilcraft XAL4020-102	4 × 4 × 2.1	5.9 A / 13.2 mΩ
1 µH	Coilcraft XFL4020-102	4 × 4 × 2.1	5.1 A / 10.8 mΩ
0.47 µH	TOKO DFE252012 R47	2.5 × 2 × 1.2	3.7 A / 39 mΩ
1 µH	TOKO DFE252012 1R0	2.5 × 2 × 1.2	3.0 A / 59 mΩ
0.68 µH	TOKO DFE322512 R68	3.2 × 2.5 × 1.2	3.5 A / 37 mΩ
1 µH	TOKO DFE322512 1R0	3.2 × 2.5 × 1.2	3.1 A / 45 mΩ

In addition, the inductor must be rated for the appropriate saturation current and DC resistance (DCR). The inductor must be rated for a saturation current as high as the typical switch current limit, of 4.6 A or according to Equation 5 and Equation 6. Equation 5 and Equation 6 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency is taken from the *Section 5.6* graphs or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$I_L = I_{OUT} + \frac{\Delta I_L}{2} \tag{5}$$

$$I_L = I_{OUT} + \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{2 \times f \times L} \tag{6}$$

where

- f = Converter switching frequency (typical 2.8 MHz or 1.4 MHz)
- L = Selected inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an conservative assumption)

Note

The calculation must be done for the maximum input voltage of the application

---

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% must be added to cover for load transients during operation.

7.2.2.2 Input and Output Capacitor Selection

For best output and input voltage filtering, low-ESR (X5R or X7R) ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-μF or larger input capacitor is recommended when FREQ = Low and a 22-μF or larger when FREQ = High.

The output capacitor value can range from 10 μF up to 150 μF and beyond. Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values. The recommended typical output capacitor value is 22 μF (nominal) and can vary over a wide range as outline in the output filter selection table. For output voltages above 1.8 V, noise can cause duty cycle jitter. This does not degrade device performance. Using an output capacitor of 2 × 22 μF (nominal) for output voltages >1.8 V avoids duty cycle jitter.

Ceramic capacitor have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating.

7.2.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation 7, Equation 8, and Equation 9.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \tag{7}$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8\ V}{5\ \mu A} \approx 160\ k\Omega \tag{8}$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \tag{9}$$

When sizing R2, use a minimum of 5 μA for the feedback current (I_{FB}) to achieve low quiescent current and acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. A feed-forward capacitor is not required for proper operation.

7.2.3 Application Curves

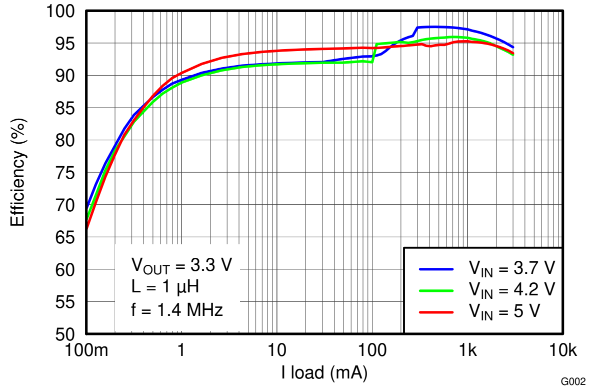


Figure 7-2. Efficiency vs Load Current

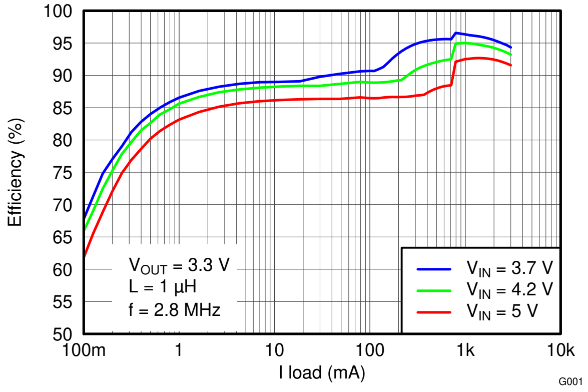


Figure 7-3. Efficiency vs Load Current

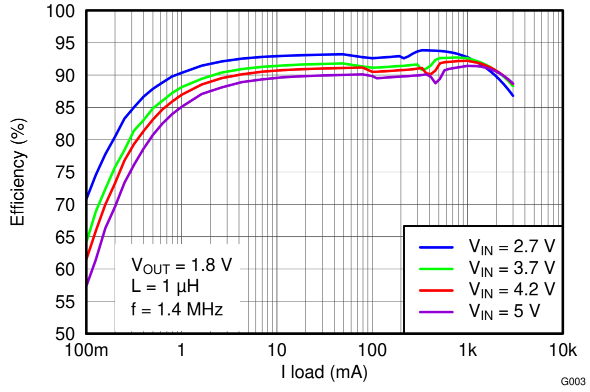


Figure 7-4. Efficiency vs Load Current

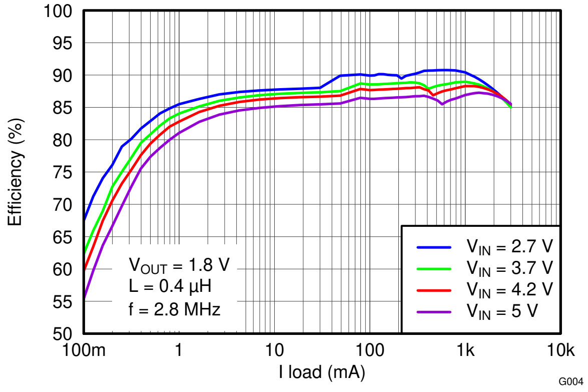


Figure 7-5. Efficiency vs Load Current

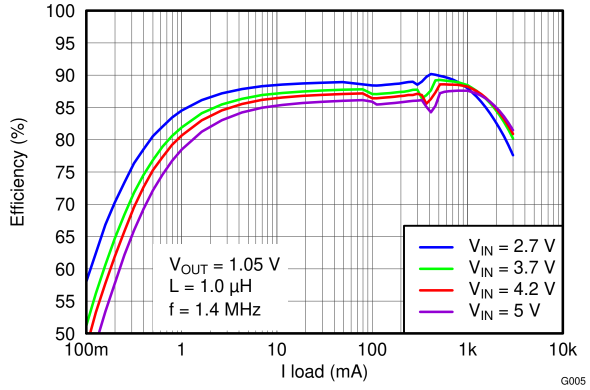


Figure 7-6. Efficiency vs Load Current

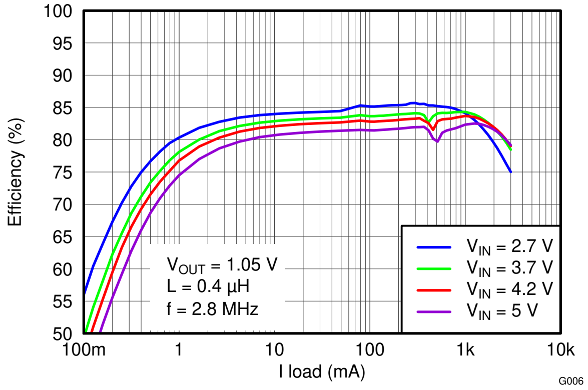


Figure 7-7. Efficiency vs Load Current

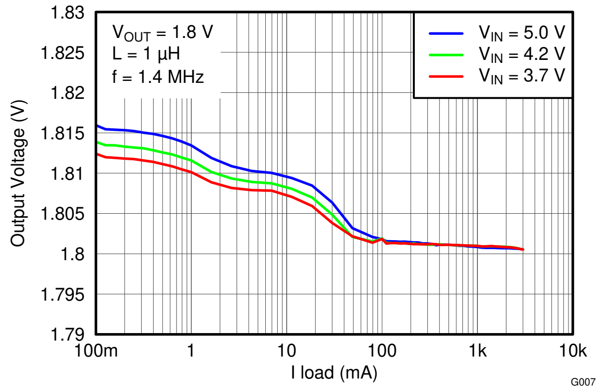


Figure 7-8. Output Voltage vs Load Current

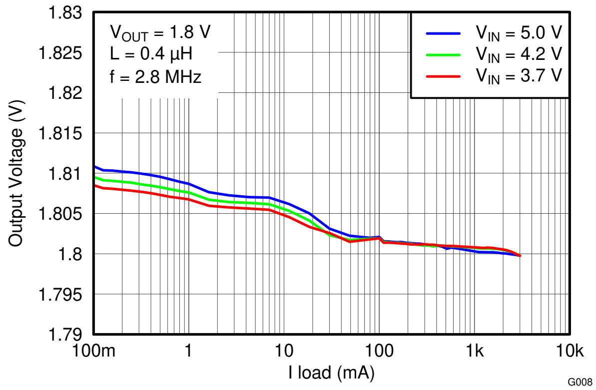


Figure 7-9. Output Voltage vs Load Current

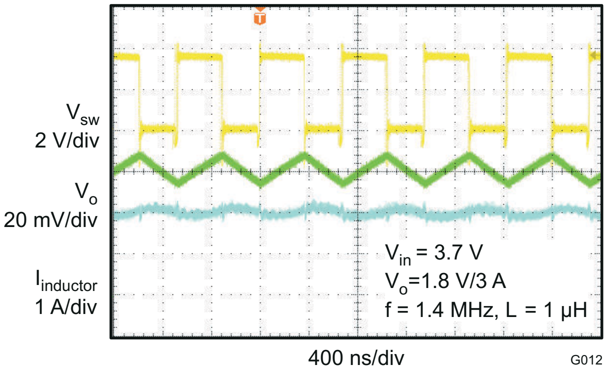


Figure 7-10. PWM Operation

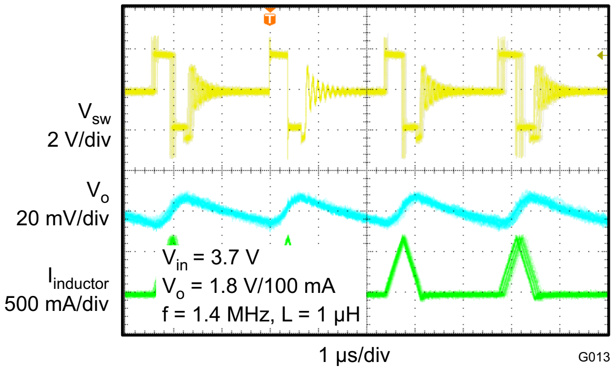


Figure 7-11. PFM Operation

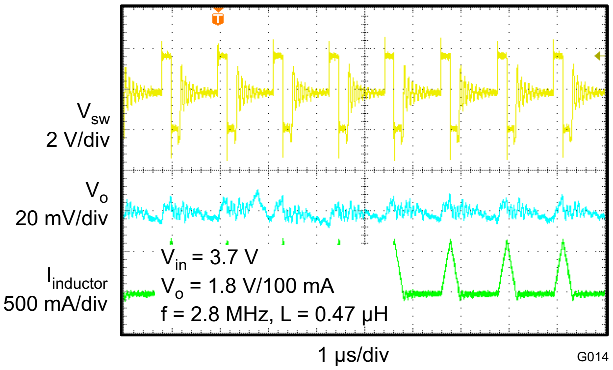


Figure 7-12. PFM Operation

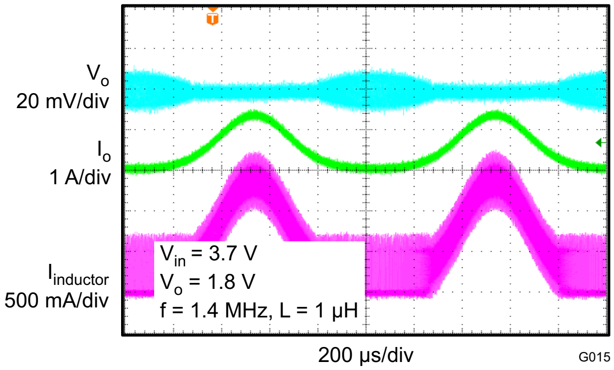


Figure 7-13. Load Sweep

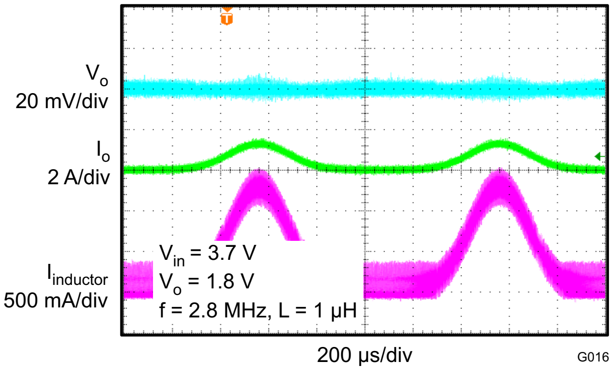
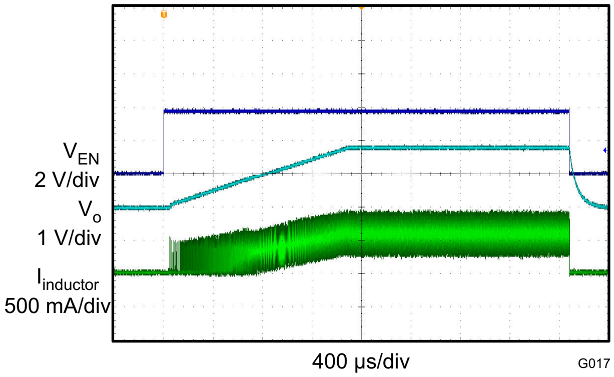
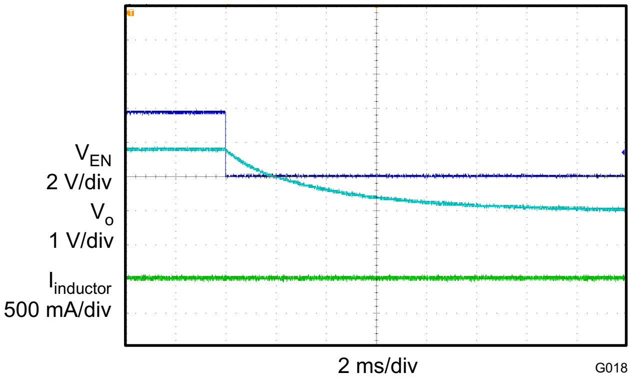


Figure 7-14. Load Sweep



V_O = 1.8 V / 600 mA f = 2.8 MHz / L = 1 µH C_{SS} = 10 nF

Figure 7-15. Start-Up



V_O = 1.8 V / No Load f = 1.4 MHz / L = 1 µH

Figure 7-16. Shutdown

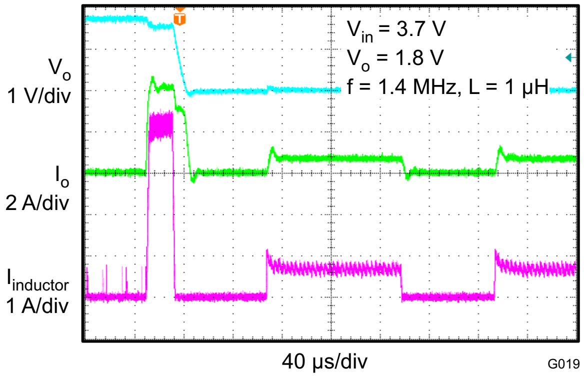


Figure 7-17. Hiccup Short-Circuit Protection

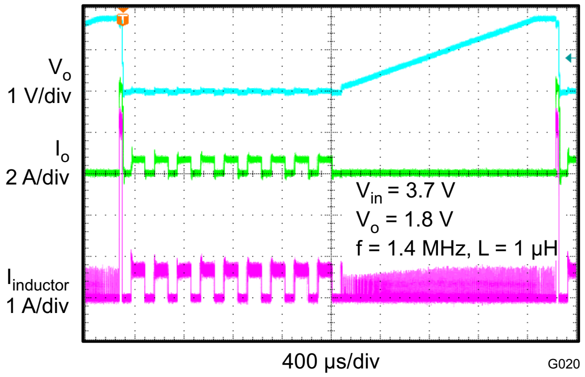


Figure 7-18. Hiccup Short-Circuit Protection

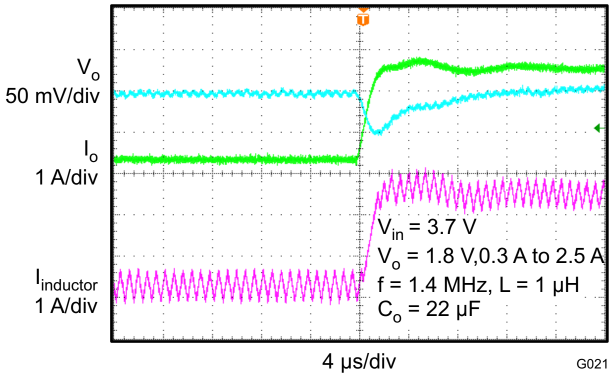


Figure 7-19. Load Transient Response

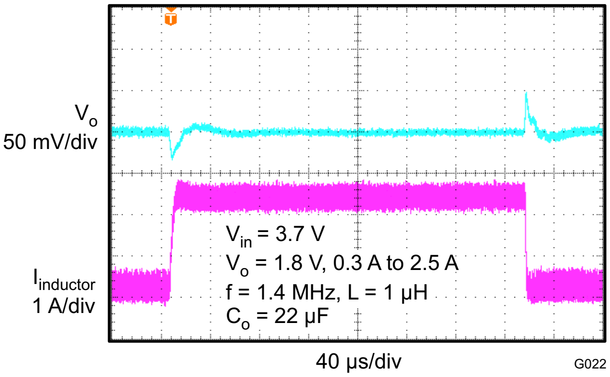


Figure 7-20. Load Transient Response

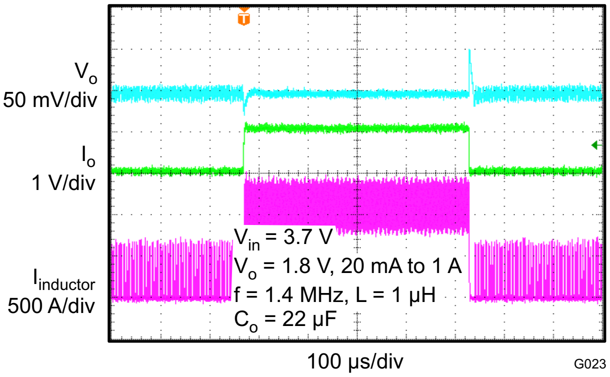


Figure 7-21. Load Transient Response

7.3 System Examples

Figure 7-22, Figure 7-23, and Figure 7-24 show additional circuits for varying voltage options.

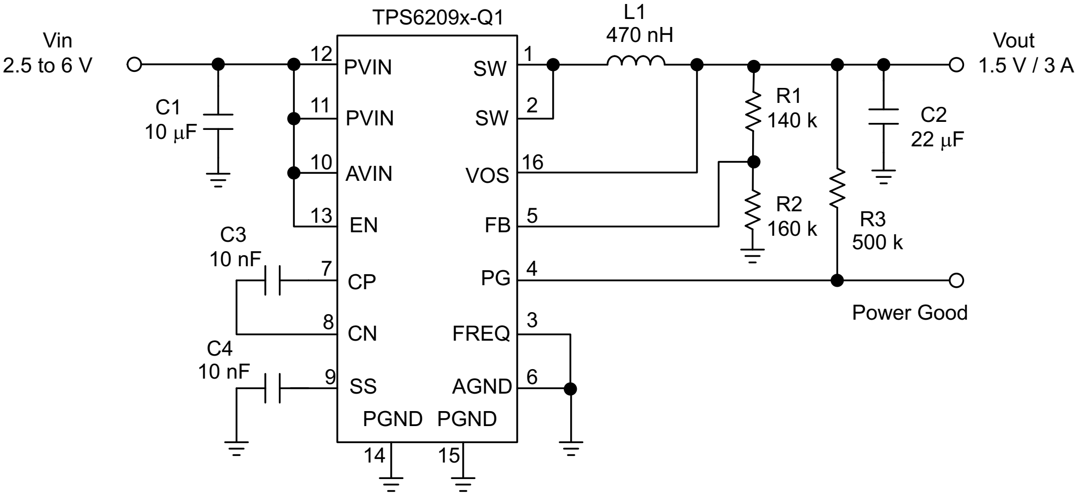


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Figure 7-22. 1.5-V Adjustable Version Operating at 2.8 MHz

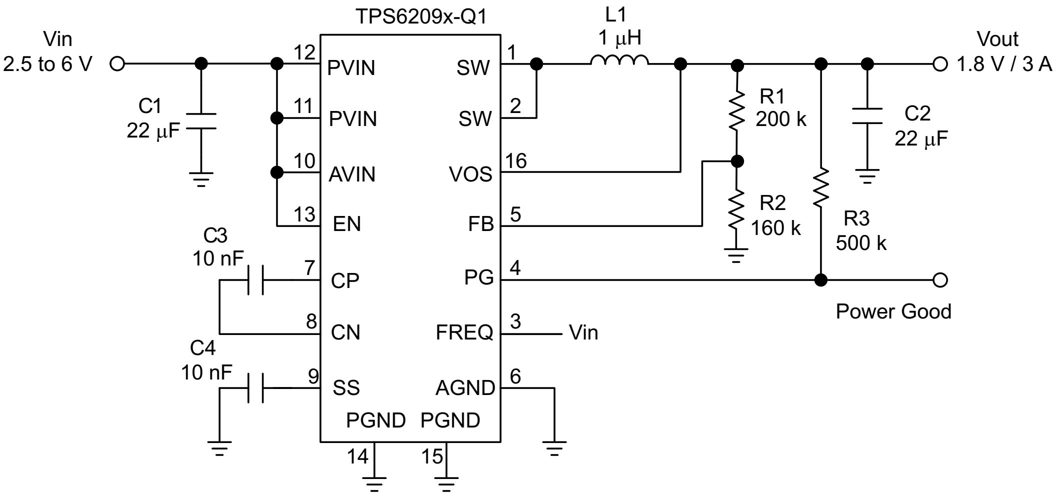

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Figure 7-23. 1.8-V Adjustable Version Operating at 1.4 MHz

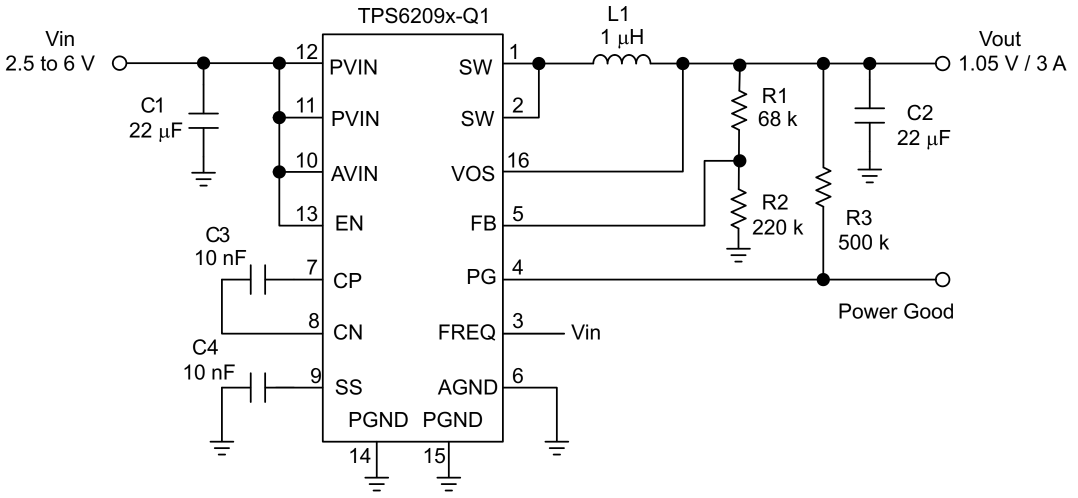

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Figure 7-24. 1.05-V Adjustable Version Operating at 1.4 MHz

7.4 Power Supply Recommendations

The power supply to the TPS62090-Q1 device must have a current rating according to the supply voltage, output voltage, and output current of the TPS62090-Q1 device.

7.5 Layout

7.5.1 Layout Guidelines

- TI recommends placing the input capacitor as close as possible to the IC pins PVIN and PGND.
- The VOS connection is noise sensitive and needs to be routed as short and directly to the output pin of the inductor.
- The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) must have a single joint connection at the exposed thermal pad of the package. This minimizes switch node jitter.
- The charge pump capacitor connected to CP and CN must be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits.
- Refer to the *TPS62090EVM-063 Evaluation Module* (SLVU670) for an example of component placement, routing, and thermal design.

7.5.2 Layout Example

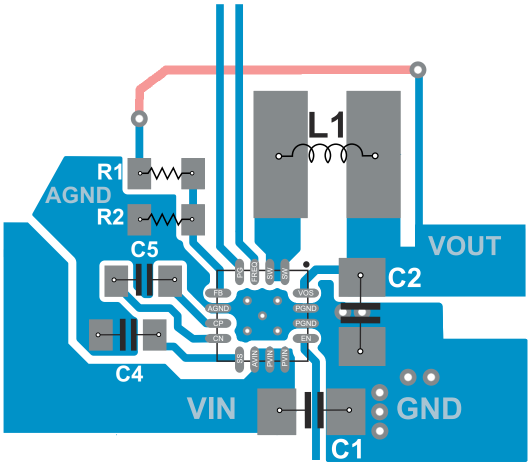

Figure 7-25. TPS62090Q Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage* application note
- Texas Instruments, *Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs* application note
- Texas Instruments, *How to Measure the Control Loop of DCS-Control™ Devices* application note
- Texas Instruments, *Optimizing the TPS62090 Output Filter* application note
- Texas Instruments, *Performing Accurate PFM Mode Efficiency Measurements* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note
- Texas Instruments, *TPS62090EVM-063 Evaluation Module* application note
- Texas Instruments, *Understanding the Absolute Maximum Ratings of the SW Node* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2021) to Revision D (June 2025)	Page
• Updated trademark information throughout the data sheet	1
• Updated the document title	1
• Added *Pin Configuration and Functions* to the data sheet	3

Changes from Revision B (December 2016) to Revision C (November 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Added link to the TPS62813-Q1	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62090QRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJG
TPS62090QRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJG

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62090-Q1 :

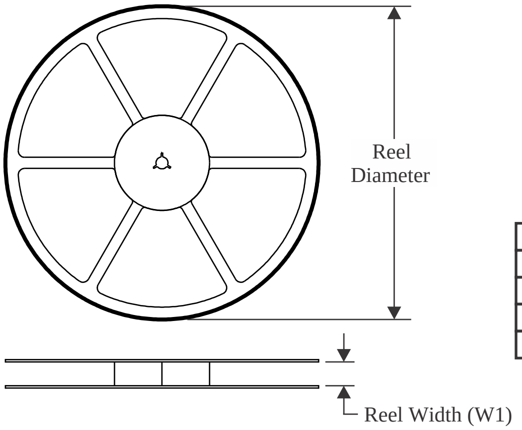
- Catalog : TPS62090

NOTE: Qualified Version Definitions:

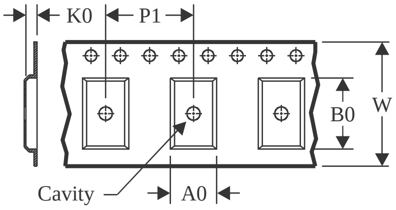
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

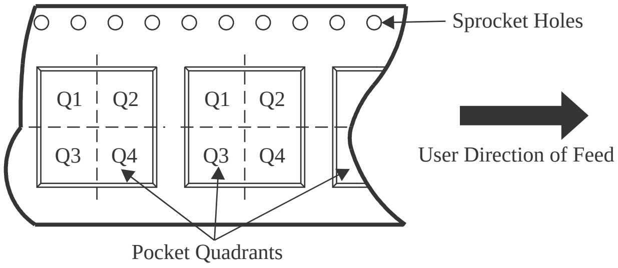


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

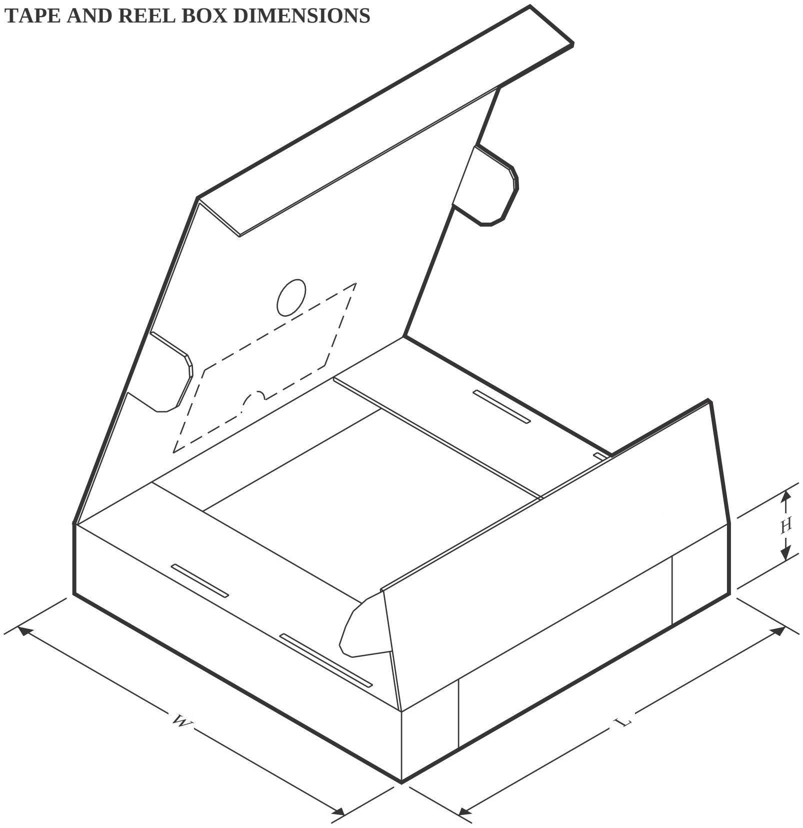
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62090QRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



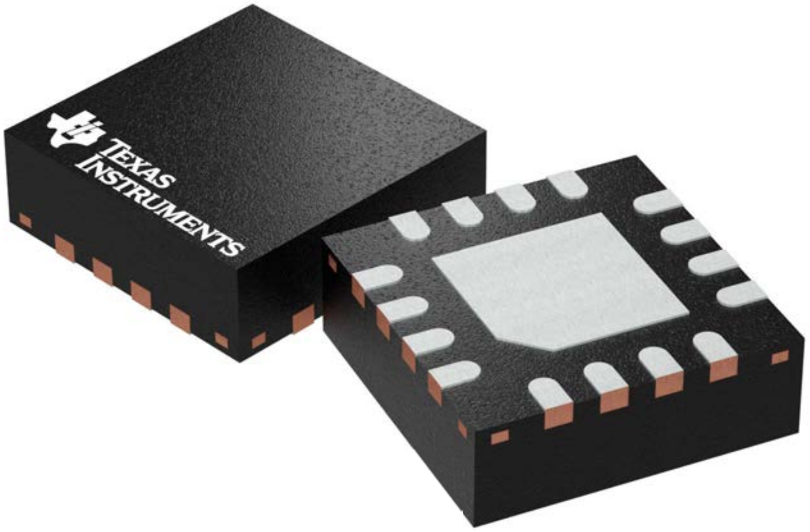
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62090QRGTRQ1	VQFN	RGT	16	3000	346.0	346.0	33.0

GENERIC PACKAGE VIEW

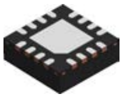
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

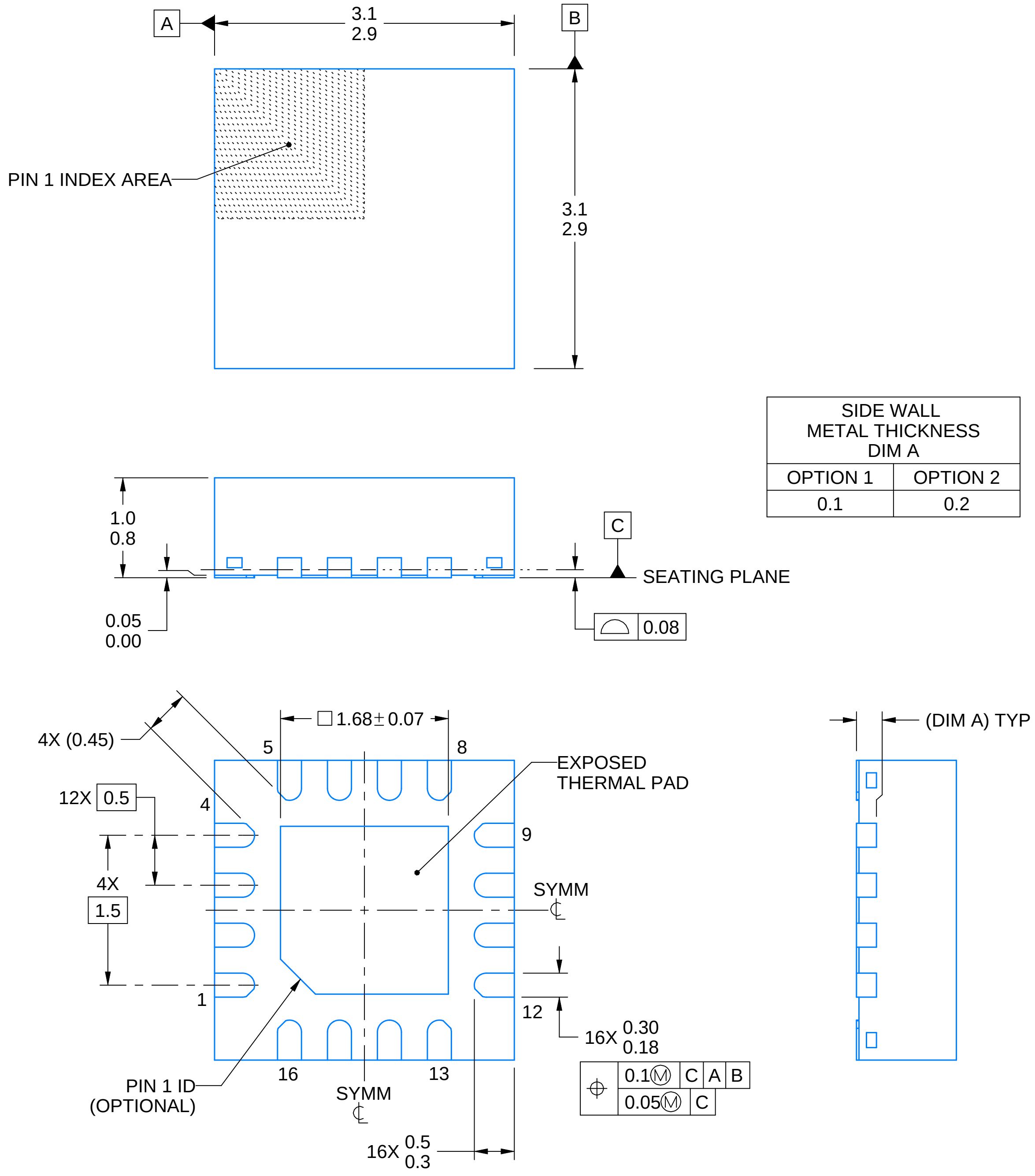
4203495/I



PACKAGE OUTLINE

VQFN - 1 mm max height

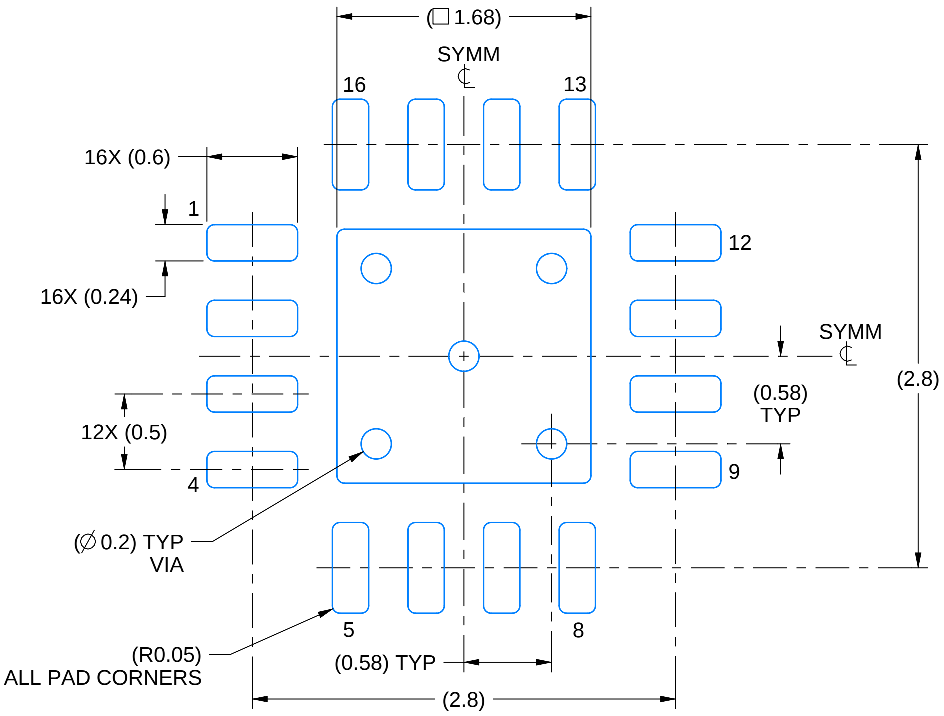
PLASTIC QUAD FLATPACK - NO LEAD



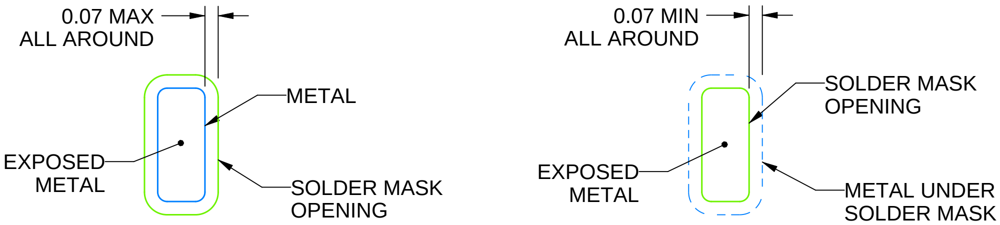
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



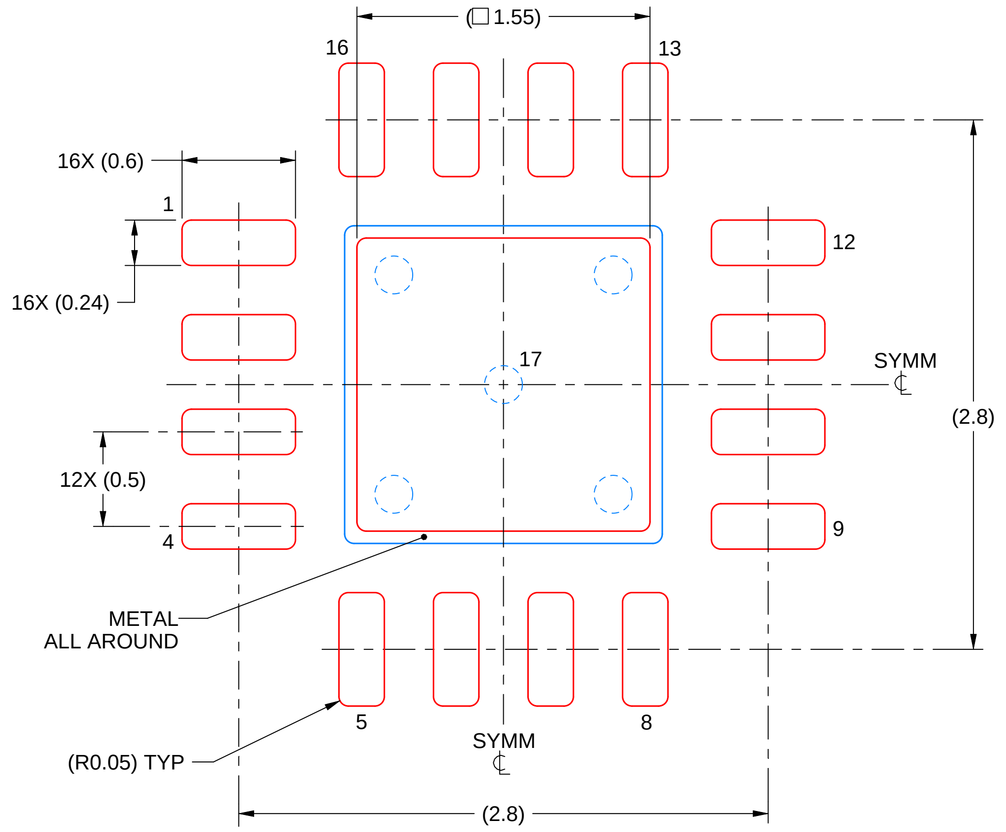
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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