

## TLVx333 2- $\mu\text{V}$ $V_{OS}$ , 0.02- $\mu\text{V}/^\circ\text{C}$ , 17- $\mu\text{A}$ , CMOS Operational Amplifiers Zero-Drift Series

### 1 Features

- Unmatched Price Performance
- Low Offset Voltage: 2  $\mu\text{V}$
- Zero Drift: 0.02  $\mu\text{V}/^\circ\text{C}$
- Low Noise: 1.1  $\mu\text{V}_{PP}$ , 0.1 Hz to 10 Hz
- Quiescent Current: 17  $\mu\text{A}$
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- Internal EMI Filtering
- *microSize* Packages: SOT23, SC70

### 2 Applications

- Battery-Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Handheld Test Equipment
- Current Sense

### 3 Description

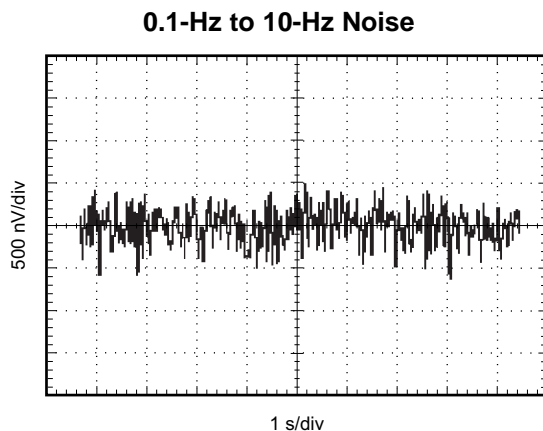
The TLVx333 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the *zero-drift* family of amplifiers that uses a proprietary auto-calibration technique to simultaneously provide low offset voltage (15  $\mu\text{V}$ , max) and near-zero drift over time and temperature at only 28  $\mu\text{A}$  (max) of quiescent current. The TLVx333 family features rail-to-rail input and output in addition to near-flat 1/f noise, making this amplifier ideal for many applications and much easier to design into a system. These devices are optimized for low-voltage operation as low as 1.8 V ( $\pm 0.9$  V) and up to 5.5 V ( $\pm 2.75$  V).

The TLV333 (single version) is available in the SC70-5, SOT23-5, and SOIC-8 packages. The TLV2333 (dual version) is offered in VSSOP-8 and SOIC-8 packages. The TLV4333 is offered in the standard SOIC-14 and TSSOP-14 packages. All versions are specified for operation from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV333	SOIC (8)	4.90 mm x 3.91 mm
	SOT-23 (5)	2.90 mm x 1.60 mm
	SC70 (5)	2.00 mm x 1.25 mm
TLV2333	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
TLV4333	SOIC (14)	8.65 mm x 3.91
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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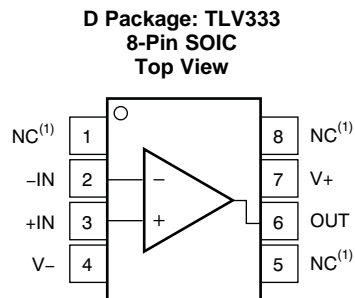
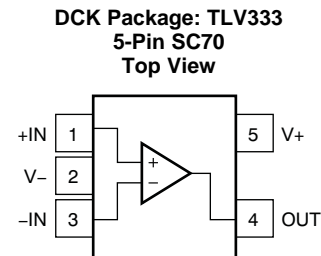
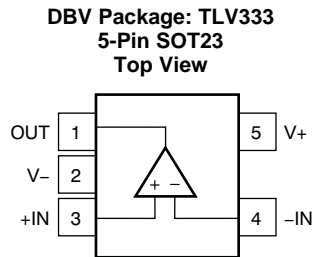
## 4 Revision History

DATE	REVISION	NOTES
December 2015	*	Initial release.

## 5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE-LEADS				
		SOIC	SOT23	SC70	VSSOP	TSSOP
TLV333	1	8	5	5	—	—
TLV2333	2	8	—	—	8	—
TLV4333	4	14	—	—	—	14

## 6 Pin Configuration and Functions

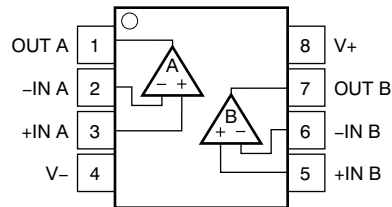


(1) NC denotes no internal connection.

### Pin Functions: TLV333

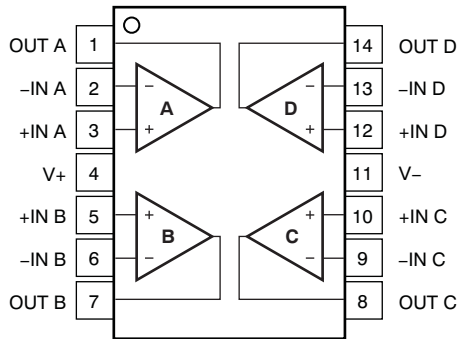
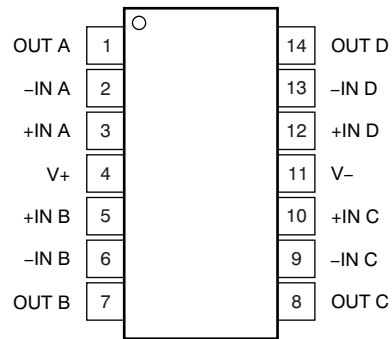
NAME	PIN			I/O	DESCRIPTION
	DBV (SOT23)	DCK (SC70)	D (SOIC)		
-IN	4	3	2	I	Inverting input
+IN	3	1	3	I	Noninverting input
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	4	6	O	Output
V-	2	2	4	—	Negative (lowest) power supply
V+	5	5	7	—	Positive (highest) power supply

**D Package: TLV2333**  
**8-Pin SOIC, VSSOP**  
**Top View**



**Pin Functions: TLV2333**

NAME	PIN		I/O	DESCRIPTION
	NO.	D (SOIC, VSSOP)		
-IN A	2		I	Inverting input, channel A
+IN A	3		I	Noninverting input, channel A
-IN B	6		I	Inverting input, channel B
+IN B	5		I	Noninverting input, channel B
OUT A	1		O	Output, channel A
OUT B	7		O	Output, channel B
V-	4		—	Negative (lowest) power supply
V+	8		—	Positive (highest) power supply

**D Package: TLV4333  
14-Pin SOIC  
Top View**

**PW Package: TLV4333  
14-Pin TSSOP  
Top View**

**Pin Functions: TLV4333**

NAME	PIN NO.		I/O	DESCRIPTION
	D (SOIC)	PW (TSSOP)		
-IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
-IN B	6	6	I	Inverting input, channel B
+IN B	5	5	I	Noninverting input, channel B
-IN C	9	9	I	Inverting input, channel C
+IN C	10	10	I	Noninverting input, channel C
-IN D	13	13	I	Inverting input, channel D
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V-	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	$V_S = (V+) - (V-)$	7		V
Signal input pins <sup>(2)</sup>	Voltage	(V-) -0.3	(V+) + 0.3	V
	Current	-10	10	mA
Output short-circuit <sup>(3)</sup>		Continuous		
Temperature	Operating	-40	150	°C
	Junction	150		
	Storage, $T_{stg}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_S$	Supply voltage	1.8		5.5	V
Specified temperature range		-40		125	°C

## 7.4 Thermal Information: TLV333

THERMAL METRIC <sup>(1)</sup>		TLV333			UNIT
		D (SOIC)	DBV (SOT23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.6	61.7	97.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	28.7	7.6	0.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	80.1	61.1	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Thermal Information: TLV2333

THERMAL METRIC <sup>(1)</sup>		TLV2333		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	180.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	18.0	2.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	63.9	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.6 Thermal Information: TLV4333

THERMAL METRIC <sup>(1)</sup>		TLV4333		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	120.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	62.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	11.6	1.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	37.7	56.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.7 Electrical Characteristics: $V_S = 1.8\text{ V to }5.5\text{ V}$

 at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to mid-supply, and  $V_{CM} = V_{OUT} = \text{mid-supply}$  (unless otherwise noted)

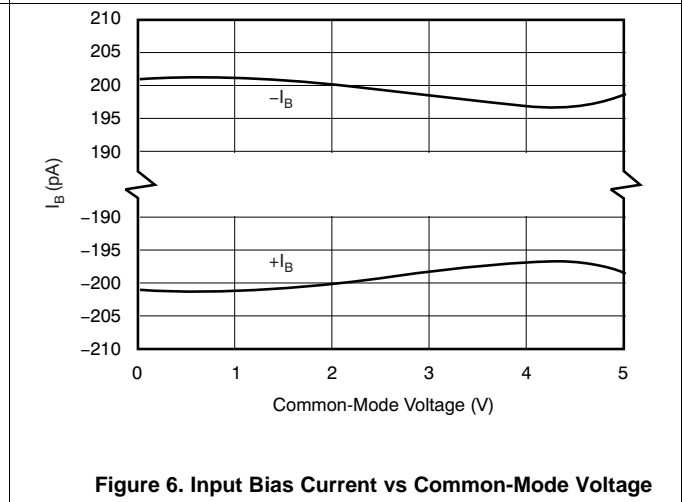
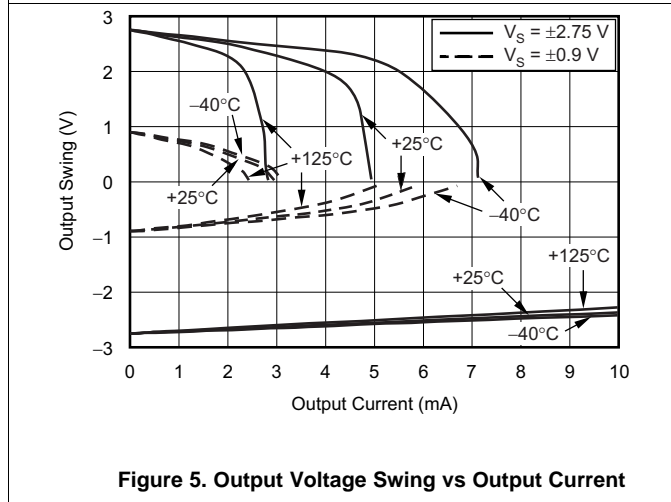
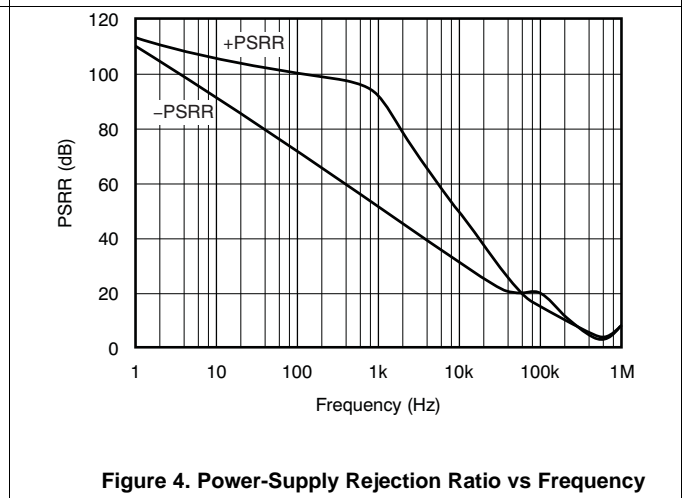
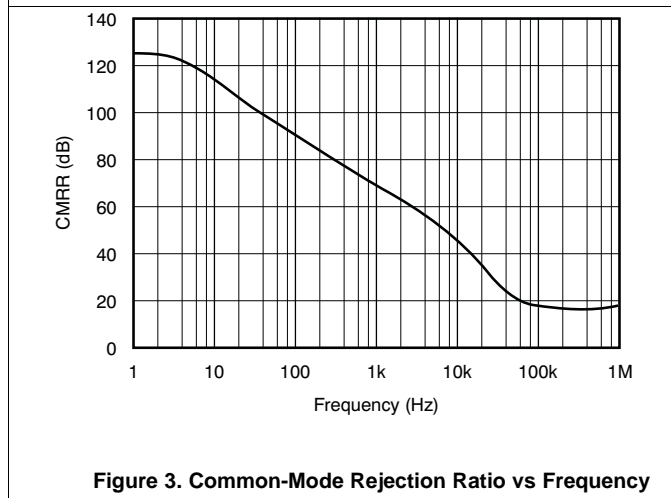
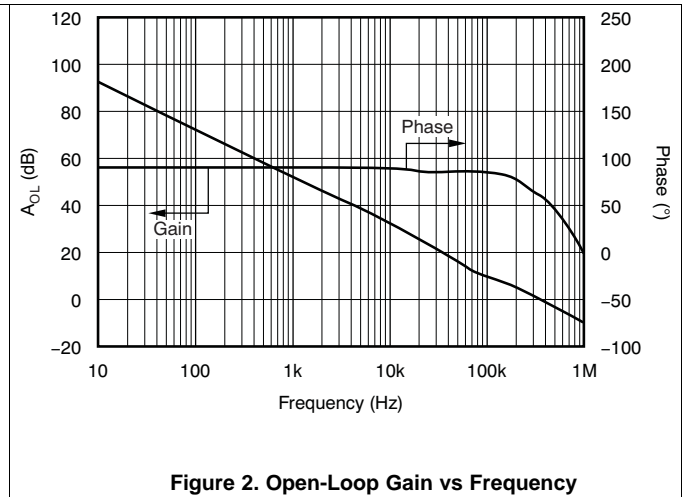
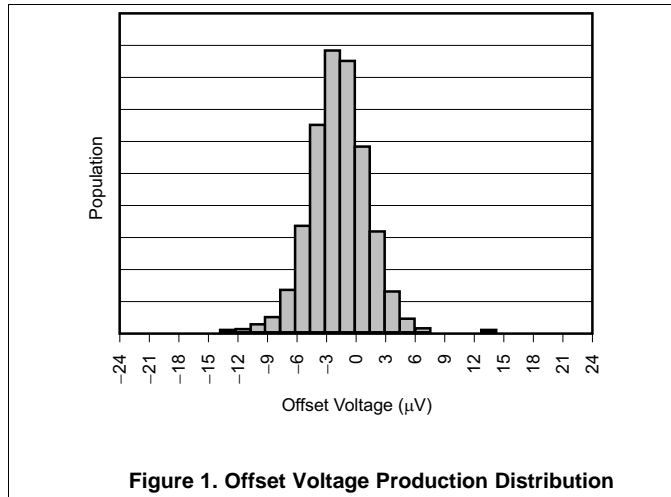
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage <sup>(1)</sup>	$V_S = 5\text{ V}$		2	15	$\mu\text{V}$
$dV_{OS}/dT$	$V_{OS}$ vs temperature	$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		0.02		$\mu\text{V}/^\circ\text{C}$
PSRR	$V_{OS}$ vs power supply	$V_S = 1.8\text{ V to }5.5\text{ V}$		1	8	$\mu\text{V/V}$
	Long-term stability <sup>(2)</sup>			1 <sup>(2)</sup>		$\mu\text{V}$
	Channel separation, dc			0.1		$\mu\text{V/V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			$\pm 70$		$\text{pA}$
	Input bias current over temperature	$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		$\pm 150$		$\text{pA}$
$I_{OS}$	Input offset current			$\pm 140$		$\text{pA}$
<b>NOISE</b>						
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$
	Input voltage noise	$f = 0.01\text{ Hz to }1\text{ Hz}$		0.3		$\mu\text{V}_{PP}$
		$f = 0.1\text{ Hz to }10\text{ Hz}$		1.1		
$i_n$	Input current noise	$f = 10\text{ Hz}$		100		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range		$(V-) - 0.1$		$(V+) + 0.1$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$	102	115		$\text{dB}$
<b>INPUT CAPACITANCE</b>						
	Differential			2		$\text{pF}$
	Common-mode			4		
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V-) + 0.1\text{ V} < V_O < (V+) - 0.1\text{ V}$	102	130		$\text{dB}$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product	$C_L = 100\text{ pF}$		350		$\text{kHz}$
SR	Slew rate	$G = 1$		0.16		$\text{V}/\mu\text{s}$
<b>OUTPUT</b>						
	Voltage output swing from rail	$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		30	70	$\text{mV}$
$I_{SC}$	Short-circuit current			$\pm 5$		$\text{mA}$
$C_L$	Capacitive load drive			See <a href="#">Typical Characteristics</a>		
$Z_O$	Open-loop output impedance	$f = 350\text{ kHz}, I_O = 0\text{ mA}$		2		$\text{k}\Omega$
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage range		1.8		5.5	$\text{V}$
$I_Q$	Quiescent current per amplifier	$I_O = 0\text{ mA}, T_A = -40^\circ\text{C to }+125^\circ\text{C}$		17	28	$\mu\text{A}$
	Turn-on time	$V_S = 5\text{ V}$		100		$\mu\text{s}$
<b>TEMPERATURE RANGE</b>						
	Specified range		-40		125	$^\circ\text{C}$
	Operating range		-40		150	$^\circ\text{C}$
	Storage range		-65		150	$^\circ\text{C}$

 (1) Specified by design and characterization. Amplifiers are 100% production screened at  $25^\circ\text{C}$  to reduce defective units.

 (2) 300-hour life test at  $150^\circ\text{C}$  demonstrated randomly distributed variation of approximately  $1\text{ }\mu\text{V}$ .

## 7.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $C_L = 0\text{ pF}$ ,  $R_L = 10\text{ k}\Omega$  connected to mid-supply,  $V_{CM} = V_{OUT} = \text{mid-supply}$  (unless otherwise noted)



### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $C_L = 0\text{ pF}$ ,  $R_L = 10\text{ k}\Omega$  connected to mid-supply,  $V_{CM} = V_{OUT} = \text{mid-supply}$  (unless otherwise noted)

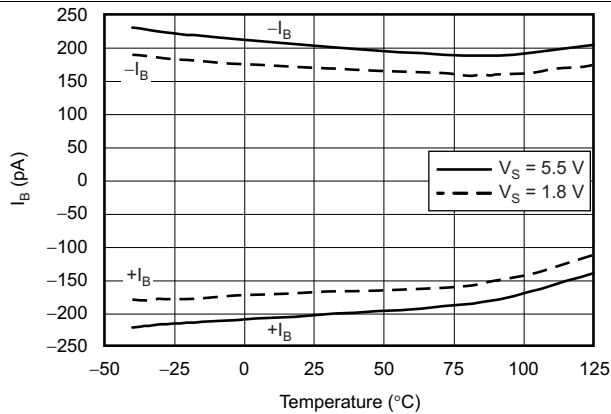


Figure 7. Input Bias Current vs Temperature

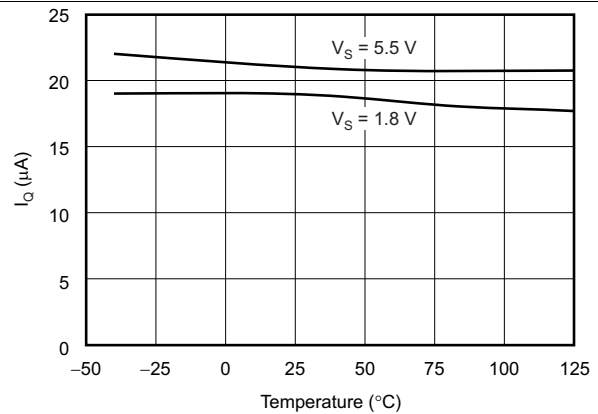


Figure 8. Quiescent Current vs Temperature

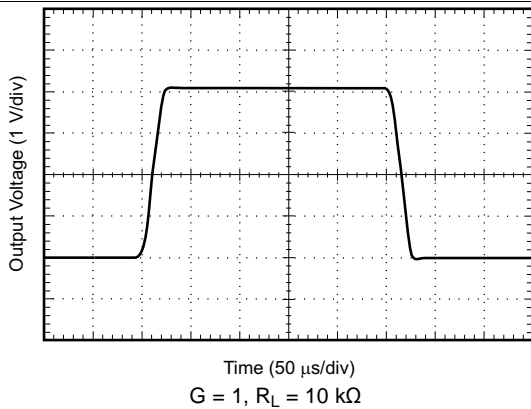


Figure 9. Large-Signal Step Response

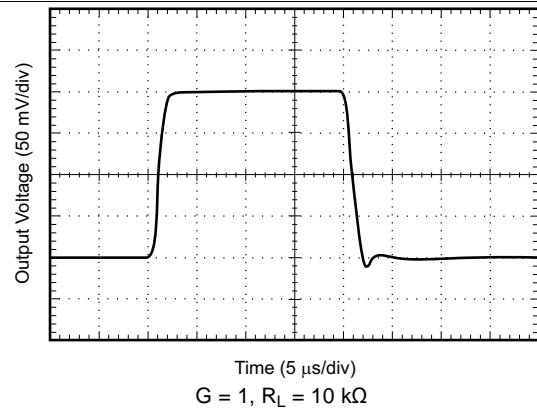


Figure 10. Small-Signal Step Response

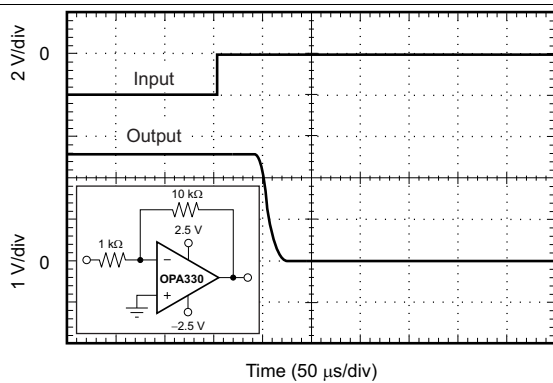


Figure 11. Positive Overvoltage Recovery

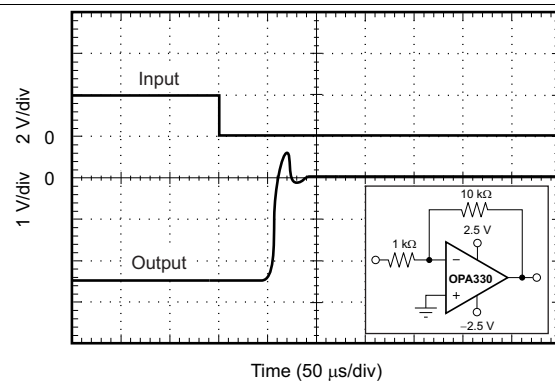


Figure 12. Negative Overvoltage Recovery

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $C_L = 0\text{ pF}$ ,  $R_L = 10\text{ k}\Omega$  connected to mid-supply,  $V_{CM} = V_{OUT} = \text{mid-supply}$  (unless otherwise noted)

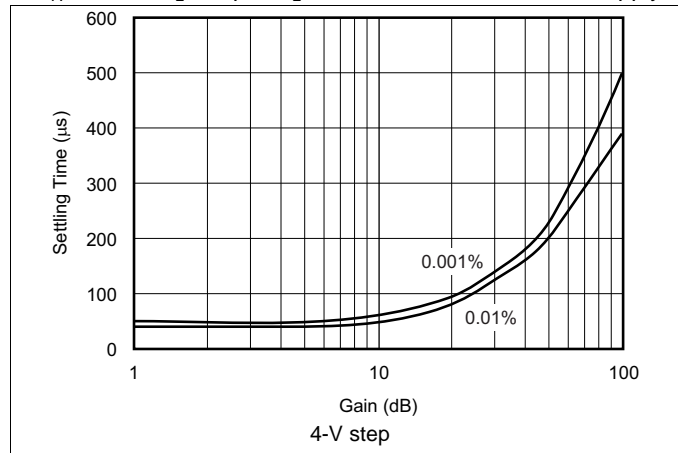


Figure 13. Settling Time vs Closed-Loop Gain

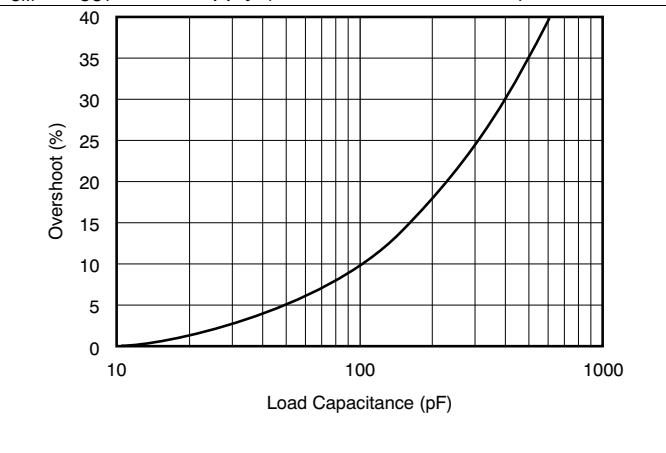


Figure 14. Small-Signal Overshoot vs Load Capacitance

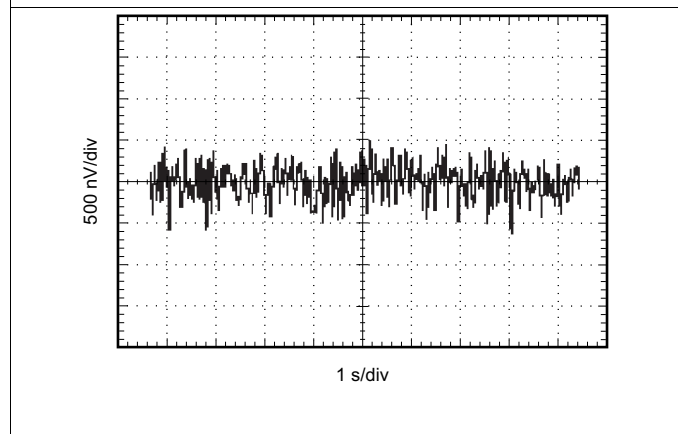


Figure 15. 0.1-Hz to 10-Hz Noise

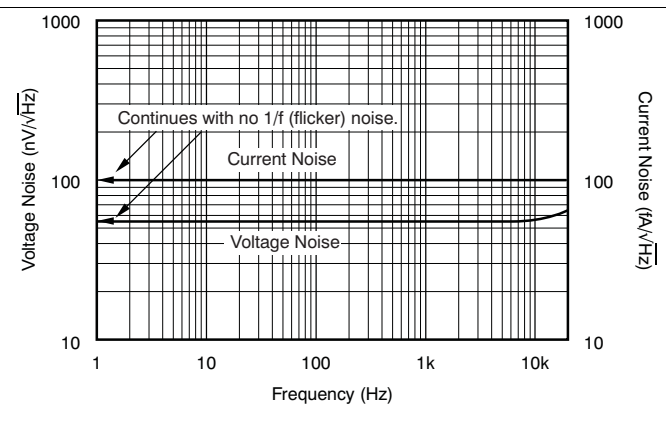


Figure 16. Current and Voltage Noise Spectral Density vs Frequency

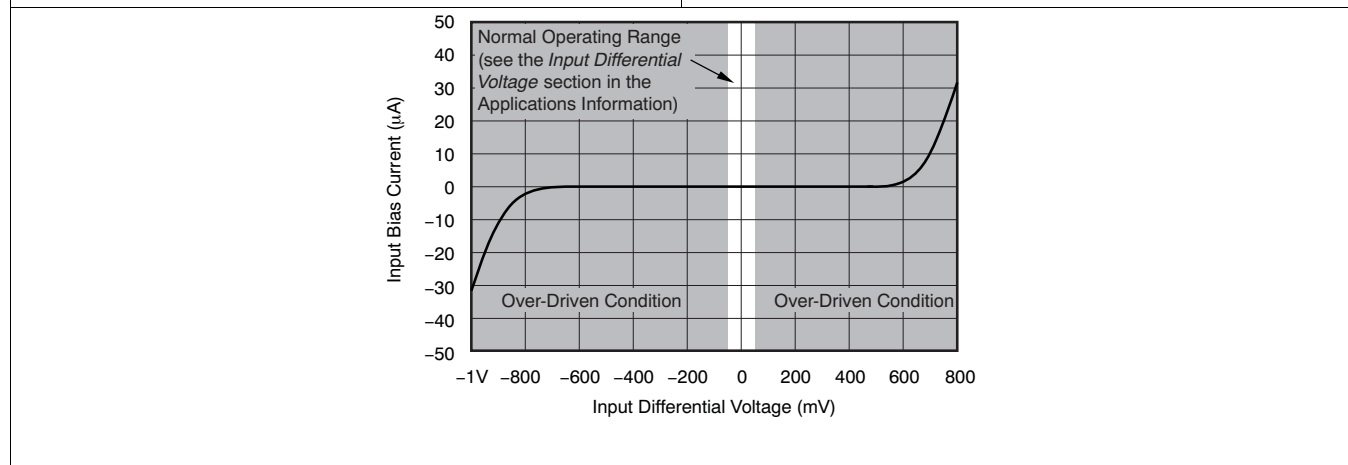


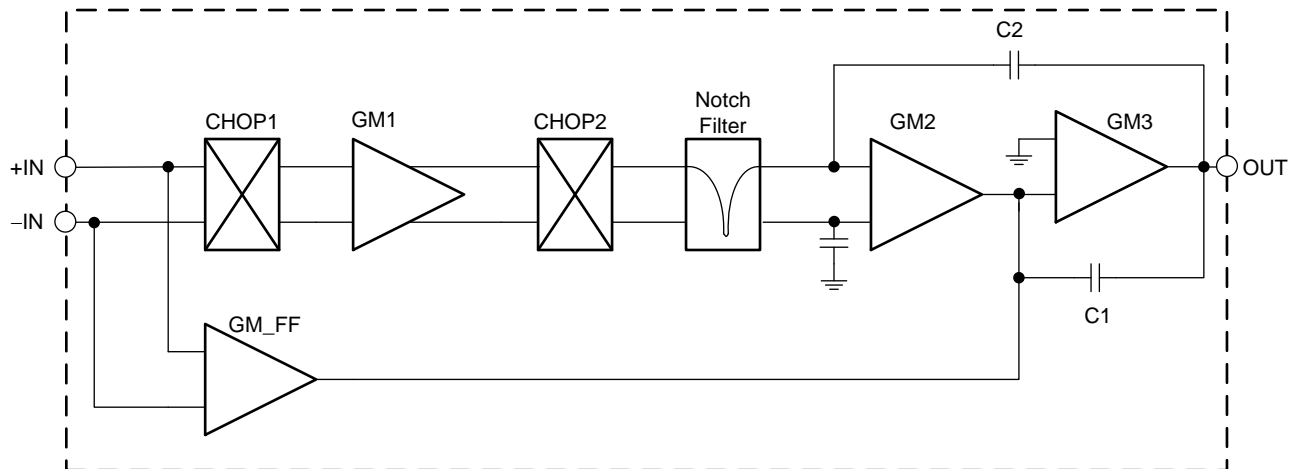
Figure 17. Input Bias Current vs Input Differential Voltage

## 8 Detailed Description

### 8.1 Overview

The TLVx333 series of low-cost operational amplifiers are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. The TLVx333 family also offers rail-to-rail input and output and near-flat 1/f noise. These features make this series of op amps ideal for many applications and much easier to design into a wide variety of systems.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The TLV333, TLV2333, and TLV4333 are unity-gain stable, precision operational amplifiers free from unexpected output phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The TLV333 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The TLV333 series are precision amplifiers for cost-sensitive applications.

#### 8.3.1 Operating Voltage

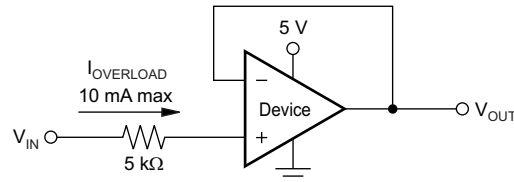
The TLV333 series op amps can be used with single or dual supplies from an operating range of  $V_S = 1.8\text{ V}$  ( $\pm 0.9\text{ V}$ ) up to  $5.5\text{ V}$  ( $\pm 2.75\text{ V}$ ). Supply voltages greater than  $7\text{ V}$  can permanently damage the device; see the [Absolute Maximum Ratings](#) table. Key parameters that vary over the supply voltage or temperature range are listed in the [Typical Characteristics](#) section.

## Feature Description (continued)

### 8.3.2 Input Voltage

The TLV333, TLV2333, and TLV4333 input common-mode voltage range extends 0.1 V beyond the supply rails. The TLV333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 200 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.



NOTE: A current-limiting resistor required if the input voltage exceeds the supply rails by  $\geq 0.3$  V.

Figure 18. Input Current Protection

### 8.3.3 Internal Offset Correction

The TLV333, TLV2333, and TLV4333 op amps use an auto-calibration technique with a time-continuous, 125-kHz op amp in the signal path. This amplifier is zero-corrected every 8  $\mu$ s using a proprietary technique. Upon power-up, the amplifier requires approximately 100  $\mu$ s to achieve specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

### 8.3.4 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp can swing close to single-supply ground, but does not reach ground. The output of the TLV333, TLV2333, and TLV4333 can be made to swing to ground, or slightly below, on a single-supply power source. This swing to ground requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. Connect a pull-down resistor between the output and the additional negative supply to pull the output down below the value that the output can otherwise achieve, as shown in Figure 19.

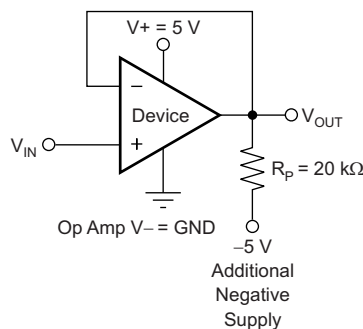


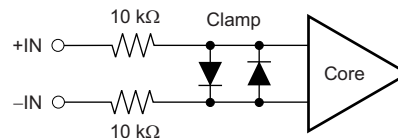
Figure 19. For  $V_{OUT}$  Range to Ground

## Feature Description (continued)

The TLV333, TLV2333, and TLV4333 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The TLV333, TLV2333, and TLV4333 are characterized to perform with this technique; the recommended resistor value is approximately 20 k $\Omega$ . Note that this configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns when the output is again driven above –2 mV. Lowering the resistance of the pull-down resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 k $\Omega$  can be used to achieve excellent accuracy down to –10 mV.

### 8.3.5 Input Differential Voltage

The typical input bias current of the TLV333 during normal operation is approximately 200 pA. In overdriven conditions, the bias current can increase significantly (see [Figure 17](#)). The most common cause of an overdriven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-k $\Omega$  electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in [Figure 20](#). Notice that the input bias current remains within specification within the linear region.



**Figure 20. Equivalent Input Circuit**

### 8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The TLV333 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a roll-off of 20 dB per decade.

## 8.4 Device Functional Modes

The TLV333 devices have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V ( $\pm 0.9$  V) and 5.5 V ( $\pm 2.75$  V).

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 System Examples

Figure 21 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 22.

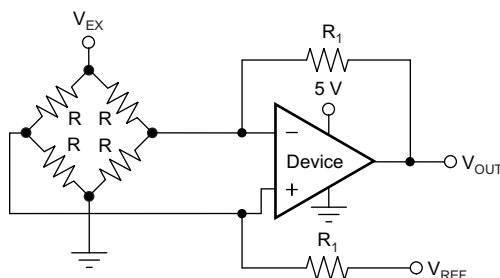
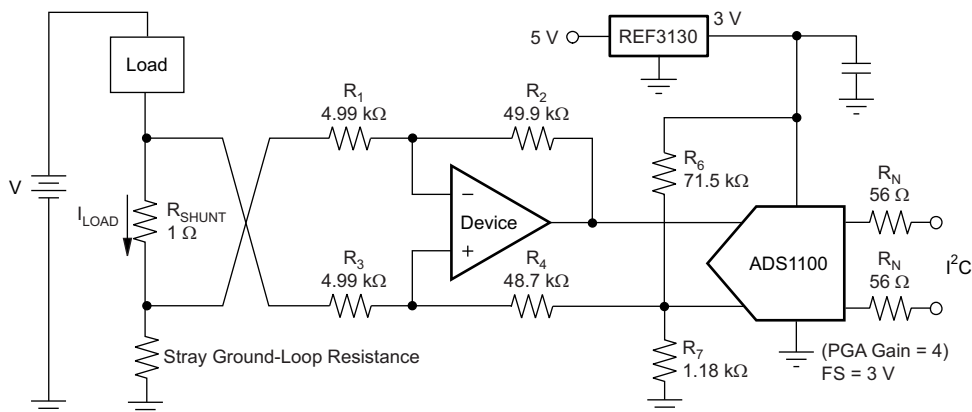


Figure 21. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 22. Low-Side Current Monitor

$R_N$  are operational resistors used to isolate the ADS1100 from the noise of the digital  $I^2C$  bus. Because the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.

Figure 23 shows the TLV333 in a typical thermistor circuit.

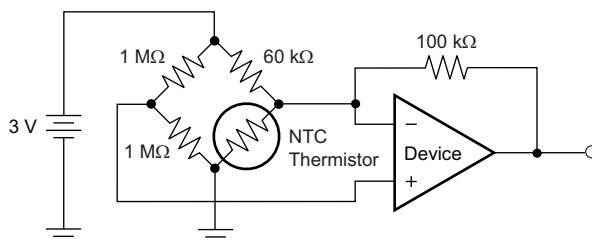


Figure 23. Thermistor Measurement

## 10 Power Supply Recommendations

The TLV333 is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

## 11 Layout

### 11.1 Layout Guidelines

#### 11.1.1 General Layout Guidelines

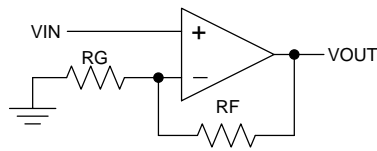
Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- $\mu\text{F}$  capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and to provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1  $\mu\text{V}/^{\circ}\text{C}$  or higher, depending on materials used.

## 11.2 Layout Example



(Schematic Representation)

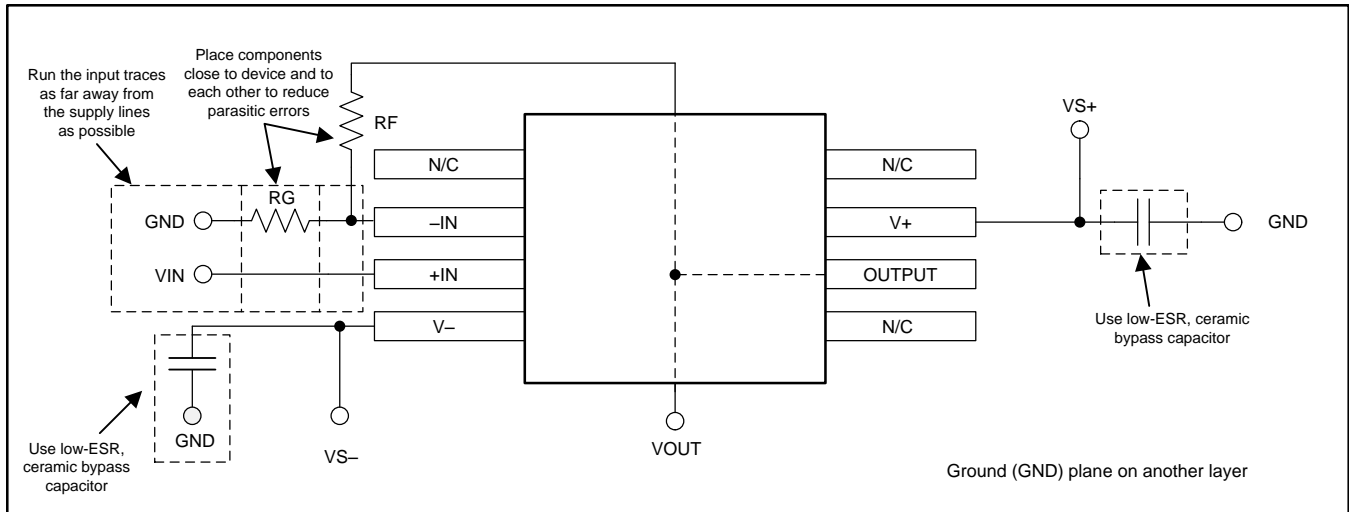


Figure 24. Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

For development support on this product, see the following:

- High-Side V-I Converter, 0 V to 2 V to 0 mA to 100 mA, 1% Full-Scale Error, [TIPD102](#)
- Low-Level V-to-I Converter Reference Design, 0-V to 5-V Input to 0-μA to 5-μA Output, [TIPD107](#)
- 18-Bit, 1-MSPS, Serial Interface, microPower, Truly-Differential Input, SAR ADC, [ADS8881](#)
- Very Low-Power, High-Speed, Rail-To-Rail Input/Output, Voltage Feedback Operational Amplifier, [THS4281](#)
- Data Acquisition Optimized for Lowest Distortion, Lowest Noise, 18-bit, 1-MSPS Reference Design, [TIPD115](#)
- Self-Calibrating, 16-Bit Analog-to-Digital Converter, [ADS1100](#)
- 20-ppm/Degrees C Max, 100-μA, SOT23-3 Series Voltage Reference, [REF3130](#)

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

- QFN/SON PCB Attachment, [SLUA271](#)
- Quad Flatpack No-Lead Logic Packages, [SCBA017](#)

### 12.3 Related Links

[Table 1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV333	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV2333	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV4333	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2333IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	12Z6
TLV2333IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Z6
<a href="#">TLV2333IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	12Z6
TLV2333IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Z6
TLV2333IDGKTG4	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Z6
TLV2333IDGKTG4.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Z6
<a href="#">TLV2333IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV233
TLV2333IDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV233
TLV2333IDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV233
TLV2333IDRG4.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV233
<a href="#">TLV333IDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	12YD
TLV333IDBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12YD
TLV333IDBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12YD
TLV333IDBVRG4.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12YD
<a href="#">TLV333IDBVT</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	12YD
TLV333IDBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12YD
<a href="#">TLV333IDCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	12B
TLV333IDCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12B
<a href="#">TLV333IDCKRG4</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12B
TLV333IDCKRG4.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12B
<a href="#">TLV333IDCKT</a>	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	12B
TLV333IDCKT.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	12B
<a href="#">TLV333IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV333
TLV333IDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV333
<a href="#">TLV4333IDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333
TLV4333IDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333
<a href="#">TLV4333IPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	TLV4333
TLV4333IPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV4333IPWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333
TLV4333IPWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4333

**(1) Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

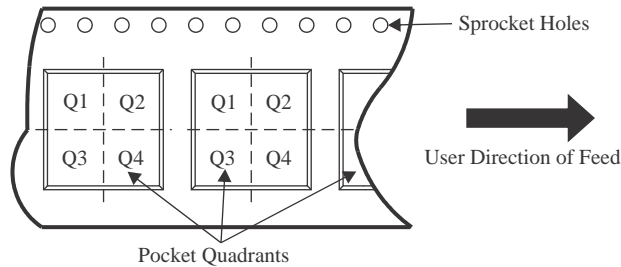
**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2333IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2333IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2333IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2333IDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2333IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2333IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV333IDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV333IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV333IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV333IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV333IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV333IDCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV333IDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV333IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4333IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4333IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4333IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2333IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2333IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV2333IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
TLV2333IDGKTG4	VSSOP	DGK	8	250	353.0	353.0	32.0
TLV2333IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2333IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLV333IDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV333IDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV333IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV333IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV333IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV333IDCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
TLV333IDCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV333IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV4333IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV4333IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV4333IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0



# EXAMPLE BOARD LAYOUT

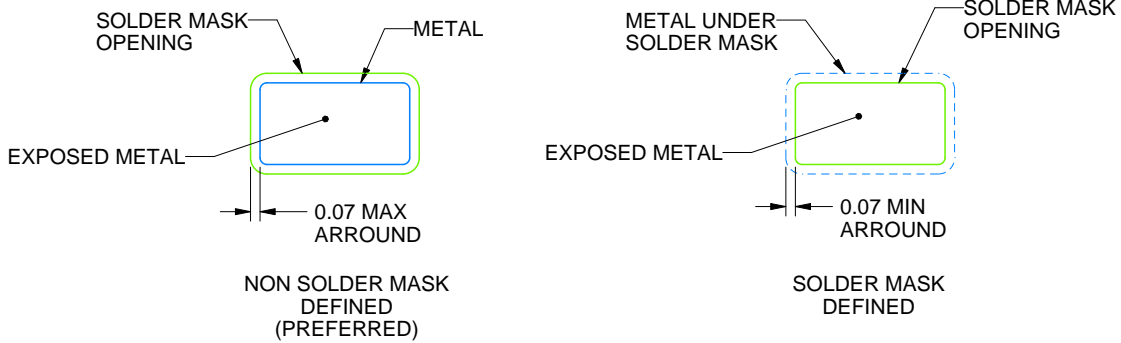
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

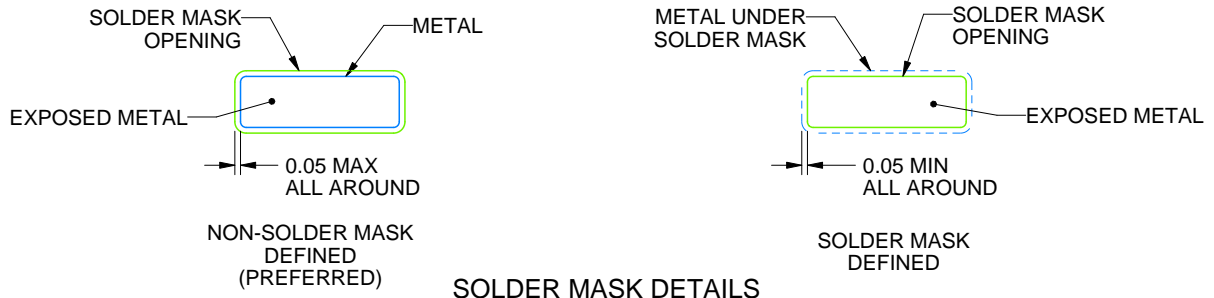
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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