

High-Slew-Rate Single-Supply Operational Amplifier

1 Features

- Qualified for Automotive Applications
- Wide Gain-Bandwidth Product: 4.5MHz
- Fast Settling Time: 2μs to 0.1%
- Wide-Range Single-Supply Operation: 4V to 36V
- Wide Input Common-Mode Range Includes Ground (V_{CC-})
- Output Short-Circuit Protection

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- [Infotainment and cluster](#)
- [Passive safety](#)
- [Body electronics and lighting](#)
- [HEV/EV inverter and motor control](#)
- [On-board \(OBC\) and wireless charger](#)
- [Powertrain current sensor](#)
- [Advanced driver assistance systems \(ADAS\)](#)
- [High-side current sensing](#)

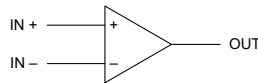
3 Description

Quality, low-cost, fabrication with remarkable design concepts is employed for the TL3472-Q1 operational amplifier. This device offers 4.5MHz of gain-bandwidth product, and fast settling time. Although the TL3472-Q1 can be operated from split supplies, TL3472-Q1 is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). This device exhibits high input resistance, low input offset voltage, and high gain. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TL3472-Q1	D (SOIC, 8)	4.90mm × 3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



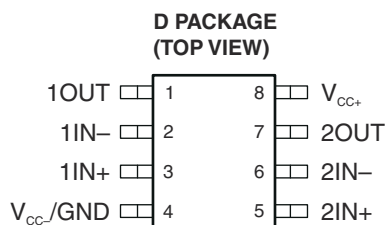
Functional Block Diagram



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4 Pin Configuration and Functions



TL3472-Q1

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	36	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage ⁽³⁾		$V_S + 0.2$	V
	Current ⁽³⁾	-10	10	mA
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
- (2) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 Recommended Operating Conditions

Parameter		Test conditions	MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	$V_{CC} = 5V$	0	2.8	V
		$V_{CC\pm} = \pm 15V$	-15	12.8	
T_A	Operating free-air temperature		-40	125	°C

5.3 Electrical Characteristics

at specified free-air temperature, $V_{CC\pm} = \pm 15V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\Omega$	$V_{CC} = 5V$	25°C	1.5	16		mV
			$V_{CC} = \pm 15V$	25°C	1	17		
				Full range		22		
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\Omega$	$V_{CC} = \pm 15V$	Full range	10			$\mu V/^\circ C$
I_{IO}	Input offset current	$V_{IC} = 0, V_O = 0, R_S = 50\Omega$	$V_{CC} = \pm 15V$	25°C	0.01	75		nA
				Full range		300		
I_{IB}	Input bias current	$V_{IC} = 0, V_O = 0, R_S = 50\Omega$	$V_{CC} = \pm 15V$	25°C	0.01	500		nA
				Full range		700		
V_{ICR}	Common-mode input voltage range	$R_S = 50\Omega$		25°C	-15 to 12.8			V
				Full range	-15 to 12.8			
V_{OH}	High-level output voltage	$V_{CC+} = 5V, V_{CC-} = 0, R_L = 2k\Omega$		25°C	3.7	4.8		V
		$R_L = 10k\Omega$		25°C	13.6	14.8		
		$R_L = 2k\Omega$		Full range	13.4			
V_{OL}	Low-level output voltage	$V_{CC+} = 5V, V_{CC-} = 0, R_L = 2k\Omega$		25°C	0.005	0.3		V
		$R_L = 10k\Omega$		25°C	-14.8	-14.3		
		$R_L = 2k\Omega$		Full range		-13.5		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10V, R_L = 2k\Omega$		25°C	25	100		V/mV
				Full range	20			
I_{OS}	Short-circuit output current	Source: $V_{ID} = 1V, V_O = 0$		25°C	-10	-75		mA
		Sink: $V_{ID} = -1V, V_O = 0$			+20	+75		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}, R_S = 50\Omega$		25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 13.5V$ to $\pm 16.5V, R_S = 100\Omega$		25°C	70	97		dB
I_{CC}	Supply current (per channel)	$V_O = 0, \text{No load}$		25°C	0.56	4.5		mA
				Full range		5.5		
		$V_{CC+} = 5V, V_O = 2.5V, V_{CC-} = 0, \text{No load}$		25°C		4.5		

(1) Full range $T_A = -40^\circ C$ to $125^\circ C$

(2) All typical values are at $T_A = 25^\circ C$.

5.4 Operating Characteristics

 $V_{CC\pm} = \pm 15V$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+ Positive slew rate	$V_I = -10V$ to $10V$, $R_L = 2k\Omega$, $C_L = 300pF$	$A_V = 1$	8	10		V/ μs
SR– Negative slew rate	$V_I = -10V$ to $10V$, $R_L = 2k\Omega$, $C_L = 300pF$	$A_V = -1$		13		V/ μs
t_s Settling time	$A_{VD} = -1$, 10V step	To 0.1%		2		μs
		To 0.01%		2.5		
V_n Equivalent input noise voltage	$f = 1kHz$, $R_S = 100\Omega$			10.8		nV/ \sqrt{Hz}
I_n Equivalent input noise current	$f = 1kHz$			2		fA/ \sqrt{Hz}
THD Total harmonic distortion	$V_{O(PP)} = 2V$ to $20V$, $R_L = 2k\Omega$, $A_{VD} = 10$, $f = 10kHz$			0.02		%
GBW Gain-bandwidth product	$f = 100kHz$			4.5		MHz
BW Power bandwidth	$V_{O(PP)} = 20V$, $R_L = 2k\Omega$, $A_{VD} = 1$, THD = 5.0%			160		kHz
ϕ_m Phase margin	$R_L = 2k\Omega$	$C_L = 0$		70		deg
		$C_L = 300pF$		50		
Gain margin	$R_L = 2k\Omega$	$C_L = 0$		12		dB
		$C_L = 300pF$		4		
r_i Differential input resistance	$V_{IC} = 0$			540		G Ω
C_i Input capacitance	$V_{IC} = 0$			10		pF
Channel separation	$f = 10kHz$			101		dB
z_o Open-loop output impedance	$f = 1MHz$, $A_V = 1$			525		Ω

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2003) to Revision A (December 2025)	Page
• Changed Wide gain bandwidth product from 4MHz to 4.5MHz.....	1
• Deleted High slew rate.....	1
• Deleted Low total harmonic distortion.....	1
• Deleted Large capacitance drive capability.....	1
• Added Application section.....	1
• Deleted "With a Darling-ton transistor input stage", and "The all NPN output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response." lines from description.....	1
• Deleted Ordering information.....	1
• Deleted 13V/μs slew rate.....	1
• Deleted Schematic Information.....	1
• Updated Absolute maximum ratings.....	4
• Updated Input bias current from 6nA to 0.01nA.....	5
• Updated Input bias current from 100nA to 0.01nA.....	5
• Updated High-level output voltage from 4V to 4.8V and 14V to 14.8V	5
• Updated Low-level output voltage from 0.1V to 0.005V and –14.7V to –14.8V.....	5
• Updated Settling time from 1.1μs to 2μs for 0.1%	6
• Updated Settling time from 2.2μs to 2.5μs for 0.01%.....	6
• Updated Equivalent input noise voltage from 49nV/√HZ to 10.8nV/√HZ	6
• Updated Equivalent input noise voltage from 0.22pA/√HZ to 2fA/√HZ	6
• Updated Gain-bandwidth product from 4MHz to 4.5MHz.....	6
• Updated Differential input resistance from 150MΩ to 540GΩ.....	6
• Updated Input capacitance from 2.5pF to 10pF.....	6
• Updated Open-loop output impedance from 20Ω to 525Ω.....	6

DATE	REVISION	NOTES
March 2008	*	Initial Release

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3472QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3472Q
TL3472QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3472Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TL3472-Q1 :

- Catalog : [TL3472](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3472QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3472QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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