

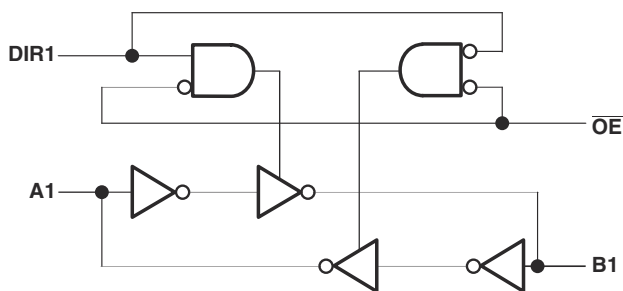
# SN74AVC2T245 Dual-Bit Dual-Supply Bus Transceiver with Configurable Level-Shifting / Voltage Translation and Tri-State Outputs

## 1 Features

- Each Channel Has Independent Direction Control
- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2V to 3.6V Power-Supply Range
- I/Os Are 4.6V Tolerant
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- $V_{CC}$  Isolation Feature - If Either  $V_{CC}$  Input is at GND, Both Ports are in High-Impedance State
- Typical Data Rates
  - 500Mbps (1.8V to 3.3V Level-Shifting)
  - 320Mbps (<1.8V to 3.3V Level-Shifting)
  - 320Mbps (Translate to 2.5V or 1.8V)
  - 280Mbps (Translate to 1.5V)
  - 240Mbps (Translate to 1.2V)
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 5000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1500V Charged-Device Model (C101)

## 2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom



A. Shown for a single channel

**Logic Diagram (Positive Logic)**

## 3 Description

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVC2T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74AVC2T245 control pins (DIR1, DIR2, and  $\overline{OE}$ ) are supplied by  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  must be connected to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74AVC2T245	UQFN (10)	1.80mm × 1.40mm

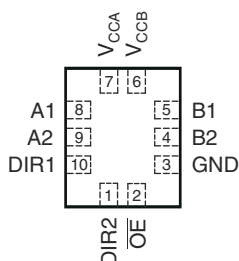
(1) For all available packages, see the orderable addendum at the end of the datasheet.



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## 4 Pin Configuration and Functions



**Figure 4-1. RSW PACKAGE 10-PIN UQFN TOP VIEW**

**Table 4-1. Pin Functions**

PIN		DESCRIPTION
NAME	NO. (UQFN)	
$V_{CCA}$	7	Supply Voltage A
$V_{CCB}$	6	Supply Voltage B
GND	3	Ground
A1	8	Output or input depending on state of DIR. Output level depends on $V_{CCA}$ .
A2	9	Output or input depending on state of DIR. Output level depends on $V_{CCA}$ .
B1	5	Output or input depending on state of DIR. Output level depends on $V_{CCB}$ .
B2	4	Output or input depending on state of DIR. Output level depends on $V_{CCB}$ .
DIR1,DIR2	10,1	Direction Pin, Connect to GND or to $V_{CCA}$
OE	2	Tri-state output-mode enables. Pull OE high to place all outputs in 3-state mode. Referenced to $V_{CCA}$

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage	–0.5	4.6	V
$V_I$	Input voltage <sup>(2)</sup>	I/O ports (A port)	–0.5	4.6
		I/O ports (B port)	–0.5	4.6
		Control inputs	–0.5	4.6
$V_O$	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	–0.5	4.6
		B port	–0.5	4.6
$V_O$	Voltage applied to any output in the high or low state <sup>(2) (3)</sup>	A port	–0.5	$V_{CCA} + 0.5$
		B port	–0.5	$V_{CCB} + 0.5$
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		±100	mA
$T_J$	Junction Temperature	–40	150	°C
$T_{stg}$	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	5000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1500

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

(3)			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs <sup>(1)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(1)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>IH</sub>	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(2)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		

### 5.3 Recommended Operating Conditions (continued)

(3)			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>IL</sub>	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(2)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	3.6	
I <sub>OH</sub>	High-level output current			1.1 V to 1.2 V	−3		mA
				1.4 V to 1.6 V	−6		
				1.65 V to 1.95 V	−8		
				2.3 V to 2.7 V	−9		
				3 V to 3.6 V	−12		
I <sub>OL</sub>	Low-level output current			1.1 V to 1.2 V	3		mA
				1.4 V to 1.6 V	6		
				1.65 V to 1.95 V	8		
				2.3 V to 2.7 V	9		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T <sub>A</sub>	Operating free-air temperature				−40	85	°C

- (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.  
 (2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.  
 (3) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AVC2T245	UNIT
		RSW (UQFN)	
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	227.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	96.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	139.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	5.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	139.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>		I <sub>OH</sub> = –100 µA	1.2 V to 3.6 V	1.2 V to 3.6 V				V <sub>CCO</sub> – 0.2		V
		I <sub>OH</sub> = –3 mA	1.2 V	1.2 V		0.95				
		I <sub>OH</sub> = –6 mA	1.4 V	1.4 V				1.05		
		I <sub>OH</sub> = –8 mA	1.65 V	1.65 V				1.2		
		I <sub>OH</sub> = –9 mA	2.3 V	2.3 V				1.75		
		I <sub>OH</sub> = –12 mA	3 V	3 V				2.3		
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	1.2 V to 3.6 V	1.2 V to 3.6 V				0.2		V
		I <sub>OL</sub> = 3 mA	1.2 V	1.2 V		0.25				
		I <sub>OL</sub> = 6 mA	1.4 V	1.4 V				0.35		
		I <sub>OL</sub> = 8 mA	1.65 V	1.65 V				0.45		
		I <sub>OL</sub> = 9 mA	2.3 V	2.3 V				0.55		
		I <sub>OL</sub> = 12 mA	3 V	3 V				0.7		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I <sub>off</sub>	A or B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 V to 3.6 V		±0.1	±1		±5	µA
			0 V to 3.6 V	0 V		±0.1	±1		±5	
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V		±0.5	±2.5		±5	µA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				8		µA
			0 V	0 V to 3.6 V				–2		
			0 V to 3.6 V	0 V				8		
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				8		µA
			0 V	0 V to 3.6 V				8		
			0 V to 3.6 V	0 V				–2		
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				16		µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V		3.5		4.5		pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = 3.3 V or GND	3.3 V	3.3 V		6		7		pF

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

## 5.6 Switching Characteristics: $V_{CCA} = 1.2\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.2\text{ V}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$t_{PLH}$	A	B	2.5	2.1	1.9	1.9	1.9	ns
$t_{PHL}$			2.5	2.1	1.9	1.9	1.9	
$t_{PLH}$	B	A	2.5	2.2	2	1.8	1.7	ns
$t_{PHL}$			2.5	2.2	2	1.8	1.7	
$t_{PZH}$	$\overline{OE}$	A	3.8	3.1	2.7	2.6	3	ns
$t_{PZL}$			3.8	3.1	2.7	2.6	3	
$t_{PZH}$	$\overline{OE}$	B	3.7	3.7	3.7	3.7	3.7	ns
$t_{PZL}$			3.7	3.7	3.7	3.7	3.7	
$t_{PHZ}$	$\overline{OE}$	A	4.4	3.6	3.5	3.3	4.1	ns
$t_{PLZ}$			4.4	3.6	3.5	3.3	4.1	
$t_{PHZ}$	$\overline{OE}$	B	4.2	4.2	4.3	4.1	4.2	ns
$t_{PLZ}$			4.2	4.2	4.3	4.1	4.2	

## 5.7 Switching Characteristics: $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.2	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	ns
$t_{PHL}$			2.2	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	
$t_{PLH}$	B	A	2	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	ns
$t_{PHL}$			2	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	
$t_{PZH}$	$\overline{OE}$	A	3.4	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	ns
$t_{PZL}$			3.4	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	
$t_{PZH}$	$\overline{OE}$	B	2.5	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	ns
$t_{PZL}$			2.5	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	
$t_{PHZ}$	$\overline{OE}$	A	4.1	1.2	7.1	0.8	6.7	0.4	5.6	1	7.4	ns
$t_{PLZ}$			4.1	1.2	7.1	0.8	6.7	0.4	5.6	1	7.4	
$t_{PHZ}$	$\overline{OE}$	B	3.3	0.3	7.4	0.2	5.7	0.3	5.6	0.3	5.6	ns
$t_{PLZ}$			3.3	0.3	7.4	0.2	5.7	0.3	5.6	0.3	5.6	

## 5.8 Switching Characteristics: $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	ns
$t_{PHL}$			2	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	
$t_{PLH}$	B	A	1.9	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	ns
$t_{PHL}$			1.9	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	
$t_{PZH}$	$\overline{OE}$	A	3.2	0.8	6.7	0.4	5.8	0.4	4.8	0.3	4.6	ns
$t_{PZL}$			3.2	0.8	6.7	0.4	5.8	0.4	4.8	0.3	4.6	
$t_{PZH}$	$\overline{OE}$	B	1.9	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	ns
$t_{PZL}$			1.9	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	
$t_{PHZ}$	$\overline{OE}$	A	3.8	0.7	6.2	0.3	6.5	0.1	5.2	0.8	6.5	ns
$t_{PLZ}$			3.8	0.7	6.2	0.3	6.5	0.1	5.2	0.8	6.5	
$t_{PHZ}$	$\overline{OE}$	B	3.4	0.1	6.8	0.1	6.8	0.1	6.7	0.1	6.7	ns
$t_{PLZ}$			3.4	0.1	6.8	0.1	6.8	0.1	6.7	0.1	6.7	

## 5.9 Switching Characteristics: $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.9	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	ns
$t_{PHL}$			1.9	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	
$t_{PLH}$	B	A	1.8	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	ns
$t_{PHL}$			1.8	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	
$t_{PZH}$	$\overline{OE}$	A	3.1	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	ns
$t_{PZL}$			3.1	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	
$t_{PZH}$	$\overline{OE}$	B	1.4	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns
$t_{PZL}$			1.4	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	
$t_{PHZ}$	$\overline{OE}$	A	3.6	0.2	5.2	0.1	5.4	0.1	4.5	0.7	6	ns
$t_{PLZ}$			3.6	0.2	5.2	0.1	5.4	0.1	4.5	0.7	6	
$t_{PHZ}$	$\overline{OE}$	B	2.1	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	ns
$t_{PLZ}$			2.1	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	



## 5.10 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.8	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	ns
$t_{PHL}$			1.8	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	
$t_{PLH}$	B	A	1.9	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	ns
$t_{PHL}$			1.9	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	
$t_{PZH}$	$\overline{OE}$	A	3.1	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	ns
$t_{PZL}$			3.1	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	
$t_{PZH}$	$\overline{OE}$	B	1.2	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	ns
$t_{PZL}$			1.2	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	
$t_{PHZ}$	$\overline{OE}$	A	3.4	0.1	4.6	0.1	4.7	0.3	4.8	0.7	4.5	ns
$t_{PLZ}$			3.4	0.1	4.6	0.1	4.7	0.3	4.8	0.7	4.5	
$t_{PHZ}$	$\overline{OE}$	B	2.9	0.1	5.4	0.1	5.3	0.1	5.3	0.1	5.3	ns
$t_{PLZ}$			2.9	0.1	5.4	0.1	5.3	0.1	5.3	0.1	5.3	

## 5.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.2\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}$ <sup>(1)</sup>	A to B	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	3	3	3	3	4	pF
		Outputs disabled		1	1	1	2	2	
	B to A	Outputs enabled		12	13	13	15	15	
		Outputs disabled		1	2	2	2	2	
$C_{pdB}$ <sup>(1)</sup>	A to B	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	12	13	13	14	16	pF
		Outputs disabled		1	2	2	2	2	
	B to A	Outputs enabled		3	3	3	4	4	
		Outputs disabled		1	1	1	2	2	

(1) Power dissipation capacitance per transceiver. Refer to the TI application report, CMOS Power Consumption and Cpd Calculation, [SCAA035](#)

## 5.12 Typical Characteristics

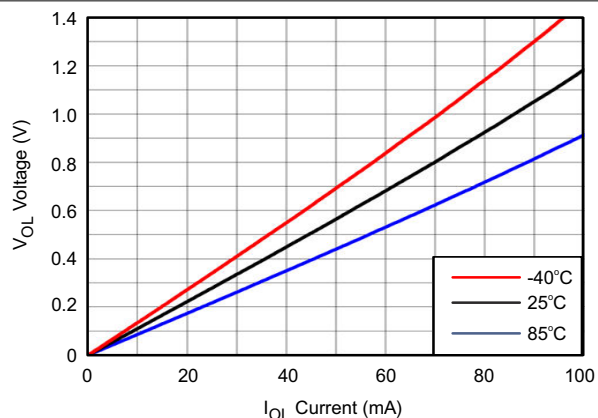


Figure 5-1. V<sub>OL</sub> Voltage vs I<sub>OL</sub> Current

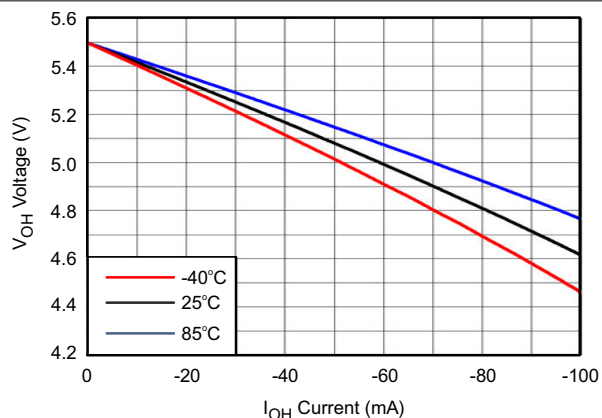
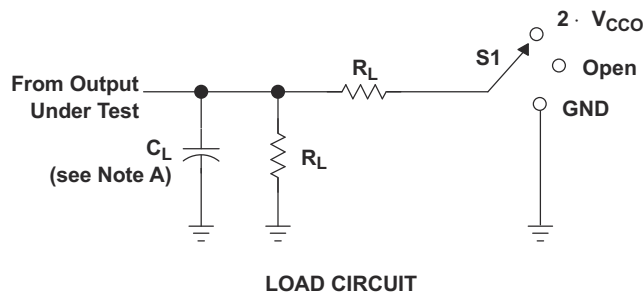


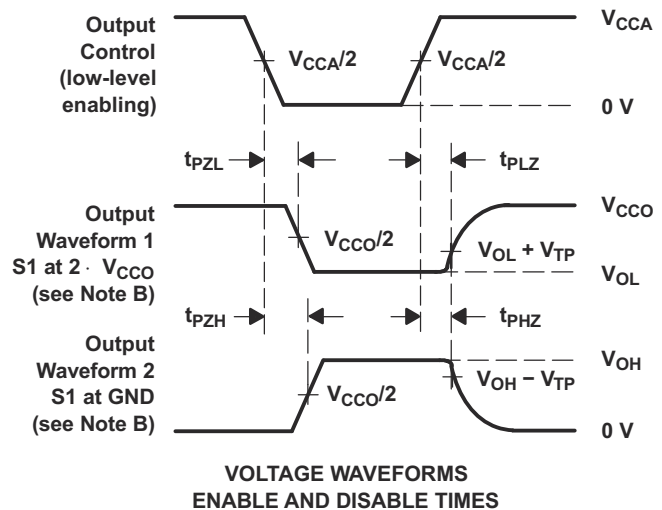
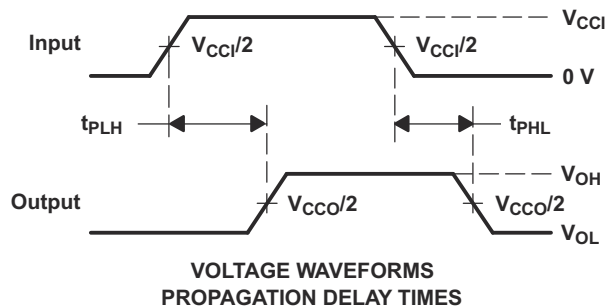
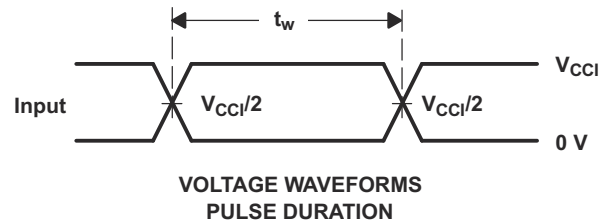
Figure 5-2. V<sub>OH</sub> Voltage vs I<sub>OH</sub> Current

## 6 Parameter Measurement Information



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \cdot V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1 \text{ V/ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- F.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- G.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

Figure 6-1. Load and Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74AVC2T245 is a dual-bit, dual-supply noninverting bidirectional voltage level translator. Pins A and control pins (DIR and  $\overline{OE}$ ) are supported by  $V_{CCA}$  and pins B are supported by  $V_{CCB}$ . The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when  $\overline{OE}$  is set to low. When  $\overline{OE}$  is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current ( $I_{off}$ ).

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are put in a high-impedance state.

### 7.2 Functional Block Diagram

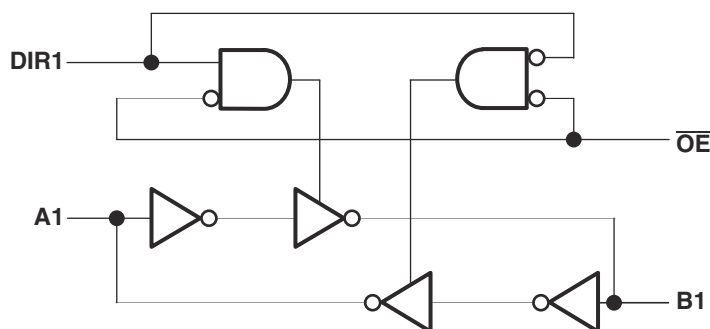


Figure 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

#### 7.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage from 1.2 V to 3.6 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

#### 7.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current ( $I_{off}$ ). The  $I_{off}$  circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

#### 7.3.3 $V_{CC}$ Isolation

The  $V_{CC}$  isolation feature ensures that if either  $V_{CCA}$  or  $V_{CCB}$  are at GND, both ports will be in a high-impedance state ( $I_{OZ}$ ). This prevents false logic levels from being presented to either bus.

### 7.4 Device Functional Modes

The SN74AVC2T245 is a voltage level translator that can operate from 1.2 V to 3.6 V ( $V_{CCA}$ ) and 1.2 V to 3.6 V ( $V_{CCB}$ ). The signal translation requires direction control and output enable control. The table below enlists the operation of the part for the respective states of the control inputs.

Table 7-1. Function Table (Each Transceiver)

CONTROL INPUTS <sup>(1)</sup>		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR1	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74AVC2T245 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

#### 8.1.1 Enable Times

Calculate the enable times for the SN74AVC16T45 using the following formulas:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

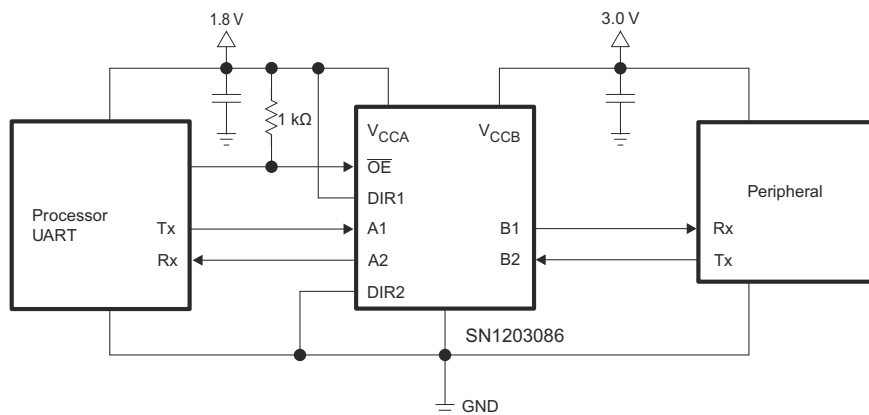
$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

### 8.2 Typical Application



**Figure 8-1. Typical Application of the SN74AVC2T245**

#### 8.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in [Table 8-1](#).

**Table 8-1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

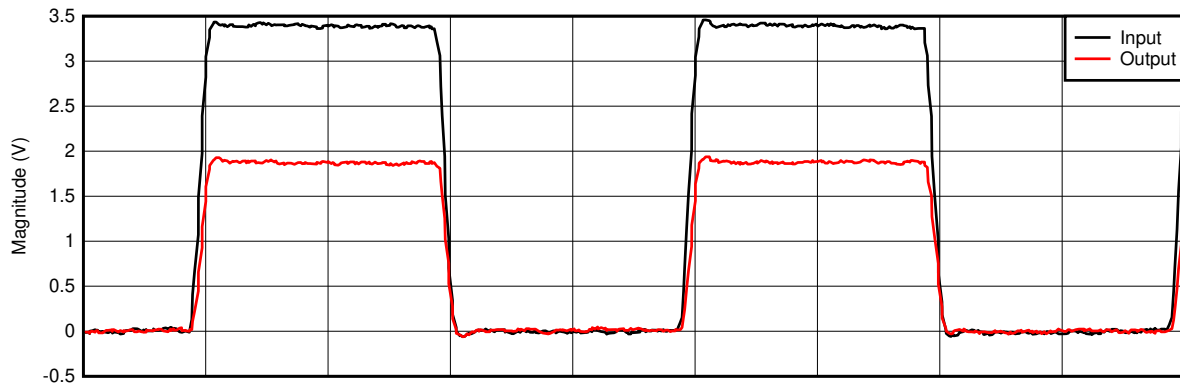
#### 8.2.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVC2T245 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.

#### 8.2.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVC2T245 device is driving to determine the output voltage range.

### 8.2.3 Application Curves



D001

**Figure 8-2. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave**

## 9 Power Supply Recommendations

The SN74AVC2T245 device uses two separate configurable power-supply rails,  $V_{CCA}$  and  $V_{CCB}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V and  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track  $V_{CCA}$  and  $V_{CCB}$  respectively allowing for low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5 V voltage nodes.

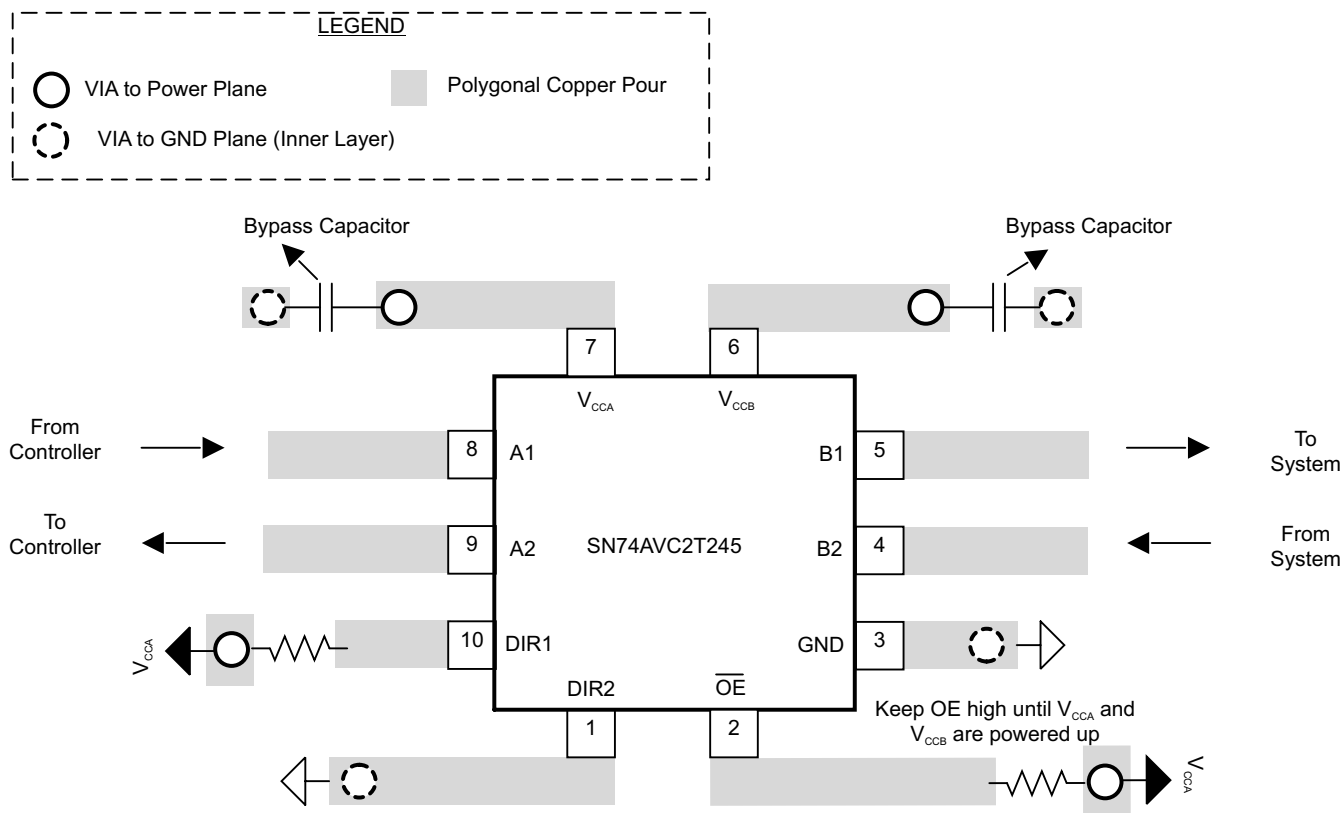
## 10 Layout

### 10.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

### 10.2 Layout Example



**Figure 10-1. Recommended Layout Example**

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.3 Trademarks

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### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.



## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (February 2016) to Revision E (September 2024) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document ..... 1
- Updated Thermal Information.....5

### Changes from Revision C (July 2015) to Revision D (February 2016) Page

- Made changes to [Pin Configuration and Functions](#) ..... 1

### Changes from Revision B (June 2015) to Revision C (July 2015) Page

- The *Ordering Information* table (formally on page 1) contained a Top-Side Marking of TQ\_. The table has been replaced with the Package Option Addendum in [Mechanical, Packaging, and Orderable Information](#). VC\_ was added to the device marking . ..... 17

### Changes from Revision A (May 2012) to Revision B (June 2015) Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... 1
- Removed the Ordering Information table. .... 1

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AVC2T245RSWR</a>	Active	Production	UQFN (RSW)   10	3000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(TQ7, TQO, TQR, TQ V) (TQH, TQJ, TQY) (VCH, VCO) (VCJ, VCR)
SN74AVC2T245RSWR.A	Active	Production	UQFN (RSW)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TQ7, TQO, TQR, TQ V) (TQH, TQJ, TQY) (VCH, VCO) (VCJ, VCR)
SN74AVC2T245RSWR.B	Active	Production	UQFN (RSW)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TQ7, TQO, TQR, TQ V) (TQH, TQJ, TQY) (VCH, VCO) (VCJ, VCR)
SN74AVC2T245RSWRG4.A	Active	Production	UQFN (RSW)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TQV TQY
SN74AVC2T245RSWRG4.B	Active	Production	UQFN (RSW)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TQV TQY

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

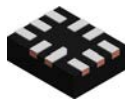
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	8.4	1.59	2.09	0.72	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

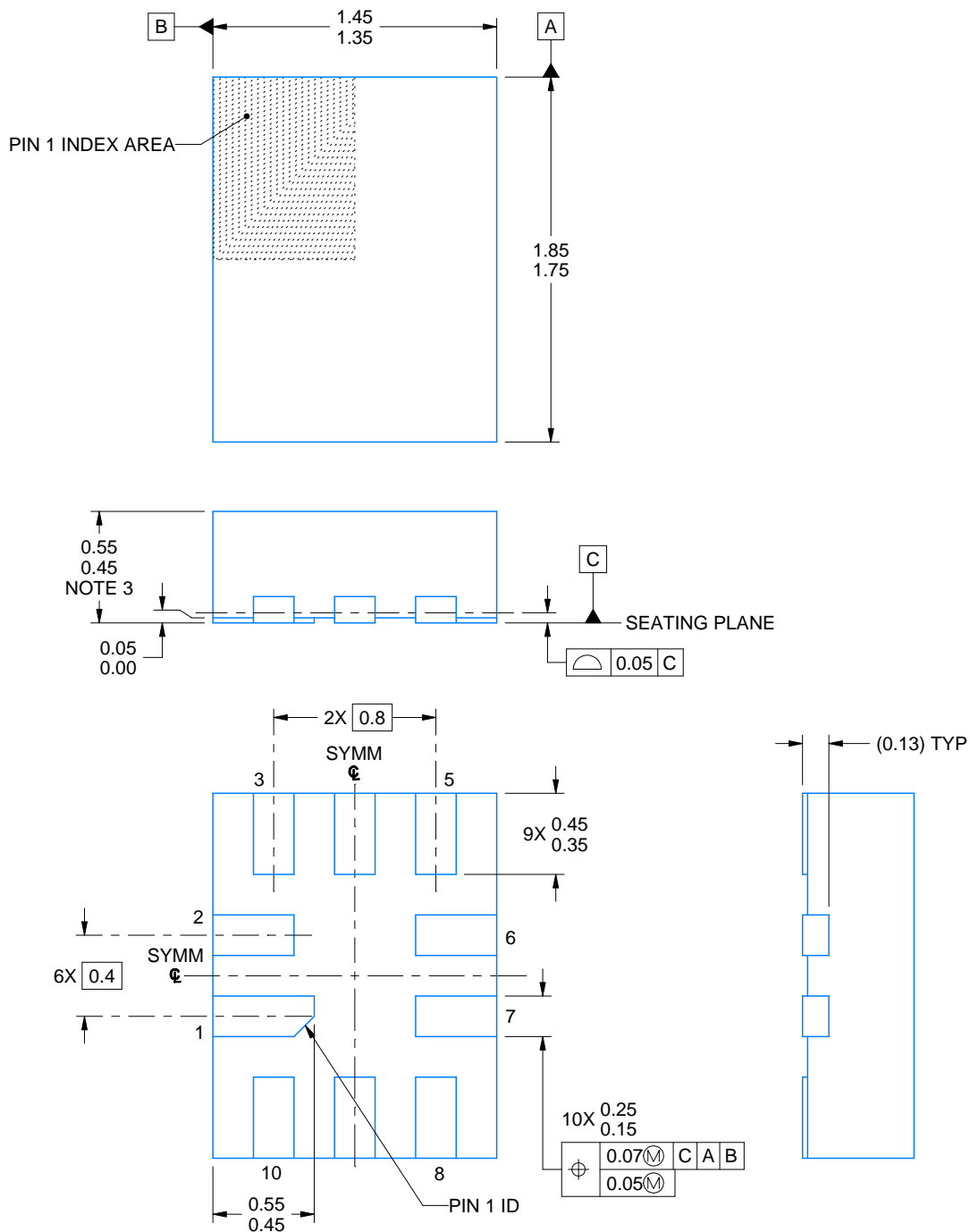


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T245RSWR	UQFN	RSW	10	3000	202.0	201.0	28.0

**RSW0010A****PACKAGE OUTLINE****UQFN - 0.55 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4224897/A 03/2019

**NOTES:**

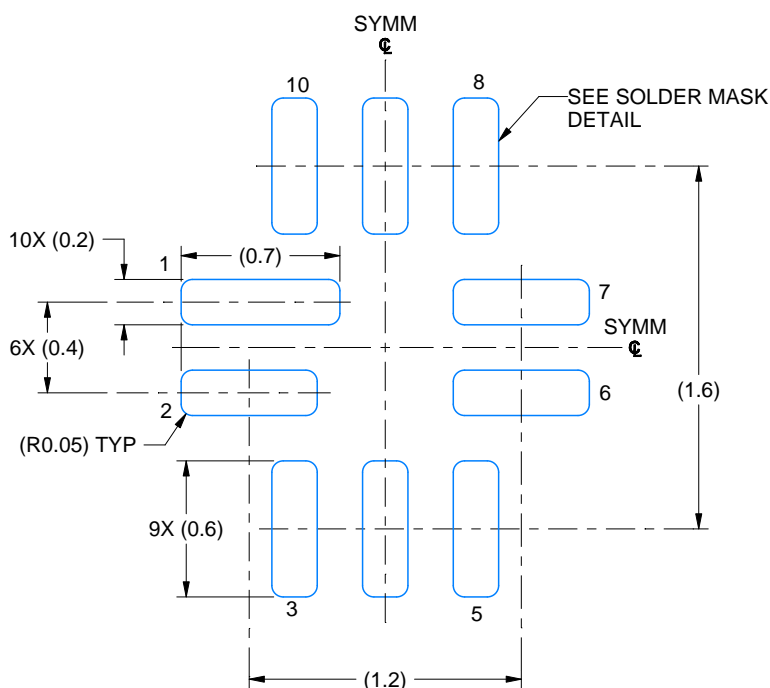
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

# EXAMPLE BOARD LAYOUT

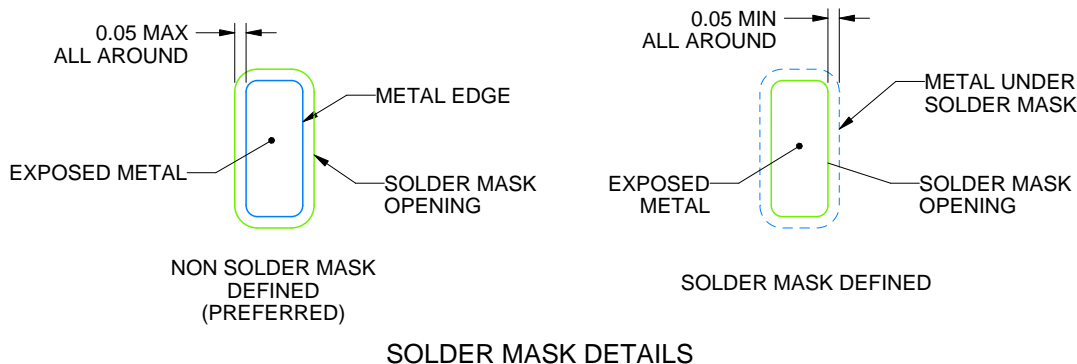
RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X



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NOTES: (continued)

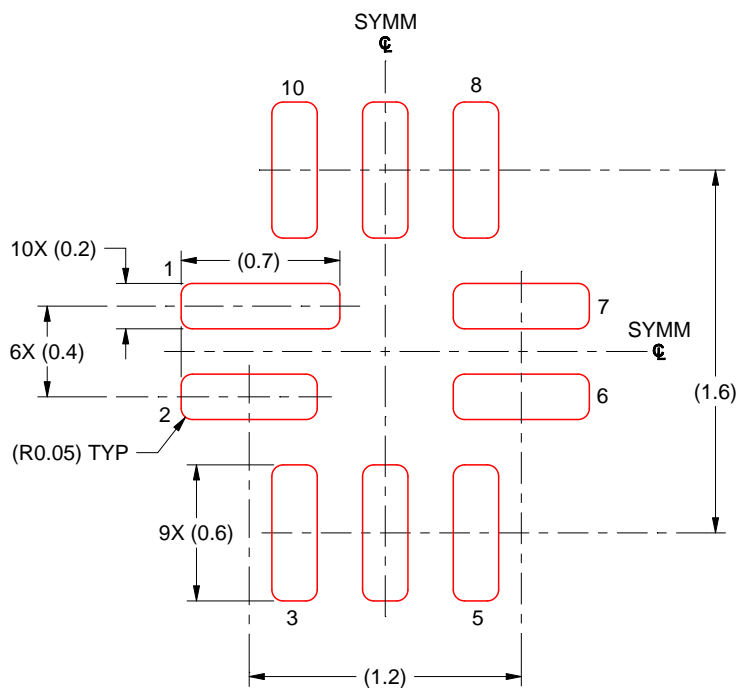
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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