Low-Power 3.3V-Supply Full-Duplex RS-485 Driver/Receiver

Check for Samples: SN65HVD37

FEATURES

- **Low-Current Standby Mode: <1 μA Typical**
- **Operational Quiescent Current < 1 mA**
- **High Receiver Hysteresis for Noise Immunity (60 mV Typical)**
- **1/8 Unit-Load (Up to 256 Nodes on the Bus)**
- **Bus-pin ESD Protection Exceeds 15 kV HBM**
- **Driver Output Transition Times Optimized for Signaling Rate up to 20 Mbps**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **5V-Tolerant Logic Inputs**
- **Bus Idle, Open, and Short-Circuit Failsafe**
- **Driver Current Limiting and Thermal Shutdown**
- **Fully Meets All TIA-485-A Specifications**

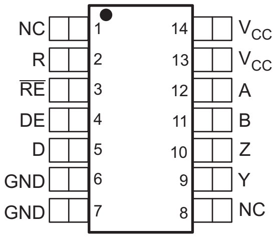
APPLICATIONS

- **Telecommunications Equipment**
- **Industrial Automation**
- **Process Automation**
- **Building Automation**
- **Point-of-Sale (POS) Terminals**
- **Improved Replacement for ADM3076, ADM3491, LTC2852, MAX3491 and SP3491**

DESCRIPTION

The SN65HVD37 combines a robust differential driver and a receiver with high noise immunity for demanding industrial applications. The driver differential outputs and the receiver differential inputs are separate pins, to form a bus port for full-duplex (four-wire) communications. The driver and receiver can be independently enabled, and feature a wide common-mode voltage range, making this device suitable for multi-point applications over long cable runs. The SN65HVD37 is characterized over the temperature range of -40ºC to 85 ºC.

D PACKAGE (TOP VIEW)



NC - No internal connection

LOGIC DIAGRAM (POSITIVE LOGIC)

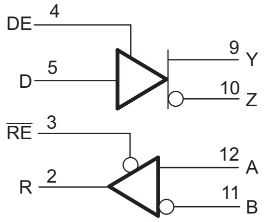


Figure 1. 60 mV Receiver Hysteresis for Noise Immunity

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

			VALUE/UNITS
V_{CC}	Supply voltage		–0.5 V to 7 V
	Voltage range at A, B, Y, Z pins		–13 V to 13 V
	Input voltage range at any logic pin		–0.3 V to 5.7 V
	Voltage range, transient pulse, A, B, Y, Z, through 100Ω		–25 V to 25 V
	Receiver output current		–24 mA to 24 mA
T_J	Junction temperature		170°C
	Continuous total power dissipation		(see Thermal Table)
	IEC 60749-26 ESD	(Human Body Model), bus terminals and GND	±16 kV
	JEDEC Standard 22	Test Method A114 (Human Body Model), all pins	±5 kV
		Test Method C101 (Charged Device Model), all pins	±1.5 kV
	JEDEC Standard 22	Test Method A115 (Machine Model), all pins	±150 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		SN65HVD37	UNITS
		D	
		14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	79.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.8	
θ_{JB}	Junction-to-board thermal resistance	33.5	
ψ_{JT}	Junction-to-top characterization parameter	13.3	
ψ_{JB}	Junction-to-board characterization parameter	33.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(1)		3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode)(2)		–7		12	V
V_{IH}	High-level input voltage (Driver, driver enable, and receiver enable inputs)		2		VCC	V
V_{IL}	Low-level input voltage (Driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
	Signaling rate	HVD37			20	Mbps
T_A	Operating free-air temperature (See application section for thermal information)		–40		85	°C
T_J	Junction Temperature		–40		150	°C

(1) Both pins 13 and 14 should be connected to the supply voltage; both pins 6 and 7 should be connected to ground.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Driver differential output voltage magnitude	See Figure 1, R_L= 60 Ω, V_{CC} ≥ 3.15 V, 375 Ω on each output to –7 V to 12 V		1.5	1.9		V
		R_L = 54 Ω (RS-485)	See Figure 3	1.5	2		V
		R_L = 100 Ω (RS-422), T_J ≥ 25°C, V_{CC} ≥ 3.3 V		2	2.2		V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF		–0.1	0	0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors, C_L = 50 pF	See Figure 3	1.5	V_{CC} /2	2.5	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–0.1	0	0.1	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				400		mV
C_{ID}	Differential input capacitance	A, B			3		pF
C_{OD}	Differential output capacitance	Y, Z			14		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See [1]	–60	–20	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold			–200	–120	See [1]	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$)			30	60		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC}-0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	μA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	μA
I_{OS}	Driver short-circuit output current			–250		250	mA
I_I	Bus input current (disabled driver)	V_{CC} = 3 to 3.6 V or V_{CC} =0 V, DE at 0 V	V_I = 12 V		75	125	μA
			V_I = –7 V	–100	–40		
I_{CC}	Supply current, steady-state, no load (quiescent)	Driver and Receiver enabled	DE = V_{CC}, RE = GND		720	850	μA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}			400	μA
		Driver disabled, receiver enabled	DE = GND, RE = GND			800	μA
		Driver and receiver disabled (standby)	DE = GND, D = open, RE = V_{CC}		0.2	1	μA
	Supply current (dynamic)	See “TYPICAL CHARACTERISTICS” section					

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than $V_{IT–}$.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 4		3	6	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay				10	20	
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					1	
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 5 and Figure 6			20	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 5 and Figure 6		8	25	ns
		Receiver disabled			2.6	8	μs
RECEIVER							
t_r , t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 7		2	5	9	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			40	50	75	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				2	5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	25	ns
$t_{PZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 8			35	50	ns
		Driver disabled, See Figure 8			3	8	μs

DRIVER FUNCTION TABLE

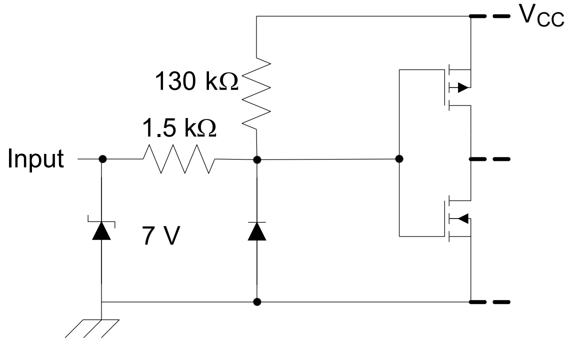
INPUT	ENABLE	OUTPUTS		
D	DE	Y	Z	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

RECEIVER FUNCTION TABLE

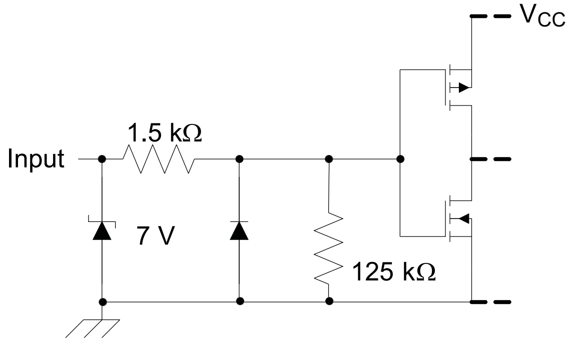
DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

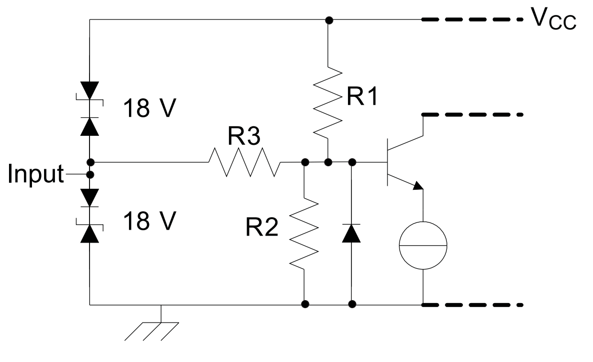
$\overline{\text{RE}}$ Input



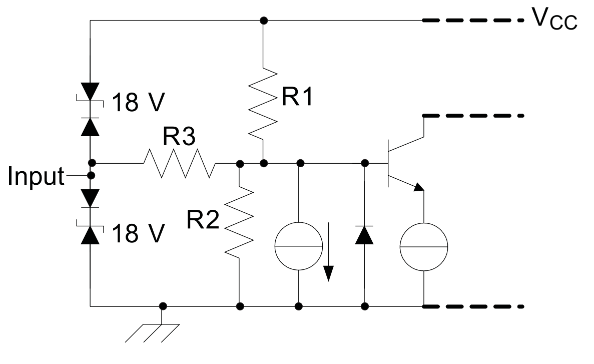
D and DE Input



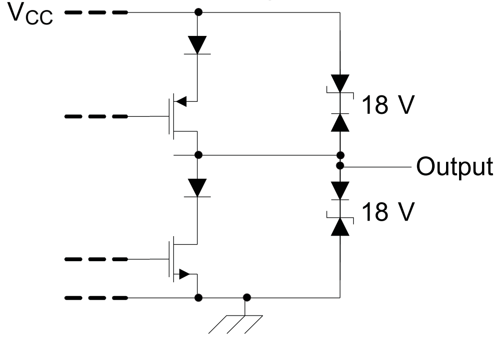
A Input



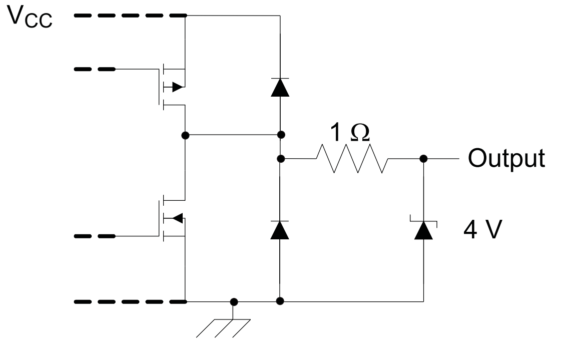
B Input



Y and Z Outputs



R Output



	R1/R2	R3
SN65HVD37	18 kΩ	190 kΩ

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω

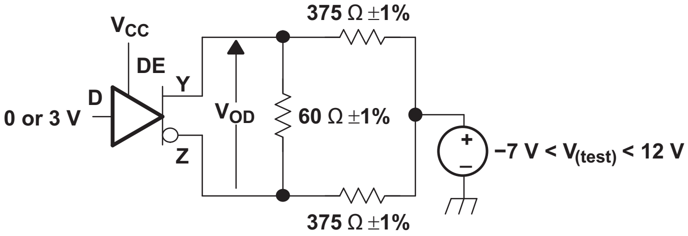
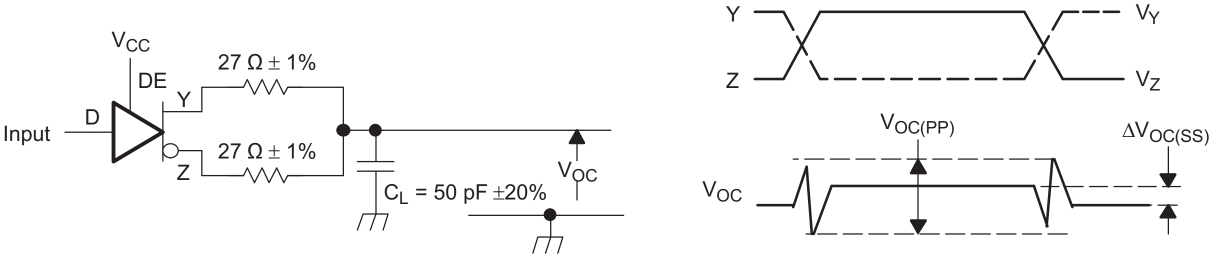


Figure 2. Measurement of Driver Differential Output Voltage With Common-mode Load



C_L Includes Fixture and Instrumentation Capacitance

Figure 3. Measurement of Driver Differential and Common-mode Output with RS-485 Load

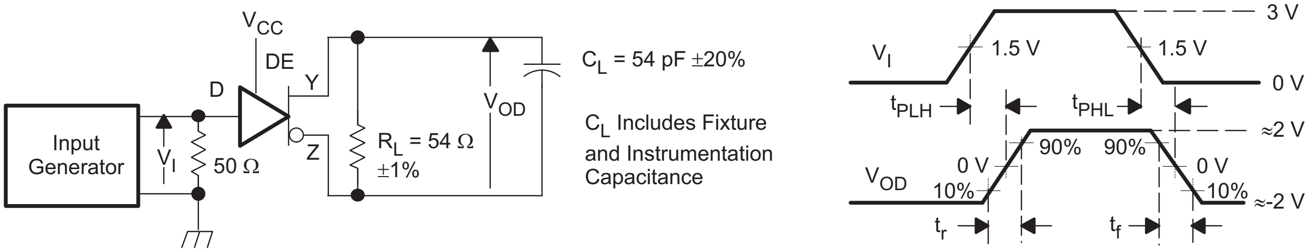
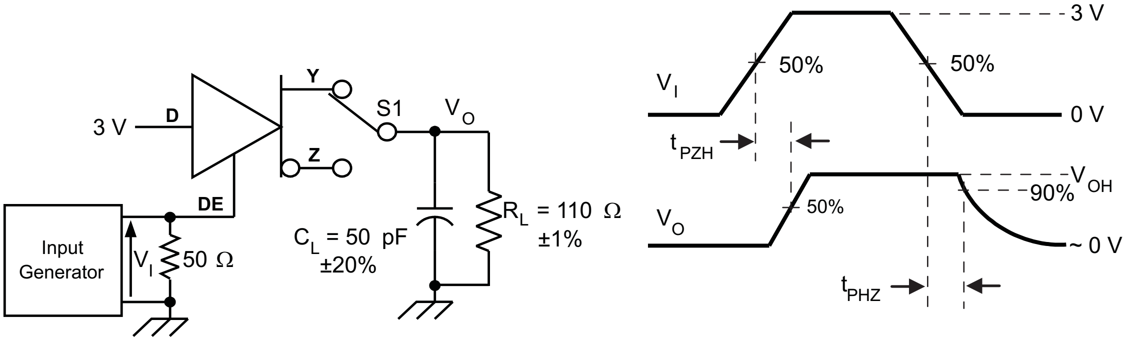


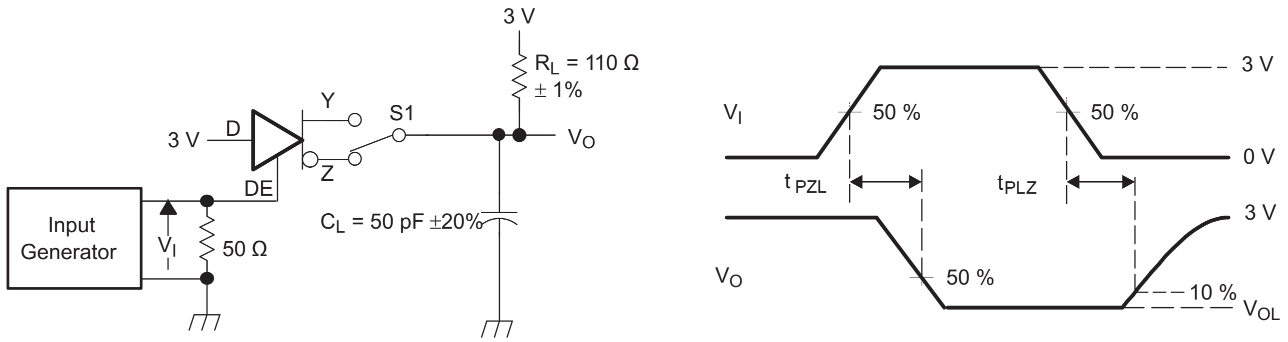
Figure 4. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.
C_L includes Fixture and Instrumentation Capacitance

Figure 5. Measurement of Driver Enable and Disable Times with Active High Output and Pull-down Load

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

C_L Includes Fixture and Instrumentation Capacitance

Figure 6. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-up Load

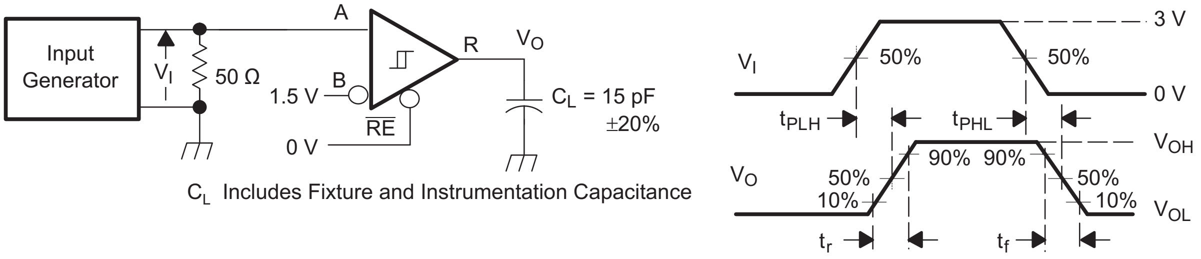


Figure 7. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

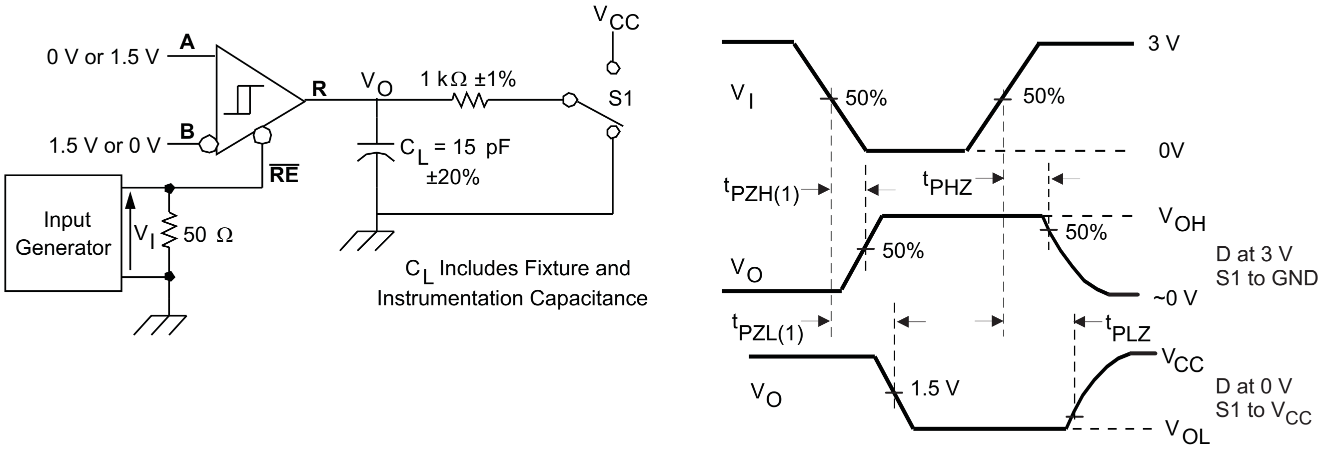


Figure 8. Measurement of Receiver Enable/Disable Times

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SIGNALING RATE

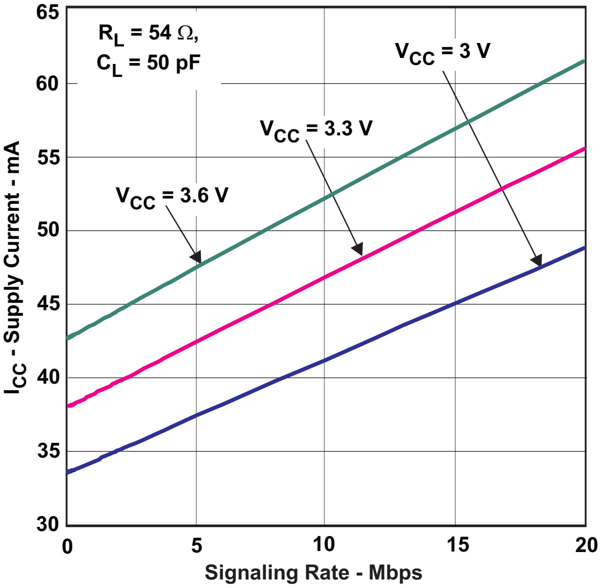


Figure 9.

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL OUTPUT CURRENT

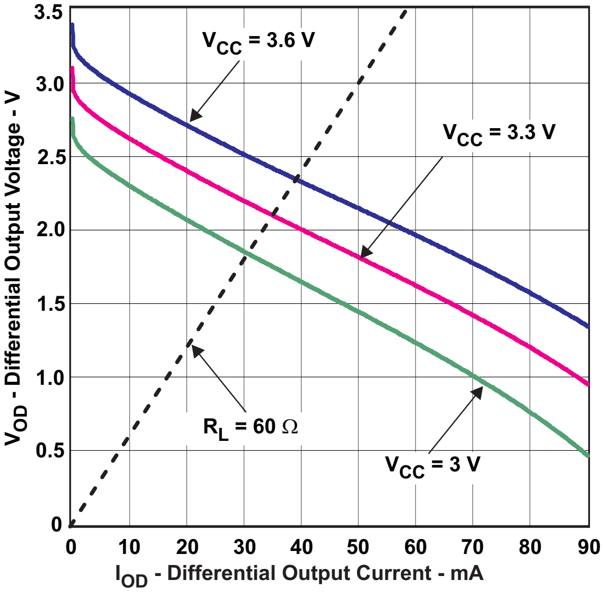


Figure 10.

RECEIVER OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

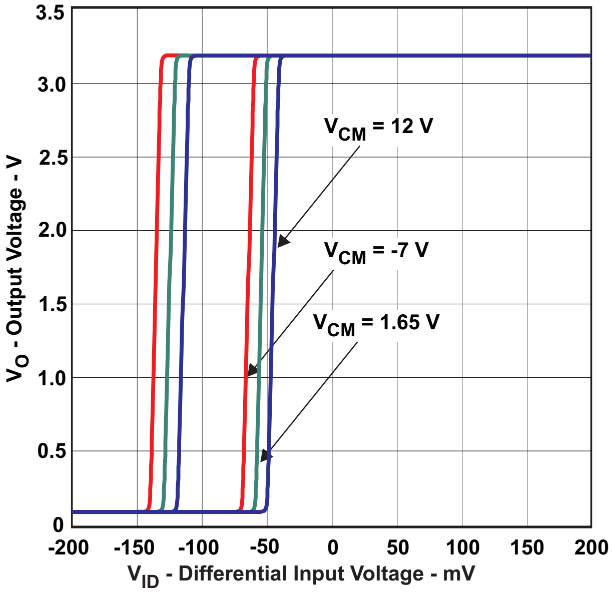


Figure 11.

RECEIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE

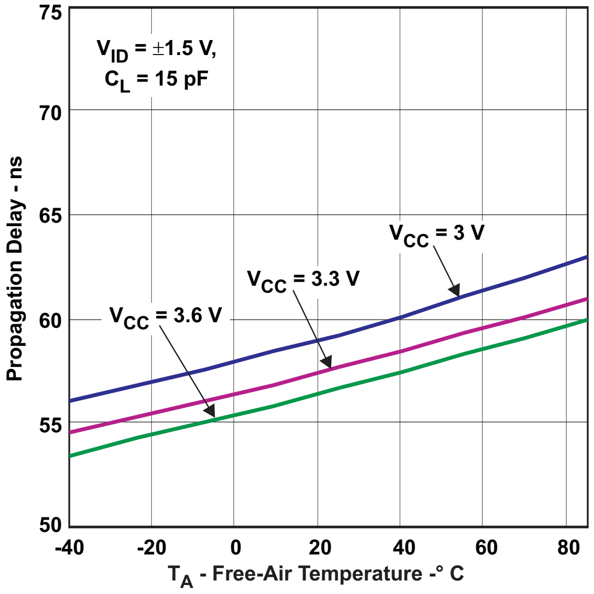


Figure 12.

TYPICAL CHARACTERISTICS (continued)

DRIVER RISE/FALL TIME
vs
FREE-AIR TEMPERATURE

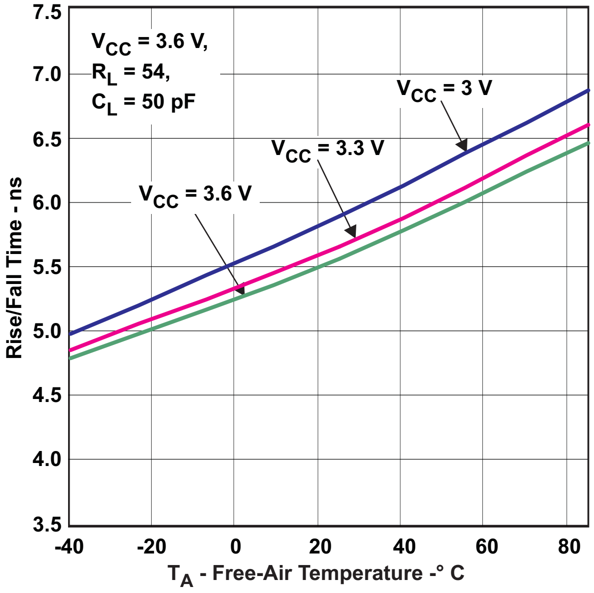


Figure 13.

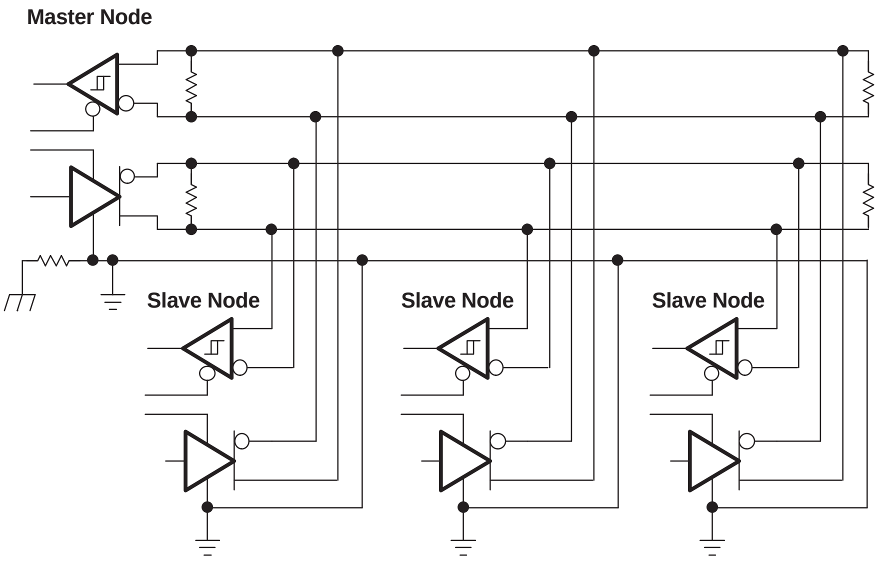


Figure 14. Example Full-Duplex Master/Slave Application Circuit

APPLICATION INFORMATION

RECEIVER FAILSAFE

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the HVD37, receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. In the Electrical Characteristics table, V_{IT-} has a typical value of -120 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of V_{IT+} is -60mV, and V_{IT+} is never more positive than -20 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

For the HVD37, the typical noise immunity is about 120 mV, which is the negative noise level needed to exceed the V_{IT-} threshold (V_{IT-} TYP = -120 mV). In the worst case, the failsafe noise immunity is never less than 50 mV, which is set by the maximum positive threshold (V_{IT+} MAX = -20mV) plus the minimum hysteresis voltage (V_{HYS} MIN = 30 mV).

HOT-PLUGGING

These devices are designed to operate in “hot swap” or “hot pluggable” applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLE, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

LOW POWER STANDBY MODE

As is customary with RS-485 devices, the receiver output is directly enabled/disabled by $\overline{\text{RE}}$, and the driver outputs are directly enabled/disabled by DE.

When both the driver and receiver are disabled, (DE=LO and $\overline{\text{RE}}$=HI) the receiver differential comparator stage enters a standby mode for reduced power.

When either the Driver or Receiver is enabled, the receiver differential comparator stage is enabled for fast response to signal changes.

REVISION HISTORY

Changes from Original (October 2011) to Revision A	Page
• Changed the device From: Product Preview To: Production	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD37D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37
SN65HVD37DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD37

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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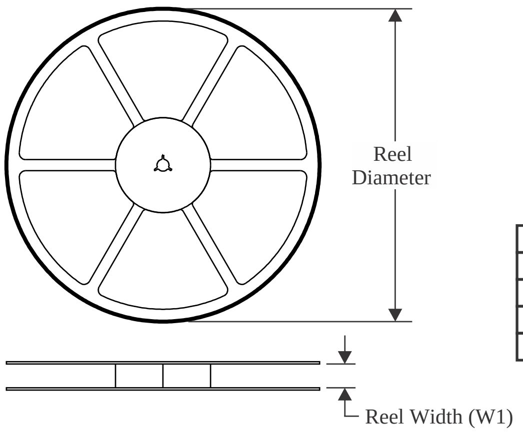
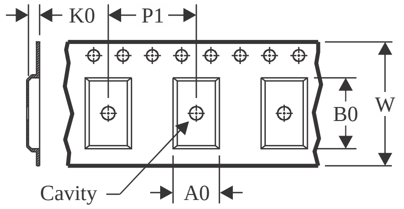
TAPE AND REEL INFORMATION

REEL DIMENSIONS

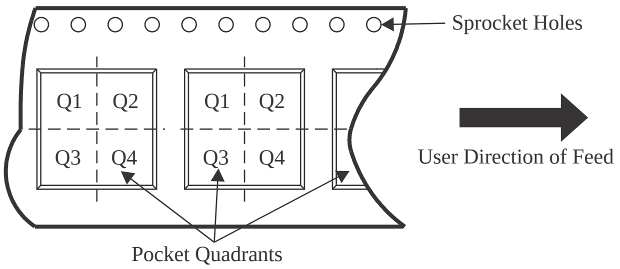


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

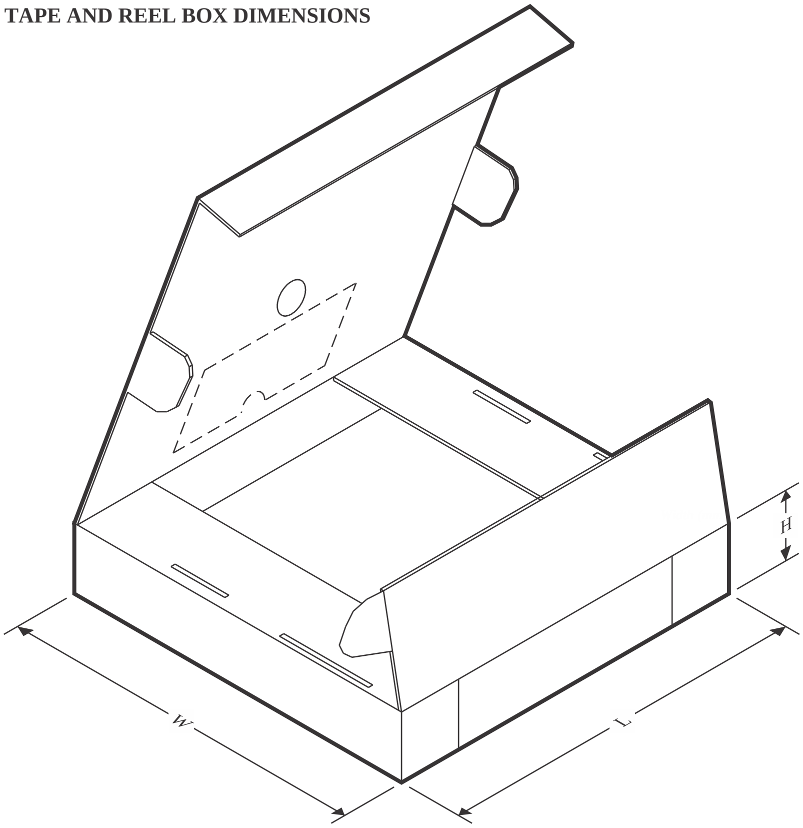
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD37DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD37DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

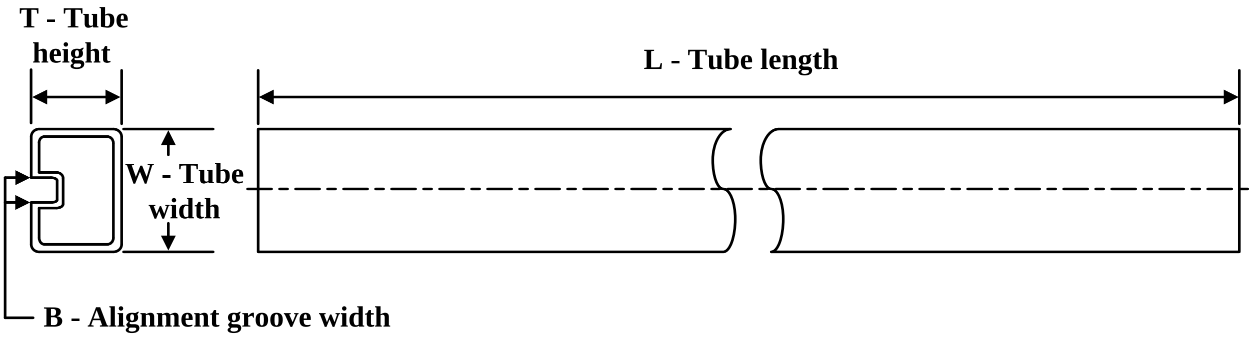
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

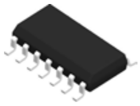
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD37DR	SOIC	D	14	2500	353.0	353.0	32.0
SN65HVD37DRG4	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD37D	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD37D.A	D	SOIC	14	50	506.6	8	3940	4.32

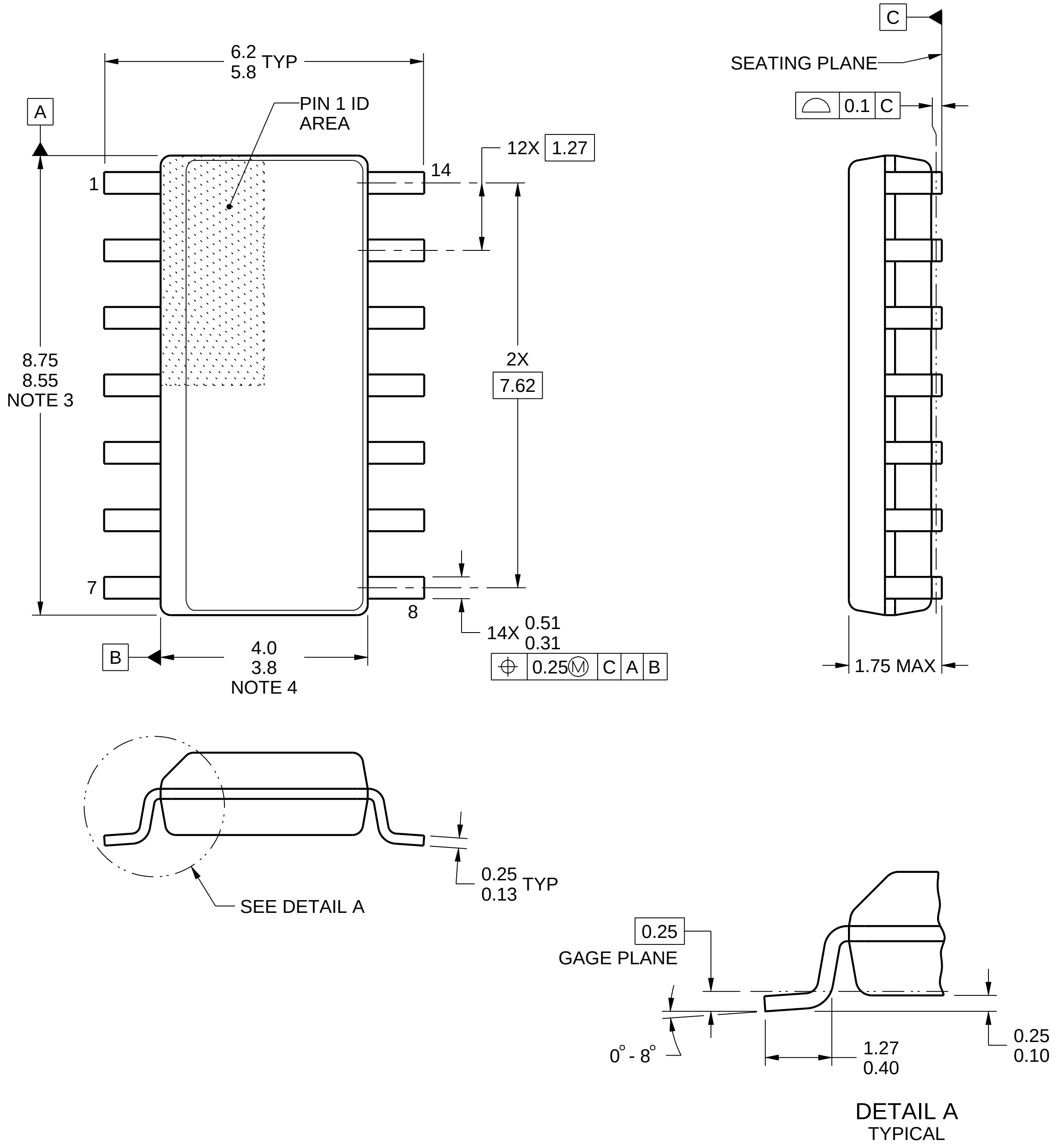


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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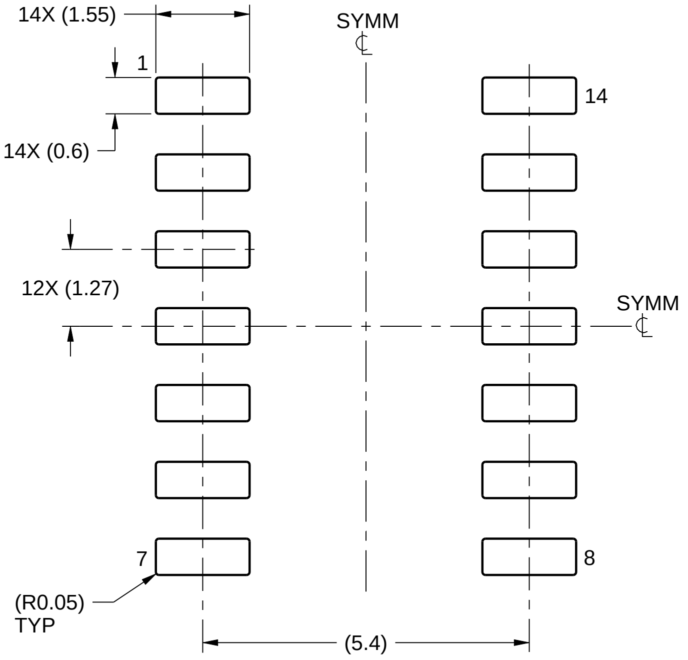
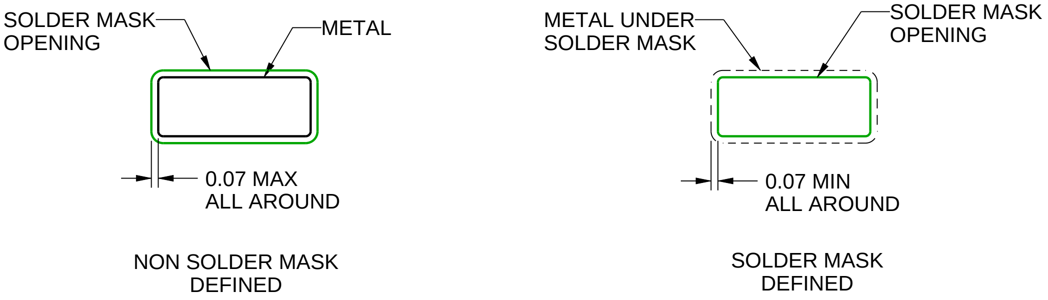
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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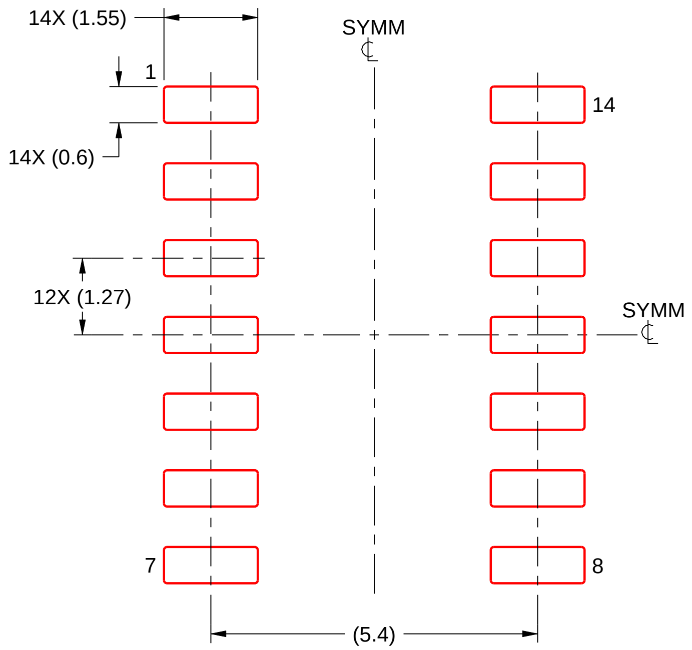
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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