

# REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer

## 1 Features

- Excellent temperature drift performance
  - 5ppm/°C (maximum) from –40°C to +125°C
- Extremely low noise
  - Total noise: 5μV<sub>RMS</sub> with 47μF capacitor
  - 1/f noise (0.1Hz to 10Hz): 3μV<sub>PP</sub>/V
- Integrated ADC drive buffer
  - Low output impedance: < 50mΩ (0kHz to 200kHz)
  - First sample precise to 18 bits with [ADS8881](#)
  - Enables burst-mode DAQ systems
- Low supply current: 820μA
- Low shutdown current: 1μA
- High initial accuracy: ±0.05%
- Very-low noise and distortion
  - SNR: 100.5dB, THD: –125dB ([ADS8881](#))
  - SNR: 106dB, THD: –120dB ([ADS127L01](#))
- Output current drive: ±4mA
- Programmable short-circuit current
- Verified to drive REF pin of [ADS88xx family](#) of SAR ADCs and [ADS127xx family](#) of wideband ΔΣ ADCs

## 2 Applications

- [ATE testers and oscilloscopes](#)
- [Test and measurement equipment](#)
- [Analog input modules for PLCs](#)
- [Medical equipment](#)
- [Precision data acquisition systems](#)

## 3 Description

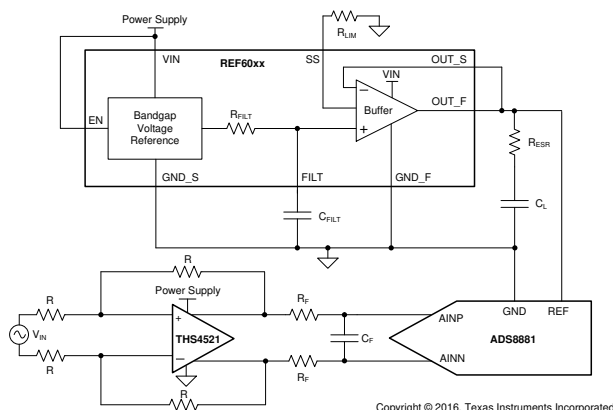
The REF6000 family of voltage references have an integrated low output impedance buffer that enable the user to directly drive the REF pin of precision data converters, while preserving linearity, distortion, and noise performance. Most precision SAR and Delta-Sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. To support this dynamic load the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF6000 family devices are an excellent choice, but not limited, to drive the REF pin of the [ADS88xx family](#) of SAR ADCs, and [ADS127xx family](#) of delta-sigma ADCs, as well as other digital-to-analog converters (DACs).

The REF6000 family of voltage references are able to maintain an output voltage within 1LSB (18-bit) with minimal droop, even during the first conversion while driving the REF pin of the ADS8881. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. The REF60xx variants of REF6000 family specify a maximum temperature drift of just 5ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low output impedance buffer combined. For various temperature drift options in REF6000 family, see the [Device Comparison Table](#).

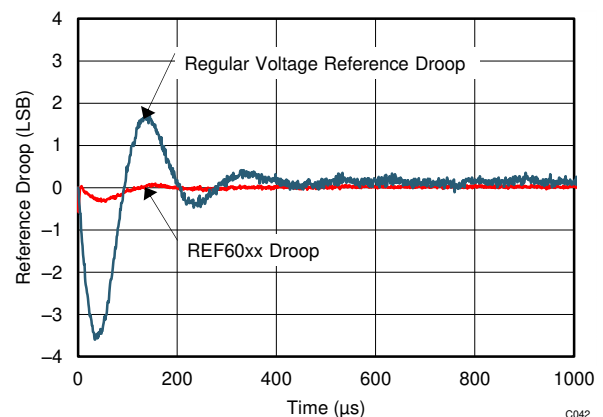
### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
REF60xx	DGK (VSSOP, 8)	3.00mm × 4.90mm

- (1) For more information, see [Section 12](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application



Reference Droop Comparison (1LSB = 19.07μV, with ADS8881 at 1MSPS)



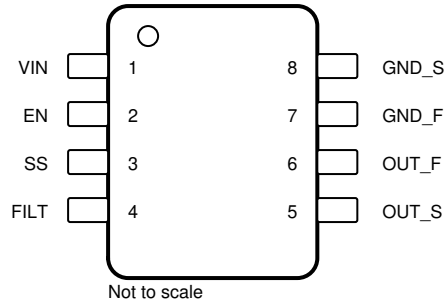
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## 4 Device Comparison Table

DEVICE FAMILY	TEMPERATURE DRIFT
REF60xx	5ppm/°C from –40 to 125°C
REF61xx	8ppm/°C from –40 to 125°C
REF62xx	3ppm/°C from 0 to 70°C

## 5 Pin Configuration and Functions



**Figure 5-1. DGK Package 8-Pin VSSOP Top View**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Input	Enable pin
FILT	4	—	Filter capacitor pin. A capacitor ( $C_{FILT} \geq 1 \mu F$ ) must be connected between the FILT pin and ground for stability.
GND_F	7	Ground	Ground force pin
GND_S	8	Ground	Ground sense pin
OUT_F	6	Output	Output voltage force pin
OUT_S	5	Input	Output voltage sense pin
SS	3	—	Short circuit current limit pin. Connect a resistor to this pin to set the output short-circuit current limit. Connect to VIN pin for highest current limit
VIN	1	Power	Input supply voltage pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	$V_{IN}$	-0.3	6	V
	$V_{EN}$	-0.3	$V_{IN} + 0.3$	V
Operating temperature, $T_A$		-55	150	°C
Junction temperature, $T_j$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{IN}$ Supply input voltage ( $I_{OUT} = 0\text{mA}$ )	REF6025	3		5.5	V
	REF6030, REF6033, REF6041, REF6045	$V_{OUT} + 0.25$		5.5	
	REF6050	5.3		5.5	
$V_{EN}$ Enable voltage		0		$V_{IN}$	V
$I_L$ Output current	REF6025, REF6030, REF6033, REF6041	-4		4	mA
	REF6045	-3.5		3.5	
	REF6050	-3		3	
$T_A$ Operating temperature		-40	25	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		REF60xx	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	5.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	78.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$  for all devices except REF6050,  $V_{IN} = 5.4\text{V}$  for REF6050,  $I_L = 0\text{mA}$ ,  $C_L = 22\ \mu\text{F}$ ,  $C_{FILT} = 1\ \mu\text{F}$ , and  $V_{EN} = 5\text{V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>ACCURACY AND DRIFT</b>							
Output voltage accuracy				-0.05%		0.05%	
Output voltage temperature coefficient <sup>(1)</sup>						5	ppm/°C
<b>LINE AND LOAD REGULATION</b>							
$\Delta V_{O(\Delta V)}$ Line regulation	REF6025	$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$	$T_A = 25^\circ\text{C}$		4	20	ppm/V
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6030, REF6033, REF6041, REF6045	$V_{OUT} + 0.25\text{V} \leq V_{IN} \leq 5.5\text{V}$	$T_A = 25^\circ\text{C}$		4	20	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6050	$V_{OUT} + 0.3\text{V} \leq V_{IN} \leq 5.5\text{V}$	$T_A = 25^\circ\text{C}$		7	60	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			120	
$\Delta V_{O(\Delta I)}$ Load regulation, sourcing and sinking	REF6025, REF6030, REF6033, REF6041	$I_L = 0\text{mA}$ to $4\text{mA}$ , $V_{IN} = V_{OUT} + 600\text{mV}$	$T_A = 25^\circ\text{C}$		2	20	ppm/mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6045	$I_L = 0\text{mA}$ to $3.5\text{mA}$ , $V_{IN} = V_{OUT} + 600\text{mV}$	$T_A = 25^\circ\text{C}$		2	20	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6050	$I_L = 0\text{mA}$ to $3\text{mA}$ , $V_{IN} = V_{OUT} + 400\text{mV}$	$T_A = 25^\circ\text{C}$		2	20	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			50	
$I_{SC}$ Short-circuit current	SS = open				10.5		mA
<b>NOISE</b>							
Total integrated noise	$C_L = 22\ \mu\text{F}$				5		$\mu\text{V}_{RMS}$
	$C_L = 47\ \mu\text{F}$				5		
Low frequency noise	$0.1\text{Hz} \leq f \leq 10\text{Hz}$				3		$\mu\text{V}_{pp}/\text{V}$
<b>OUTPUT IMPEDANCE</b>							
Output impedance	$f = \text{DC}$ to $200\text{kHz}$ , $C_L = 47\ \mu\text{F}$				50		m $\Omega$
<b>TURN-ON TIME</b>							
$t_{on}$ Turn-on time	0.1% settling, $C_L = 47\ \mu\text{F}$ , SS = open, REF6025				100		ms
<b>HYSTERESIS AND LONG TERM DRIFT</b>							
Long term stability	0 to 1000h at $25^\circ\text{C}$				80		ppm
	1000h to 2000h at $25^\circ\text{C}$				20		
Output voltage hysteresis <sup>(2)</sup>	25°C, -40°C, 125°C, 25°C (cycle 1)				33		ppm
	25°C, -40°C, 125°C, 25°C (cycle 2)				8		
<b>CAPACITIVE LOAD</b>							
$C_L$ Stable output capacitor value					10	47	$\mu\text{F}$

## 6.5 Electrical Characteristics (continued)

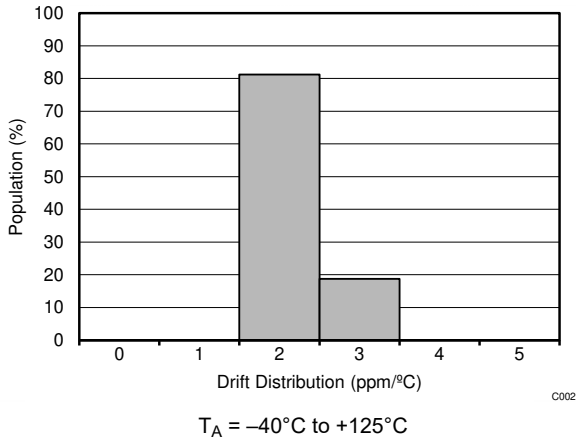
at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$  for all devices except REF6050,  $V_{IN} = 5.4\text{V}$  for REF6050,  $I_L = 0\text{mA}$ ,  $C_L = 22\ \mu\text{F}$ ,  $C_{FILT} = 1\ \mu\text{F}$ , and  $V_{EN} = 5\text{V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OUTPUT VOLTAGE</b>							
$V_{OUT}$	Output voltage	REF6025			2.5		V
		REF6030			3		
		REF6033			3.3		
		REF6041			4.096		
		REF6045			4.5		
		REF6050			5		
<b>POWER SUPPLY</b>							
$I_{CC}$	Supply current	REF6025, REF6030, REF6033, REF6041	Active mode, $V_{EN} = 5\text{V}$	$T_A = 25^\circ\text{C}$	0.82	0.90	mA
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1.1	
		REF6045, REF6050	Active mode, $V_{EN} = 5\text{V}$	$T_A = 25^\circ\text{C}$	0.83	0.95	mA
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1.15	
		Shutdown mode, $V_{EN} = 0\text{V}$		$T_A = 25^\circ\text{C}$	1	3	$\mu\text{A}$
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		15	
Enable pin voltage		Voltage reference in active mode ( $EN = 1$ )		1.6			V
		Voltage reference in shutdown mode ( $EN = 0$ )				0.6	
Enable pin current		$V_{EN} = 5\text{V}$			100	150	nA
Dropout voltage		REF6025		$I_L = 0\text{mA}$	500	500	mV
				$I_L = 4\text{mA}$		600	
		REF6030, REF6033, REF6041		$I_L = 0\text{mA}$	50	250	
				$I_L = 4\text{mA}$		600	
		REF6045		$I_L = 0\text{mA}$	50	250	
				$I_L = 3.5\text{mA}$		600	
		REF6050		$I_L = 0\text{mA}$	100	300	
				$I_L = 3\text{mA}$		400	

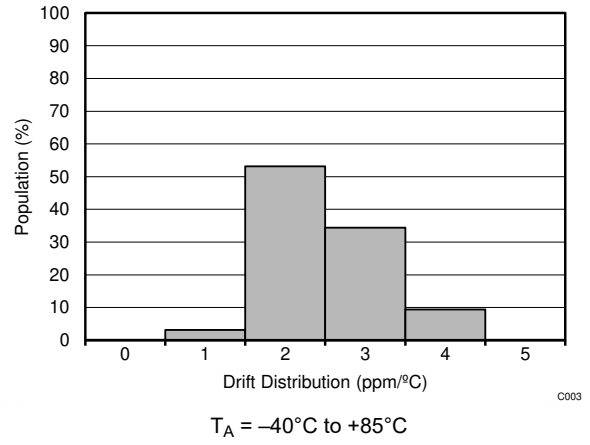
- (1) Temperature drift is specified according to the box method. See [Section 8.3](#) for more details.  
(2) See [Section 7.2](#).

## 6.6 Typical Characteristics

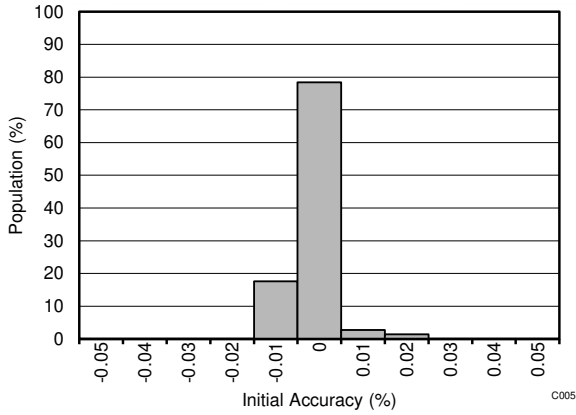
at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)



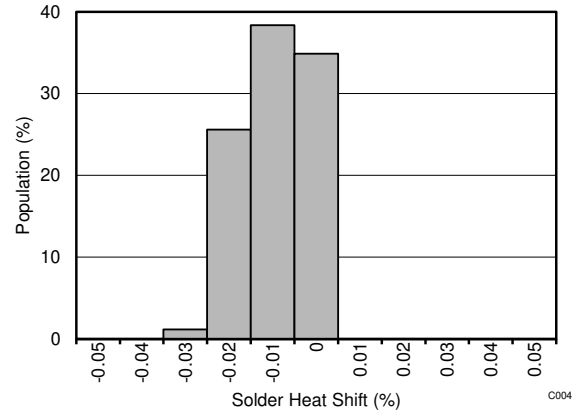
**Figure 6-1. Drift Distribution**



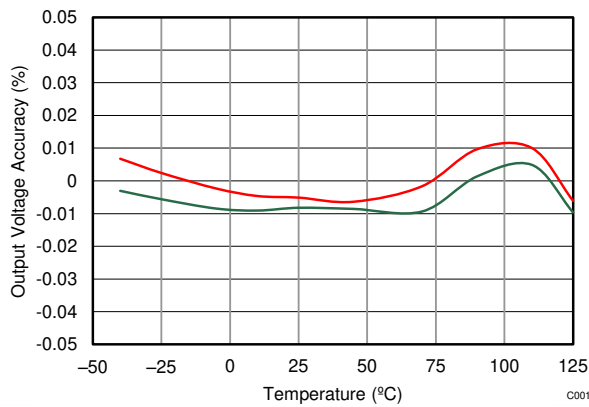
**Figure 6-2. Drift Distribution**



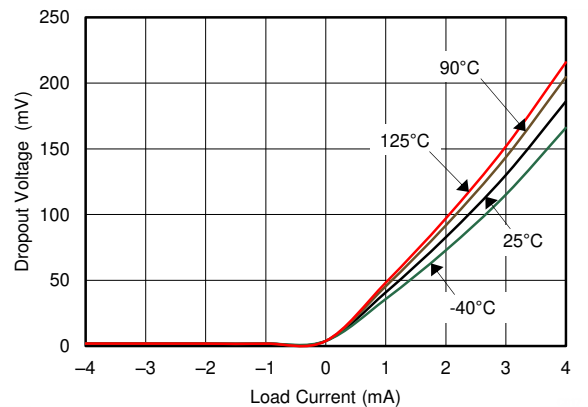
**Figure 6-3. Initial Accuracy Distribution**



**Figure 6-4. Solder-Heat Shift Distribution**



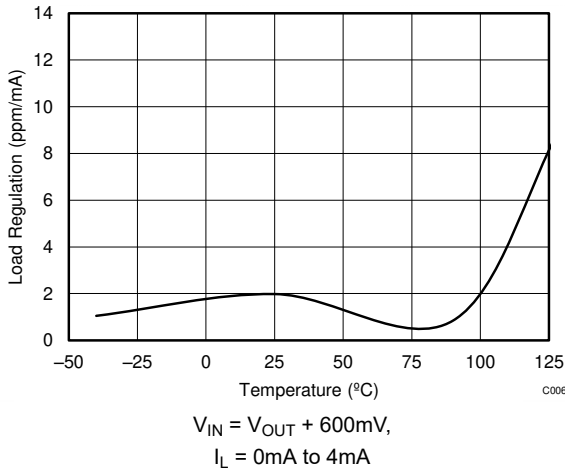
**Figure 6-5. Output Voltage Accuracy vs Temperature**



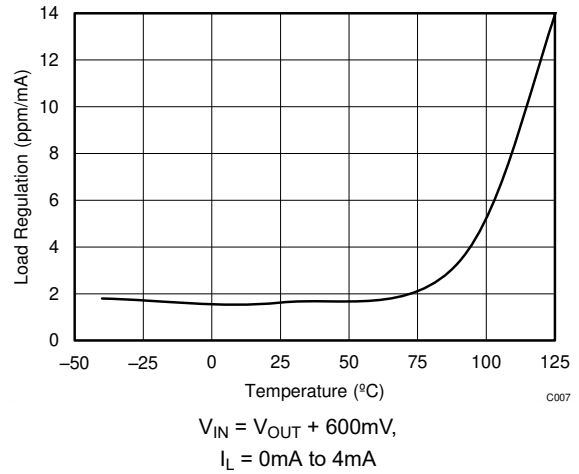
**Figure 6-6. Dropout Voltage vs Load Current**

### 6.6 Typical Characteristics (continued)

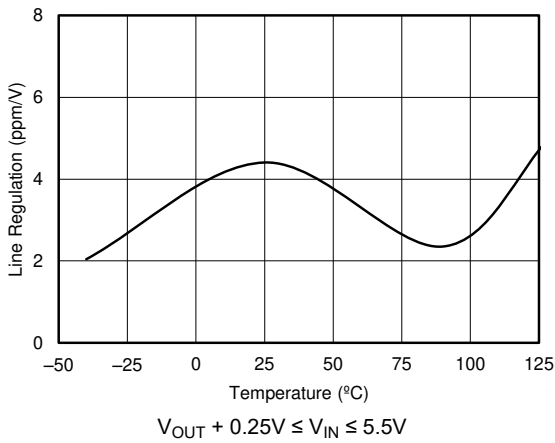
at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)



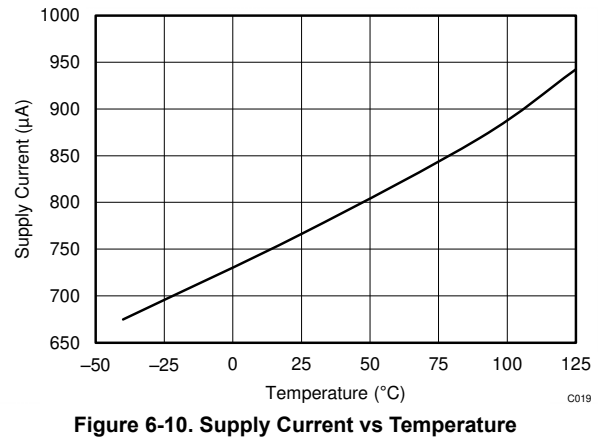
**Figure 6-7. Load Regulation Sourcing vs Temperature**



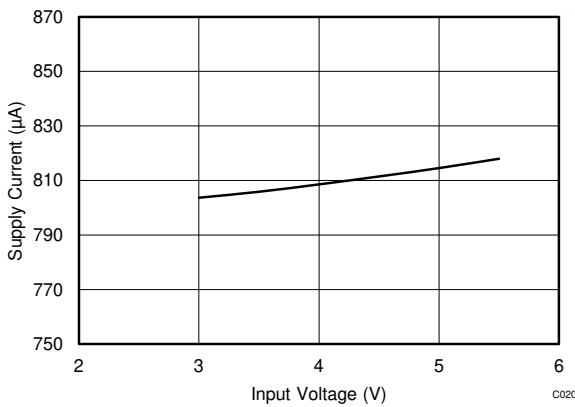
**Figure 6-8. Load Regulation Sinking vs Temperature**



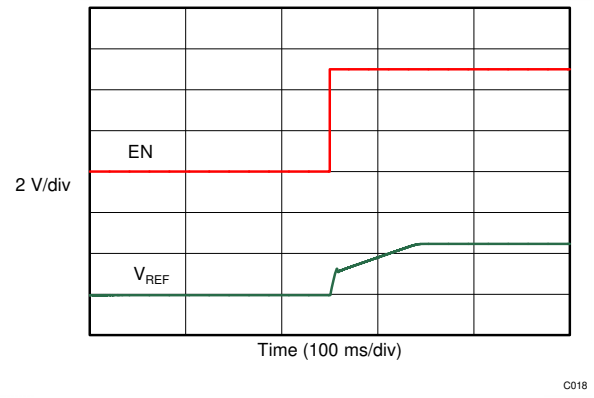
**Figure 6-9. Line Regulation vs Temperature**



**Figure 6-10. Supply Current vs Temperature**



**Figure 6-11. Supply Current vs Input Voltage**



**Figure 6-12. Turn-On Settling Time**

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)

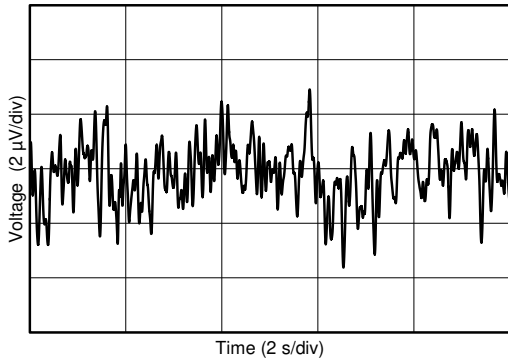


Figure 6-13. 0.1Hz to 10Hz Noise

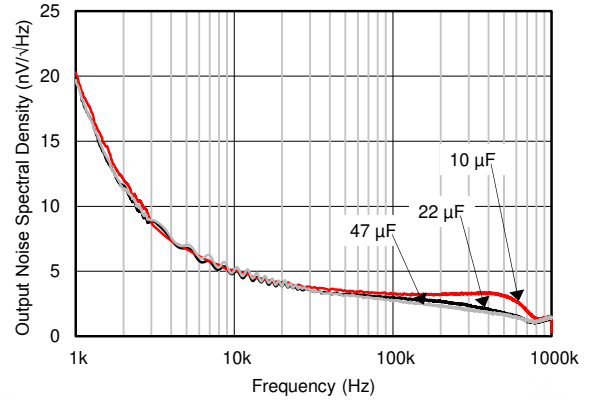


Figure 6-14. Output-Voltage Noise Spectrum

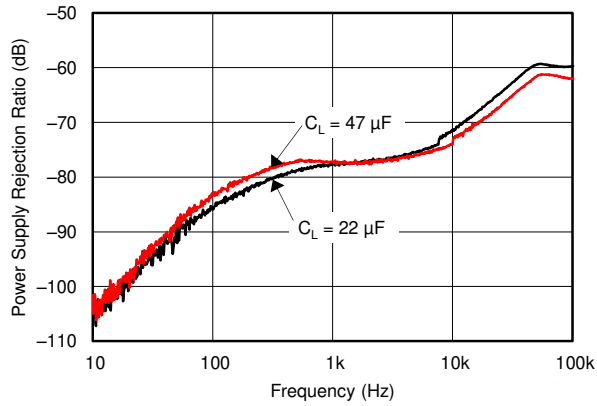
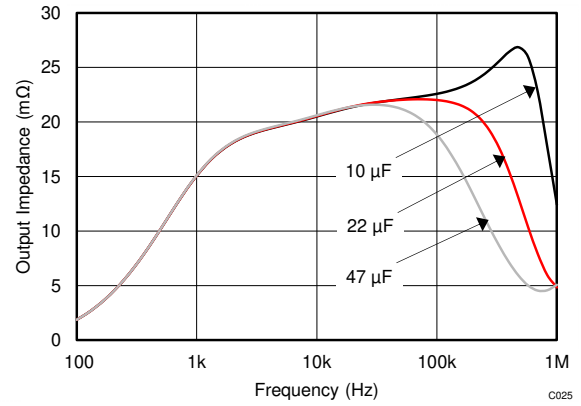
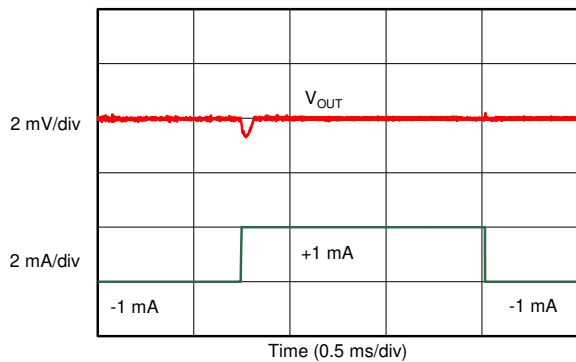


Figure 6-15. PSRR vs Frequency



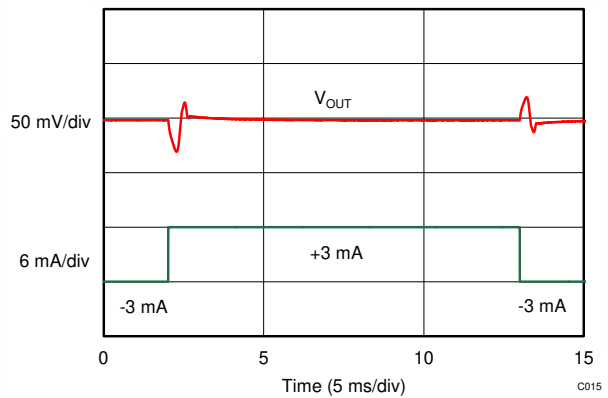
Graph obtained by design simulation

Figure 6-16. Output Impedance vs Frequency



Load current =  $\pm 1\text{mA}$

Figure 6-17. Load Transient Response



Load current =  $\pm 3\text{mA}$

Figure 6-18. Load Transient Response

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)

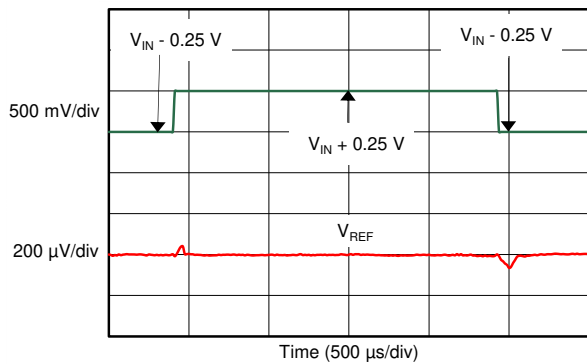


Figure 6-19. Line Transient Response

C013

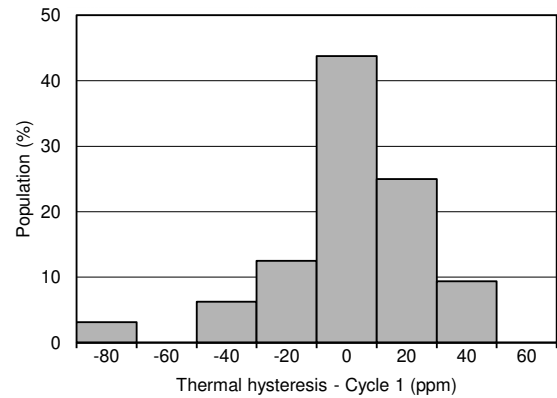


Figure 6-20. Thermal Hysteresis Distribution (Cycle 1)

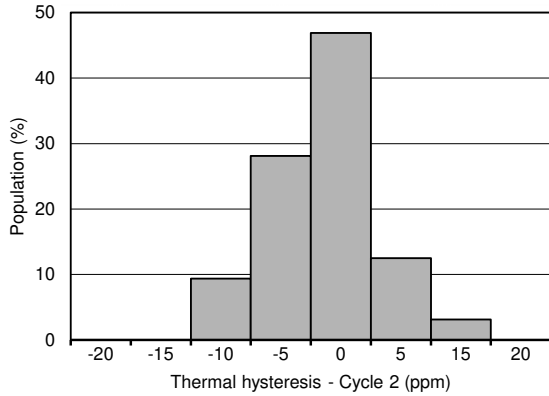


Figure 6-21. Thermal Hysteresis Distribution (Cycle 2)

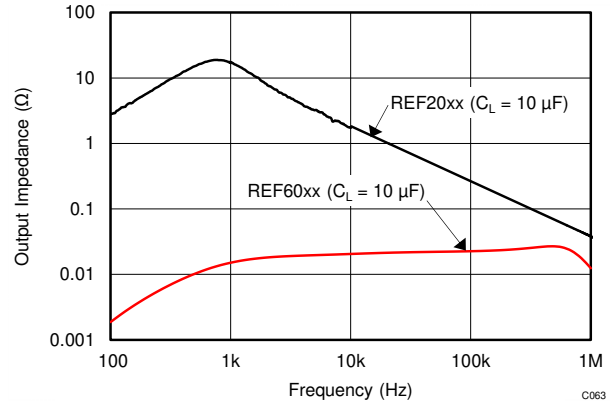
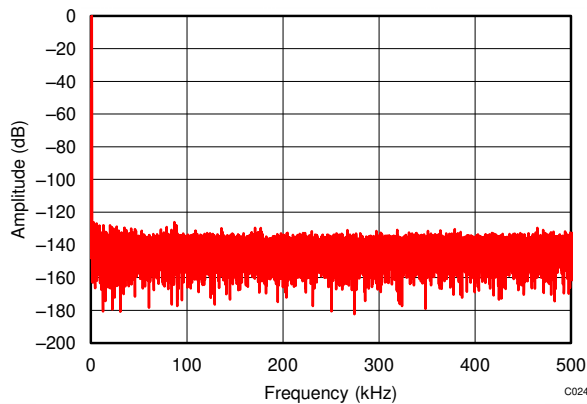


Figure 6-22. Output Impedance Comparison

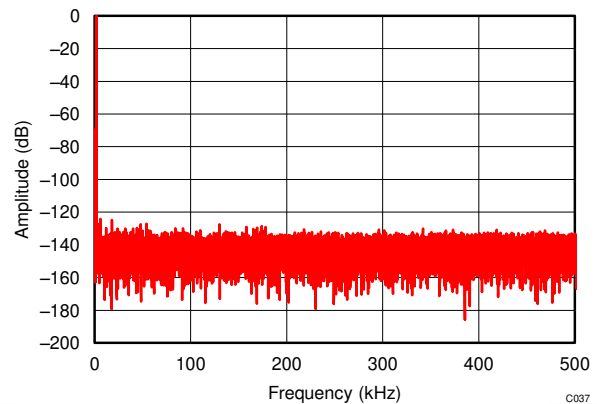
C063



REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 1\text{kHz}$ , SNR = 100.5dB, THD = -125.9dB

Figure 6-23. Typical FFT Plot

C024



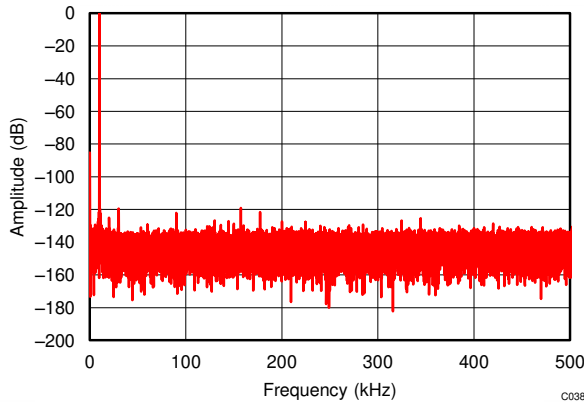
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 2\text{kHz}$ , SNR = 100.4dB, THD = -123.9dB

Figure 6-24. Typical FFT Plot

C037

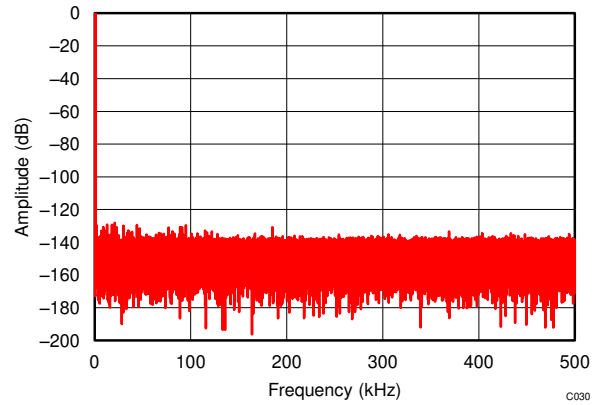
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)



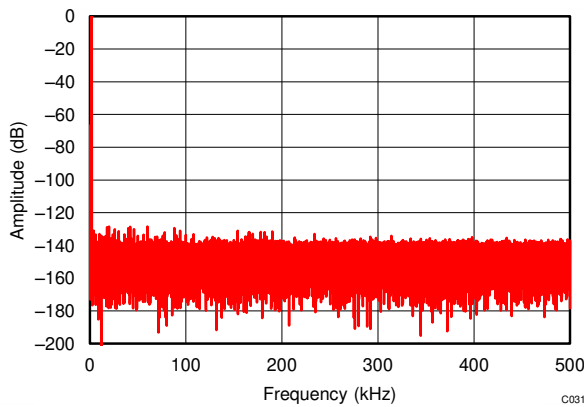
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{kHz}$ , SNR = 99.2dB, THD = -119.4dB

**Figure 6-25. Typical FFT Plot**



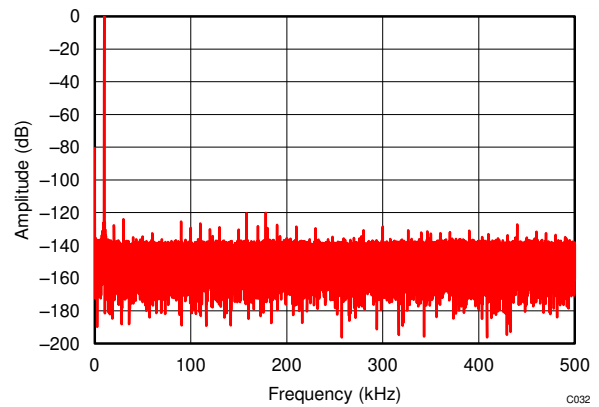
REF6041 driving REF pin of ADS8881,  
 $f_{IN} = 1\text{kHz}$ , SNR = 99dB, THD = -124.4dB

**Figure 6-26. Typical FFT Plot**



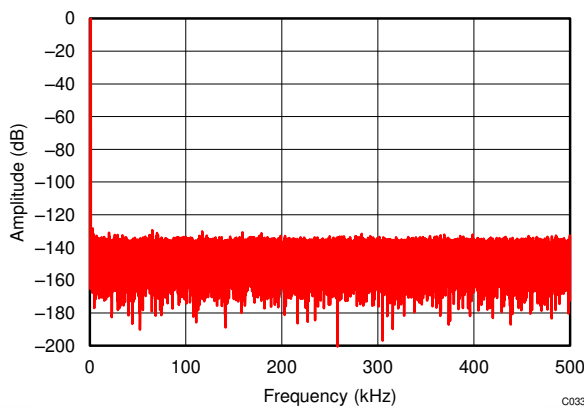
REF6041 driving REF pin of ADS8881,  
 $f_{IN} = 2\text{kHz}$ , SNR = 99dB, THD = -123.6dB

**Figure 6-27. Typical FFT Plot**



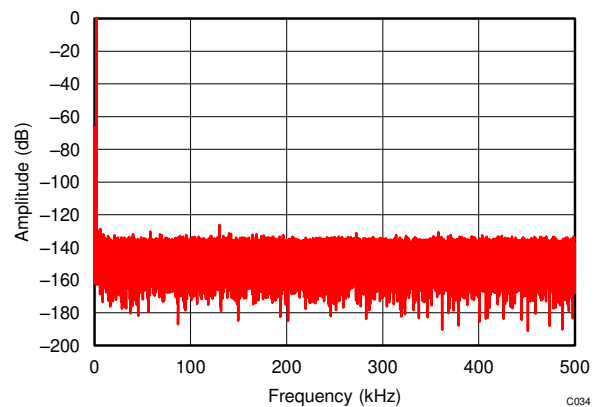
REF6041 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{kHz}$ , SNR = 97.2dB, THD = -119.7dB

**Figure 6-28. Typical FFT Plot**



REF6025 driving REF pin of ADS8881,  
 $f_{IN} = 1\text{kHz}$ , SNR = 95.4dB, THD = -124dB

**Figure 6-29. Typical FFT Plot**

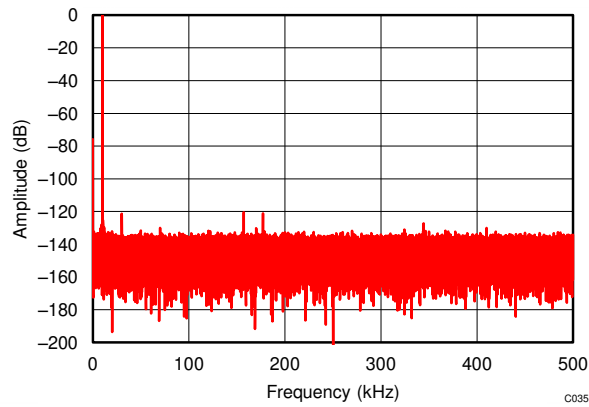


REF6025 driving REF pin of ADS8881,  
 $f_{IN} = 2\text{kHz}$ , SNR = 95.4dB, THD = -123.5dB

**Figure 6-30. Typical FFT Plot**

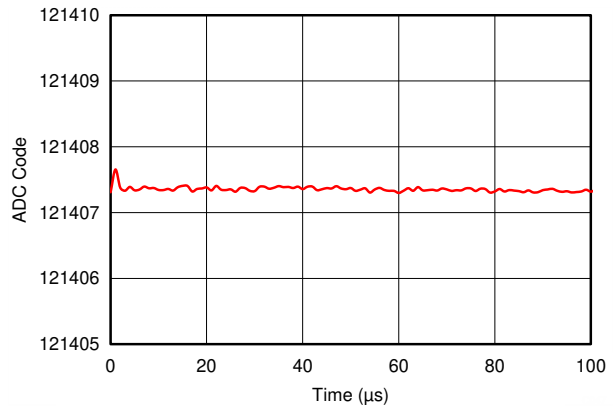
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)



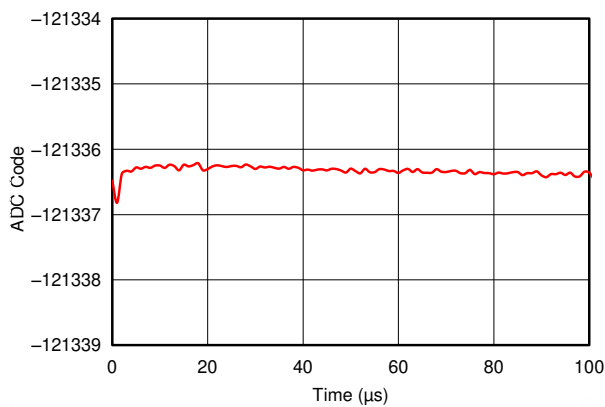
REF6025 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{kHz}$ , SNR = 94.0dB, THD = -119.3dB

**Figure 6-31. Typical FFT Plot**



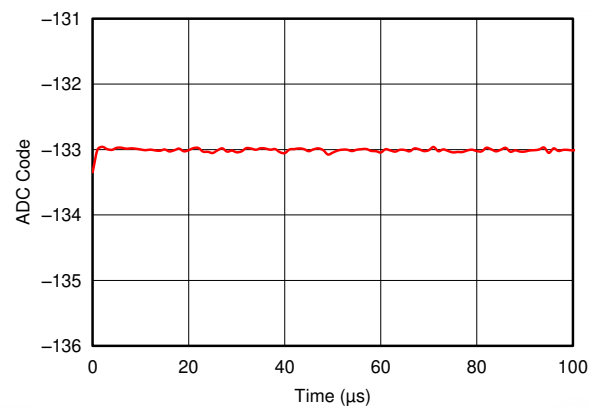
REF6050 driving REF pin of ADS8881 operating at 1MSPS,  
positive full-scale input to ADS8881

**Figure 6-32. Reference Droop**



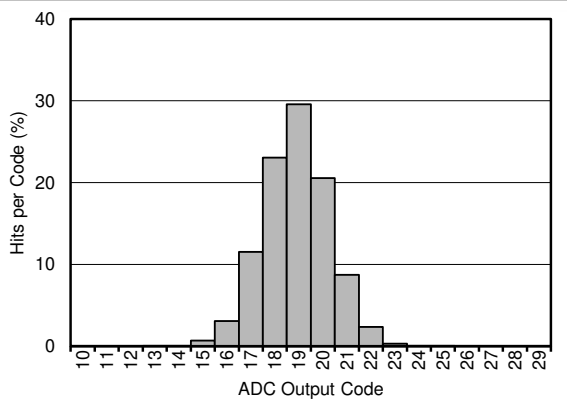
REF6050 driving REF pin of ADS8881 operating at 1MSPS,  
negative full-scale input to ADS8881

**Figure 6-33. Reference Droop**



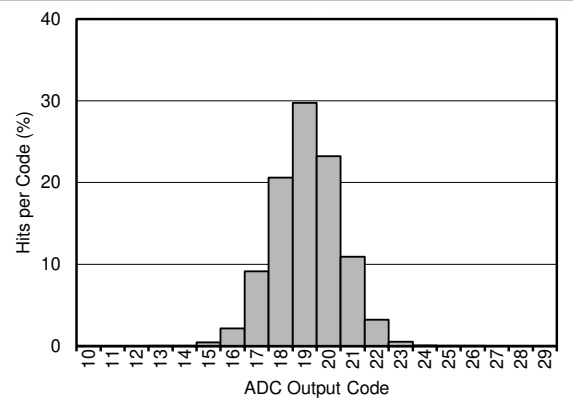
REF6050 driving REF pin of ADS8881 operating at 1MSPS,  
 $A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881

**Figure 6-34. Reference Droop**



$A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881,  
sampling rate = 1MSPS

**Figure 6-35. DC Input Histogram**

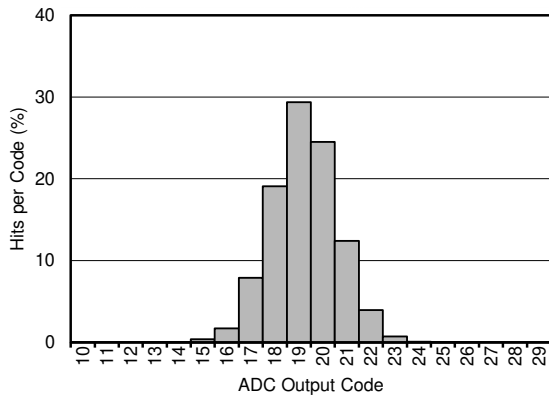


$A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881,  
sampling rate = 500 kSPS

**Figure 6-36. DC Input Histogram**

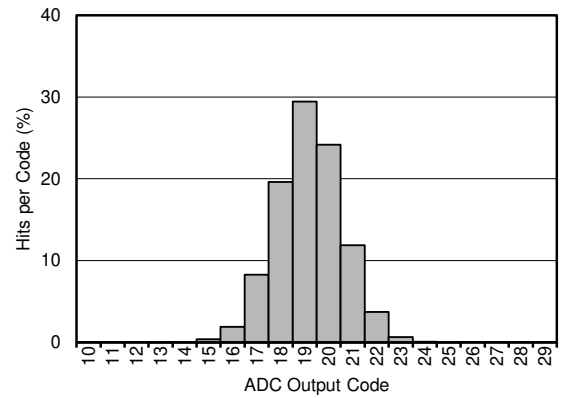
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{mA}$ , and  $V_{IN} = 5\text{V}$ , using REF6025 (unless otherwise noted)



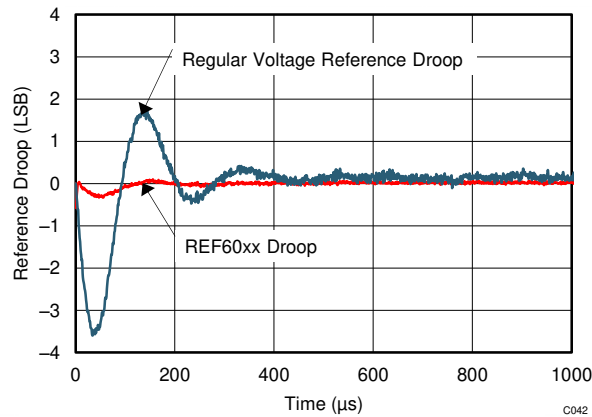
AINP = AINN =  $V_{REF} / 2$  for ADS8881,  
sampling rate = 100 kSPS

**Figure 6-37. DC Input Histogram**



AINP = AINN =  $V_{REF} / 2$  for ADS8881,  
sampling rate = 20 kSPS

**Figure 6-38. DC Input Histogram**



1LSB = 19.07µV, with ADS8881 at 1MSPS

**Figure 6-39. Reference Droop Comparison**

## 7 Parameter Measurement Information

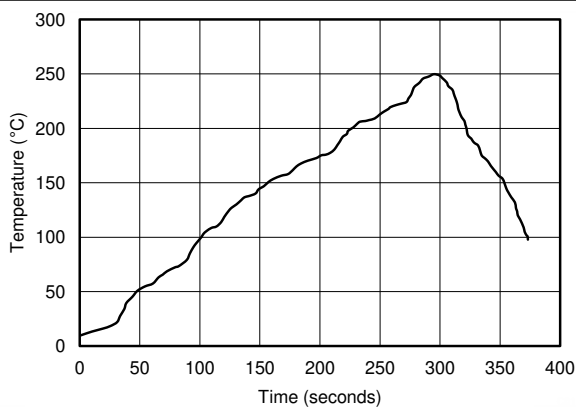
### 7.1 Solder Heat Shift

The materials used in the manufacture of the REF60xx have differing coefficients of thermal expansion, and result in stress on the device die when the part is heated. Mechanical and thermal stress on the device die sometimes causes the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

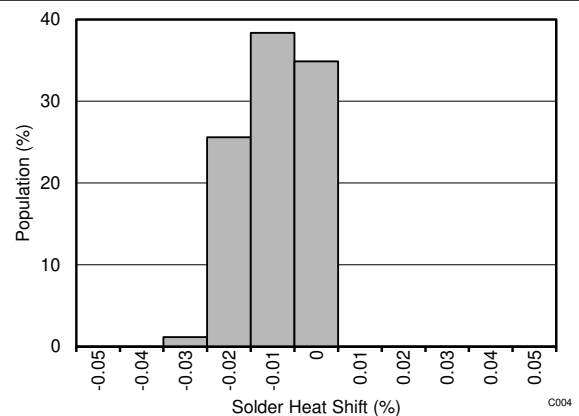
In order to illustrate this effect, a total of 128 devices were soldered on eight printed circuit boards (PCBs), with 16 devices on each PCB, using lead-free solder paste, and the manufacturer-suggested reflow profile. The reflow profile is as shown in [Figure 7-1](#). The printed circuit board is comprised of FR4 material. The board thickness is 1.65mm and the area is 101.6mm × 127mm.

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in [Figure 7-2](#). Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the PCB.

The histogram displays the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the final pass to minimize exposure to thermal stress.



**Figure 7-1. Reflow Profile**



**Figure 7-2. Solder Heat Shift Distribution**

## 7.2 Thermal Hysteresis

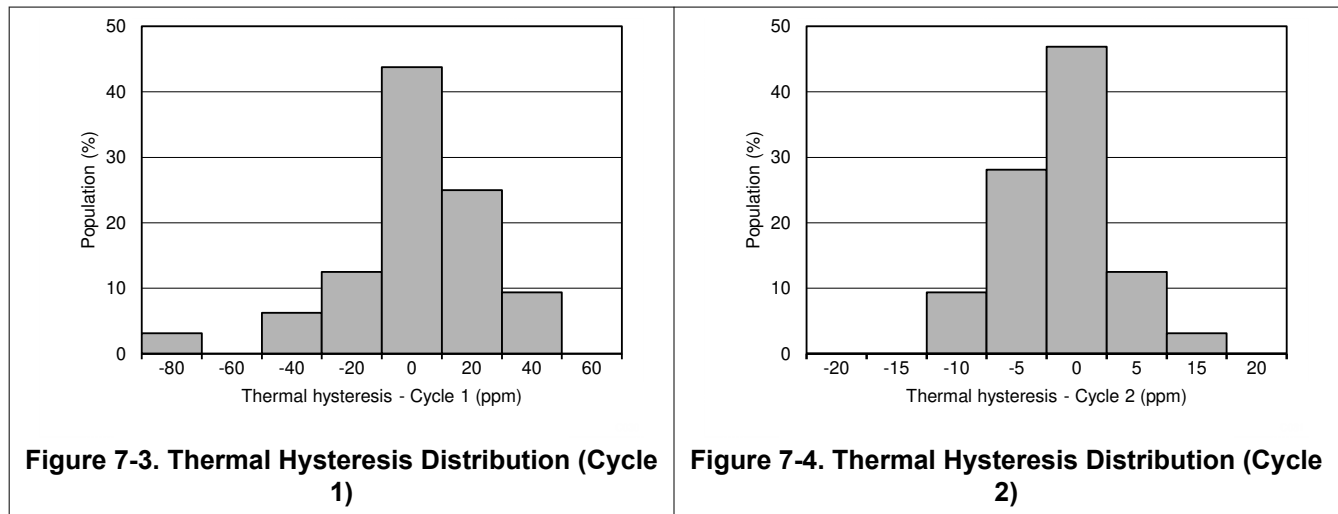
Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Thermal hysteresis was measured with the REF60xx soldered to a PCB, similar to a real-world application. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Thermal hysteresis is expressed as:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \quad (\text{ppm}) \tag{1}$$

where

- $V_{\text{HYST}}$  = thermal hysteresis (in units of ppm).
- $V_{\text{NOM}}$  = the specified output voltage.
- $V_{\text{PRE}}$  = output voltage measured at 25°C pretemperature cycling.
- $V_{\text{POST}}$  = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.

Typical thermal hysteresis distribution is shown in [Figure 7-3](#) and [Figure 7-4](#).

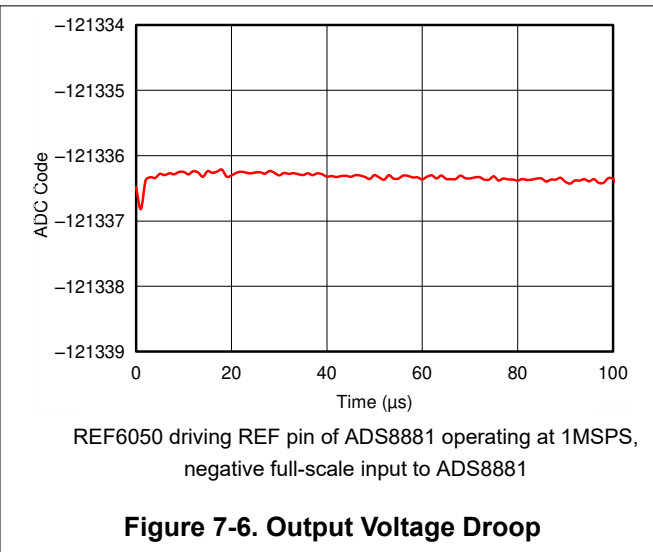
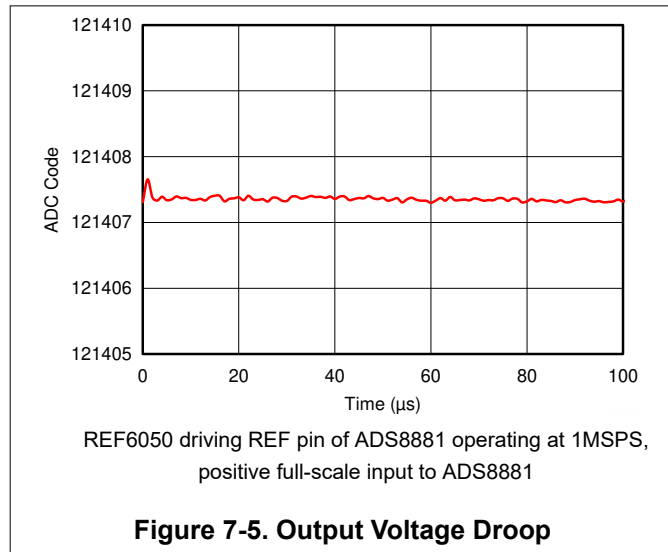


**Figure 7-3. Thermal Hysteresis Distribution (Cycle 1)**

**Figure 7-4. Thermal Hysteresis Distribution (Cycle 2)**

### 7.3 Reference Droop Measurements

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data-acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is a very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. The REF60xx have an integrated ADC drive buffer that makes sure the reference droop is less than 1LSB at 18-bit precision when used with the ADS8881, even at full throughput. [Figure 7-5](#) and [Figure 7-6](#) show the REF60xx output voltage droop when driving the REF pin of the ADS8881 at positive and negative full-scale inputs, respectively.

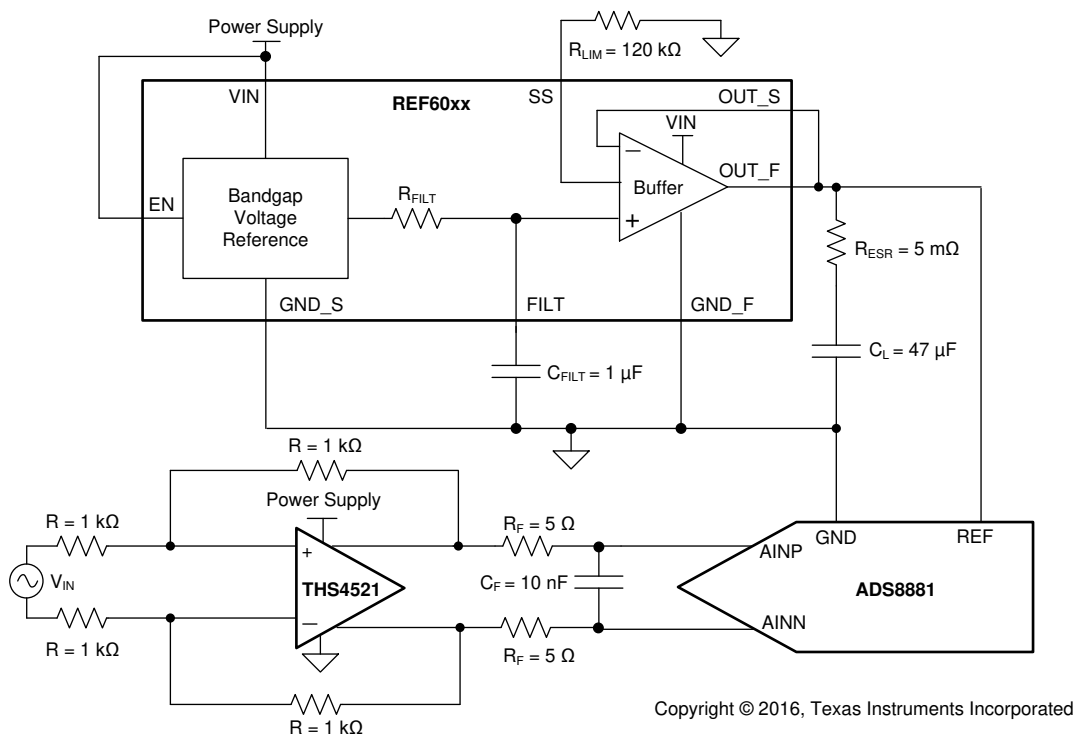


Direct measurement of the reference droop to 18-bit accuracy can be a challenging process. Therefore, the plots in [Figure 7-5](#) and [Figure 7-6](#) were obtained by processing the output code of the ADC. The ADC output code is given by:

$$C = (\text{Input Voltage} / V_{\text{REF}}) \times 2^N \quad (2)$$

If the input voltage is kept constant,  $V_{\text{REF}}$  is computed by monitoring the ADC output code  $C$ . The ADC code usually has six to seven LSBs of code spread due to the inherent noise of the ADC. In order to measure reference droop, this noise must be reduced drastically. Noise reduction is done by averaging the output code multiple times, as described in the next paragraph.

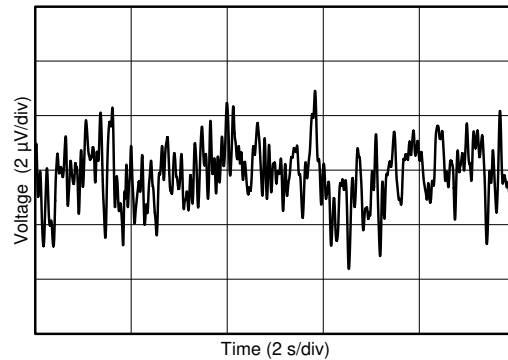
Figure 7-7 shows the setup that was used to measure the reference droop. The output ADC code was captured using a field-programmable gate array (FPGA), and post-processing was done on a personal computer. The input to the THS4521, and hence in turn to the ADS8881, is a constant dc voltage (close to positive or negative full-scale because this condition is the worst-case for charge drawn from the REF pin). The dc source must have extremely low noise. After the REF60xx device is powered up and stable, the FPGA sends commands to the ADS8881 to capture data in bursts. The ADS8881 is initially in idle mode for 100ms. The FPGA then sends a command to the ADS8881 to perform 100 conversions at 1MSPS. The ADC code corresponding to these 100 conversions (one burst of data) is stored as the first row in a 1000 × 100 dimensional array. This operation is repeated 1000 times, and the data corresponding to each burst is stored in a new row of the 1000 × 100 dimensional array. Finally, each column in this array is averaged to get a final data-set of 100 elements. This final data-set now has code spread that is much less than 1LSB because most of the noise has now been removed through averaging. This data-set was plotted on a graph with X axis = column number (each column number corresponds to 1μs of time because the sampling rate is 1MSPS), and Y axis = ADC output code to obtain reference-droop measurements.



**Figure 7-7. Burst-Mode Measurement Setup**

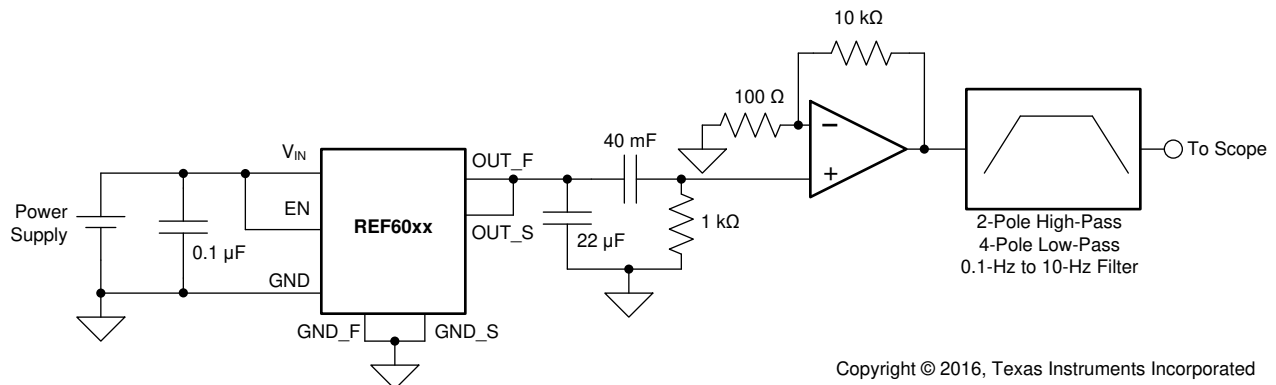
## 7.4 1/f Noise Performance

Typical 0.1Hz to 10Hz voltage noise for the REF6025 is shown in [Figure 7-8](#). The 1/f noise scales with output voltage, but remains  $3\mu\text{V}_{\text{pp}}/\text{V}$  for all the variants. Peak-to-peak noise measurement setup is shown in [Figure 7-9](#).



C021

**Figure 7-8. 0.1Hz to 10Hz Noise**



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**Figure 7-9. 0.1Hz to 10Hz Noise Measurement Setup**

## 8 Detailed Description

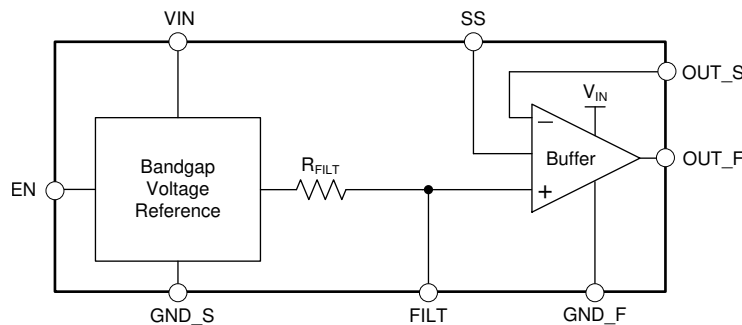
### 8.1 Overview

Most SAR ADCs, and a few delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. If a voltage reference is directly connected to the REF pin of these ADCs, the reference voltage droops because of the dynamic input signal dependent load of the binary-weighted capacitors. Because the reference voltage droop now has input signal dependence, significant degradation in THD and linearity for the system occurs.

In order to support this dynamic load and preserve the ADC linearity, distortion and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF60xx family of voltage references have an integrated low output impedance buffer that enables the user to directly drive the REF pin of a SAR ADC, while preserving ADC linearity and distortion. In addition, the total noise in the full bandwidth of the REF60xx is extremely low, thus preserving the noise performance of the ADC. [Voltage-Reference Impact on Total Harmonic Distortion \(SLYY097\)](#) correlates the effect of reference settling to ADC distortion, and how the REF60xx achieves lowest distortion with minimal components and lowest power consumption.

The output voltage of the REF60xx does not droop below 1LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8881. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. [Section 8.2](#) shows a simplified schematic of the REF60xx.

### 8.2 Functional Block Diagram

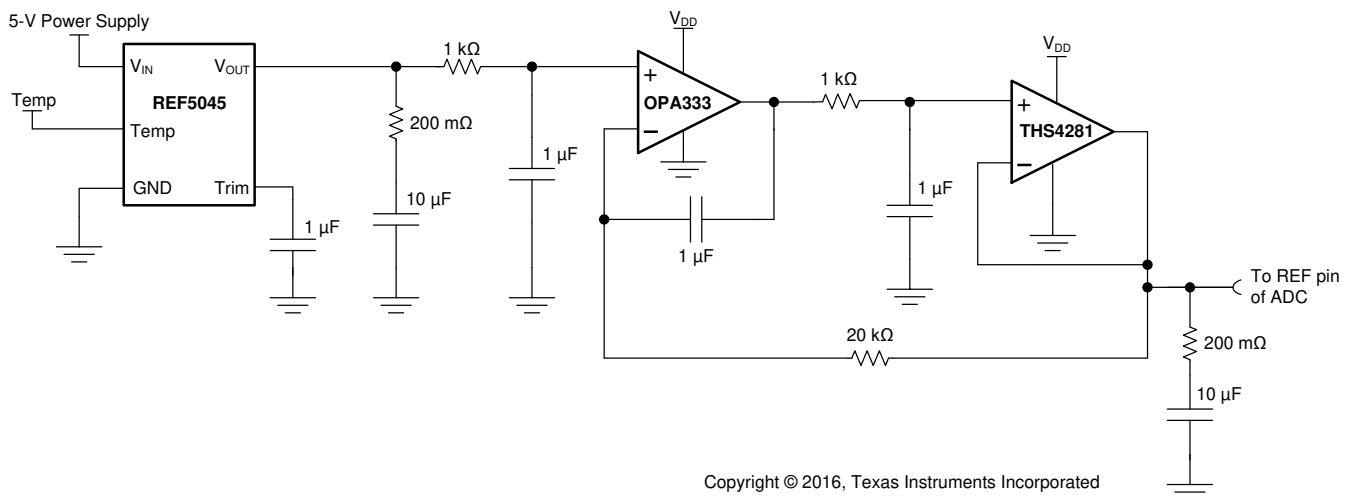


## 8.3 Feature Description

### 8.3.1 Integrated ADC Drive Buffer

Many ADC data sheets specify a few microamps of average current draw from the REF pin. Almost all voltage references provide these few microamps of average current; but not all voltage references are practical for driving a high-resolution, high-throughput SAR ADC because the peak current drawn can be very high when the capacitors are switched on the REF pin. The worst-case demand for the voltage reference is during a burst-mode conversion, when the ADC is idle for a very long time, before a conversion is initiated, and the first sample converted is expected to be precise. Usually, a large capacitor is connected between the REF pin and ground pin (or sometimes between the REFP and REFM pins) of the ADC to smooth the current load and reduce the burden on the voltage reference. The voltage reference must then be capable of providing the average current required to completely charge the reference capacitor, but without causing the reference voltage to droop significantly. Most voltage references lack the ability to completely charge the reference capacitor, and settle when the binary-weighted capacitors are being switched onto the REF pin because of the large output impedance. Usually, voltage references have output impedances in the range of 10's of ohms at frequencies higher than 100Hz. The output voltage of the voltage reference must be buffered with a low output impedance (usually high bandwidth) amplifier to achieve excellent linearity and distortion performance.

The key amplifier specifications to be considered when designing a reference buffer for a high-precision ADC are: low offset, low drift, wide bandwidth, and low output impedance. While it is possible to select an amplifier that sufficiently meets all these requirements, the amplifier comes at a cost of excessive power consumption. For example, the OPA350 is a 38MHz bandwidth amplifier with a maximum offset of 0.5mV, and low offset drift of  $4\mu\text{V}/^\circ\text{C}$ , but consumes a quiescent current of 5.2mA. This is because (from an amplifier design perspective) offset and drift are dc specifications, whereas bandwidth, low output impedance, and high capacitive drive capability are high-frequency specifications. Therefore, achieving all the performance in one amplifier requires power. However, a more efficient design to meet the low power budget is to use a composite reference buffer, which uses an amplifier with superior high-frequency specifications in the feedback loop of a dc precision amplifier to get the overall performance at much lower power consumption. Figure 8-1 shows such a composite amplifier design with the OPA333 (dc precision amplifier) and THS4281 (high-bandwidth amplifier). This reference buffer design requires three devices, and a large number of external components. This solution still consumes close to 2mA of quiescent current.



**Figure 8-1. Composite Amplifier Reference Buffer**

The REF60xx family of voltage references have an integrated low output impedance buffer (ADC drive buffer); therefore, there is no need for an external buffer while driving the REF pin of high-precision, high-throughput SAR ADCs, as shown in Figure 8-2. The ADC drive buffer of the REF60xx is capable of replenishing a charge of 70 pC on a 47- $\mu\text{F}$  capacitor in 1 $\mu\text{s}$ , without allowing the voltage on the capacitor to droop more than 1LSB at 18-bit precision. The REF60xx are trimmed at multiple temperatures in production, achieving a max drift of just

5ppm/°C for both the voltage reference and the buffer combined, while operating at a typical quiescent current of 820  $\mu$ A. Figure 8-3 compares the output impedance of a regular voltage reference (REF20xx) and a voltage reference with integrated ADC drive buffer (REF60xx). Figure 8-4 compares the burst-mode, reference-settling performance of a regular voltage reference and the REF60xx.

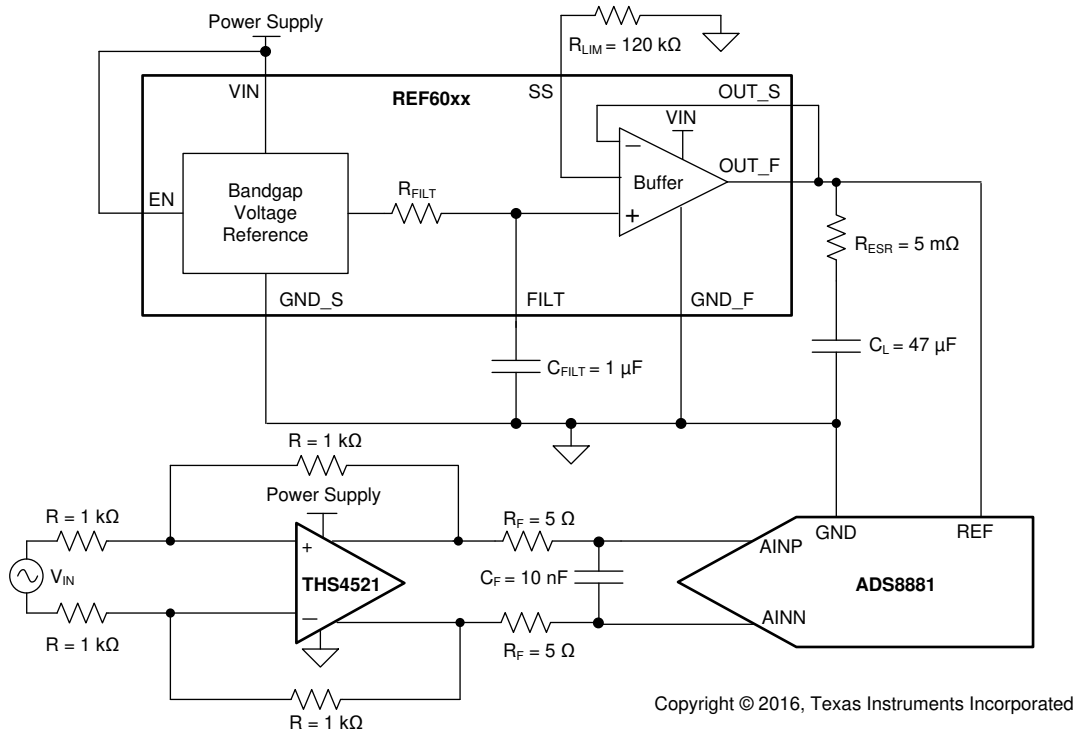


Figure 8-2. REF60xx Driving REF Pin of ADS8881 SAR ADC

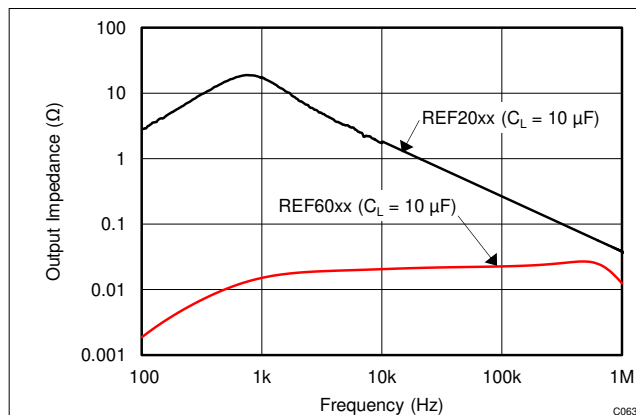


Figure 8-3. Output Impedance Comparison

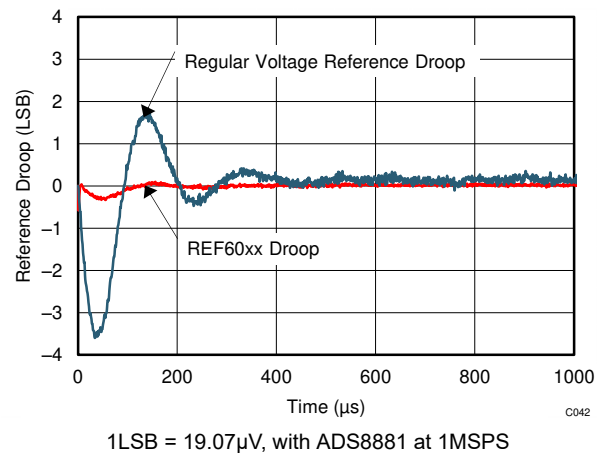


Figure 8-4. Reference Droop Comparison

### 8.3.2 Temperature Drift

The REF60xx family is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left( \frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

### 8.3.3 Load Current

The REF6025, REF6030, REF6033 and REF6041 are specified to deliver current load of  $\pm 4\text{mA}$ . The REF6045 is specified to deliver  $\pm 3.5\text{mA}$ , and the REF6050 is specified to deliver  $\pm 3\text{mA}$ . The REF60xx are protected from short circuits at the output by limiting the output short-circuit current.

The short-circuit current limit ( $I_{\text{SC}}$ ) of the REF60xx family of devices is adjusted by connecting a resistor ( $R_{\text{SS}}$ ) on the SS pin. The short-circuit current limit when the REF60xx device is sourcing current can be calculated as shown in [Equation 4](#):

$$I_{\text{SC}} = (80 \cdot 10^{-9}) \cdot R_{\text{SS}} + (3 \cdot 10^{-3}) \quad (4)$$

The short circuit current limit when the REF60xx device is sinking is calculated as shown in [Equation 5](#):

$$I_{\text{SC}} = (115 \cdot 10^{-9}) \cdot R_{\text{SS}} + (4.6 \cdot 10^{-3}) \quad (5)$$

The recommended output current of the REF60xx also depends on the resistor connected to the SS pin. The recommended output current (sourcing and sinking) for the REF6025, REF6030, REF6033 and REF6041 is given by [Equation 6](#):

$$I_{\text{L}} = (31.25 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (6)$$

The recommended output current (sourcing and sinking) for the REF6045 is given by [Equation 7](#):

$$I_{\text{L}} = (27.08 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (7)$$

The recommended output current (sourcing and sinking) for the REF6050 is given by [Equation 8](#):

$$I_{\text{L}} = (23.75 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.15 \cdot 10^{-3}) \quad (8)$$

The temperature of the device increases according to [Equation 9](#):

$$T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \cdot R_{\theta\text{JA}} \quad (9)$$

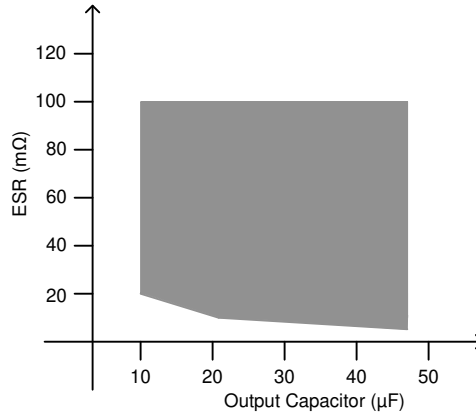
where:

- $T_{\text{J}}$  = junction temperature ( $^{\circ}\text{C}$ ).
- $T_{\text{A}}$  = ambient temperature ( $^{\circ}\text{C}$ ).
- $P_{\text{D}}$  = power dissipated (W).
- $R_{\theta\text{JA}}$  = junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ ).

The REF60xx maximum junction temperature must not exceed the absolute maximum rating of  $150^{\circ}\text{C}$ .

### 8.3.4 Stability

The REF60xx family of voltage references are stable with output capacitor values ranging from 10  $\mu\text{F}$  to 47  $\mu\text{F}$ . At a low output-capacitor value of 10  $\mu\text{F}$ , an effective series resistance (ESR) of 20m $\Omega$  to 100m $\Omega$  is required for stability; whereas, at a higher value of 47  $\mu\text{F}$ , an ESR of 5m $\Omega$  to 100m $\Omega$  is required. The shaded region in [Figure 8-5](#) shows the stable region of operation for the REF60xx devices.



**Figure 8-5. Stable Output Capacitor Range**

A capacitor of value 1  $\mu\text{F}$  is required at the FILT pin for stability and noise performance. A low ESR (5m $\Omega$  to 20m $\Omega$ ) is easily achieved by increasing the PCB trace length, thus eliminating the need for a discrete resistor. Higher values of ESR (greater than 20m $\Omega$ , but lesser than 100m $\Omega$ ) can be intentionally added to increase the output bandwidth of the REF60xx. This higher ESR improves the transient performance of the REF60xx, but worsens noise performance because of increased bandwidth.

### 8.4 Device Functional Modes

When the EN pin of the REF60xx is pulled high, the device is in active mode. The device must be in active mode for normal operation.

To place the REF60xx into a shutdown mode, pull the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 1  $\mu\text{A}$  (typ). See the enable pin voltage parameter in [Section 6.5](#) for logic high and logic low voltage levels.



## 9.2.2 Detailed Design Procedure

The data acquisition system shown in [Figure 9-1](#) has three major contributors to the noise and accuracy in the system: the input driver, the reference with driver, and the data converter. Each analog block is carefully designed so that the data converter specifications limit the system specifications. The [THS4551](#), a fully differential operational amplifier is used to drive the 18-bit ADC ([ADS8881](#)). The charge-kickback RC filter at the output of the THS4551 is used to reduce the charge kickback created by the opening and closing of the sampling switch inside the ADC. Design the RC filter so that the voltage at the sampling capacitor settles to 18-bit accuracy within the acquisition time of the ADC.

Data-acquisition systems require stable and accurate voltage references in order to perform the most accurate data conversion. The REF60xx family of voltage references have integrated an ADC drive buffer, and can therefore drive the REF pin of the ADS8881 directly, without the need for an external reference buffer. See [Section 8.3.1](#) for more details about reference-buffer requirements. Correct output capacitor selection for the REF60xx is very important in this design. [Section 8.3.4](#) describes the ESR requirements of the output capacitor for stability and burst-mode requirements. A capacitance of 1 $\mu$ F is connected to the FILT pin to reduce broadband noise of the REF60xx.

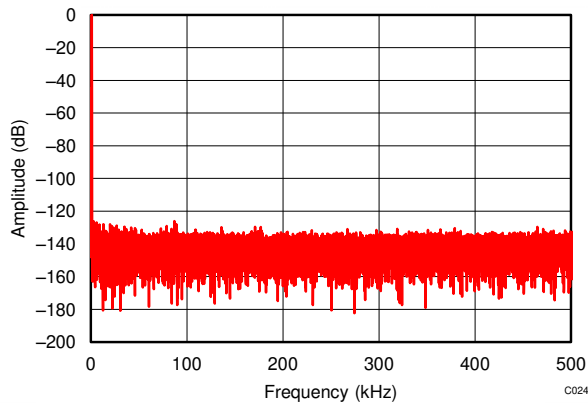
### 9.2.2.1 Results

[Table 9-1](#) summarizes the measured results.

**Table 9-1. Measured Results**

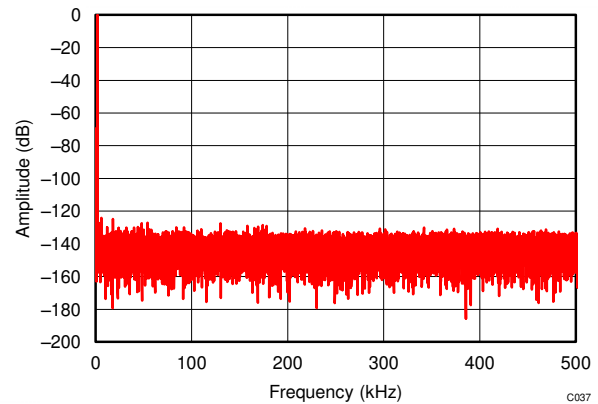
SPECIFICATION	MEASURED RESULT
SNR	100.5dB
ENOB	16.4
THD	-125.9dB
Throughput	1MSPS
Burst mode	First sample > 18-bit precision
Power consumption	40mW

### 9.2.3 Application Curves



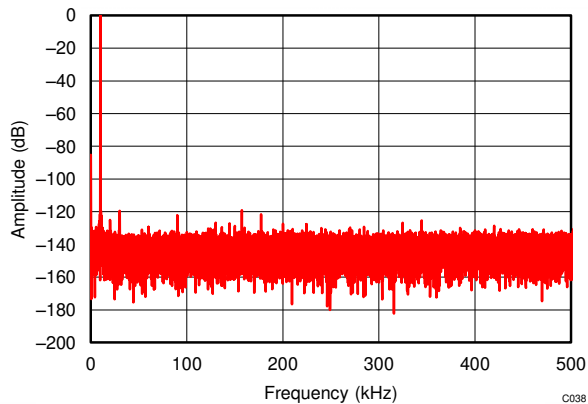
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 1\text{kHz}$ , SNR = 100.5dB, THD = -125.9dB

**Figure 9-2. Typical FFT Plot**



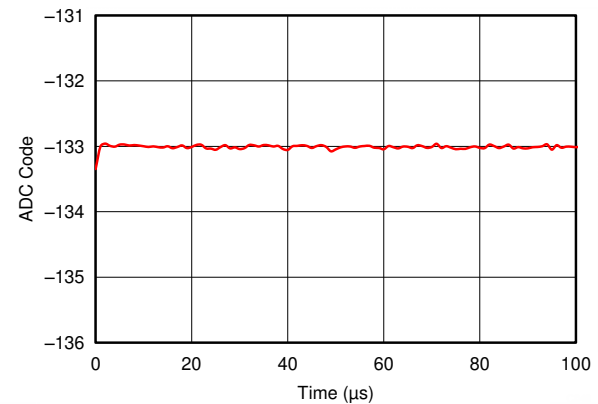
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 2\text{kHz}$ , SNR = 100.4dB, THD = -123.9dB

**Figure 9-3. Typical FFT Plot**



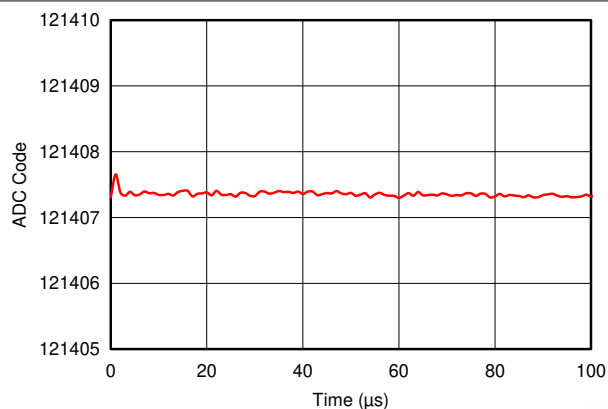
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{kHz}$ , SNR = 99.2dB, THD = -119.4dB

**Figure 9-4. Typical FFT Plot**



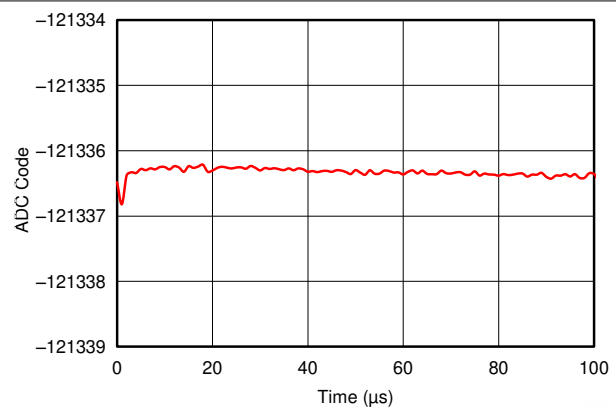
REF6050 driving REF pin of ADS8881 operating at 1MSPS,  
 $A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881

**Figure 9-5. Reference Droop**



REF6050 driving REF pin of ADS8881 operating at 1MSPS,  
positive full-scale input to ADS8881

**Figure 9-6. Reference Droop**



REF6050 driving REF pin of ADS8881 operating at 1MSPS,  
negative full-scale input to ADS8881

**Figure 9-7. Reference Droop**



## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [ADS8881x 18-Bit, 1MSPS, Serial Interface, microPower, Miniature, True-Differential Input, SAR Analog-to-Digital Converter Data Sheet](#) datasheet
- Texas Instruments, [ADS127L01 24-Bit, High-Speed, Wide-Bandwidth Analog-to-Digital Converter](#) datasheet
- Texas Instruments, [REF6025EVM-PDK User's Guide](#)
- Texas Instruments, [Voltage-Reference Impact on Total Harmonic Distortion](#) marketing white paper

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.4 Trademarks

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### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

Changes from Revision B (August 2016) to Revision C (April 2026)	Page
• Moved the REF6025, REF6030, REF6033, REF6041, REF6045, REF6050 devices to the REF60 product folder on TI.com and updated the datasheet header.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed <i>Device Information</i> table to <i>Package Information</i> .....	1

Changes from Revision A (June 2016) to Revision B (August 2016)	Page
• Changed the <i>Description</i> .....	1
• Changed the <i>Description</i> .....	1
• Changed the <i>Device Comparison Table</i> .....	2
• Changed list of devices for output current in Recommended Operating Conditions .....	4
• Changed load regulation max value for REF6050 at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ from 30 to 50.....	5

- 
- Changed Figure 2.....7
  - Changed "second pass" to "final pass" in last paragraph of *Solder Heat Shift* section .....14
  - Added link to SLYY097 in *Overview* section.....19
- 

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">REF6025IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
<a href="#">REF6025IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKTG4	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
REF6025IDGKTG4.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV
<a href="#">REF6030IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
REF6030IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
<a href="#">REF6030IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
REF6030IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV
<a href="#">REF6033IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
REF6033IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
<a href="#">REF6033IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
REF6033IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV
<a href="#">REF6041IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
<a href="#">REF6041IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKTG4	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
REF6041IDGKTG4.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV
<a href="#">REF6045IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
REF6045IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
<a href="#">REF6045IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
REF6045IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG
<a href="#">REF6050IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKR.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKRG4	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
REF6050IDGKRG4.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV
<a href="#">REF6050IDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF6050IDGKT.B	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF6025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6025IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6025IDGKTG4	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKTG4	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF6025IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6025IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6025IDGKTG4	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6030IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6030IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6033IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6033IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6041IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6041IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6041IDGKTG4	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6045IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6045IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6050IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6050IDGKRG4	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6050IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0

DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

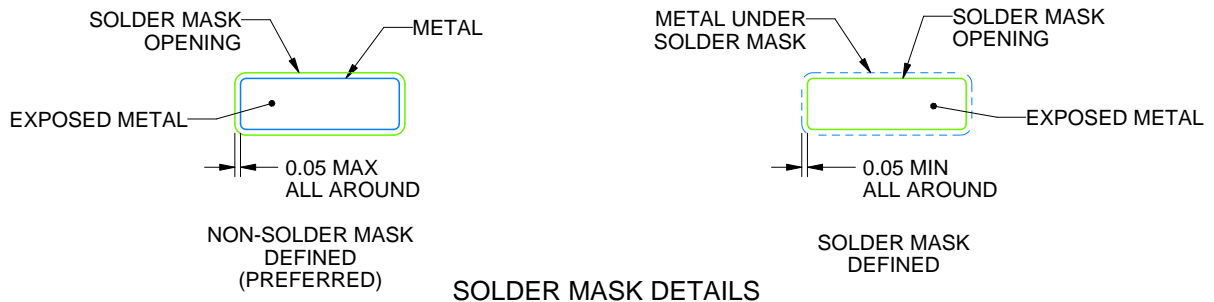
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025