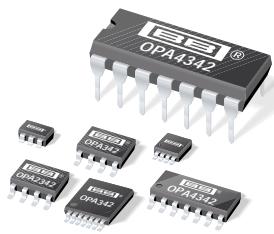




Burr-Brown Products  
from Texas Instruments



OPA342  
OPA2342  
OPA4342

[www.ti.com](http://www.ti.com)

## Low-Cost, Low-Power, Rail-to-Rail OPERATIONAL AMPLIFIERS

### *MicroAmplifier™ Series*

#### FEATURES

- LOW QUIESCENT CURRENT: 150 $\mu$ A typ
- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 1mV)
- SINGLE SUPPLY CAPABILITY
- LOW COST
- *MicroSIZE PACKAGE OPTIONS:*
  - SOT23-5
  - MSOP-8
  - TSSOP-14
- BANDWIDTH: 1MHz
- SLEW RATE: 1V/ $\mu$ s
- THD + NOISE: 0.006%

#### APPLICATIONS

- COMMUNICATIONS
- PCMCIA CARDS
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- ACTIVE FILTERS
- TEST EQUIPMENT
- CONSUMER ELECTRONICS

#### DESCRIPTION

The OPA342 series rail-to-rail CMOS operational amplifiers are designed for low-cost, low-power, miniature applications. They are optimized to operate on a single supply as low as 2.5V with an input common-mode voltage range that extends 300mV beyond the supplies.

Rail-to-rail input/output and high-speed operation make them ideal for driving sampling Analog-to-Digital Converters (ADC). They are also well suited for general-purpose and audio applications and providing I/V conversion at the output of Digital-to-Analog Converters (DAC). Single, dual, and quad versions have identical specs for design flexibility.

The OPA342 series offers excellent dynamic response with a quiescent current of only 250 $\mu$ A max. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

PACKAGE	SINGLE OPA342	DUAL OPA2342	QUAD OPA4342
SOT23-5	✓		
MSOP-8		✓	
SO-8	✓	✓	
TSSOP-14			✓
SO-14			✓
DIP-14			✓

SPICE MODEL available at [www.burr-brown.com](http://www.burr-brown.com).



# SPECIFICATIONS: $V_S = 2.7V$ to $5.5V$

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.

**Boldface** limits apply over the temperature range,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

PARAMETER	CONDITION	OPA342NA, UA OPA2342EA, UA OPA4342EA, UA, PA			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage $T_A = -40^\circ C$ to $+85^\circ C$ <b>vs Temperature</b> vs Power Supply $T_A = -40^\circ C$ to $+85^\circ C$ Channel Separation, dc $f = 1kHz$	$V_{OS}$ $dV_{OS}/dT$ PSRR	$V_{CM} = V_S/2$ $V_S = 2.7V$ to $5.5V$ , $V_{CM} < (V+) - 1.8V$ $V_S = 2.7V$ to $5.5V$ , $V_{CM} < (V+) - 1.8V$	$\pm 1$ $\pm 1$ $\pm 3$ 30 0.2 132	$\pm 6$ $\pm 6$ $200$ $250$	mV mV $\mu V^\circ C$ $\mu V/V$ $\mu V/V$ $\mu V/V$ dB
<b>INPUT BIAS CURRENT</b> Input Bias Current $T_A = -40^\circ C$ to $+85^\circ C$ Input Offset Current	$I_B$ $I_{OS}$		$\pm 0.2$ See Typical Curve $\pm 0.2$	$\pm 10$ $\pm 10$	pA pA pA
<b>NOISE</b> Input Voltage Noise, $f = 0.1Hz$ to $50kHz$ Input Voltage Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$	$e_n$ $i_n$		8 30 0.5		$\mu V_{rms}$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range Common-Mode Rejection Ratio $T_A = -40^\circ C$ to $+85^\circ C$ Common-Mode Rejection Ratio $T_A = -40^\circ C$ to $+85^\circ C$ Common-Mode Rejection Ratio $T_A = -40^\circ C$ to $+85^\circ C$	$V_{CM}$ CMRR	$V_S = +5.5V$ , $-0.3V < V_{CM} < (V+) - 1.8$ $V_S = +5.5V$ , $-0.3V < V_{CM} < (V+) - 1.8$ $V_S = +5.5V$ , $-0.3V < V_{CM} < 5.8V$ $V_S = +5.5V$ , $-0.3V < V_{CM} < 5.8V$ $V_S = +2.7V$ , $-0.3V < V_{CM} < 3V$ $V_S = +2.7V$ , $-0.3V < V_{CM} < 3V$	-0.3 76 74 66 64 62 60	88 78 74	$(V+) + 0.3$
<b>INPUT IMPEDANCE</b> Differential Common-Mode				$10^{13} \parallel 3$ $10^{13} \parallel 6$	$\Omega \parallel pF$ $\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$	$A_{OL}$	$R_L = 100k\Omega$ , $10mV < V_O < (V+) - 10mV$ $R_L = 100k\Omega$ , $10mV < V_O < (V+) - 10mV$ $R_L = 5k\Omega$ , $400mV < V_O < (V+) - 400mV$ $R_L = 5k\Omega$ , $400mV < V_O < (V+) - 400mV$	104 100 96 90	124 114	dB dB dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time, 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise, $f = 1kHz$	GBW SR	$C_L = 100pF$ $G = 1$ $V_S = 5.5V$ , 2V Step $V_S = 5.5V$ , 2V Step $V_{IN} \cdot G = V_S$ $V_S = 5.5V$ , $V_O = 3V_{p-p}^{(1)}$ , $G = 1$		1 1 5 8 2.5 0.006	MHz $V/\mu s$ $\mu s$ $\mu s$ $\mu s$ %
<b>OUTPUT</b> Voltage Output Swing from Rail <sup>(2)</sup> $T_A = -40^\circ C$ to $+85^\circ C$ $T_A = -40^\circ C$ to $+85^\circ C$ Short-Circuit Current Capacitive Load Drive	$I_{SC}$ $C_{LOAD}$	$R_L = 100k\Omega$ , $A_{OL} \geq 96dB$ $R_L = 100k\Omega$ , $A_{OL} \geq 104dB$ <b><math>R_L = 100k\Omega</math>, <math>A_{OL} \geq 100dB</math></b> $R_L = 5k\Omega$ , $A_{OL} \geq 96dB$ <b><math>R_L = 5k\Omega</math>, <math>A_{OL} \geq 90dB</math></b> Per Channel		1 3 20 400 $\pm 15$ See Typical Curve	mV mV mV mV mA
<b>POWER SUPPLY</b> Specified Voltage Range Operating Voltage Range Quiescent Current (per amplifier) $T_A = -40^\circ C$ to $+85^\circ C$	$V_S$ $I_Q$	$I_O = 0A$	2.7 2.5 to 5.5 150	5.5 250 <b>300</b>	V V $\mu A$ $\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance SOT23-5 Surface Mount MSOP-8 Surface Mount SO-8 Surface Mount TSSOP-14 Surface Mount SO-14 Surface Mount DIP-14	$\theta_{JA}$		-40 -55 -65	+85 +125 +150	°C °C °C °C/W °C/W °C/W °C/W °C/W °C/W

NOTES: (1)  $V_{OUT} = 0.25V$  to  $3.25V$ . (2) Output voltage swings are measured between the output and power-supply rails.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V-	7.5V
Signal Input Terminals, Voltage <sup>(2)</sup>	(V-) -0.5V to (V+) +0.5V
Current <sup>(2)</sup>	10mA
Output Short-Circuit <sup>(3)</sup>	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Tolerance (Human Body Model)	4000V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

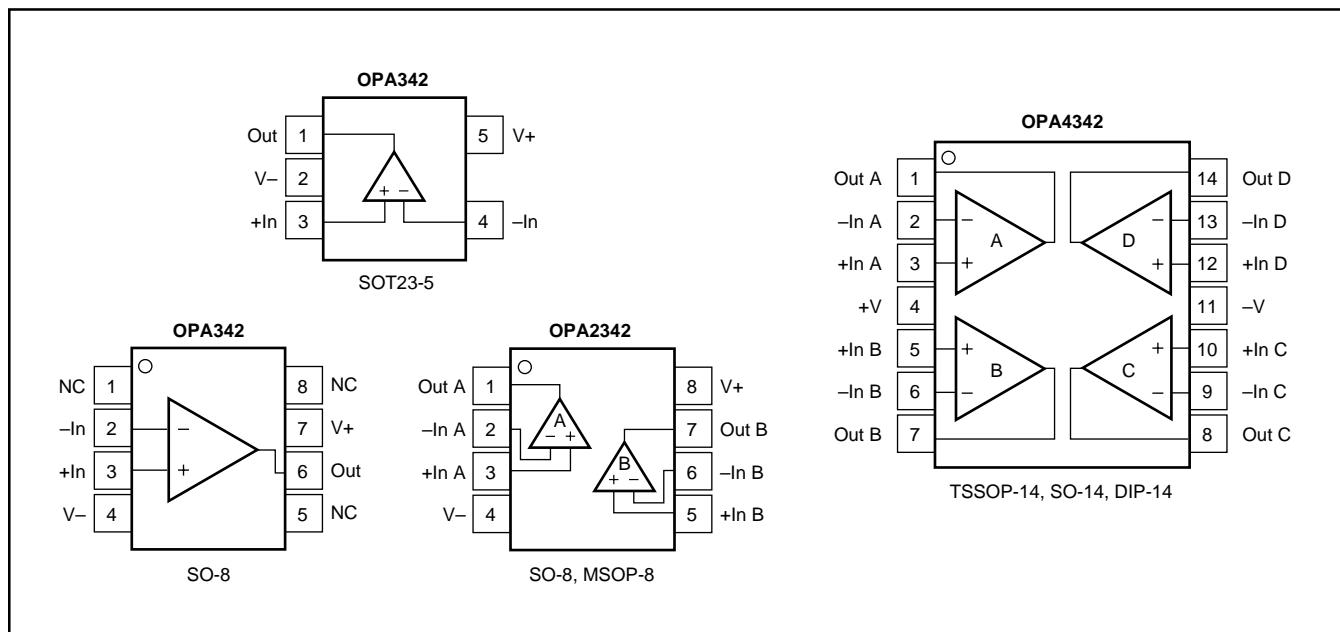
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(1)</sup>	TRANSPORT MEDIA
OPA342NA	SOT23-5	331	-40°C to +85°C	B42	OPA342NA/250	Tape and Reel
"	"	"	"	"	OPA342NA/3K	Tape and Reel
OPA342UA	SO-8	182	-40°C to +85°C	OPA342UA	OPA342UA	Rails
"	"	"	"	"	OPA342UA/2K5	Tape and Reel
OPA2342EA	MSOP-8	337	-40°C to +85°C	C42	OPA2342EA/250	Tape and Reel
"	"	"	"	"	OPA2342EA/2K5	Tape and Reel
OPA2342UA	SO-8	182	-40°C to +85°C	OPA2342UA	OPA2342UA	Rails
"	"	"	"	"	OPA2342UA/2K5	Tape and Reel
OPA4342EA	TSSOP-14	357	-40°C to +85°C	OPA4342EA	OPA4342EA/250	Tape and Reel
"	"	"	"	"	OPA4342EA/2K5	Tape and Reel
OPA4342UA	SO-14	235	-40°C to +85°C	OPA4342UA	OPA4342UA	Rails
"	"	"	"	"	OPA4342UA/2K5	Tape and Reel
OPA4342PA	DIP-14	010	-40°C to +85°C	OPA4342PA	OPA4342PA	Tape and Reel

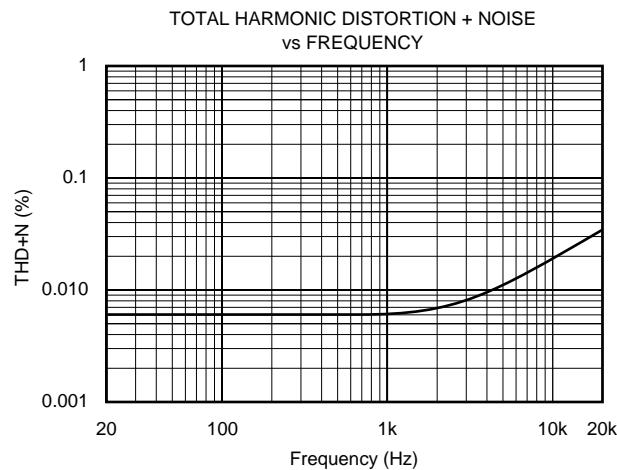
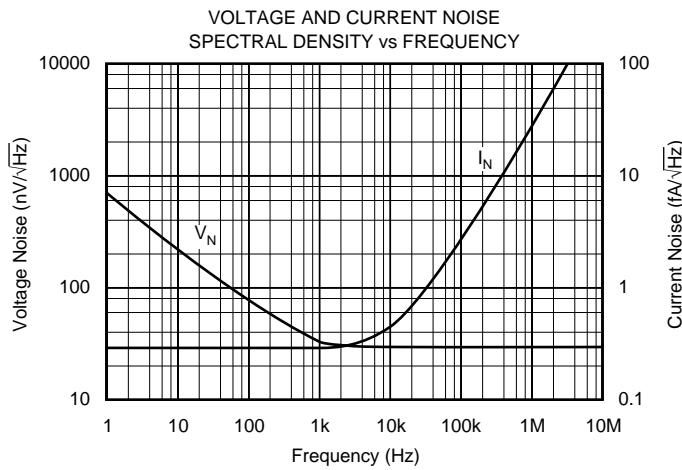
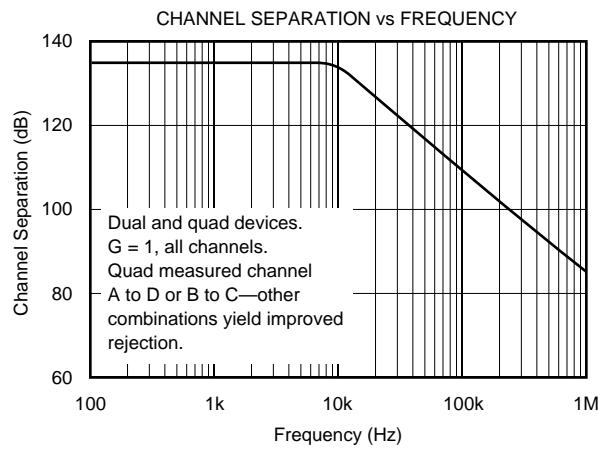
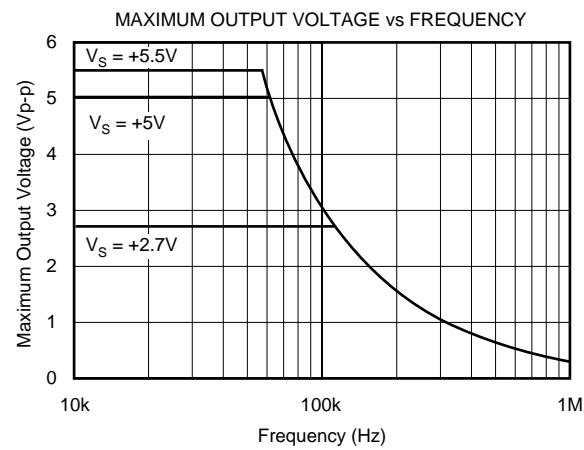
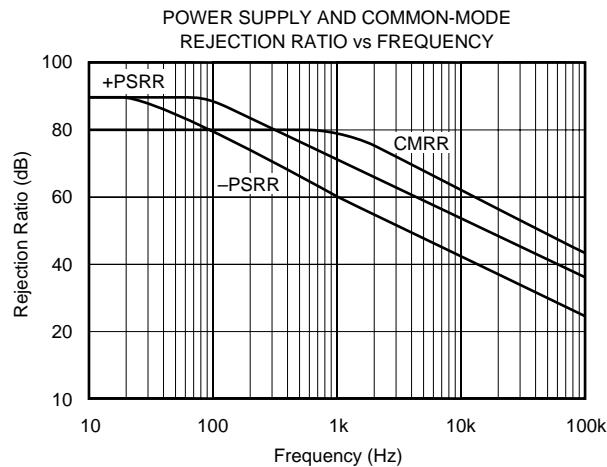
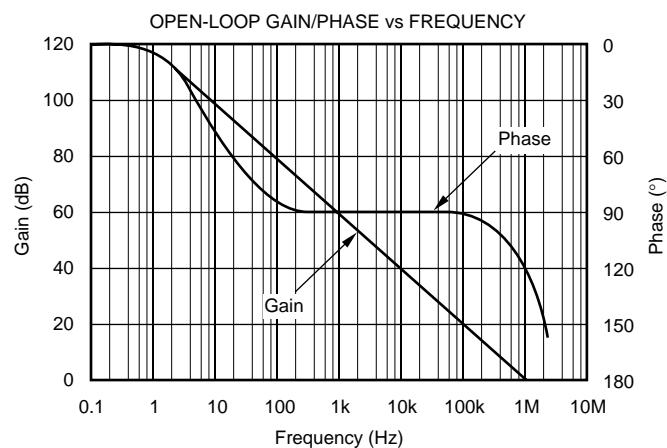
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /3K indicates 3000 devices per reel). Ordering 3000 pieces of "OPA342NA/3K" will get a single 3000-piece Tape and Reel.

## PIN CONFIGURATIONS



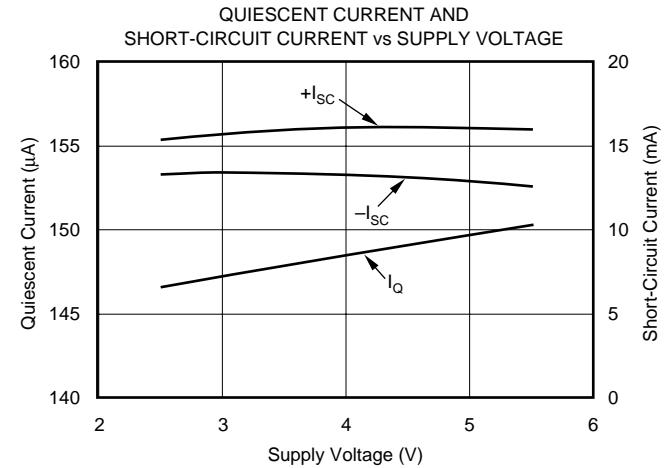
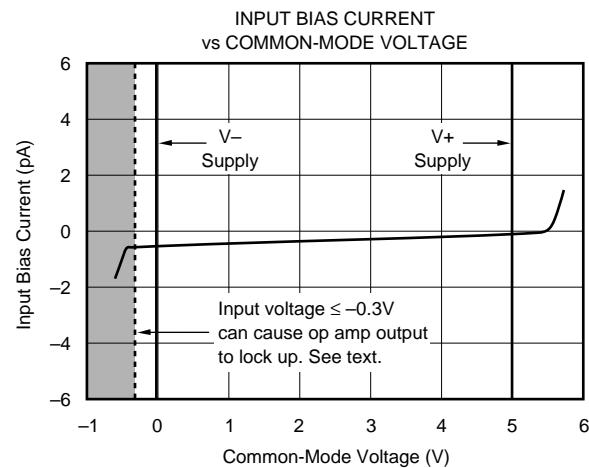
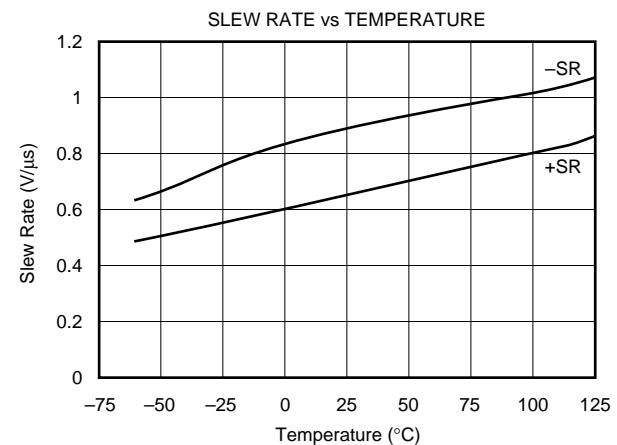
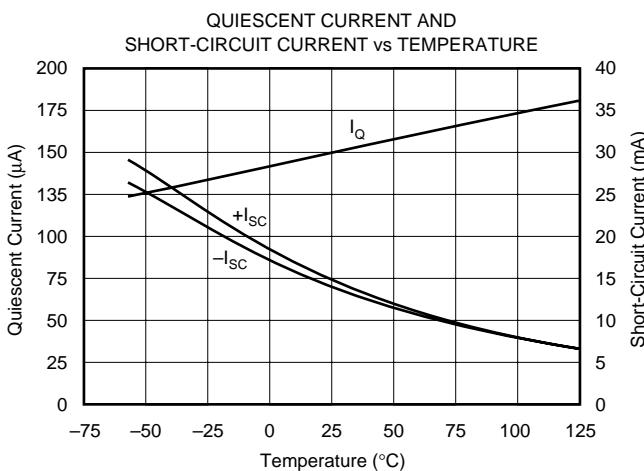
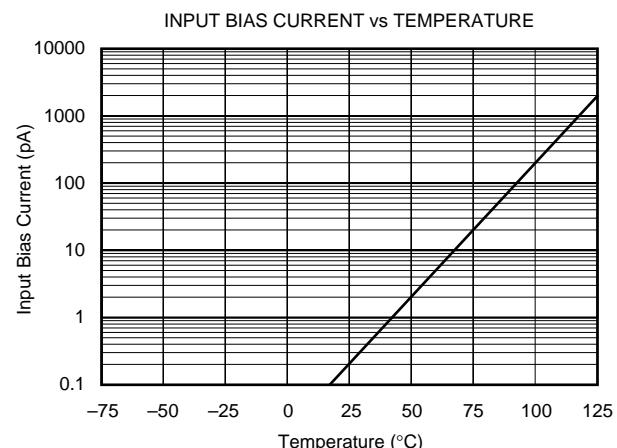
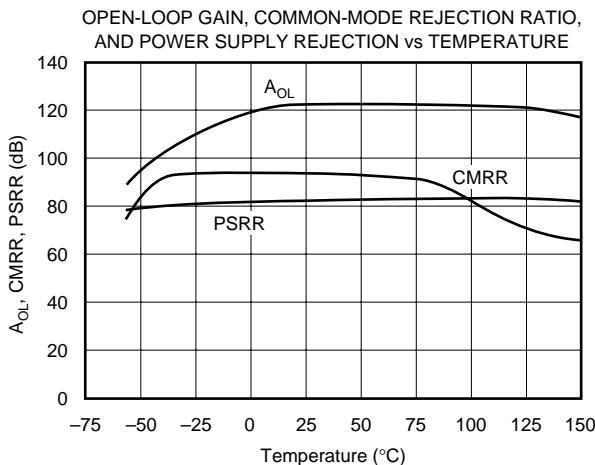
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



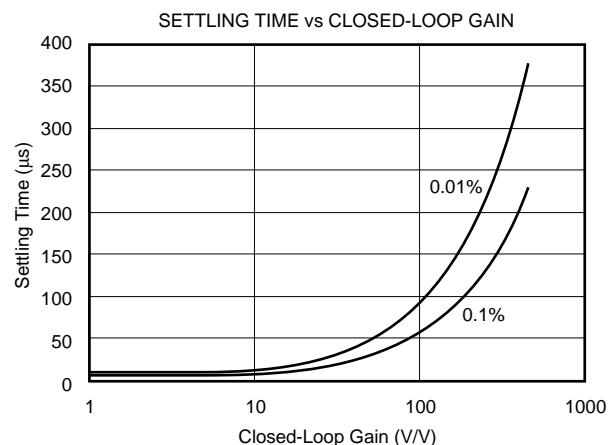
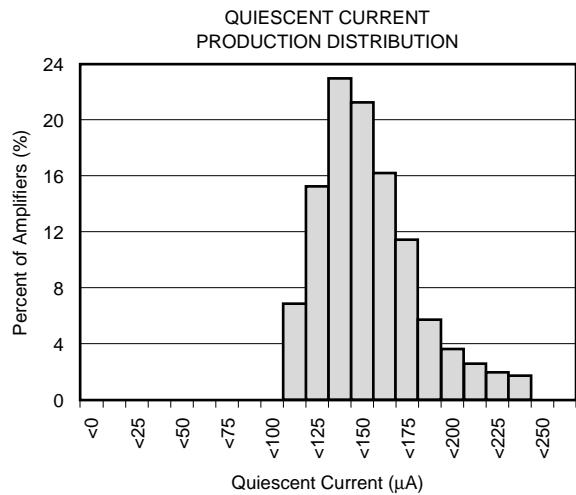
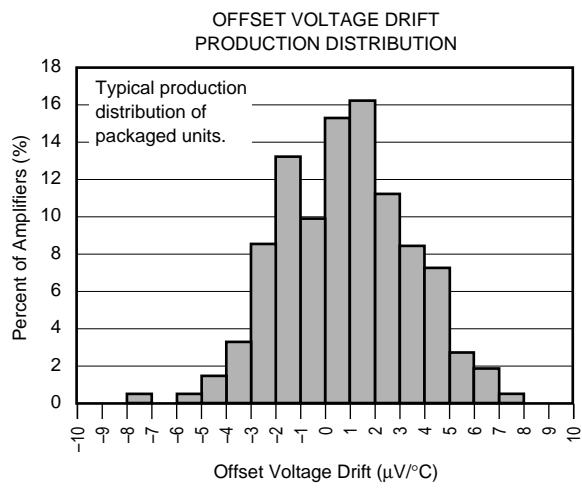
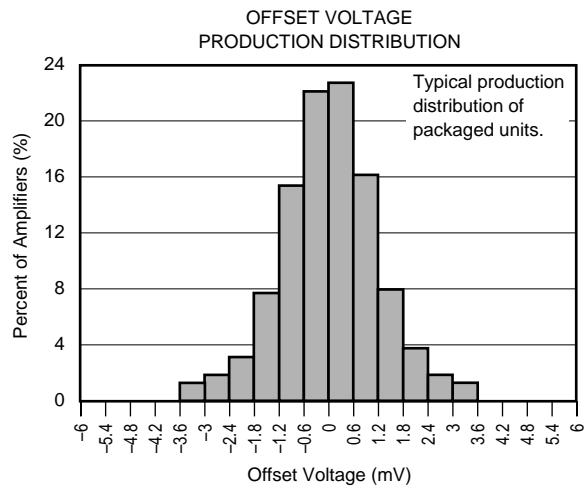
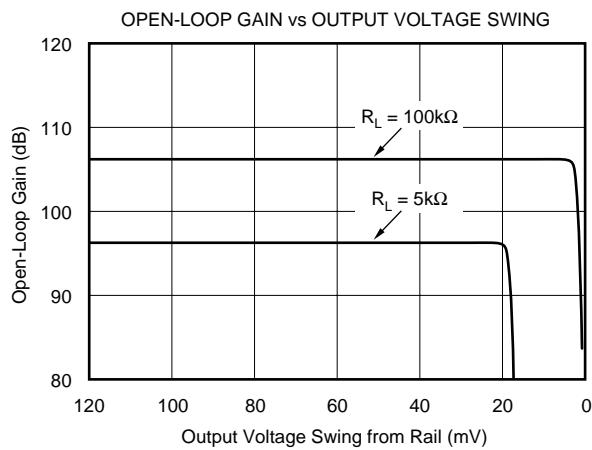
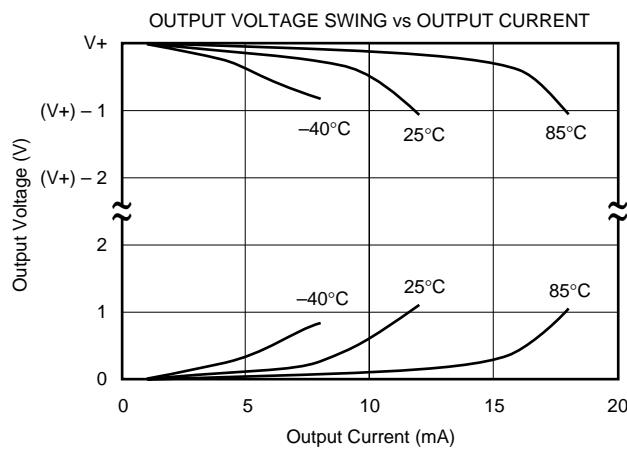
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



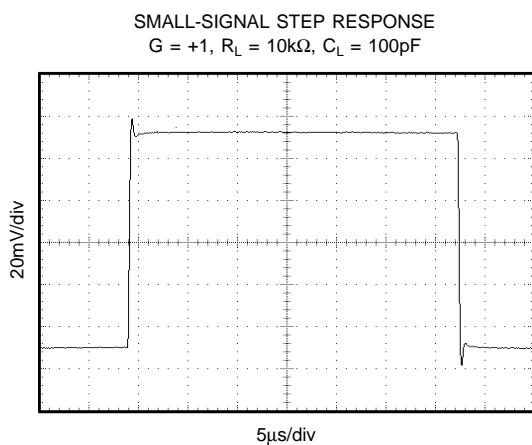
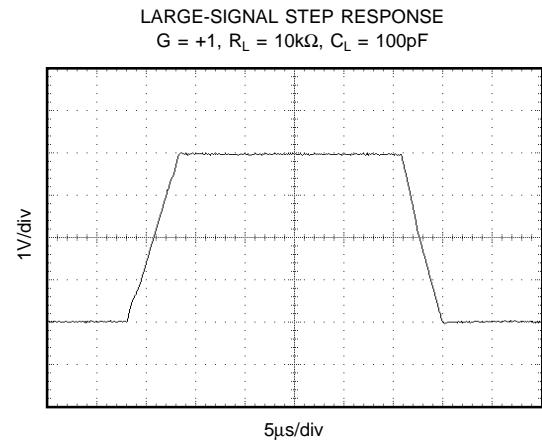
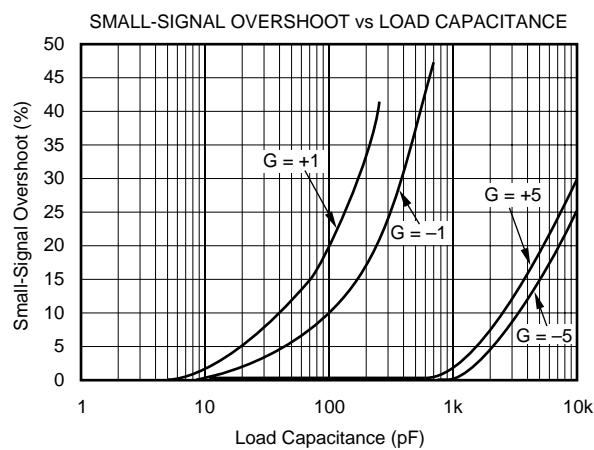
## TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



## TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



# APPLICATIONS INFORMATION

OPA342 series op amps are unity gain stable and can operate on a single supply, making them highly versatile and easy to use.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA342 in unity-gain configuration. Operation is from  $V_S = +5V$  with a  $10k\Omega$  load connected to  $V_S/2$ . The input is a  $5Vp-p$  sinusoid. Output voltage is approximately  $4.997Vp-p$ .

Power supply pins should be bypassed with  $0.01\mu F$  ceramic capacitors.

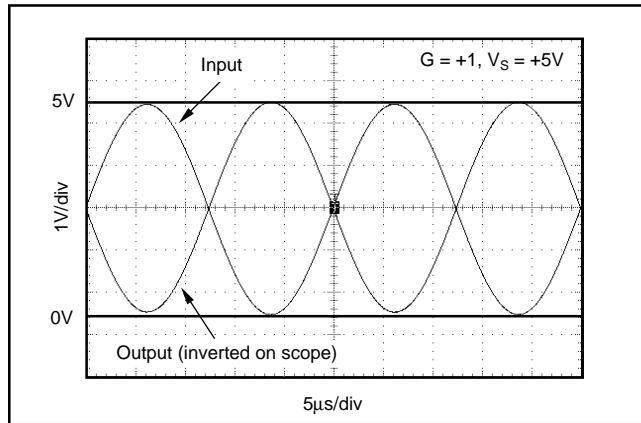


FIGURE 1. Rail-to-Rail Input and Output.

## OPERATING VOLTAGE

OPA342 series op amps are fully specified and guaranteed from  $+2.7V$  to  $+5.5V$ . In addition, many specifications apply from  $-40^\circ C$  to  $+85^\circ C$ . Parameters that vary significantly with operating voltages or temperature are shown in the Typical Performance Curves.

## RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA342 series extends 300mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (see Figure 2). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.3V$  to 300mV above the positive supply, while the P-channel pair is on for inputs from 300mV below the negative supply to approximately  $(V+) - 1.3V$ . There is a small transition region, typically  $(V+) - 1.5V$  to  $(V+) - 1.1V$ , in which both pairs are on. This 400mV transition region can vary 300mV with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 1.8V$  to  $(V+) - 1.4V$  on the low end, up to  $(V+) - 1.2V$  to  $(V+) - 0.8V$  on the high end. Within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3 "Design Optimization with Rail-to-Rail Input Op Amps."

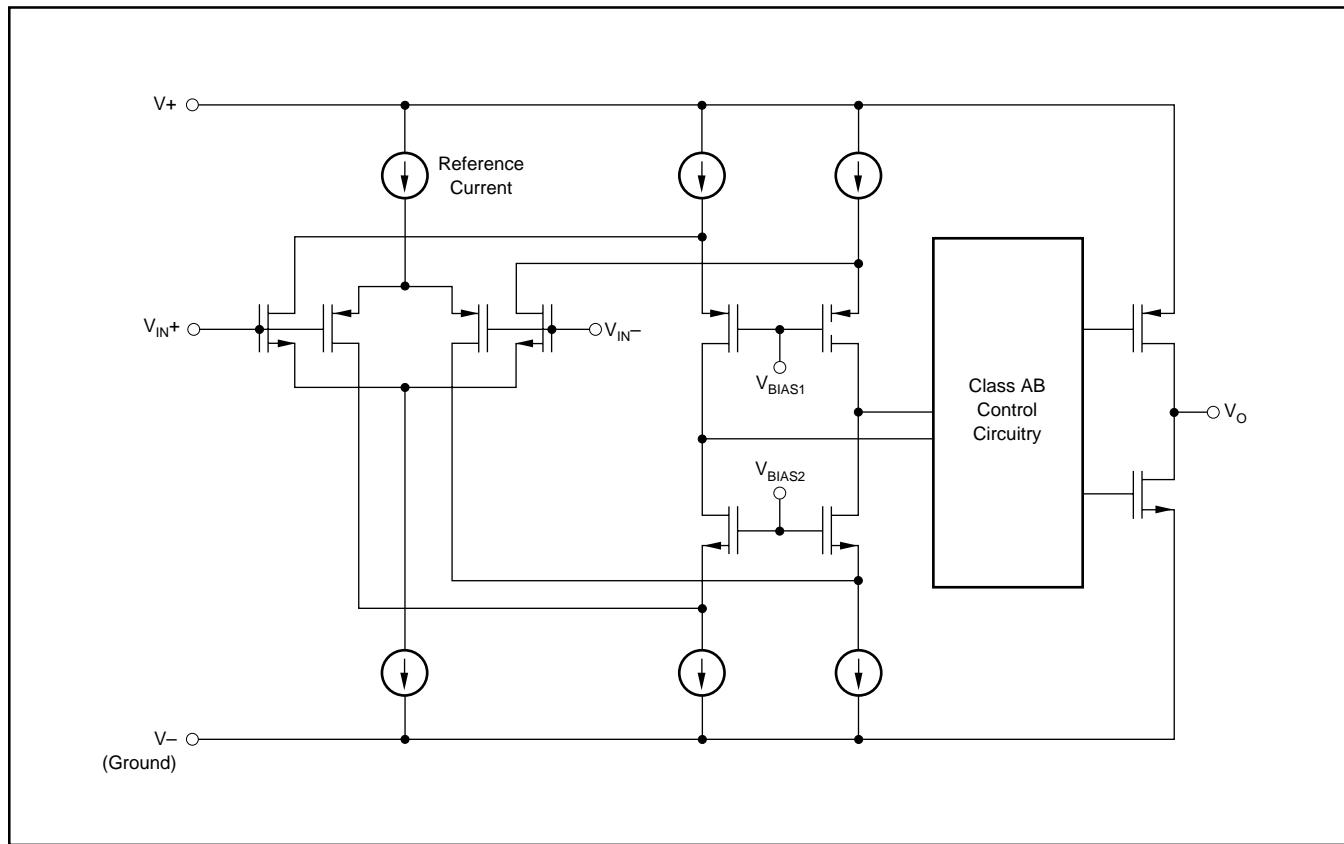


FIGURE 2. Simplified Schematic.

## DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However some applications exercise the amplifier through the transition region of both differential input stages. Although the two input stages are laser trimmed for excellent matching, a small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below  $V_+$  supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the non-inverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to  $V_B$ . If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

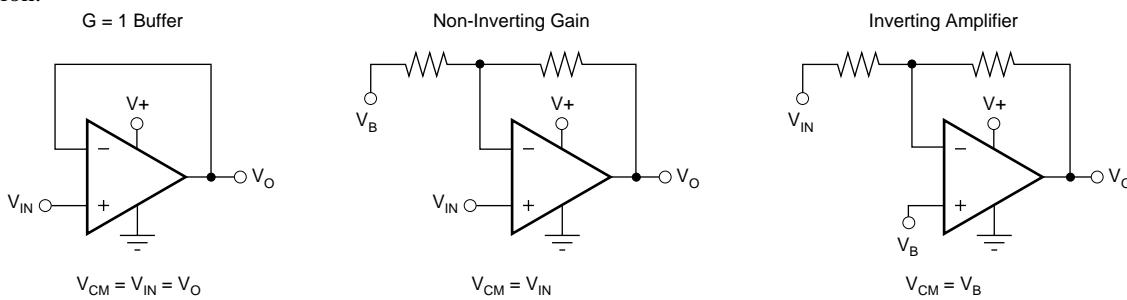


FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

### COMMON-MODE REJECTION

The CMRR for the OPA342 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ( $V_{CM} < (V_+ - 1.8V)$ ) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at  $V_S = 5.5V$  over the entire common-mode range is specified. Third, the CMRR at  $V_S = 2.7V$  over the entire common-mode range is provided. These last two values include the variations seen through the transition region.

### INPUT VOLTAGE BEYOND THE RAILS

If the input voltage can go more than 0.3V below the negative power supply rail (single-supply ground), special precautions are required. If the input voltage goes sufficiently negative, the op amp output may lock up in an inoperative state. A Schottky diode clamp circuit will prevent this—see Figure 4. The series resistor prevents excessive current (greater than 10mA) in the Schottky diode and in the internal ESD protection diode, if the input voltage can exceed the positive supply voltage. If the signal source is limited to less than 10mA, the input resistor is not required.

### RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving  $600\Omega$  loads connected to any potential

between  $V_+$  and ground. For light resistive loads ( $> 50k\Omega$ ), the output voltage can typically swing to within 1mV from supply rail. With moderate resistive loads ( $2k\Omega$  to  $50k\Omega$ ), the output can swing to within a few tens of milli-volts from the supply rails while maintaining high open-loop gain. See the typical performance curve “Output Voltage Swing vs Output Current.”

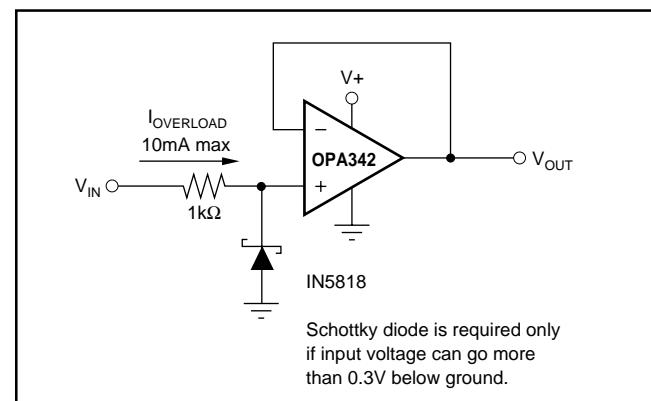


FIGURE 4. Input Current Protection for Voltages Exceeding the Supply Voltage.

### CAPACITIVE LOAD AND STABILITY

The OPA342 in a unity-gain configuration can directly drive up to  $250pF$  pure capacitive load. Increasing the gain enhances the amplifier’s ability to drive greater capacitive loads. See the typical performance curve “Small-Signal

Overshoot vs Capacitive Load.” In unity-gain configurations, capacitive load drive can be improved by inserting a small ( $10\Omega$  to  $20\Omega$ ) resistor,  $R_S$ , in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_S/R_L$ , and is generally negligible.

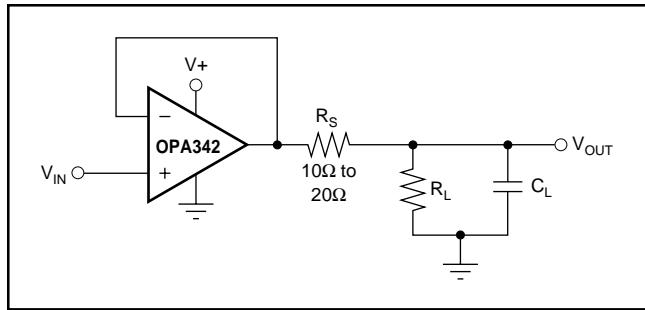


FIGURE 5. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

## DRIVING A/D CONVERTERS

The OPA342 series op amps are optimized for driving medium-speed sampling ADCs. The OPA342 op amps buffer the ADC's input capacitance and resulting charge injection while providing signal gain.

Figures 6 shows the OPA342 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, micro-power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA342, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC's input can be used to filter charge injection.

Figure 7 shows the OPA2342 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with  $V_S = +2.7V$  to  $+5V$  with less than  $500\mu A$  quiescent current.

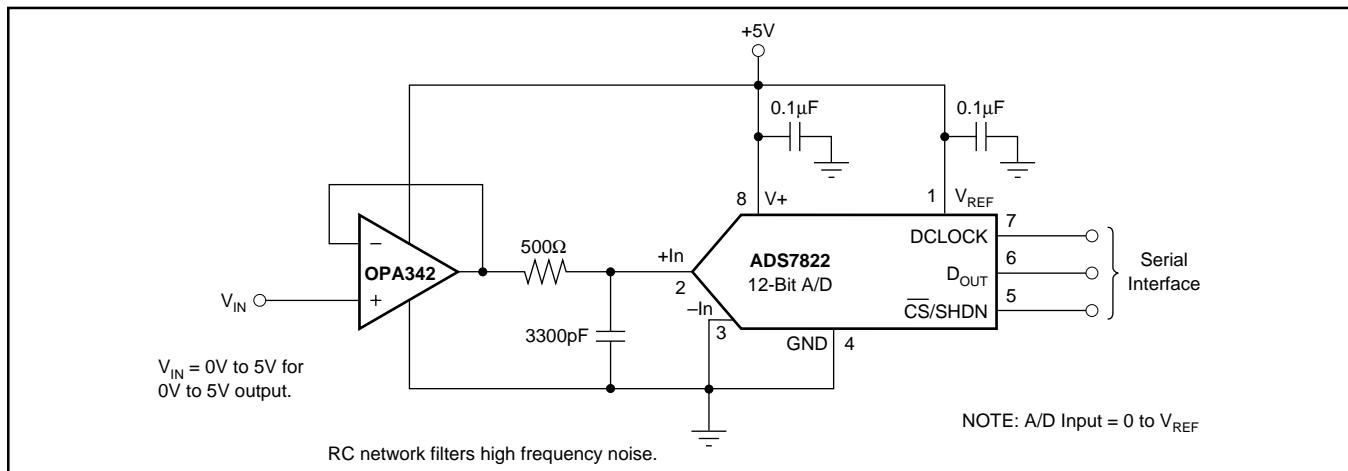


FIGURE 6. OPA342 in Noninverting Configuration Driving ADS7822.

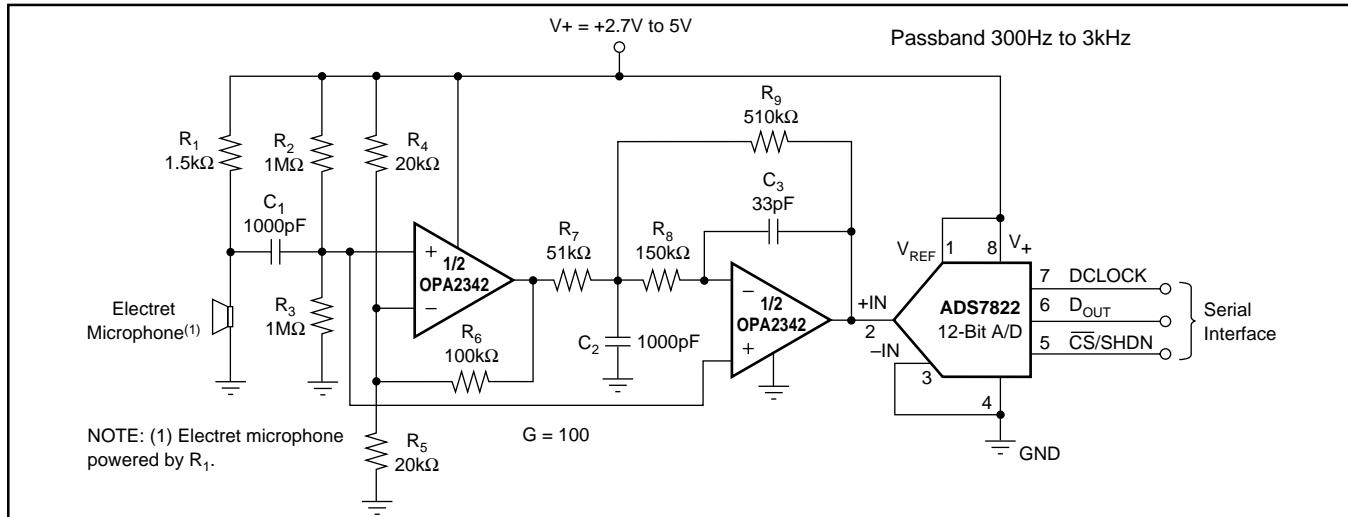


FIGURE 7. Speech Bandpass Filtered Data Acquisition System.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2342EA/250	Last Time Buy	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Nipdaugag   Nipdau	Level-2-260C-1 YEAR	-40 to 85	C42
OPA2342EA/250.B	Last Time Buy	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C42
OPA2342EA/2K5	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI   Nipdaugag   Nipdau	Level-2-260C-1 YEAR	-40 to 85	C42
OPA2342EA/2K5.B	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C42
OPA2342UA	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2342UA
OPA2342UA.B	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2342UA
OPA2342UA/2K5	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2342UA
OPA2342UA/2K5.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2342UA
OPA342NA/250	Last Time Buy	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B42
OPA342NA/250.B	Last Time Buy	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B42
OPA342NA/3K	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B42
OPA342NA/3K.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B42
OPA342NA/3KG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B42
OPA342UA	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 342UA
OPA342UA.B	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 342UA
OPA342UAG4	Last Time Buy	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 342UA
OPA4342EA/250	Last Time Buy	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4342EA
OPA4342EA/250.B	Last Time Buy	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4342EA

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4342UA	Last Time Buy	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4342UA
OPA4342UA.B	Last Time Buy	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4342UA
OPA4342UAG4	Last Time Buy	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4342UA

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

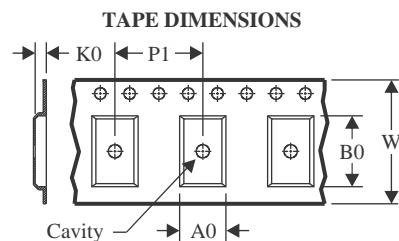
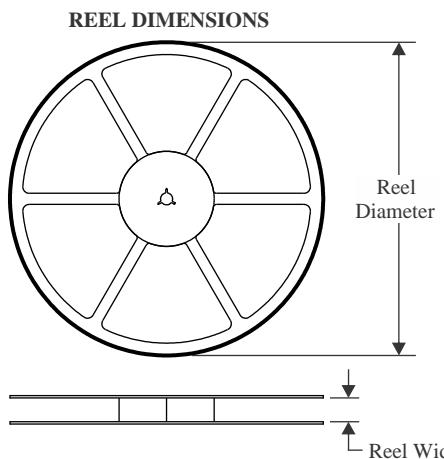
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

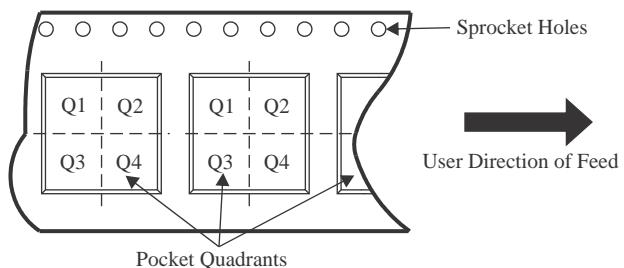
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

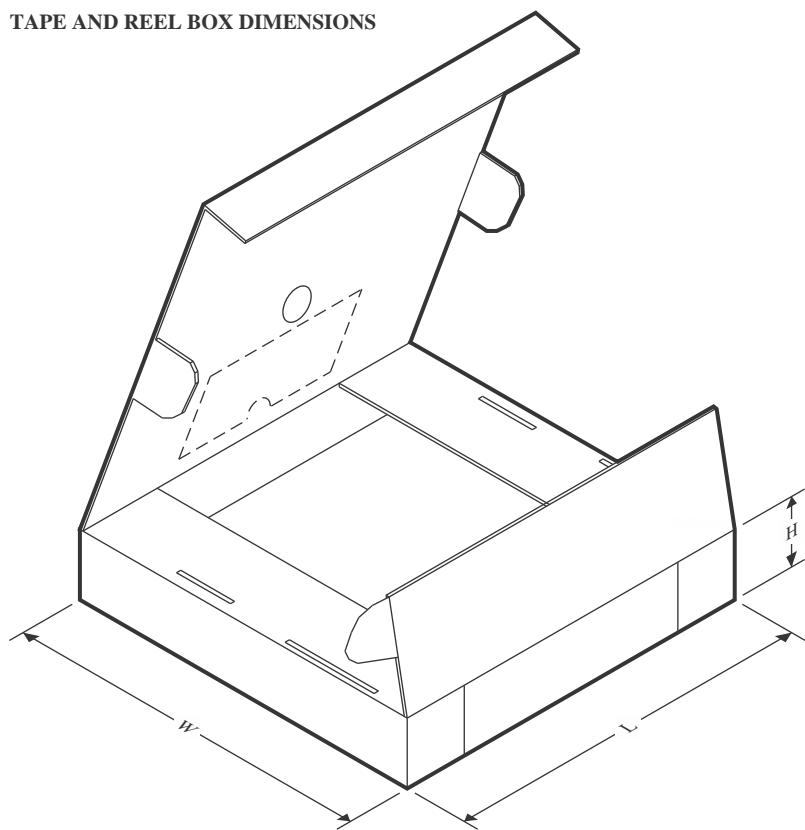
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


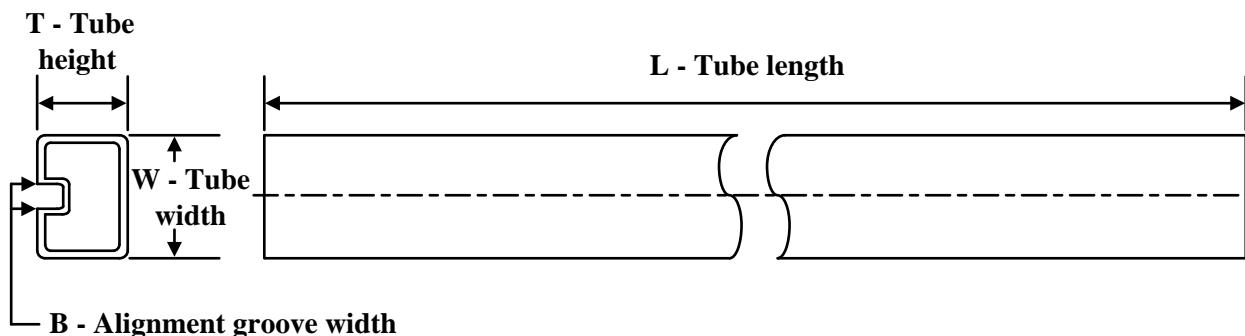
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2342EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2342EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2342UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA342NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA342NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA4342EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2342EA/250	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2342EA/2K5	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2342UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA342NA/250	SOT-23	DBV	5	250	445.0	220.0	345.0
OPA342NA/3K	SOT-23	DBV	5	3000	445.0	220.0	345.0
OPA4342EA/250	TSSOP	PW	14	250	213.0	191.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
OPA2342UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2342UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA342UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA342UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA342UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA4342UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4342UA.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4342UAG4	D	SOIC	14	50	506.6	8	3940	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025