



# 1.8V, 700nA, Zero-Crossover RAIL-TO-RAIL I/O OPERATIONAL AMPLIFIER

## FEATURES

- **nanoPOWER:**
  - OPA369: 800nA
  - OPA2369: 700nA/ch.
- **LOW OFFSET VOLTAGE: 250 $\mu$ V**
  - ZERO-CROSSOVER
- **LOW OFFSET DRIFT: 0.4 $\mu$ V/ $^{\circ}$ C**
- **DC PRECISION:**
  - CMRR: 114dB
  - PSRR: 106dB
  - AOL: 134dB
- **GAIN-BANDWIDTH PRODUCT: 12kHz**
- **SUPPLY VOLTAGE: 1.8V to 5.5V**
- **microSIZE PACKAGES:**
  - SC70-5, SOT23-5, MSOP-8

## DESCRIPTION

The OPA369 and OPA2369 are ultra-low-power, low-voltage operational amplifiers from Texas Instruments designed especially for battery-powered applications.

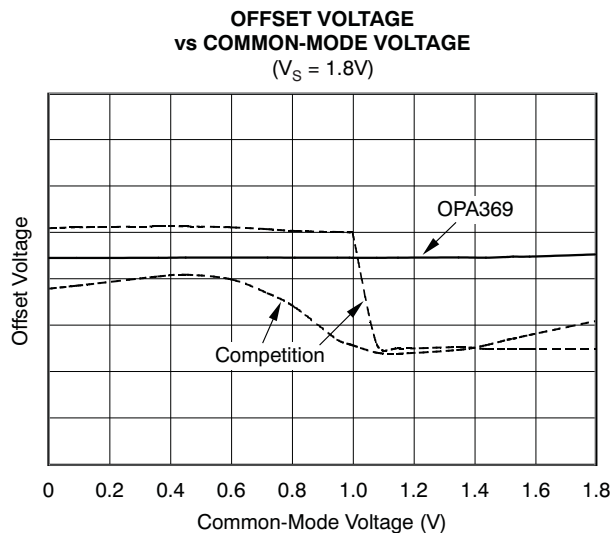
The OPA369 operates on a supply voltage as low as 1.8V and has true rail-to-rail operation that makes it useful for a wide range of applications. The *zero-crossover* feature resolves the problem of input crossover distortion that becomes very prominent in low voltage (< 3V), rail-to-rail input applications.

In addition to *microsize* packages and very low quiescent current, the OPA369 features 12kHz bandwidth, low offset drift (1.75 $\mu$ V/ $^{\circ}$ C, max), and low noise 3.6 $\mu$ V<sub>PP</sub> (0.1Hz to 10Hz).

The OPA369 (single version) is offered in an SC70-5 package. The OPA2369 (dual version) comes in both MSOP-8 and SOT23-8 packages.

## APPLICATIONS

- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT
- LOW-POWER SENSOR SIGNAL CONDITIONING



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage $V_S = (V+) - (V-)$		+7	V
Single Input Terminals	Voltage <sup>(2)</sup>	$(V-) - 0.5$ to $(V+) + 0.5$	V
	Current <sup>(2)</sup>	$\pm 10$	mA
Output Short-Circuit <sup>(3)</sup>		Continuous	
Ambient Operating Temperature		-55 to +125	°C
Ambient Storage Temperature		-65 to +150	°C
Junction Temperature $T_J$		+150	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

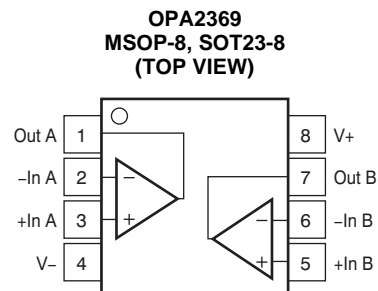
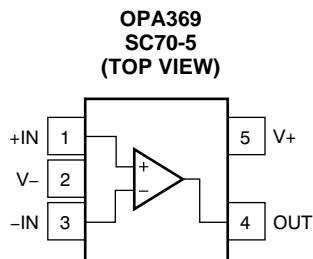
- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to  $V_S/2$ , one amplifier per package.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA369	SC70-5	DCK	CJS
OPA2369	MSOP-8	DGK	OCCQ
	SOT23-8	DCN	OCBQ

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS



**ELECTRICAL CHARACTERISTICS:  $V_S = +1.8V$  to  $+5.5V$** 
**BOLDFACE** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

 At  $T_A = +25^{\circ}C$ , and  $R_L = 100k\Omega$  connected to  $V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA369, OPA2369			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage	$V_{OS}$		250	750	$\mu V$
<b>over Temperature</b>				<b>1</b>	<b>mV</b>
<b>Drift</b>	$dV_{OS}/dT$		<b>0.4</b>	<b>1.75</b>	$\mu V/^{\circ}C$
<b>vs Power Supply</b>	PSRR	$V_S = 1.8V$ to $5.5V$	<b>5</b>	<b>20</b>	$\mu V/V$
Channel Separation	dc		140		dB
	f = 1kHz		120		dB
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{CM}$	(V–)		(V+)	V
Common-Mode Rejection Ratio	CMRR	$(V-) \leq V_{CM} \leq (V+)$	100	114	dB
<b>over Temperature</b>		$(V-) \leq V_{CM} \leq (V+)$	<b>90</b>		<b>dB</b>
<b>INPUT BIAS CURRENT</b>					
Input Bias Current	$I_B$		10	50	pA
<b>over Temperature</b>			See Figure 16		<b>pA</b>
Input Offset Current	$I_{OS}$		10	50	pA
<b>INPUT IMPEDANCE</b>					
Differential			$10^{13} \parallel 3$		$\Omega \parallel pF$
Common-Mode			$10^{13} \parallel 6$		$\Omega \parallel pF$
<b>NOISE</b>					
Input Voltage Noise		f = 0.1Hz to 10Hz	3.6		$\mu V_{PP}$
Input Voltage Noise Density		f = 100Hz	220		$nV/\sqrt{Hz}$
		f = 1kHz	290		$nV/\sqrt{Hz}$
Current Noise Density		f = 1kHz	1		$fA/\sqrt{Hz}$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain	$A_{OL}$	$100mV \leq V_O \leq (V+)-100mV$ , $R_L = 100k\Omega$	114	134	dB
<b>Over Temperature</b>		$100mV \leq V_O \leq (V+)-100mV$ , $R_L = 100k\Omega$	<b>100</b>		<b>dB</b>
		$500mV \leq V_O \leq (V+)-500mV$ , $R_L = 10k\Omega$	114	134	dB
<b>Over Temperature</b>		$500mV \leq V_O \leq (V+)-500mV$ , $R_L = 10k\Omega$	<b>90</b>		<b>dB</b>
<b>OUTPUT</b>					
Voltage Output Swing from Rail		$R_L = 100k\Omega$ $R_L = 10k\Omega$		<b>10</b> <b>25</b>	<b>mV</b> <b>mV</b>
Short-Circuit Current	$I_{SC}$		10		mA
Capacitive Load Drive	$C_{LOAD}$		See Figure 20		pF
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW		12		kHz
Slew Rate	SR	G = +1	0.005		V/ $\mu s$
Overload Recovery Time		$V_{IN} \times Gain > V_S$	250		$\mu s$

**ELECTRICAL CHARACTERISTICS:  $V_S = +1.8V$  to  $+5.5V$  (continued)**

**BOLDFACE** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

At  $T_A = +25^{\circ}C$ , and  $R_L = 100k\Omega$  connected to  $V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA369, OPA2369			UNIT
		MIN	TYP	MAX	
<b>POWER SUPPLY</b>					
Specified Voltage	$V_S$	1.8		5.5	V
Quiescent Current	$I_Q$				
OPA369	$I_{OUT} = 0A$		0.8	1.2	$\mu A$
OPA2369 (per channel)			0.7	1	$\mu A$
<b>Over Temperature</b>					
<b>OPA369</b>				<b>1.45</b>	<b><math>\mu A</math></b>
<b>OPA2369 (per channel)</b>				<b>1.25</b>	<b><math>\mu A</math></b>
<b>TEMPERATURE RANGE</b>					
Specified Range	$T_A$	-40		+85	$^{\circ}C$
Operating Range	$T_A$	-55		+125	$^{\circ}C$
Thermal Resistance	$\theta_{JA}$				
SC70			250		$^{\circ}C/W$
SOT23			223		$^{\circ}C/W$
MSOP			252		$^{\circ}C/W$

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ , and  $R_L = 100\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.

**OFFSET VOLTAGE PRODUCTION DISTRIBUTION**

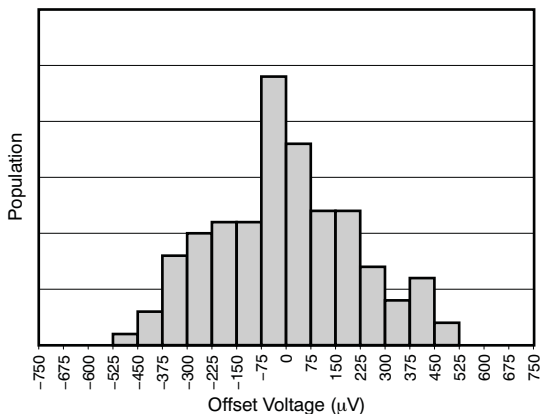


Figure 1.

**OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION**

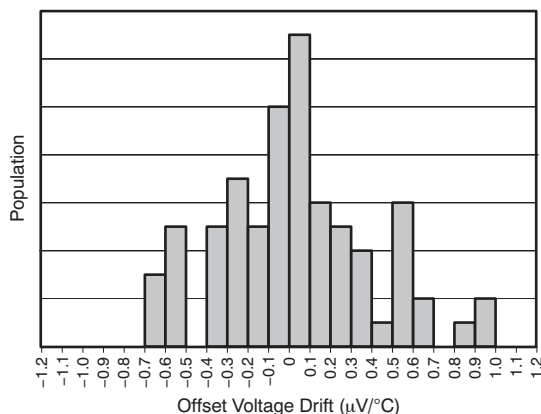


Figure 2.

**OFFSET VOLTAGE vs TEMPERATURE**

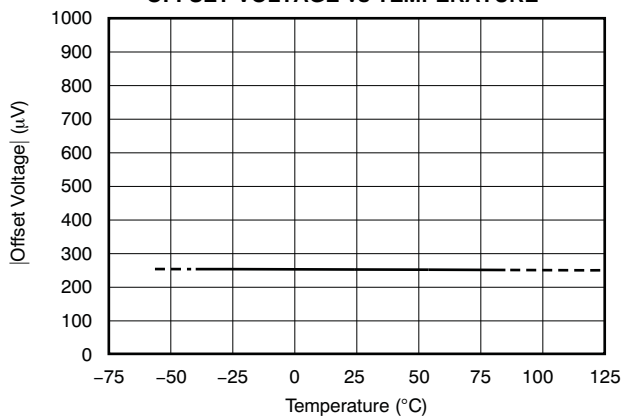


Figure 3.

**NORMALIZED OFFSET VOLTAGE vs COMMON-MODE VOLTAGE**

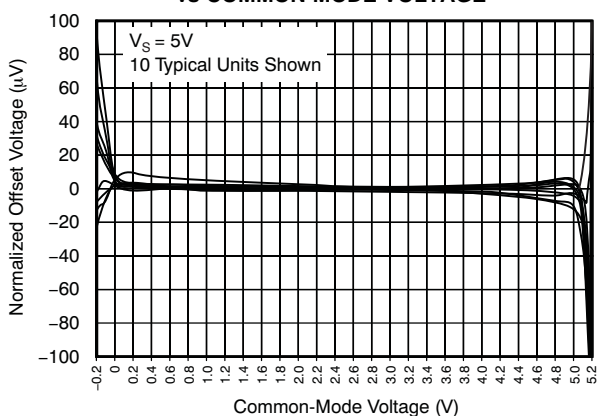


Figure 4.

**0.1Hz to 10Hz NOISE**

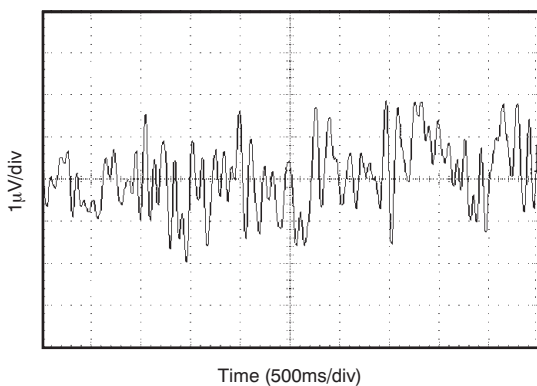


Figure 5.

**INPUT-REFERRED VOLTAGE NOISE vs FREQUENCY**

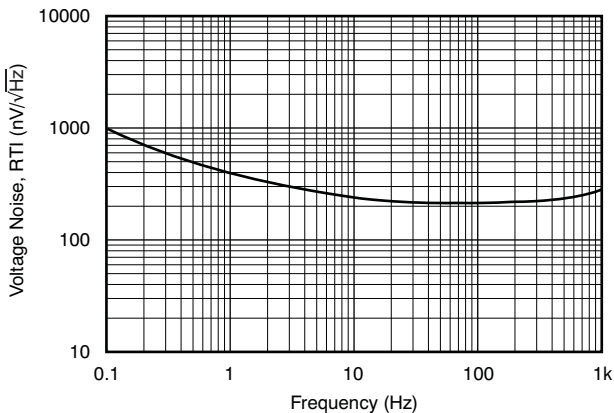


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ , and  $R_L = 100\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

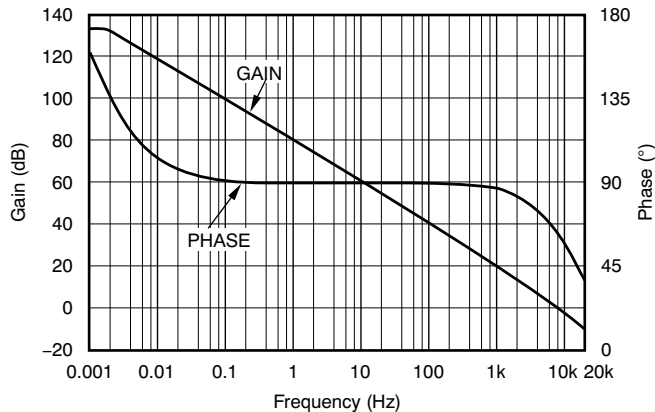


Figure 7.

**OPEN-LOOP GAIN vs TEMPERATURE**

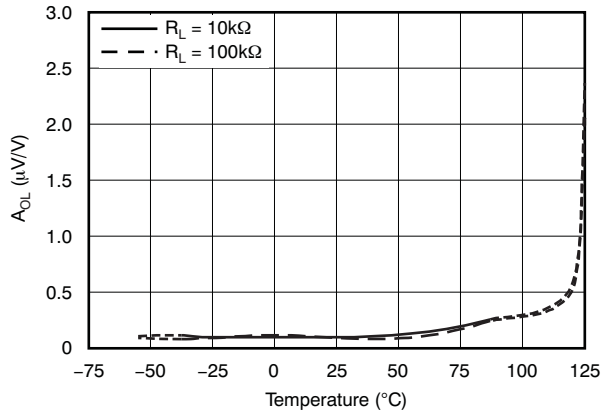


Figure 8.

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

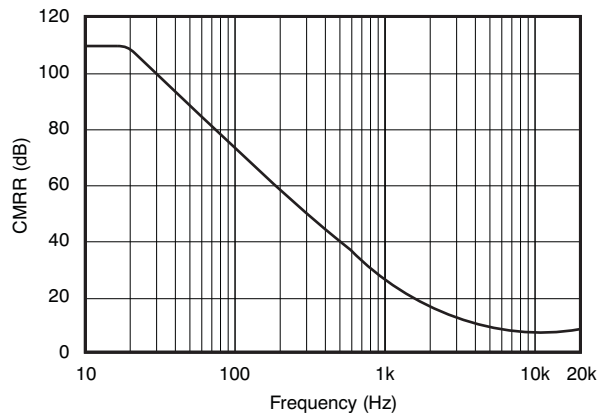


Figure 9.

**COMMON-MODE REJECTION RATIO vs TEMPERATURE**

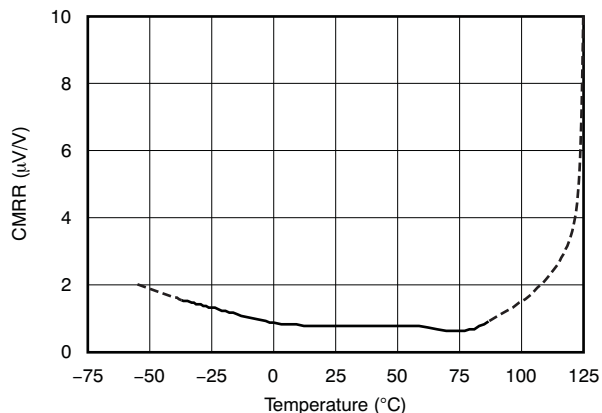


Figure 10.

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

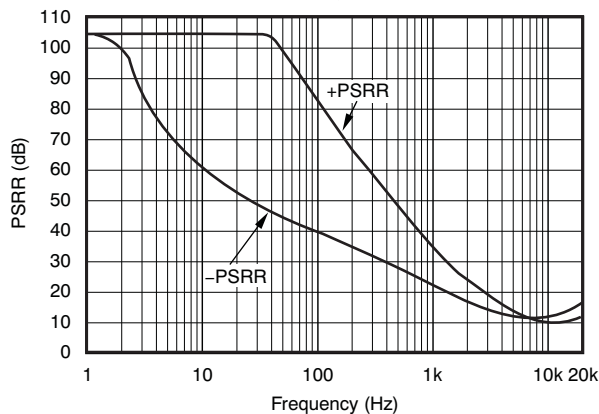


Figure 11.

**POWER-SUPPLY REJECTION RATIO vs TEMPERATURE**

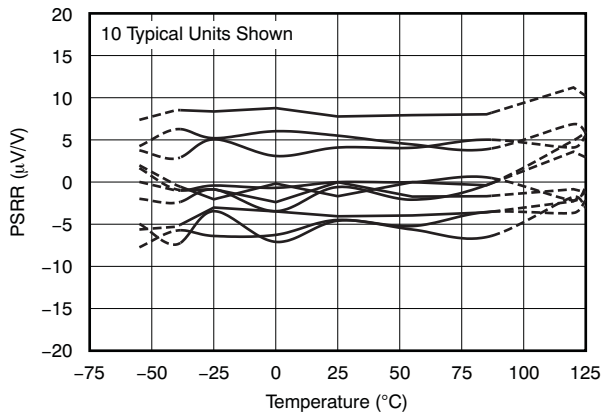


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ , and  $R_L = 100\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.

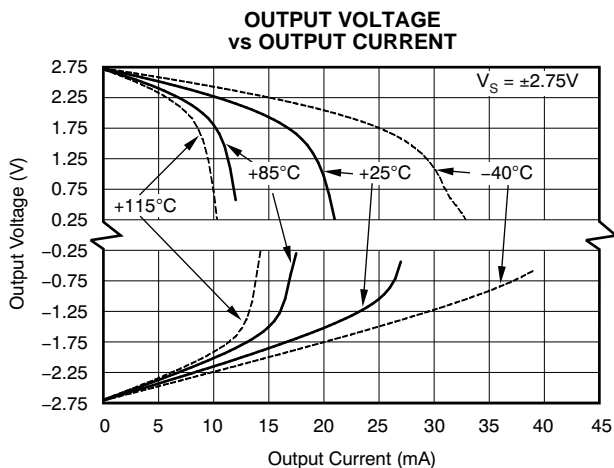


Figure 13.

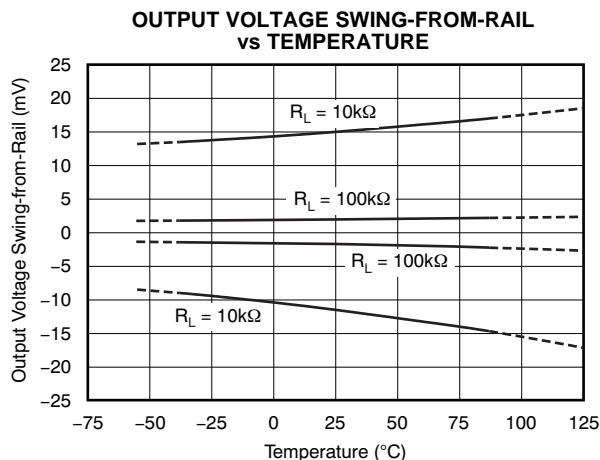


Figure 14.

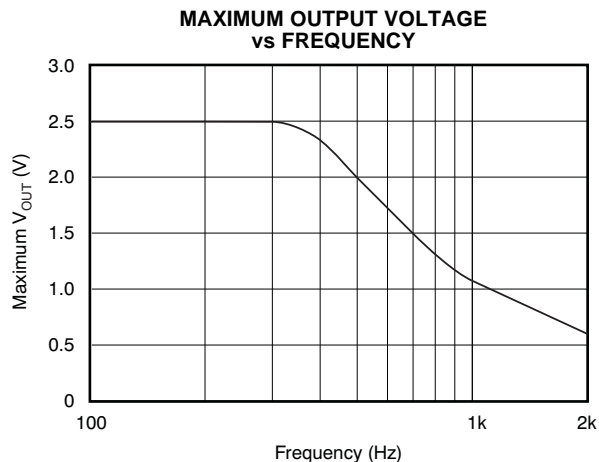


Figure 15.

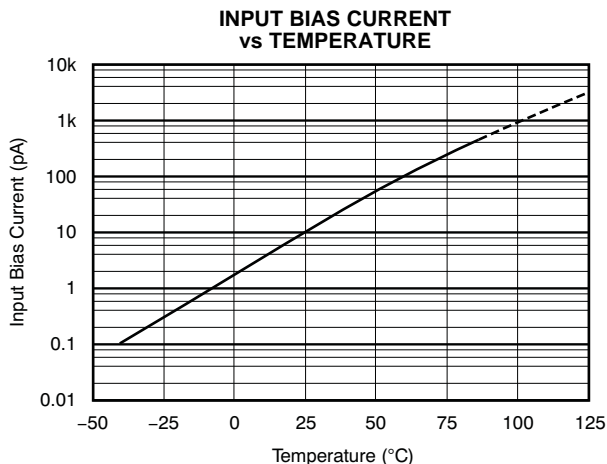


Figure 16.

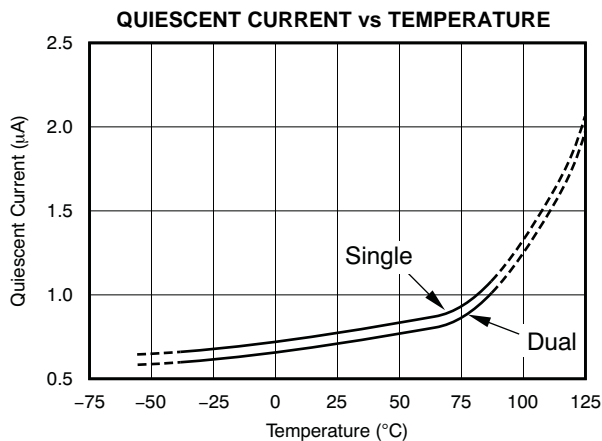


Figure 17.

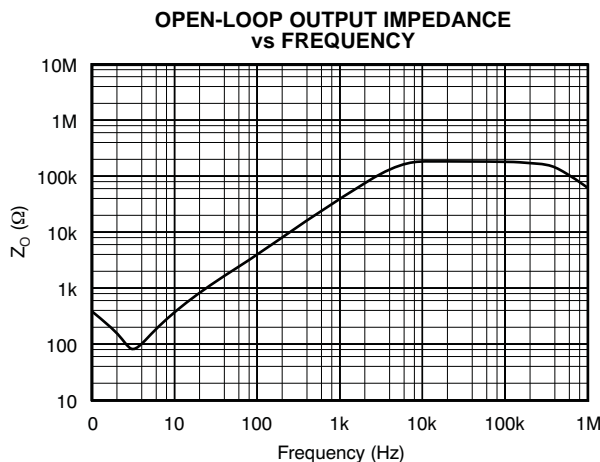


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ , and  $R_L = 100\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.

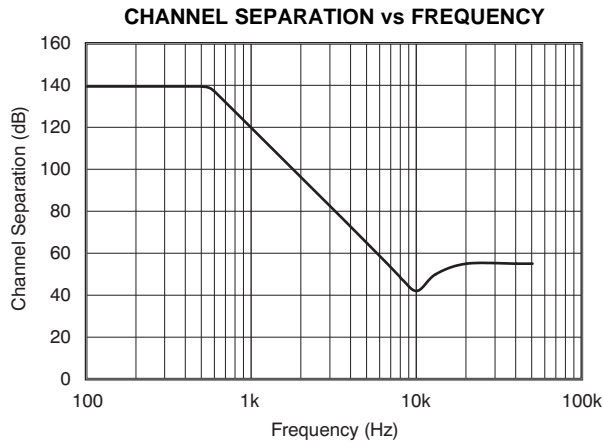


Figure 19.

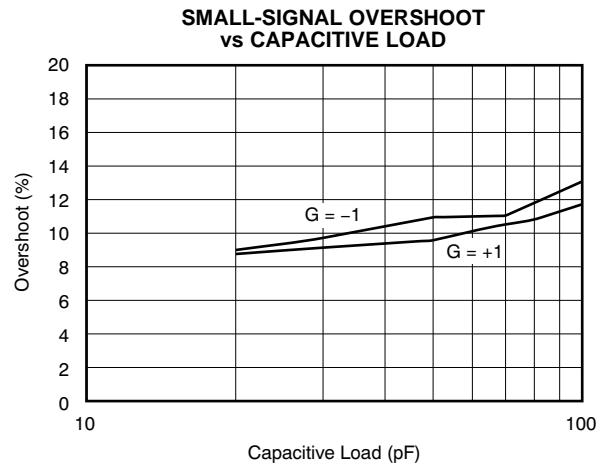


Figure 20.

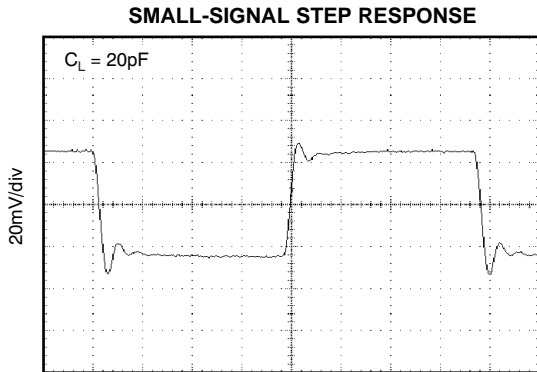


Figure 21.

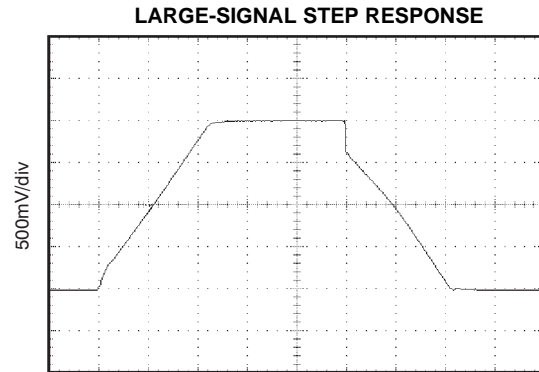


Figure 22.

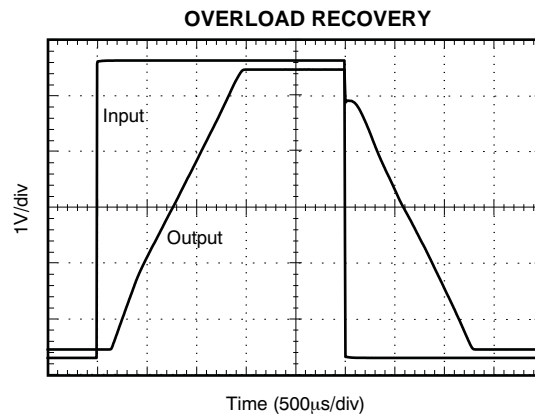


Figure 23.

## APPLICATION INFORMATION

The OPA369 family of operational amplifiers minimizes power consumption and operates on supply voltages as low as 1.8V. Power-supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and open-loop gain ( $A_{OL}$ ) typical values are in the range of 100dB or better.

When designing for ultralow power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

Good layout practice mandates the use of a 0.1 $\mu$ F bypass capacitor placed closely across the supply pins.

### OPERATING VOLTAGE

OPA369 series op amps are fully specified and tested from +1.8V to +5.5V ( $\pm 0.9V$  to  $\pm 2.75V$ ). Parameters that vary significantly with supply voltage are shown in the [Typical Characteristic](#) curves.

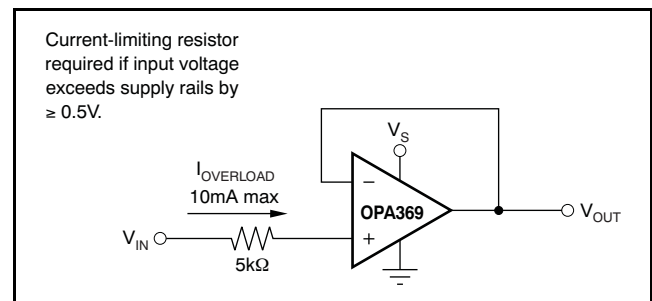
### INPUT COMMON-MODE VOLTAGE RANGE

The OPA369 family is designed to eliminate the input offset transition region typically present in most rail-to-rail complementary stage operational amplifiers, which allows the OPA369 family of amplifiers to provide superior common-mode performance over the entire input range.

The input common-mode voltage range of the OPA369 family typically extends to each supply rail. CMRR is specified from the negative rail to the positive rail. See [Figure 4](#), *Normalized Offset Voltage vs Common-Mode Voltage*.

### PROTECTING INPUTS FROM OVER-VOLTAGE

Input currents are typically 10pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, in addition to keeping the input voltage between the supply rails, it is also important to limit the input current to less than 10mA. This limiting is easily accomplished with an input resistor, as shown in [Figure 24](#).



**Figure 24. Input Current Protection for Voltages Exceeding the Supply Voltage**

## BATTERY MONITORING

The low operating voltage and quiescent current of the OPA369 series make it an excellent choice for battery monitoring applications, as shown in Figure 25. In this circuit,  $V_{STATUS}$  is high as long as the battery voltage remains above 2V. A low-power reference is used to set the trip point. Resistor values are selected as follows:

1. Selecting  $R_F$ : Select  $R_F$  such that the current through  $R_F$  is approximately 1000x larger than the maximum bias current over temperature:

$$R_F = \frac{V_{REF}}{1000(I_{BMAX})}$$

$$= \frac{1.2V}{1000(50pA)}$$

$$= 24M\Omega \approx 20M\Omega \quad (1)$$

2. Choose the hysteresis voltage,  $V_{HYST}$ . For battery-monitoring applications, 50mV is adequate.

3. Calculate  $R_1$  as follows:

$$R_1 = R_F \left[ \frac{V_{HYST}}{V_{BATT}} \right] = 20M\Omega \left[ \frac{50mV}{2.4V} \right] = 420k\Omega \quad (2)$$

4. Select a threshold voltage for  $V_{IN}$  rising ( $V_{THRS}$ ) = 2.0V

5. Calculate  $R_2$  as follows:

$$R_2 = \frac{1}{\left[ \left( \frac{V_{THRS}}{V_{REF} \times R_1} \right) - \frac{1}{R_1} - \frac{1}{R_F} \right]}$$

$$= \frac{1}{\left[ \left( \frac{2V}{1.2V \times 420k\Omega} \right) - \frac{1}{420k\Omega} - \frac{1}{20M\Omega} \right]}$$

$$= 650k\Omega \quad (3)$$

6. Calculate  $R_{BIAS}$ : The minimum supply voltage for this circuit is 1.8V. The REF1112 has a current requirement of 1.2μA (max). Providing the REF1112 with 2μA of supply current assures proper operation. Therefore:

$$R_{BIAS} = \frac{(V_{BATTMIN} - V_{REF})}{I_{BIAS}} = \frac{(1.8V - 1.2V)}{2\mu A} = 0.3M\Omega \quad (4)$$

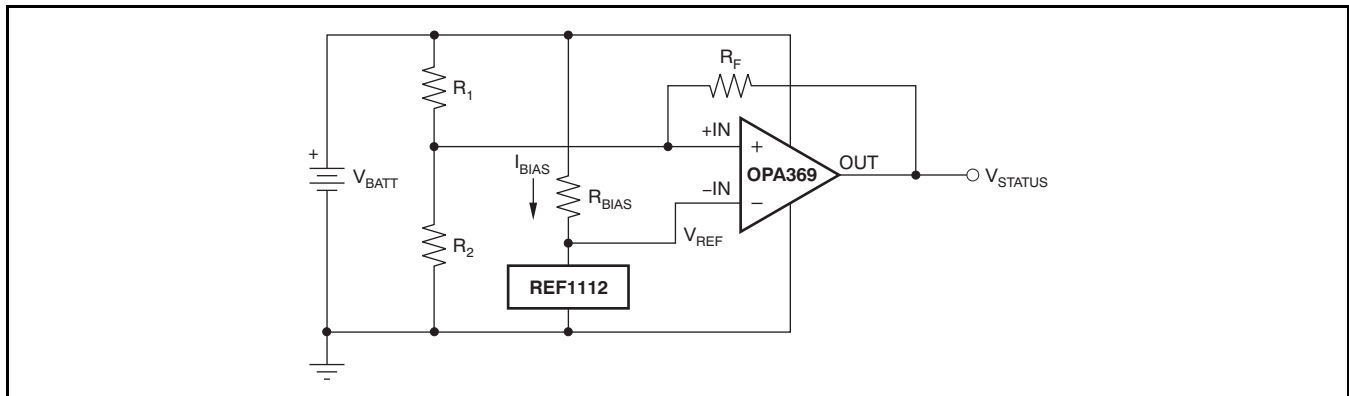


Figure 25. Battery Monitor

## WINDOW COMPARATOR

Figure 26 shows the OPA2369 used as a window comparator. The threshold limits are set by  $V_H$  and  $V_L$ , with  $V_H > V_L$ . When  $V_{IN} < V_H$ , the output of A1 is low. When  $V_{IN} > V_L$ , the output of A2 is low. Therefore, both op amp outputs are at 0V as long as  $V_{IN}$  is between  $V_H$  and  $V_L$ . This architecture results in no current flowing through either diode, Q1 in cutoff, with the base voltage at 0V, and  $V_{OUT}$  forced high.

If  $V_{IN}$  falls below  $V_L$ , the output of A2 is high, current flows through D2, and  $V_{OUT}$  is low. Likewise, if  $V_{IN}$  rises above  $V_H$ , the output of A1 is high, current flows through D1, and  $V_{OUT}$  is low. The window comparator threshold voltages are set as follows:

$$V_H = \frac{R_2}{R_1 + R_2} \times V_S \quad (5)$$

$$V_L = \frac{R_4}{R_3 + R_4} \times V_S \quad (6)$$

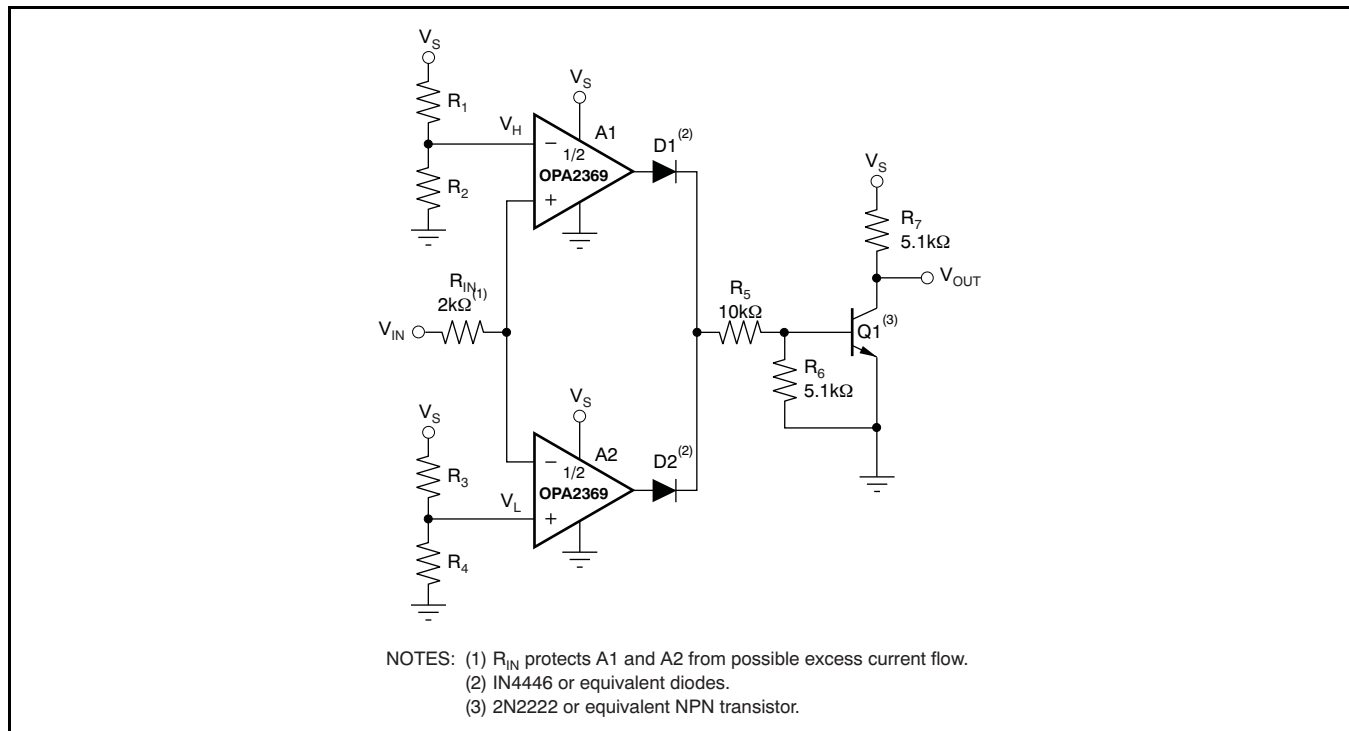
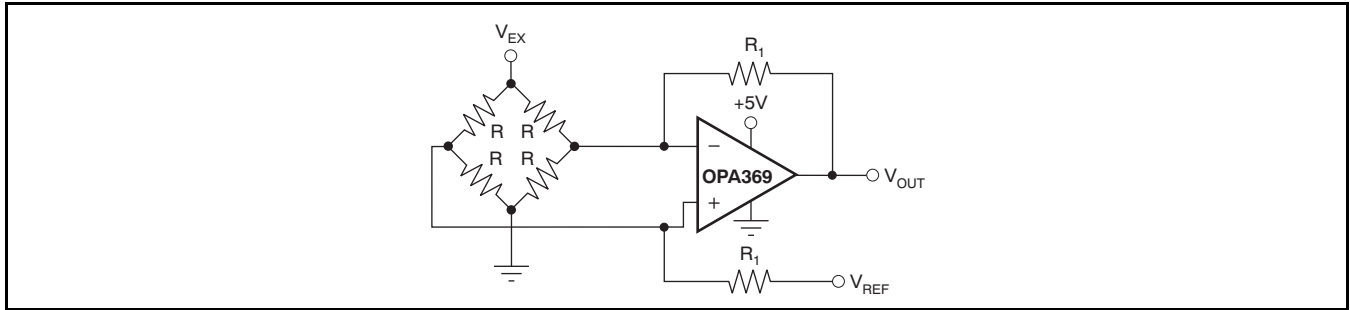


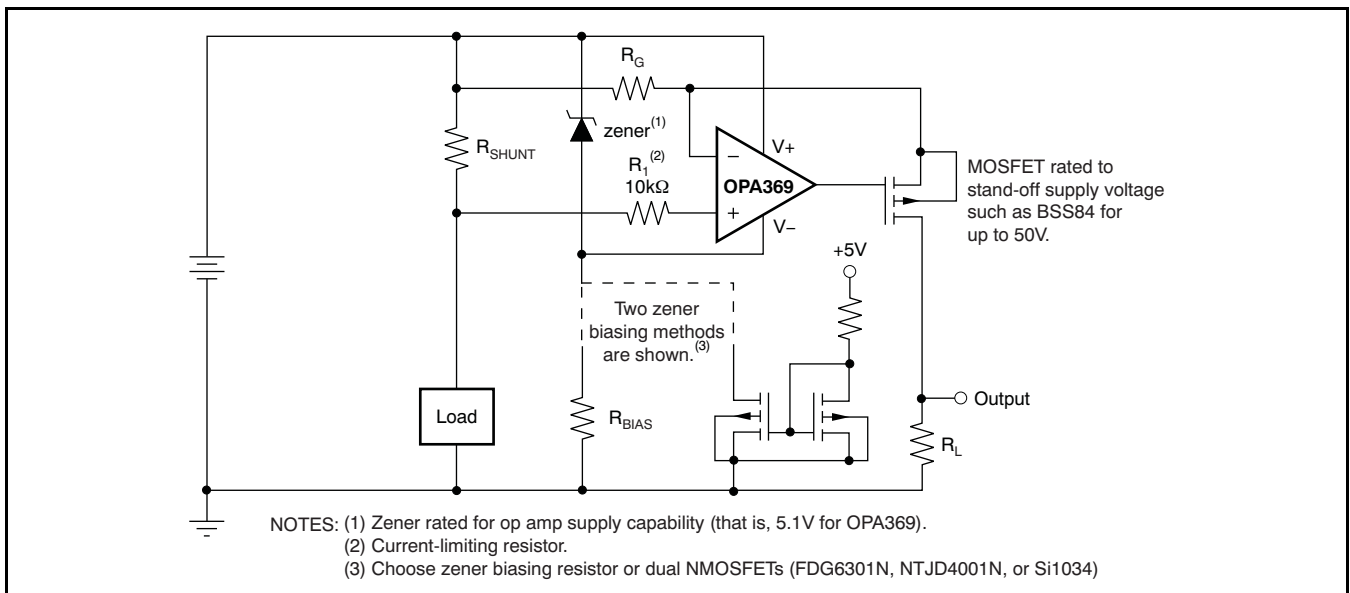
Figure 26. OPA2369 as a Window Comparator

**ADDITIONAL APPLICATION EXAMPLES**

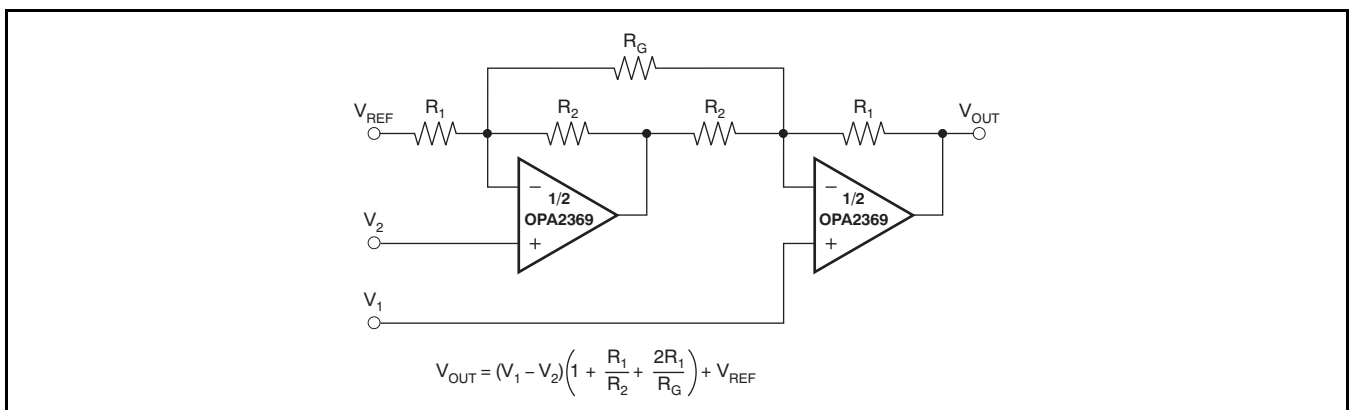
Figure 27 through Figure 29 illustrate additional application examples.



**Figure 27. Single Op Amp Bridge Amplifier**



**Figure 28. High-Side Current Monitor**



**Figure 29. Two Op Amp Instrumentation Amplifier**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">OPA2369AIDCNR</a>	Active	Production	SOT-23 (DCN)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCBQ
OPA2369AIDCNR.A	Active	Production	SOT-23 (DCN)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCBQ
OPA2369AIDCNRG4	Active	Production	SOT-23 (DCN)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCBQ
<a href="#">OPA2369AIDCNT</a>	Active	Production	SOT-23 (DCN)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCBQ
OPA2369AIDCNT.A	Active	Production	SOT-23 (DCN)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCBQ
<a href="#">OPA2369AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 85	OCCQ
OPA2369AIDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCCQ
<a href="#">OPA2369AIDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	Call TI   Nipdauag   Nipdau	Level-2-260C-1 YEAR	-40 to 85	OCCQ
OPA2369AIDGKT.A	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCCQ
OPA2369AIDGKTG4	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCCQ
<a href="#">OPA369AIDCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKRG4	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKRG4.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKRG4.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
<a href="#">OPA369AIDCKT</a>	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKT.A	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS
OPA369AIDCKT.B	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CJS

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2369AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2369AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2369AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2369AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA369AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA369AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA369AIDCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA369AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA369AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2369AIDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
OPA2369AIDCNT	SOT-23	DCN	8	250	213.0	191.0	35.0
OPA2369AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2369AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA369AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA369AIDCKR	SC70	DCK	5	3000	213.0	191.0	35.0
OPA369AIDCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
OPA369AIDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA369AIDCKT	SC70	DCK	5	250	213.0	191.0	35.0

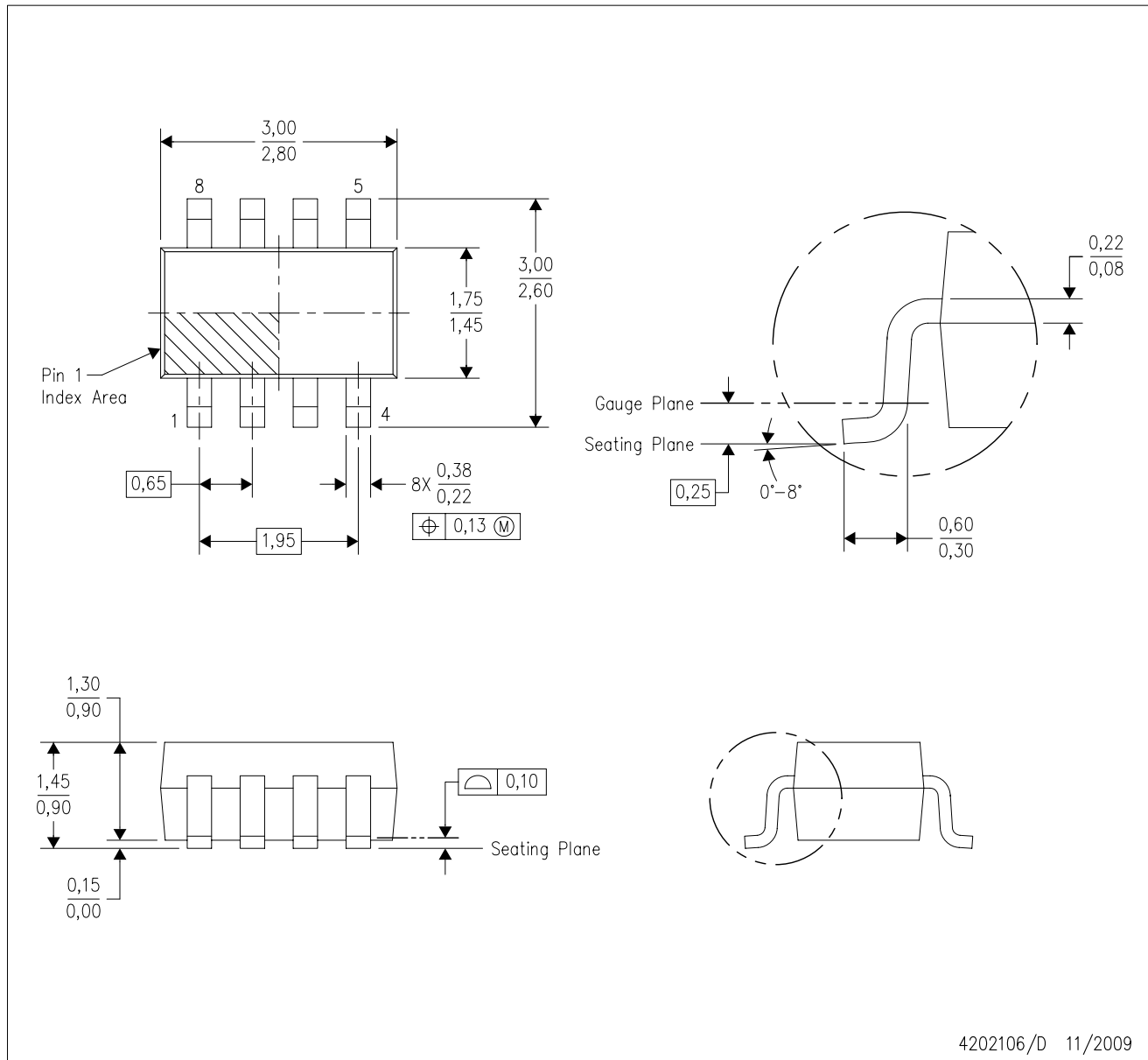
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2369AIDGKR	DGK	VSSOP	8	2500	274	6.55	500	2.88
OPA2369AIDGKR.A	DGK	VSSOP	8	2500	274	6.55	500	2.88
OPA2369AIDGKT	DGK	VSSOP	8	250	274	6.55	500	2.88
OPA2369AIDGKT.A	DGK	VSSOP	8	250	274	6.55	500	2.88
OPA2369AIDGKTG4	DGK	VSSOP	8	250	274	6.55	500	2.88

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.
  - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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