Single and Dual Precision, 17 MHz, Low Noise, CMOS Input Amplifiers

Check for Samples: LMP7711

FEATURES

- **Unless Otherwise Noted, Typical Values at V_S = 5V.**
- **Input Offset Voltage ±150 µV (Max)**
- **Input Bias Current 100 fA**
- **Input Voltage Noise 5.8 nV/√Hz**
- **Gain Bandwidth Product 17 MHz**
- **Supply Current (LMP7711) 1.15 mA**
- **Supply Current (LMP7712) 1.30 mA**
- **Supply Voltage Range 1.8V to 5.5V**
- **THD+N @ f = 1 kHz 0.001%**
- **Operating Temperature Range −40°C to 125°C**
- **Rail-to-rail Output Swing**
- **Space Saving SOT Package (LMP7711)**
- **10-pin VSSOP Package (LMP7712)**

APPLICATIONS

- **Active Filters and Buffers**
- **Sensor Interface Applications**
- **Transimpedance Amplifiers**

DESCRIPTION

The LMP7711/LMP7712 are single and dual low noise, low offset, CMOS input, rail-to-rail output precision amplifiers with a high gain bandwidth product and an enable pin. The LMP7711/LMP7712 are part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

Utilizing a CMOS input stage, the LMP7711/LMP7712 achieve an input bias current of 100 fA, an input referred voltage noise of 5.8 nV/√Hz, and an input offset voltage of less than ±150 µV. These features make the LMP7711/LMP7712 superior choices for precision applications.

Consuming only 1.15 mA of supply current, the LMP7711 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains.

The LMP7711/LMP7712 have a supply voltage range of 1.8V to 5.5V, which makes these ideal choices for portable low power applications with low supply voltage requirements. In order to reduce the already low power consumption the LMP7711/LMP7712 have an enable function. Once in shutdown, the LMP7711/LMP7712 draw only 140 nA of supply current.

The LMP7711/LMP7712 are built with TI's advanced VIP50 process technology. The LMP7711 is offered in a 6-pin SOT package and the LMP7712 is offered in a 10-pin VSSOP.

TYPICAL PERFORMANCE

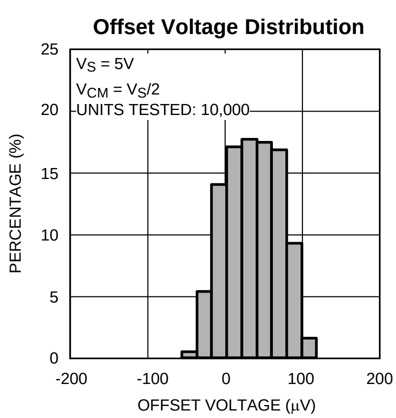

Figure 1.

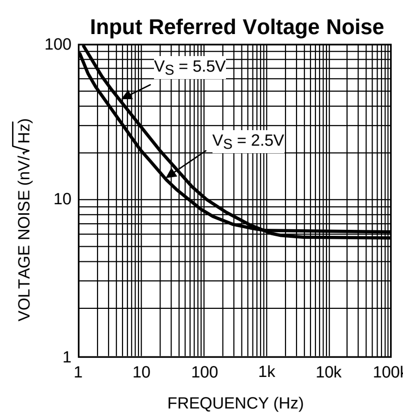

Figure 2.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±0.3V
Supply Voltage ($V_S = V^+ – V^−$)		6.0V
Voltage on Input/Output Pins		V^+ +0.3V, $V^−$ −0.3V
Storage Temperature Range		−65°C to 150°C
Junction Temperature(4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

OPERATING RATINGS(1)

Temperature Range(2)		−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^−$)	0°C ≤ T_A ≤ 125°C	1.8V to 5.5V
	−40°C ≤ T_A ≤ 125°C	2.0V to 5.5V
Package Thermal Resistance (θ_{JA}(2))	6-Pin SOT	170°C/W
	10-Pin VSSOP	236°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V ,V_O = V_{CM} = $V^+/2$, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
V_{OS}	Input Offset Voltage			±20	±180 **±480**	μV
TC V_{OS}	Input Offset Voltage Temperature Drift[3][4]	LMP7711 LMP7712	–1.75	–1	±4	μV/°C
I_B	Input Bias Current	V_{CM} = 1.0V[5][4], −40°C ≤ TA ≤ 85°C		0.05	1 **25**	pA
		V_{CM} = 1.0V[5][4], −40°C ≤ TA ≤ 125°C		0.05	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 1.0V[4]		0.006	0.5 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V	83 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	−0.3 **–0.3**		1.5 **1.5**	V
A_{VOL}	Open Loop Voltage Gain	LMP7711, V_O = 0.15 to 2.2V R_L = 2 kΩ to $V^+/2$	88 **82**	98		dB
		LMP7712, V_O = 0.15 to 2.2V R_L = 2 kΩ to $V^+/2$	84 **80**	92		
		LMP7711, V_O = 0.15 to 2.2V R_L = 10 kΩ to $V^+/2$	92 **88**	114		
		LMP7712, V_O = 0.15 to 2.2V R_L = 10 kΩ to $V^+/2$	90 **86**	95		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to $V^+/2$		25	70 **77**	mV from either rail
		R_L = 10 kΩ to $V^+/2$		20	60 **66**	
	Output Voltage Swing Low	R_L = 2 kΩ to $V^+/2$		30	70 **73**	
		R_L = 10 kΩ to $V^+/2$		15	60 **62**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV[6]	36 **30**	52		mA
		Sinking to V^+ V_{IN} = −200 mV[6]	7.5 **5.0**	15		
I_S	Supply Current	LMP7711 Enable Mode V_{EN} ≥ 2.1		0.95	1.30 **1.65**	mA
		LMP7712 (per channel) Enable Mode V_{EN} ≥ 2.1		1.10	1.50 **1.85**	
		Shutdown Mode (per channel) V_{EN} ≤ 0.4		0.03	1 **4**	μA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		8.3		V/μs
		A_V = +1, Falling (90% to 10%)		10.3		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The short circuit test is a momentary open loop test.

2.5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V ,V_O = V_{CM} = $V^+/2$, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
GBW	Gain Bandwidth			14		MHz
e_n	Input Referred Voltage Noise Density	f = 400 Hz		6.8		$nV/\sqrt{Hz}$
		f = 1 kHz		5.8		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		$pA/\sqrt{Hz}$
t_{on}	Turn-on Time			140		ns
t_{off}	Turn-off Time			1000		ns
V_{EN}	Enable Pin Voltage Range	Enable Mode	2.1	2 - 2.5		V
		Shutdown Mode		0 - 0.5	0.4	
I_{EN}	Enable Pin Input Current	V_{EN} = 2.5V (5)		1.5	3.0	μA
		V_{EN} = 0V (5)		0.003	0.1	
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ V_O = 0.9 V_{PP}		0.003		%
		f = 1 kHz, A_V = 1, R_L = 600Ω V_O = 0.9 V_{PP}		0.004		

5V ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage				±10	±150 **±450**	μV
TC V_{OS}	Input Offset Voltage Temperataure Drift (3)(4)	LMP7711		–1.75	–1	±4	μV/°C
		LMP7712					
I_B	Input Bias Current	V_{CM} = 2.0V (5)(4)	−40°C ≤ TA ≤ 85°C		0.1	1 **25**	pA
			−40°C ≤ TA ≤ 125°C		0.1	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V (4)			0.01	0.5 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		85 **82**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		−0.3 **–0.3**		4 **4**	V

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
A_{VOL}	Open Loop Voltage Gain	LMP7711, V_O = 0.3 to 4.7V R_L = 2 kΩ to V^+/2	88 **82**	107		dB
		LMP7712, V_O = 0.3 to 4.7V R_L = 2 kΩ to V^+/2	84 **80**	90		
		LMP7711, V_O = 0.3 to 4.7V R_L = 10 kΩ to V^+/2	92 **88**	114		
		LMP7712, V_O = 0.3 to 4.7V R_L = 10 kΩ to V^+/2	90 **86**	95		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2		32	70 **77**	mV from either rail
		R_L = 10 kΩ to V^+/2		22	60 **66**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2 (LMP7711)		42	70 **73**	
		R_L = 2 kΩ to V^+/2 (LMP7712)		50	75 **78**	
		R_L = 10 kΩ to V^+/2		20	60 **62**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV (6)	46 **38**	66		mA
		Sinking to V^+ V_{IN} = −200 mV (6)	10.5 **6.5**	23		
I_S	Supply Current	LMP7711 Enable Mode V_{EN} ≥ 4.6		1.15	1.40 **1.75**	mA
		LMP7712 (per channel) Enable Mode V_{EN} ≥ 4.6		1.30	1.70 **2.05**	
		Shutdown Mode V_{EN} ≤ 0.4 (per channel)		0.14	1 **4**	μA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)	6.0	9.5		V/μs
		A_V = +1, Falling (90% to 10%)	7.5	11.5		
GBW	Gain Bandwidth			17		MHz
e_n	Input Referred Voltage Noise Density	f = 400 Hz		7.0		nV/√Hz
		f = 1 kHz		5.8		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
t_{on}	Turn-on Time			114		ns
t_{off}	Turn-off Time			800		ns
V_{EN}	Enable Pin Voltage Range	Enable Mode	4.6	4.5 – 5		V
		Shutdown Mode		0 – 0.5	0.4	
I_{EN}	Enable Pin Input Current	V_{EN} = 5V (7)		5.6	10	μA
		V_{EN} = 0V (7)		0.005	0.2	
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ V_O = 4 V_{PP}		0.001		%
		f = 1 kHz, A_V = 1, R_L = 600Ω V_O = 4 V_{PP}		0.004		

(6) The short circuit test is a momentary open loop test.
(7) Positive current corresponds to current flowing into the device.

CONNECTION DIAGRAM

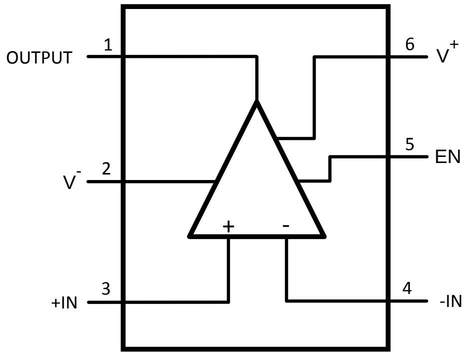


Figure 3. 6-Pin SOT - Top View
See Package Number DDC

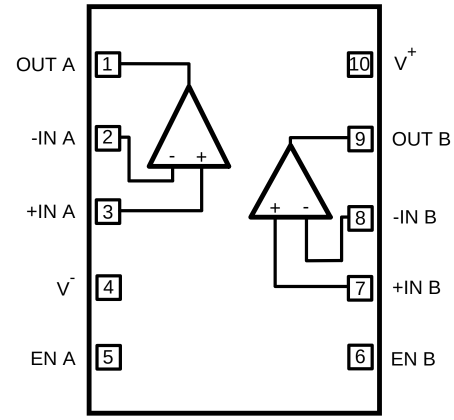


Figure 4. 10-Pin VSSOP-Top View
See Package Number DGS

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

Offset Voltage Distribution

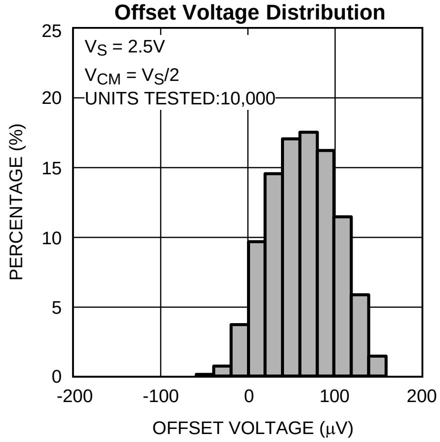


Figure 5.

TCV$_{OS}$ Distribution (LMP7711)

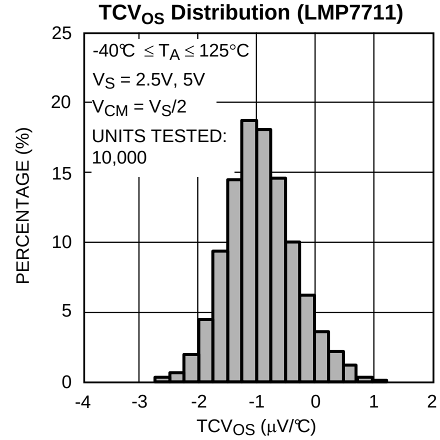


Figure 6.

Offset Voltage Distribution

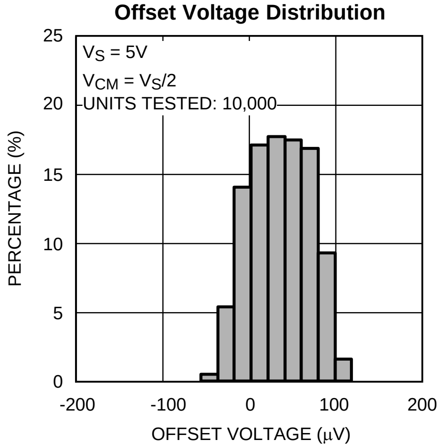


Figure 7.

TCV$_{OS}$ Distribution (LMP7712)

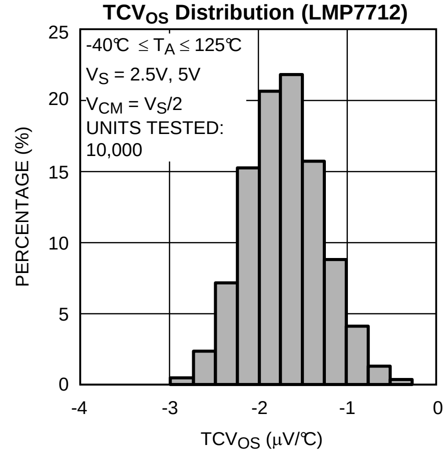


Figure 8.

Offset Voltage vs. V$_{CM}$

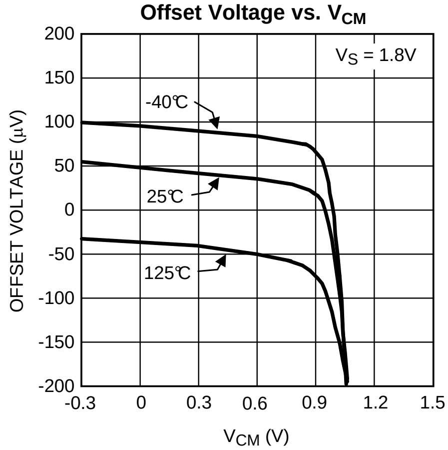


Figure 9.

Offset Voltage vs. V$_{CM}$

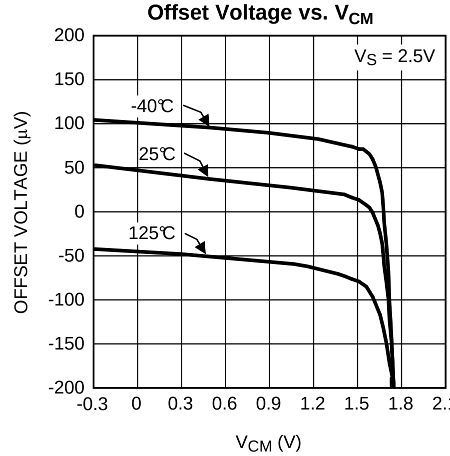


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

Offset Voltage vs. V_{CM}

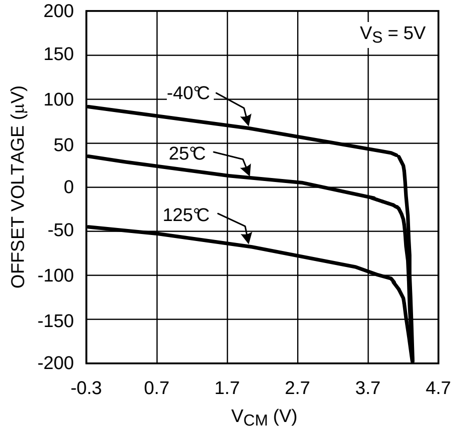


Figure 11.

Offset Voltage vs. Supply Voltage

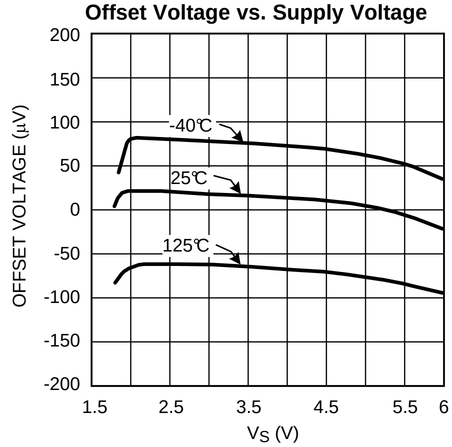


Figure 12.

Offset Voltage vs. Temperature

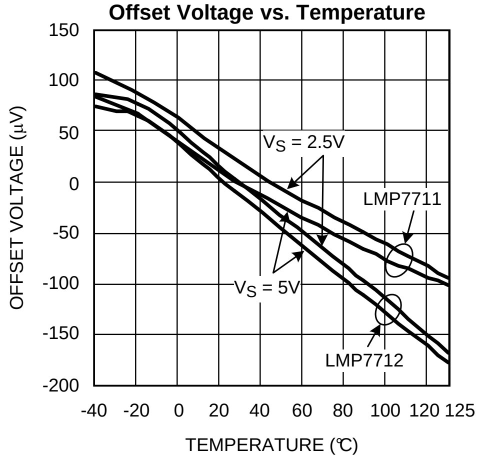


Figure 13.

CMRR vs. Frequency

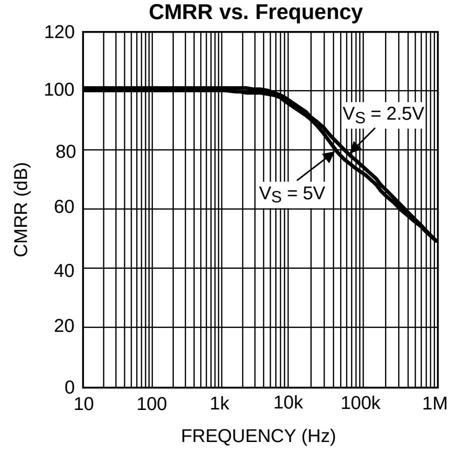


Figure 14.

Input Bias Current Over Temperature

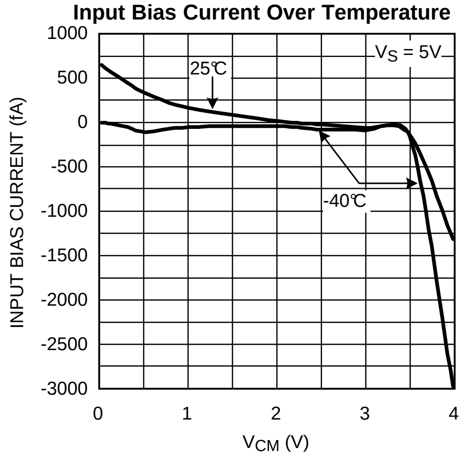


Figure 15.

Input Bias Current Over Temperature

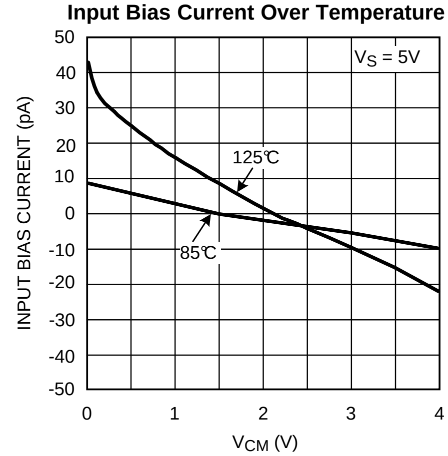


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

Supply Current vs. Supply Voltage (LMP7711)

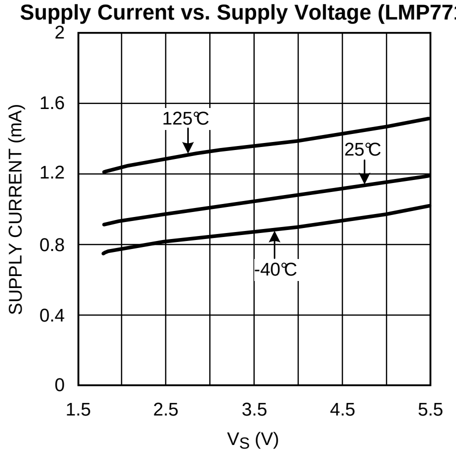


Figure 17.

Supply Current vs. Supply Voltage (LMP7712)

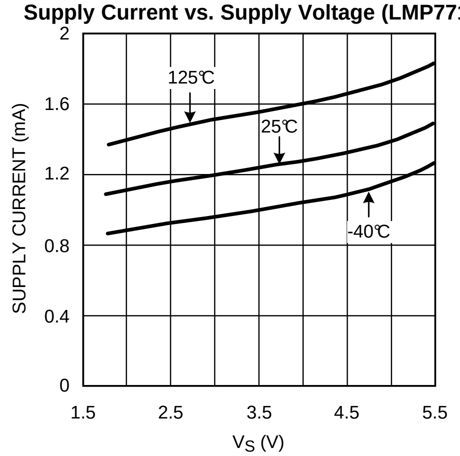


Figure 18.

Supply Current vs. Supply Voltage (Shutdown)

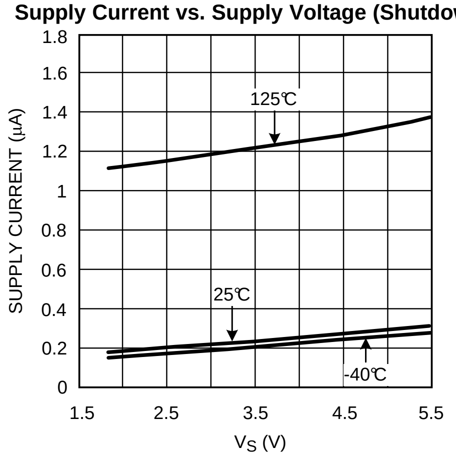


Figure 19.

Crosstalk Rejection Ratio (LMP7712)

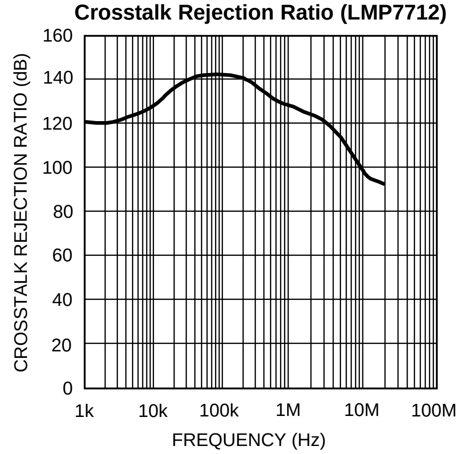


Figure 20.

Supply Current vs. Enable Pin Voltage (LMP7711)

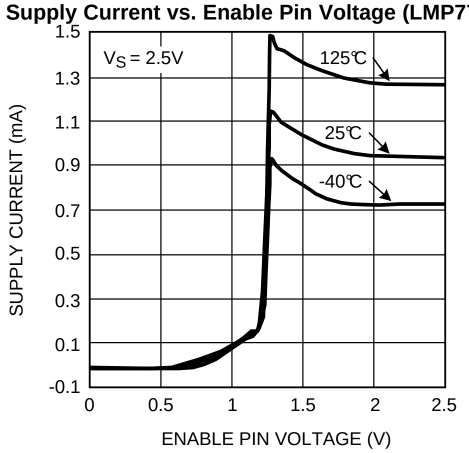


Figure 21.

Supply Current vs. Enable Pin Voltage (LMP7711)

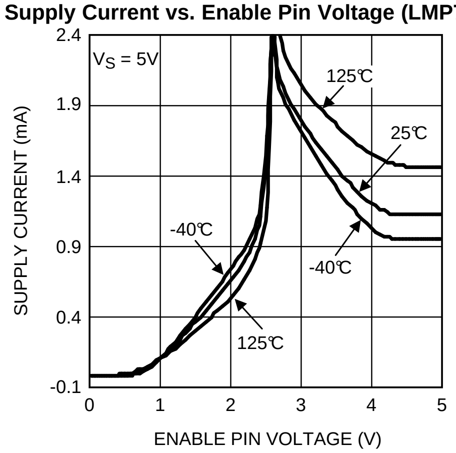


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: $T_A = 25°C$, $V_S = 5V$, $V_{CM} = V_S/2$, $V_{EN} = V^+$.

Supply Current vs. Enable Pin Voltage (LMP7712)

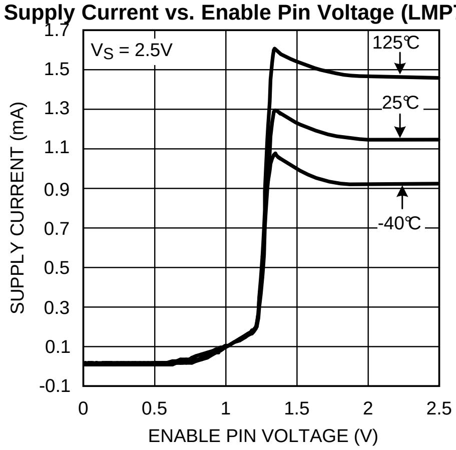


Figure 23.

Supply Current vs. Enable Pin Voltage (LMP7712)

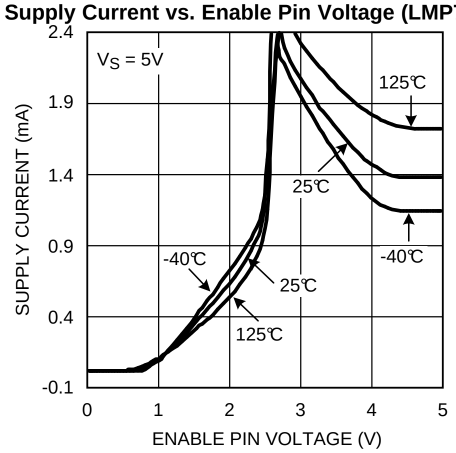


Figure 24.

Sourcing Current vs. Supply Voltage

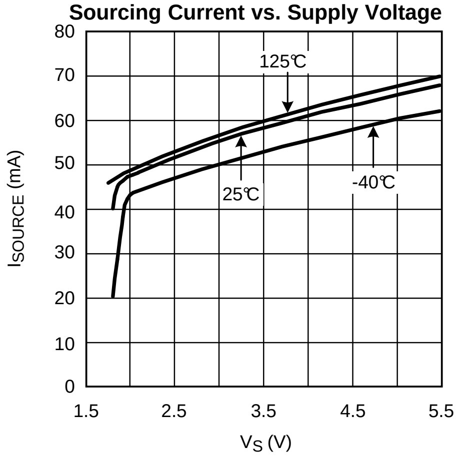


Figure 25.

Sinking Current vs. Supply Voltage

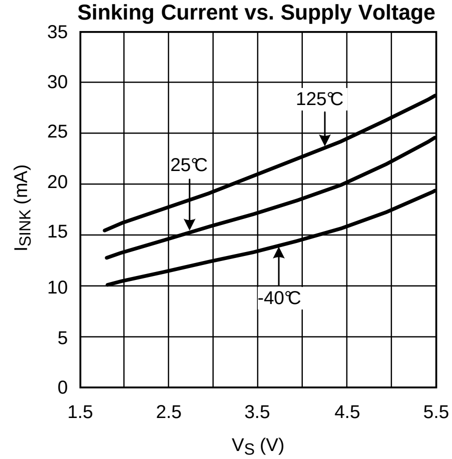


Figure 26.

Sourcing Current vs. Output Voltage

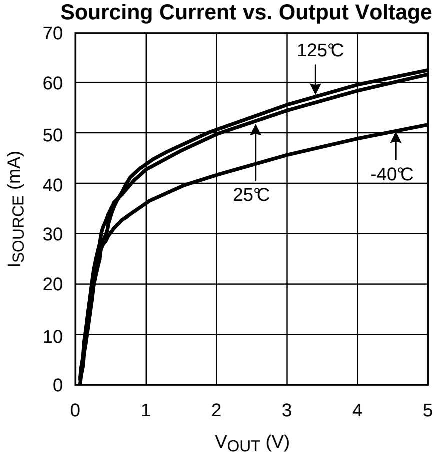


Figure 27.

Sinking Current vs. Output Voltage

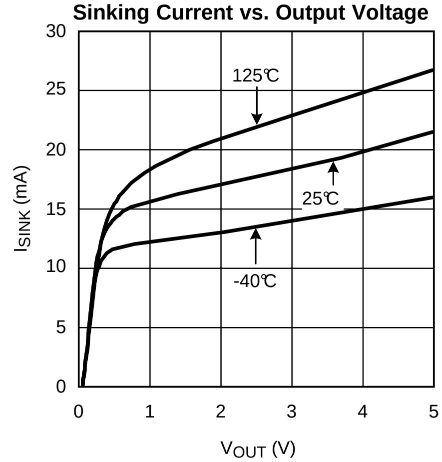


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

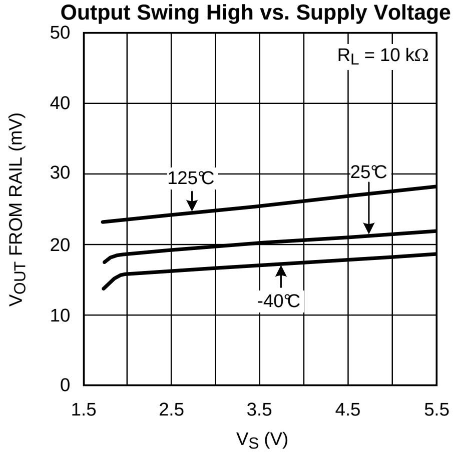


Figure 29.

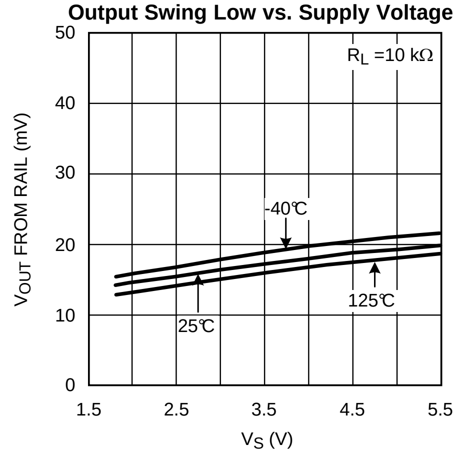


Figure 30.

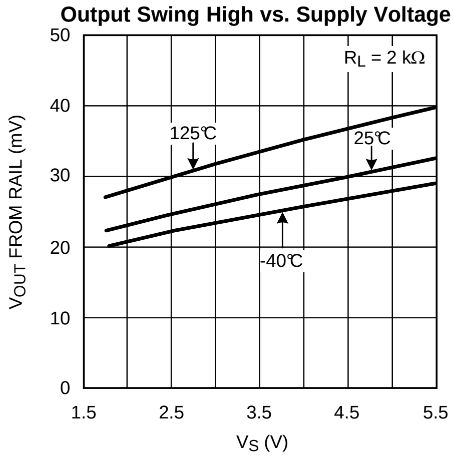


Figure 31.

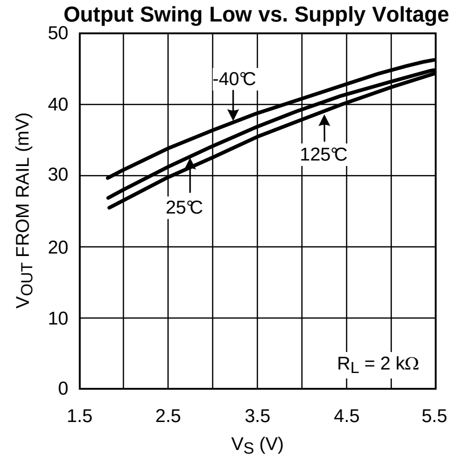


Figure 32.

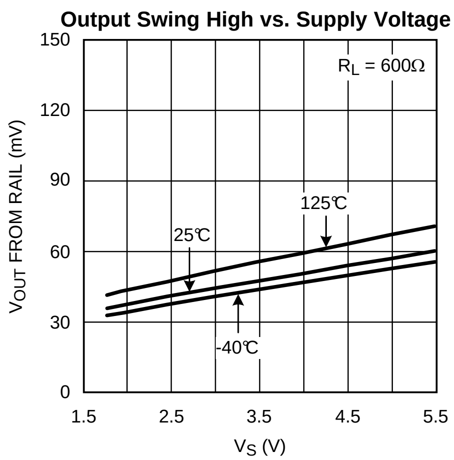


Figure 33.

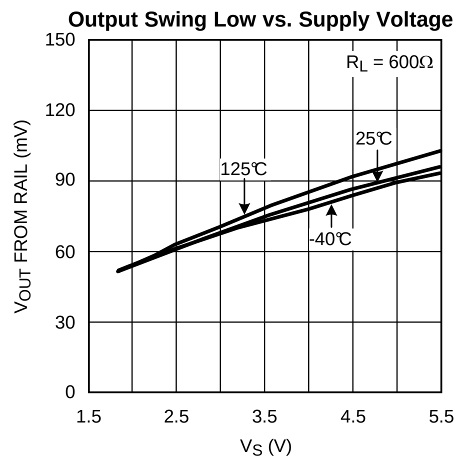


Figure 34.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

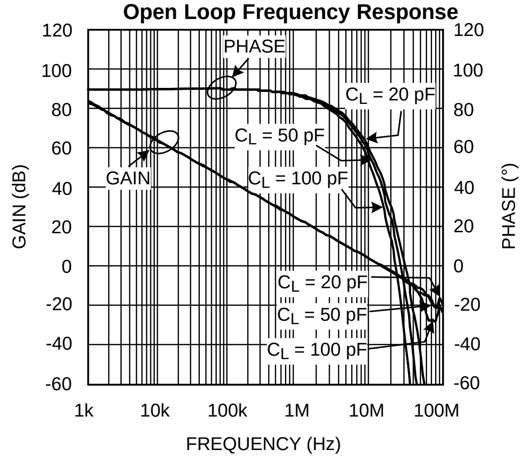


Figure 35.

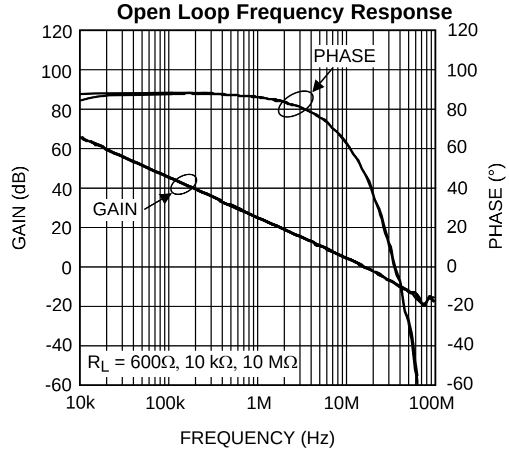


Figure 36.

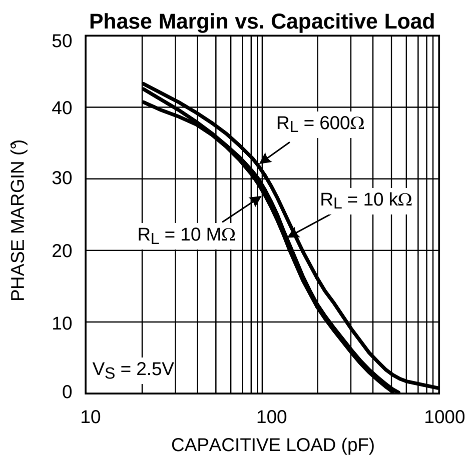


Figure 37.

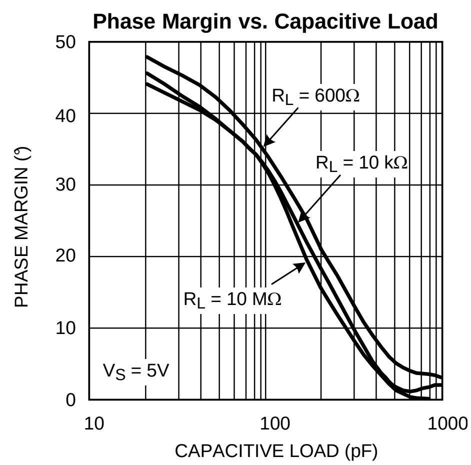


Figure 38.

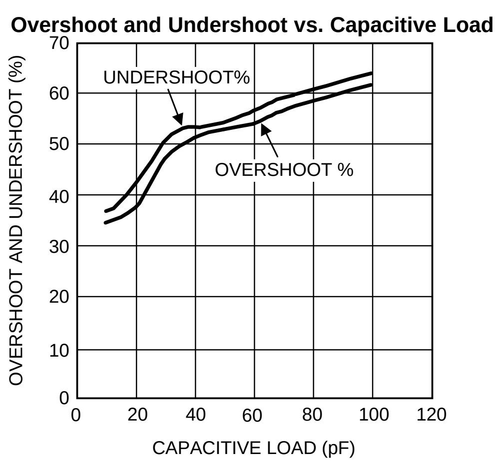


Figure 39.

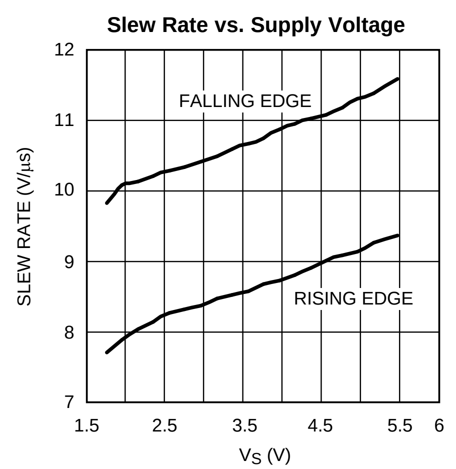


Figure 40.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

Small Signal Step Response

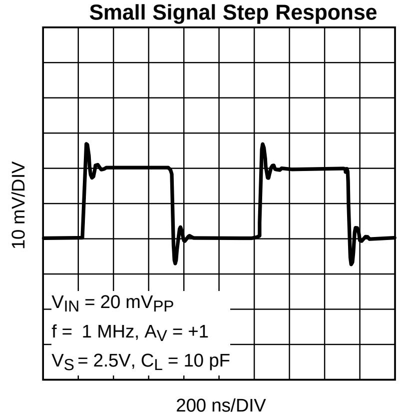


Figure 41.

Large Signal Step Response

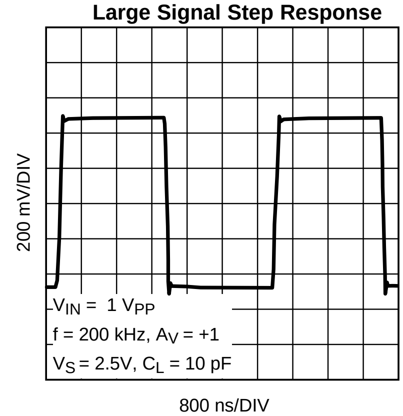


Figure 42.

Small Signal Step Response

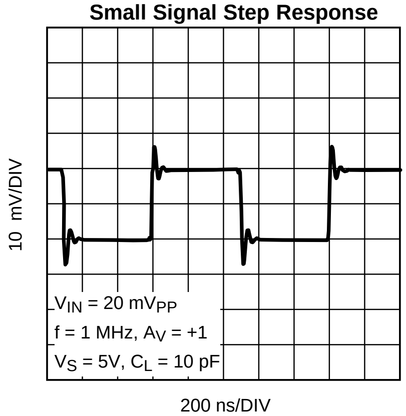


Figure 43.

Large Signal Step Response

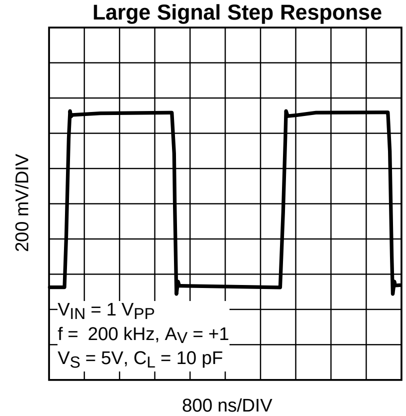


Figure 44.

THD+N vs. Output Voltage

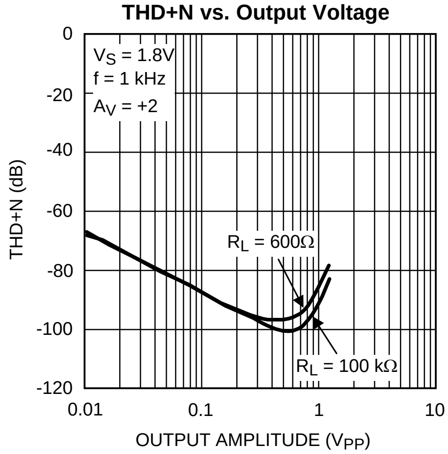


Figure 45.

THD+N vs. Output Voltage

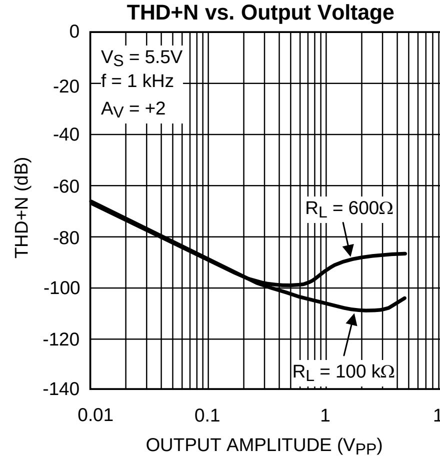


Figure 46.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

THD+N vs. Frequency

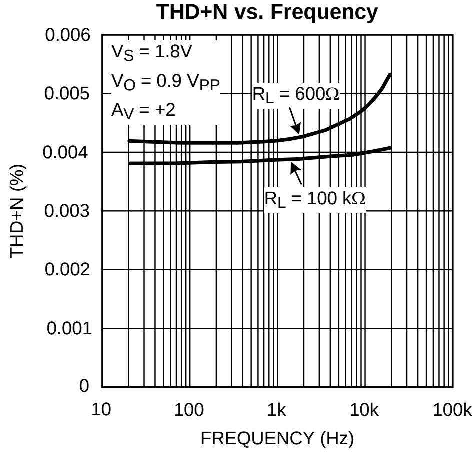


Figure 47.

THD+N vs. Frequency

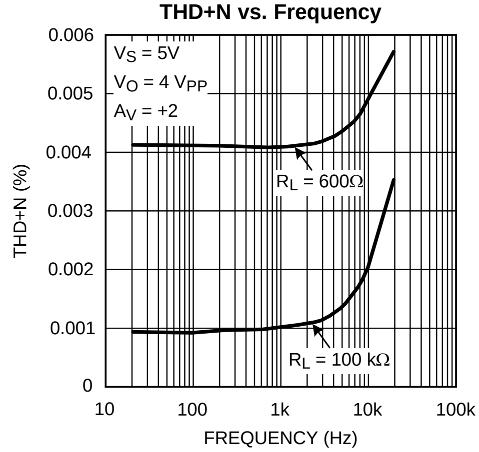


Figure 48.

PSRR vs. Frequency

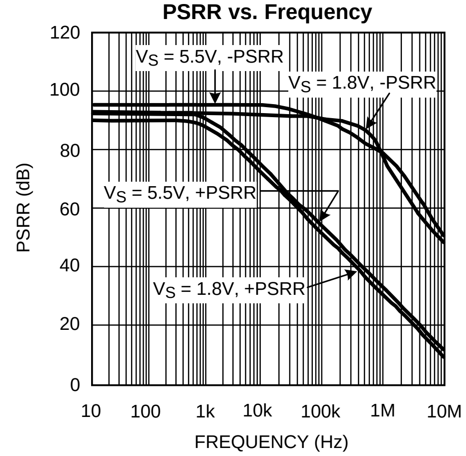


Figure 49.

Time Domain Voltage Noise

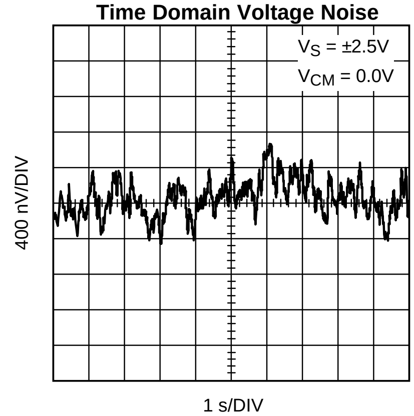


Figure 50.

Input Referred Voltage Noise vs. Frequency

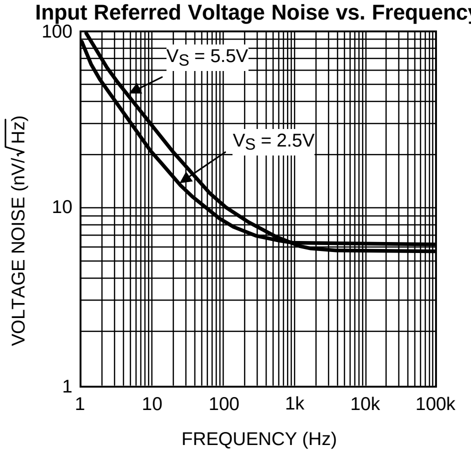


Figure 51.

Closed Loop Frequency Response

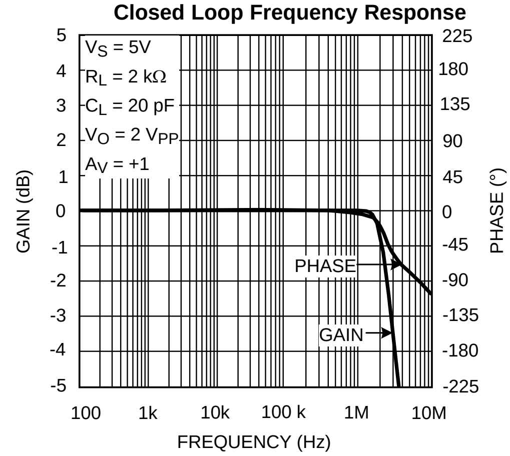


Figure 52.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2, V_{EN} = V^+.

Closed Loop Output Impedance vs. Frequency

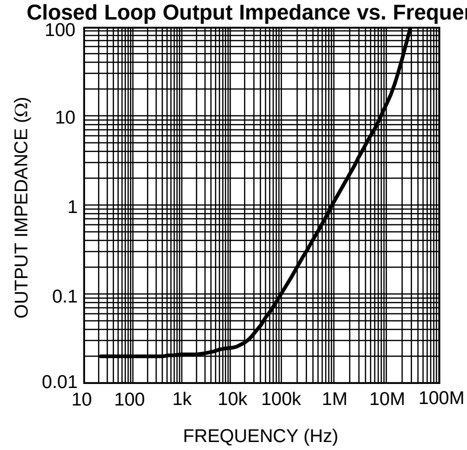


Figure 53.

APPLICATION NOTES

LMP7711/LMP7712

The LMP7711/LMP7712 are single and dual, low noise, low offset, rail-to-rail output precision amplifiers with a wide gain bandwidth product of 17 MHz and low supply current. The wide bandwidth makes the LMP7711/LMP7712 ideal choices for wide-band amplification in portable applications. The low supply current along with the enable feature that is built-in on the LMP7711/LMP7712 allows for even more power efficient designs by turning the device off when not in use.

The LMP7711/LMP7712 are superior for sensor applications. The very low input referred voltage noise of only 5.8 nV/$\sqrt{Hz}$ at 1 kHz and very low input referred current noise of only 10 fA/ $\sqrt{Hz}$ mean more signal fidelity and higher signal-to-noise ratio.

The LMP7711/LMP7712 have a supply voltage range of 1.8V to 5.5V over a wide temperature range of 0°C to 125°C. This is optimal for low voltage commercial applications. For applications where the ambient temperature might be less than 0°C, the LMP7711/LMP7712 are fully operational at supply voltages of 2.0V to 5.5V over the temperature range of −40°C to 125°C.

The outputs of the LMP7711/LMP7712 swing within 25 mV of either rail providing maximum dynamic range in applications requiring low supply voltage. The input common mode range of the LMP7711/LMP7712 extends to 300 mV below ground. This feature enables users to utilize this device in single supply applications.

The use of a very innovative feedback topology has enhanced the current drive capability of the LMP7711/LMP7712, resulting in sourcing currents as much as 47 mA with a supply voltage of only 1.8V.

The LMP7711 is offered in the space saving SOT package and the LMP7712 is offered in a 10-pin VSSOP. These small packages are ideal solutions for applications requiring minimum PC board footprint.

Texas Instruments is heavily committed to precision amplifiers and the market segments they serves. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

CAPACITIVE LOAD

The unity gain follower is the most sensitive configuration to capacitive loading. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will be either underdamped or the amplifier will oscillate.

The LMP7711/LMP7712 can directly drive capacitive loads of up to 120 pF without oscillating. To drive heavier capacitive loads, an isolation resistor, R_{ISO} in Figure 54, should be used. This resistor and C_L form a pole and hence delay the phase lag or increase the phase margin of the overall system. The larger the value of R_{ISO}, the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

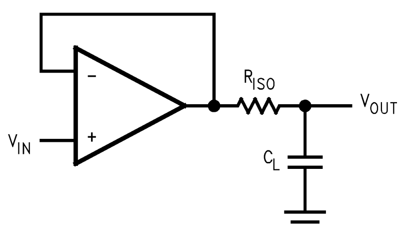


Figure 54. Isolating Capacitive Load

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7711/LMP7712 enhance this performance by having the low input bias current of only 50 fA, as well as, a very low input referred voltage noise of 5.8 nV/$\sqrt{Hz}$. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7711/LMP7712. Figure 55 shows typical input common mode input capacitance of the LMP7711/LMP7712.

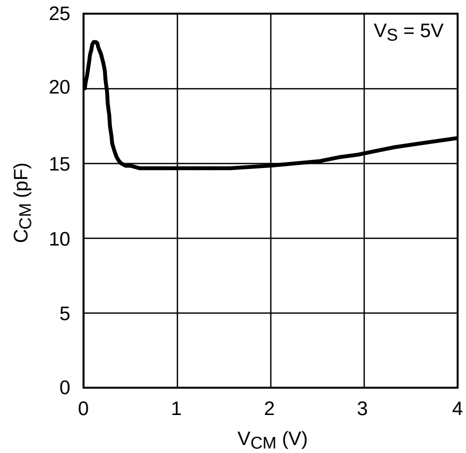
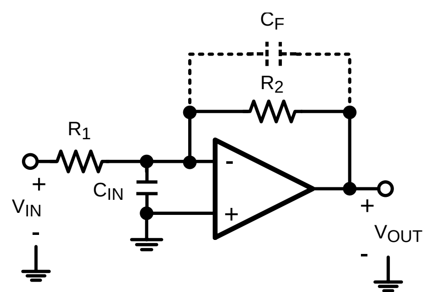


Figure 55. Input Common Mode Capacitance

This input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and under DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and also causes gain peaking. In order to compensate for the input capacitance, care must be taken in choosing feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 56 is simply $-R_2/R_1$.



$$A_V = -\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

Figure 56. Compensating for Input Capacitance

For the time being, ignore C_F. The AC gain of the circuit in Figure 56 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \quad (1)$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4 A_0 C_{IN}}{R_2}}\right] \quad (2)$$

As shown in Equation 2, as the values of R_1 and R_2 are increased, the magnitude of the poles are reduced, which in turn decreases the bandwidth of the amplifier. Figure 57 shows the frequency response with different value resistors for R_1 and R_2. Whenever possible, it is best to chose smaller feedback resistors.

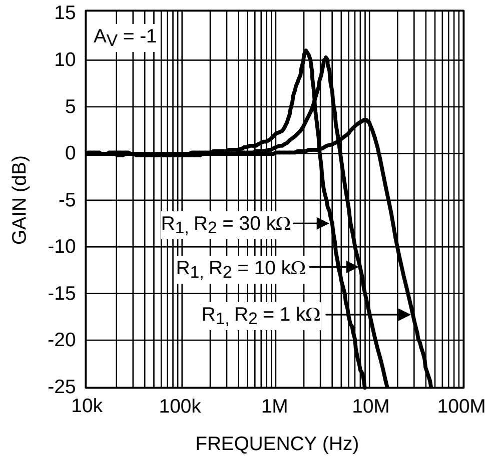


Figure 57. Closed Loop Frequency Response

As mentioned before, adding a capacitor to the feedback path will decrease the peaking. This is because C_F will form yet another pole in the system and will prevent pairs of poles, or complex conjugates from forming. It is the presence of pairs of poles that cause the peaking of gain. Figure 58 shows the frequency response of the schematic presented in Figure 56 with different values of C_F. As can be seen, using a small value capacitor significantly reduces or eliminates the peaking.

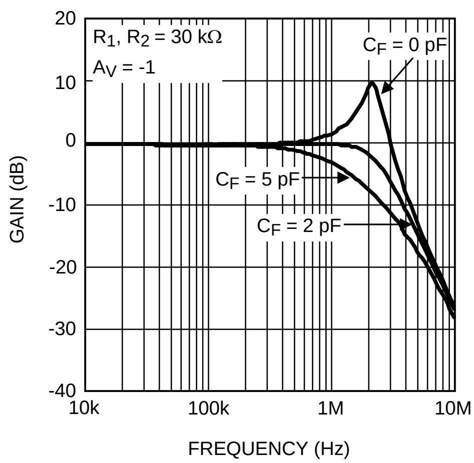


Figure 58. Closed Loop Frequency Response

TRANSIMPEDANCE AMPLIFIER

In many applications, the signal of interest is a very small amount of current that needs to be detected. Current that is transmitted through a photodiode is a good example. Barcode scanners, light meters, fiber optic receivers, and industrial sensors are some typical applications utilizing photodiodes for current detection. This current needs to be amplified before it can be further processed. This amplification is performed using a current-to-voltage converter configuration or transimpedance amplifier. The signal of interest is fed to the inverting input of an op amp with a feedback resistor in the current path. The voltage at the output of this amplifier will be equal to the negative of the input current times the value of the feedback resistor. Figure 59 shows a transimpedance amplifier configuration. C_D represents the photodiode parasitic capacitance and C_{CM} denotes the common-mode capacitance of the amplifier. The presence of all of these capacitances at higher frequencies might lead to less stable topologies at higher frequencies. Care must be taken when designing a transimpedance amplifier to prevent the circuit from oscillating.

With a wide gain bandwidth product, low input bias current and low input voltage and current noise, the LMP7711/LMP7712 are ideal for wideband transimpedance applications.

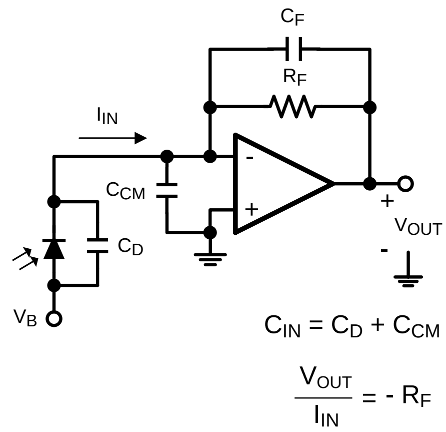


Figure 59. Transimpedance Amplifier

A feedback capacitance C_F is usually added in parallel with R_F to maintain circuit stability and to control the frequency response. To achieve a maximally flat, 2nd order response, R_F and C_F should be chosen by using Equation 3

$$C_F = \sqrt{\frac{C_{IN}}{GBWP * 2 \pi R_F}} \quad (3)$$

Calculating C_F from Equation 3 can sometimes result in capacitor values which are less than 2 pF. This is especially the case for high speed applications. In these instances, its often more practical to use the circuit shown in Figure 60 in order to allow more sensible choices for C_F. The new feedback capacitor, C'_F, is (1+ R_B/R_A) C_F. This relationship holds as long as $R_A << R_F$.

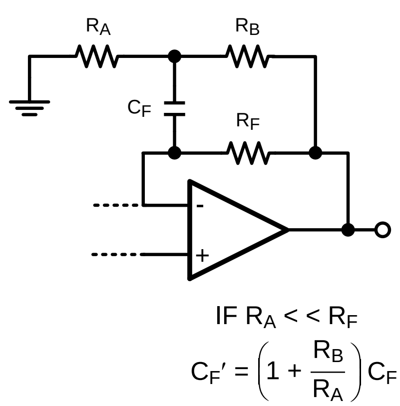


Figure 60. Modified Transimpedance Amplifier

SENSOR INTERFACE

The LMP7711/LMP7712 have low input bias current and low input referred noise, which make them ideal choices for sensor interfaces such as thermopiles, Infra Red (IR) thermometry, thermocouple amplifiers, and pH electrode buffers.

Thermopiles generate voltage in response to receiving radiation. These voltages are often only a few microvolts. As a result, the operational amplifier used for this application needs to have low offset voltage, low input voltage noise, and low input bias current. Figure 61 shows a thermopile application where the sensor detects radiation from a distance and generates a voltage that is proportional to the intensity of the radiation. The two resistors, R_A and R_B, are selected to provide high gain to amplify this signal, while C_F removes the high frequency noise.

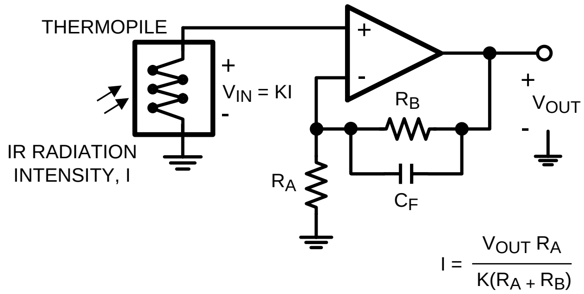


Figure 61. Thermopile Sensor Interface

PRECISION RECTIFIER

Rectifiers are electrical circuits used for converting AC signals to DC signals. Figure 62 shows a full-wave precision rectifier. Each operational amplifier used in this circuit has a diode on its output. This means for the diodes to conduct, the output of the amplifier needs to be positive with respect to ground. If V_{IN} is in its positive half cycle then only the output of the bottom amplifier will be positive. As a result, the diode on the output of the bottom amplifier will conduct and the signal will show at the output of the circuit. If V_{IN} is in its negative half cycle then the output of the top amplifier will be positive, resulting in the diode on the output of the top amplifier conducting and, delivering the signal on the amplifier's output to the circuits output.

For $R_2/ R_1 \geq 2$, the resistor values can be found by using the equation shown in Figure 62. If $R_2/ R_1 = 1$, then R_3 should be left open, no resistor needed, and R_4 should simply be shorted.

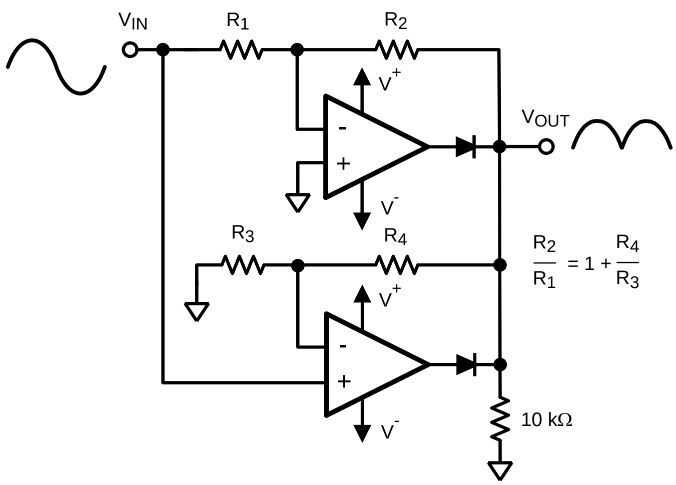


Figure 62. Precision Rectifier

REVISION HISTORY

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP7711MK/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC3A
LMP7711MK/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC3A
LMP7711MKE/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC3A
LMP7711MKE/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC3A
LMP7711MKX/NOPB	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC3A
LMP7711MKX/NOPB.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC3A
LMP7712MM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD3A
LMP7712MM/NOPB.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD3A
LMP7712MME/NOPB	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD3A
LMP7712MME/NOPB.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD3A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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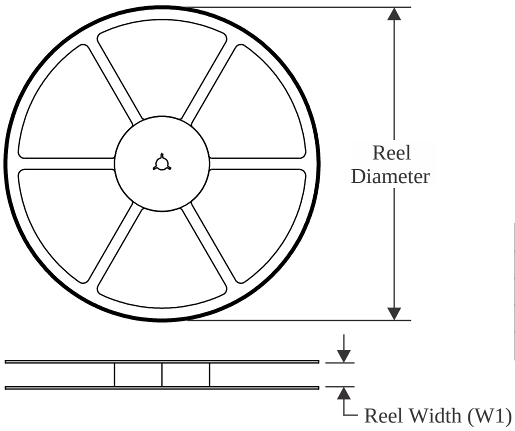
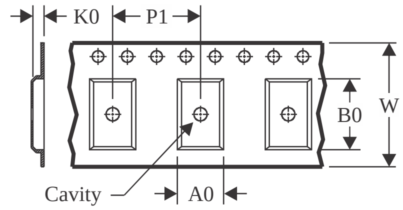
TAPE AND REEL INFORMATION

REEL DIMENSIONS

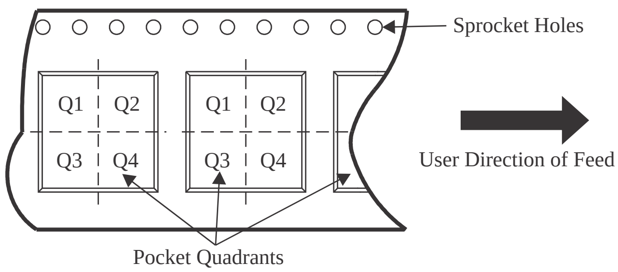


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

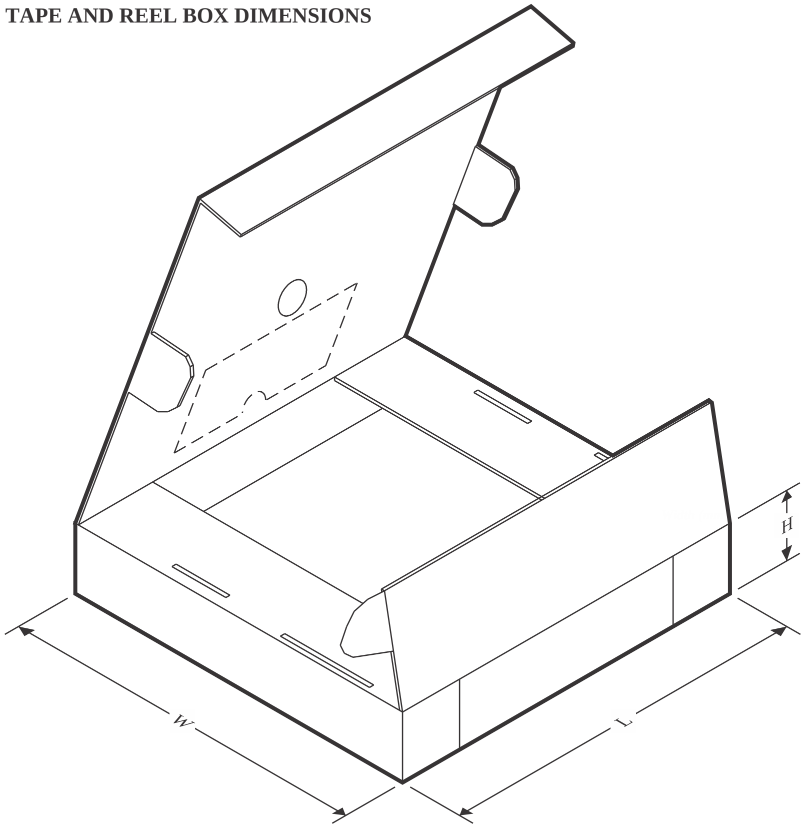
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7711MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7712MM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7712MME/NOPB	VSSOP	DGS	10	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7711MK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LMP7711MKE/NOPB	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMP7711MKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMP7712MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LMP7712MME/NOPB	VSSOP	DGS	10	250	208.0	191.0	35.0