LMK1C110x-Q1 1.8V, 2.5V, and 3.3V Low Noise LVCMOS Clock Buffer Family

ADVANCE INFORMATION

1 Features

- High-performance 1:2, 1:4, 1:6 and 1:8 LVCMOS clock buffer
- Very low output skew:
  - LMK1C1102-Q1 and LMK1C1104-Q1
    - < 50ps
  - LMK1C1106-Q1 and LMK1C1108-Q1
    - < 55ps
- Extremely low additive jitter:
  - LMK1C1102-Q1 and LMK1C1104-Q1
    - 7.5fs typical at V_{DD} = 3.3V
    - 10fs typical at V_{DD} = 2.5V
    - 19.2fs typical at V_{DD} = 1.8V
  - LMK1C1106-Q1 and LMK1C1108-Q1
    - 12fs typical at V_{DD} = 3.3V
    - 15fs typical at V_{DD} = 2.5V
    - 28fs typical at V_{DD} = 1.8V
- Very low propagation delay < 3ns
- Synchronous output enable
- Supply voltage: 3.3V, 2.5V, or 1.8V
  - 3.3V tolerant input at all supply voltages
  - Fail-safe inputs
- f_{max} = 250MHz for 3.3V
  f_{max} = 200MHz for 2.5V and 1.8V
- Automotive Grade 1 (–40°C to 125°C)
- AEC-Q100 qualified
- Available in:
  - 14 and 16-Pin TSSOP Package
  - 8-Pin WSON Package

2 Applications

- Automotive
  - ADAS
  - Infotainment & Cluster
  - Radar

3 Description

The LMK1C110x-Q1 is a modular, high-performance, low-skew, general-purpose clock buffer family from Texas Instruments. The entire family is designed with a modular approach in mind. Five different fan-out variations, 1:2, 1:4, 1:6 and 1:8 are available.

All family members share the same high performing characteristics such as low additive jitter, low skew, and wide operating temperature range.

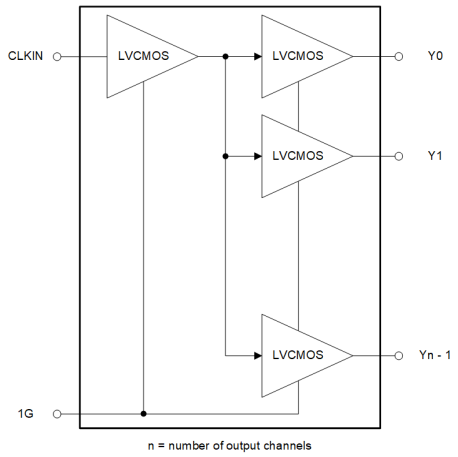
The LMK1C110x-Q1 supports a synchronous output enable control (1G) which switches the outputs into a low state when 1G is low. These devices have a fail-safe input that prevents oscillation at the outputs in the absence of an input signal and allows for input signals before VDD is supplied.

The LMK1C110x-Q1 family are available in an Automotive Grade 1 (–40°C to 125°C) and AEC-Q100 qualified.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMK1C1106-Q1	PW (TSSOP, 14)	5.00mm × 4.40mm
LMK1C1108-Q1	PW (TSSOP, 16)	
LMK1C1102-Q1	DQF (WSON, 8)	2.00mm × 2.00mm
LMK1C1104-Q1		

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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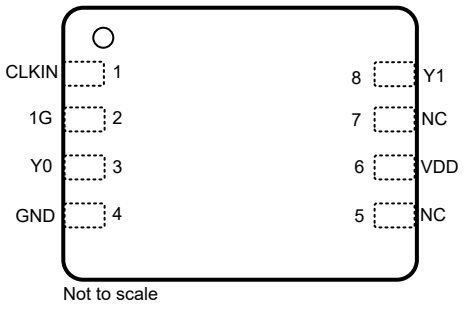
4 Device Comparison

Table 4-1. Device Comparison

DEVICE	Input	Output	Output Enable Option (1G)	PACKAGE
LMK1C1102	1	2	Synchronous	WSON (8), 2.00mm × 2.00mm
LMK1C1104	1	4	Synchronous	WSON (8), 2.00mm × 2.00mm
LMK1C1102	1	2	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1103	1	3	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1104	1	4	Synchronous	TSSOP (8), 3.00mm × 4.40mm
LMK1C1106	1	6	Synchronous	TSSOP (14), 5.00mm × 4.40mm
LMK1C1108	1	8	Synchronous	TSSOP (16), 5.00mm × 4.40mm
LMK1C1102-Q1 (1)	1	2	Synchronous	WSON (8), 2.00mm × 2.00mm
LMK1C1104-Q1 (1)	1	4	Synchronous	WSON (8), 2.00mm × 2.00mm
LMK1C1106-Q1	1	6	Synchronous	TSSOP (14), 5.00mm × 4.40mm
LMK1C1108-Q1	1	8	Synchronous	TSSOP (16), 5.00mm × 4.40mm

(1) Preview Only. Contact TI for more information on the device.

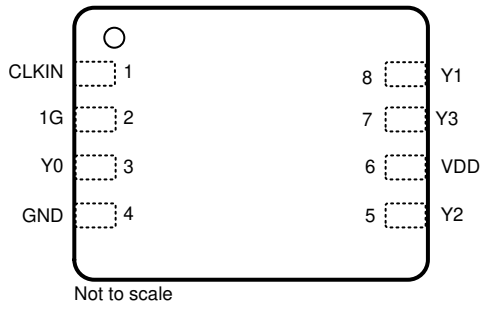
5 Pin Configuration and Functions



Not to scale

1. The DQF (WSON) package is equivalent to the DFN package of other vendors.

Figure 5-1. LMK1C1102-Q1, 8-Pin DQF WSON Package (Top View)



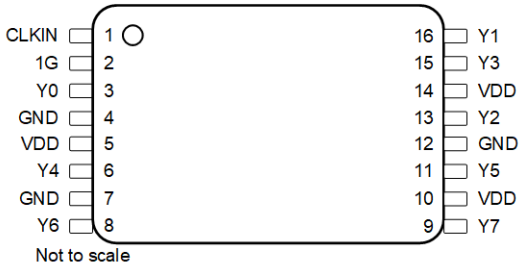
Not to scale

1. The DQF (WSON) package is equivalent to the DFN package of other vendors.

Figure 5-2. LMK1C1104-Q1, 8-Pin DQF WSON Package (Top View)

Not to scale

Figure 5-3. LMK1C1106-Q1, 14-Pin PW TSSOP Package (Top View)



Not to scale

Figure 5-4. LMK1C1108-Q1, 16-Pin PW TSSOP Package (Top View)

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
LMK1C 1102-Q1	LMK1C 1104-Q1	LMK1C 1106-Q1	LMK1C 1108-Q1		
LVCMOS CLOCK INPUT					
1	1	1	1	Input	Single-ended clock input with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
CLOCK OUTPUT ENABLE					
2	2	2	2	Input	Global Output Enable with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
LVCMOS CLOCK OUTPUT					
3	3	3	3	Output	LVCMOS output. Typically connected to a receiver. Unused outputs can be left floating.
8	8	14	16		
—	5	11	13		
—	7	13	15		
—	—	6	6		
—	—	9	11		
—	—	—	8		
—	—	—	9		
SUPPLY VOLTAGE					
6	6	5	5	Power	Power supply terminal. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-µF capacitor near the pin.
		8	10		
		12	14		
GROUND					
4	4	4	4	GND	Power supply ground.
		7	7		
		10	12		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	3.6	V
V_{CLKIN}	Input voltage (CLKIN)			
V_{IN}	Input voltage (1G)			
V_{Yn}	Output pins (Yn)	–0.5	V_{DD} + 0.3	
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±9000	V
V(ESD)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-0111	±1500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMK1C1102-Q1, LMK1C1104-Q1	LMK1C1106-Q1	LMK1C1108-Q1	UNIT
		DQF(WSON)	PW (TSSOP)	PW(TSSOP)	
		8 PINS	14 PINS	16 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	163	114.4	123.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	105.7	45.2	53.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	84.2	60.6	66.4	°C/W
Y_{JT}	Junction-to-top characterization parameter	16.7	5.9	8.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	83.9	60	65.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Electrical Characteristics

VDD = 3.3V ± 5%, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{DD}	Core supply current, static	All-outputs disabled, f_{IN} = 0V		25	45	µA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100MHz, V_{DD} = 1.8V		2	6	mA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100MHz, V_{DD} = 2.5V		6.5	10	mA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100MHz, V_{DD} = 3.3V		15	21	mA
I_{DD}	Output current	Per output, f_{IN} = 100MHz, C_L = 5pF, V_{DD} = 1.8V		3.2	3.5	
		Per output, f_{IN} = 100MHz, C_L = 5pF, V_{DD} = 2.5V		4.6	5.5	
		Per output, f_{IN} = 100MHz, C_L = 5pF, V_{DD} = 3.3V		6	7	
CLOCK INPUT						
f_{IN_SE}	Input frequency	V_{DD} = 3.3V	DC		250	MHz
		V_{DD} = 2.5V and 1.8V	DC		200	
V_{IH}	Input high voltage		0.7x V_{DD}			V
V_{IL}	Input low voltage				0.3x V_{DD}	
dV_{IN}/dt	Input slew rate	20% - 80% of input swing	0.1			V/ns
I_{IN_LEAK}	Input leakage current		–50		50	µA
C_{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V_{DD} LEVELS						
f_{OUT}	Output frequency	V_{DD} = 3.3V			250	MHz
		V_{DD} = 2.5V and 1.8V			200	
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_{1G_ON}	Output enable time	See (1)			5	cycles
t_{1G_OFF}	Output disable time	See (2)			5	cycles
CLOCK OUTPUT FOR V_{DD} = 3.3V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1mA	2.8			V
V_{OL}	Output low voltage	I_{OL} = 1mA			0.2	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5pF, fIN = 156.25MHz		0.3	0.7	ns
$t_{OUTPUT-SKEW}$	Output-output skew	LMK1C1102-Q1, LMK1C1104-Q1. See (3)		25	50	ps
$t_{OUTPUT-SKEW}$	Output-output skew	LMK1C1106-Q1, LMK1C1108-Q1. See (3)		25	50	ps
$t_{PART-SKEW}$	Part-to-part skew	LMK1C1102-Q1, LMK1C1104-Q1			250	ps
$t_{PART-SKEW}$	Part-to-part skew	LMK1C1106-Q1, LMK1C1108-Q1			280	ps
$t_{PROP-DELAY}$	Propagation delay	LMK1C1102-Q1, LMK1C1104-Q1. See (4)		1.5	2	ns
$t_{PROP-DELAY}$	Propagation delay	LMK1C1106-Q1, LMK1C1108-Q1. See (4)		1.5	2.2	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25MHz, Input slew rate = 1.6V/ns, Integration range = 12kHz - 20MHz		12	20	fs, RMS
R_{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V_{DD} = 2.5V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1mA	0.8x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1mA			0.2x V_{DD}	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5pF, f_{IN} = 156.25MHz		0.33	0.8	ns

VDD = 3.3V ± 5%, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OUTPUT-SKEW}$	Output-output skew	LMK1C1102-Q1, LMK1C1104-Q1. See (3)			50	ps
$t_{OUTPUT-SKEW}$	Output-output skew	LMK1C1106-Q1, LMK1C1108-Q1. See (3)			55	ps
$t_{PART-SKEW}$	Part-to-part skew	LMK1C1102-Q1, LMK1C1104-Q1			400	ps
$t_{PART-SKEW}$	Part-to-part skew	LMK1C1106-Q1, LMK1C1108-Q1			450	ps
$t_{PROP-DELAY}$	Propagation delay	LMK1C1102-Q1, LMK1C1104-Q1. See (4)		1.5	2.5	ns
$t_{PROP-DELAY}$	Propagation delay	LMK1C1106-Q1, LMK1C1108-Q1. See (4)		1.5	2.5	
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25MHz, Input slew rate = 1.2V/ns, Integration range = 12kHz - 20MHz		15	27	fs, RMS
R_{OUT}	Output impedance			55		Ω
CLOCK OUTPUT FOR V_{DD} = 1.8V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1mA	0.8x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1mA			0.2x V_{DD}	
$t_{RISE-FALL}$	Output rise and fall time	20/80%, C_L= 5pF, f_{IN} = 156.25MHz		0.38	1	ns
$t_{OUTPUT-SKEW}$	Output-output skew	LMK1C1102-Q1, LMK1C1104-Q1. See (3)			50	ps
$t_{OUTPUT-SKEW}$	Output-output skew	LMK1C1106-Q1, LMK1C1108-Q1. See (3)			55	ps
$t_{PART-SKEW}$	Part-to-part skew	LMK1C1102-Q1, LMK1C1104-Q1			900	ps
$t_{PART-SKEW}$	Part-to-part skew	LMK1C1106-Q1, LMK1C1108-Q1			930	ps
$t_{PROP-DELAY}$	Propagation delay	LMK1C1102-Q1, LMK1C1104-Q1. See (4)		1.5	3	ns
$t_{PROP-DELAY}$	Propagation delay	LMK1C1106-Q1, LMK1C1108-Q1. See (4)		1.5	3	ns
$t_{JITTER-ADD}$	Additive Jitter	f_{IN} = 156.25MHz, Input slew rate = 1.2V/ns, Integration range = 12kHz - 20MHz		28	60	fs, RMS
R_{OUT}	Output impedance			64		Ω
GENERAL PURPOSE INPUT (1G)						
V_{IH}	High-level input voltage		0.75x V_{DD}			V
V_{IL}	Low-level input voltage	LMK1C1102-Q1, LMK1C1104-Q1			0.38x V_{DD}	V
V_{IL}	Low-level input voltage	LMK1C1106-Q1, LMK1C1108-Q1			0.25x V_{DD}	V
I_{IH}	Input high-level current	V_{IH} = V_{DD_REF}	–50		50	µA
I_{IL}	Input low-level current	V_{IL} = GND	–50		50	

(1) Measured from 1G rising edge crossing VIH to first rising edge of Yn.
(2) Measured from 1G falling edge crossing VIL to last falling edge of Yn.
(3) Measured from rising edge of any Yn output to any other Ym output.
(4) Measured from rising edge of CLKIN to any Yn output.

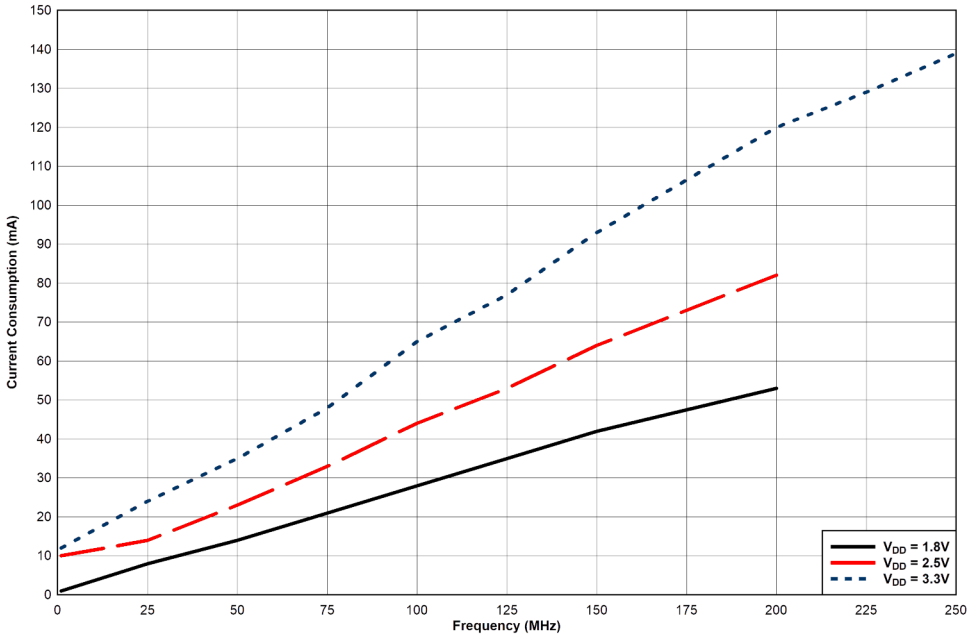
6.6 Timing Requirements

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V/t_{RAMP}	V_{DD} ramp rate		0.1		50	V/ms

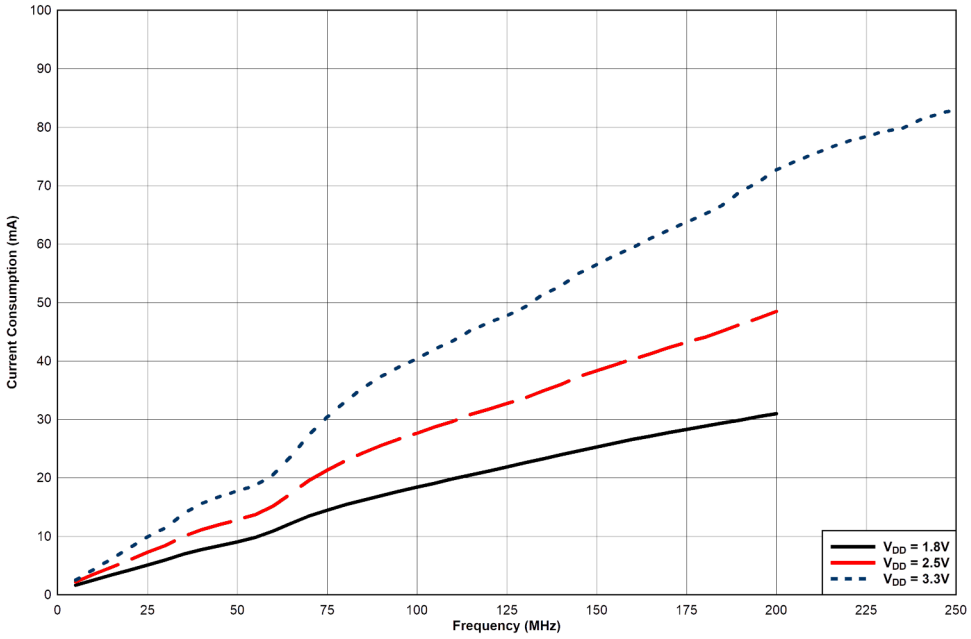
ADVANCE INFORMATION

6.7 Typical Characteristics



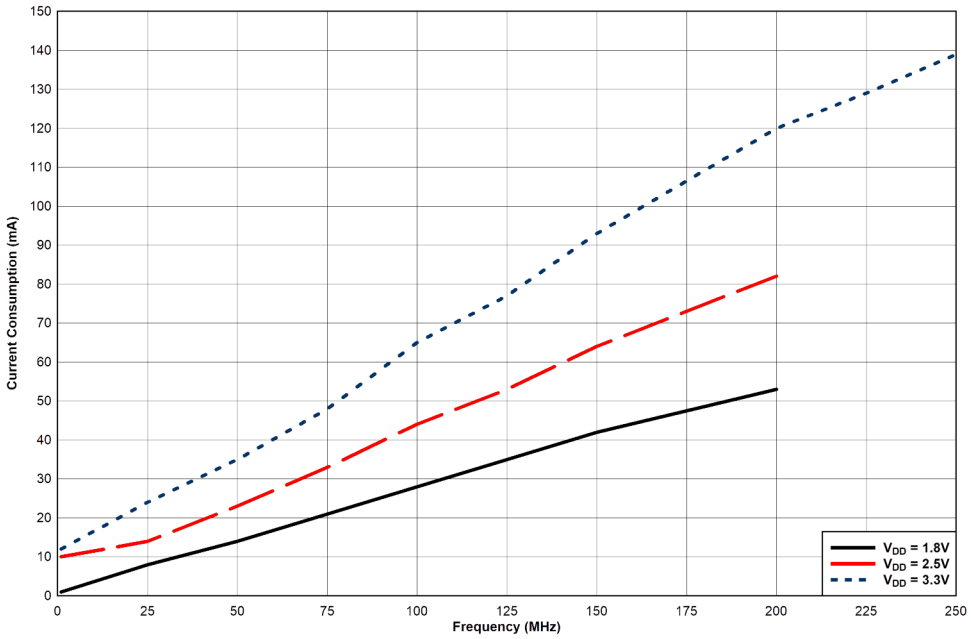
1. All outputs enabled.

LMK1C1106-Q1 and LMK1C1108-Q1 Device Power Consumption vs. Clock Frequency (Load 5 pF)



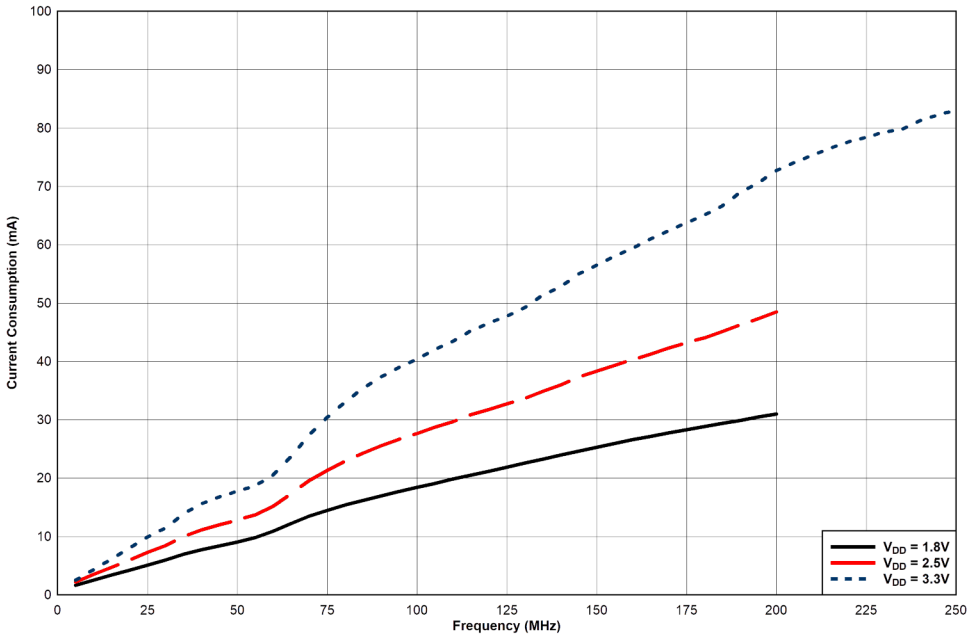
1. All outputs enabled.

Figure 6-1. LMK1C1102-Q1 and LMK1C1104-Q1 Device Power Consumption vs. Clock Frequency (Load 5 pF)



1. All outputs enabled.

LMK1C1106-Q1 and LMK1C1108-Q1 Device Power Consumption vs. Clock Frequency (Load 5 pF)



1. All outputs enabled.

Figure 6-2. LMK1C1102-Q1 and LMK1C1104-Q1 Device Power Consumption vs. Clock Frequency (Load 5 pF)

ADVANCE INFORMATION

7 Parameter Measurement Information

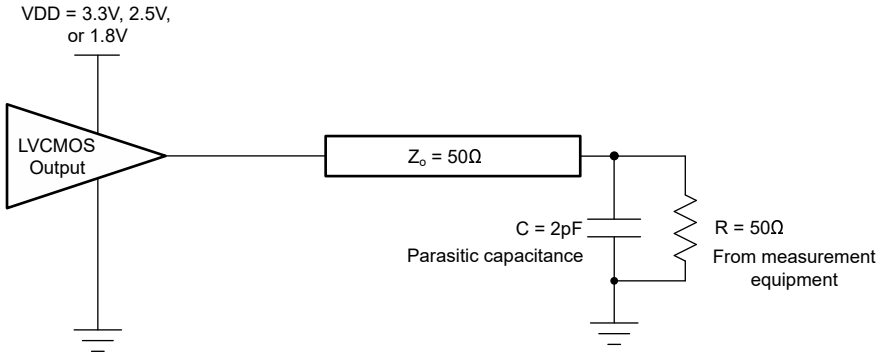


Figure 7-1. Test Load Circuit

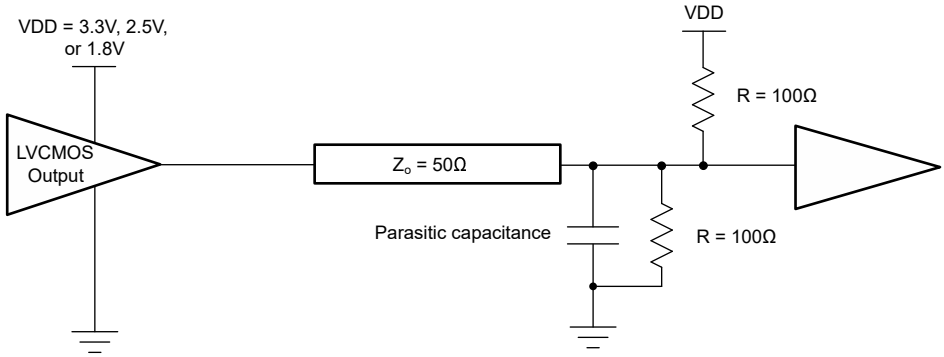


Figure 7-2. Application Load With 50-Ω Termination

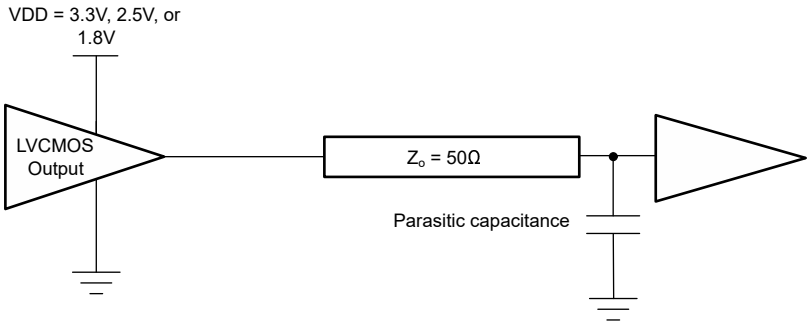


Figure 7-3. Application Load With Termination

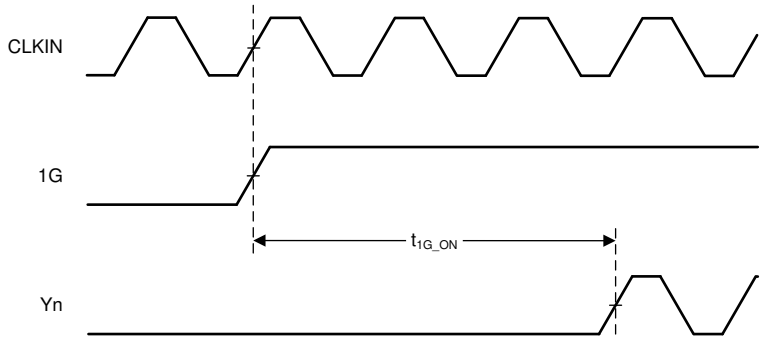


Figure 7-4. t_{1G_ON} Output Enable Time

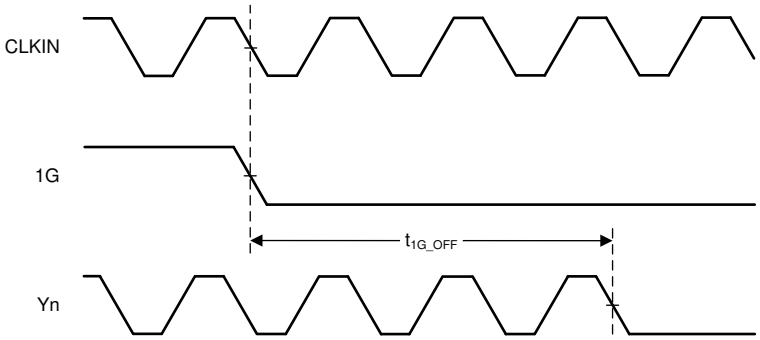


Figure 7-5. t_{1G_OFF} Output Disable Time

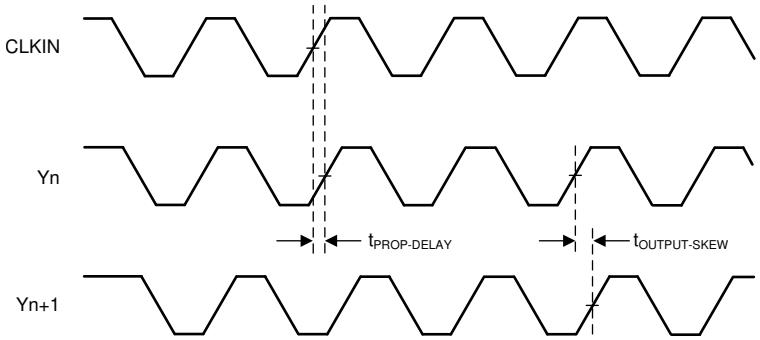


Figure 7-6. Propagation Delay $t_{PROP-DELAY}$ and Output Skew $t_{OUTPUT-SKEW}$

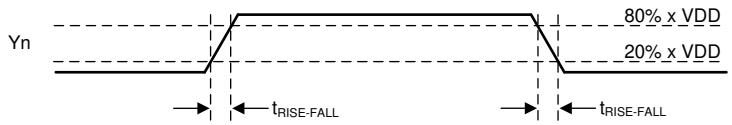


Figure 7-7. Rise and Fall Time $t_{RISE-FALL}$

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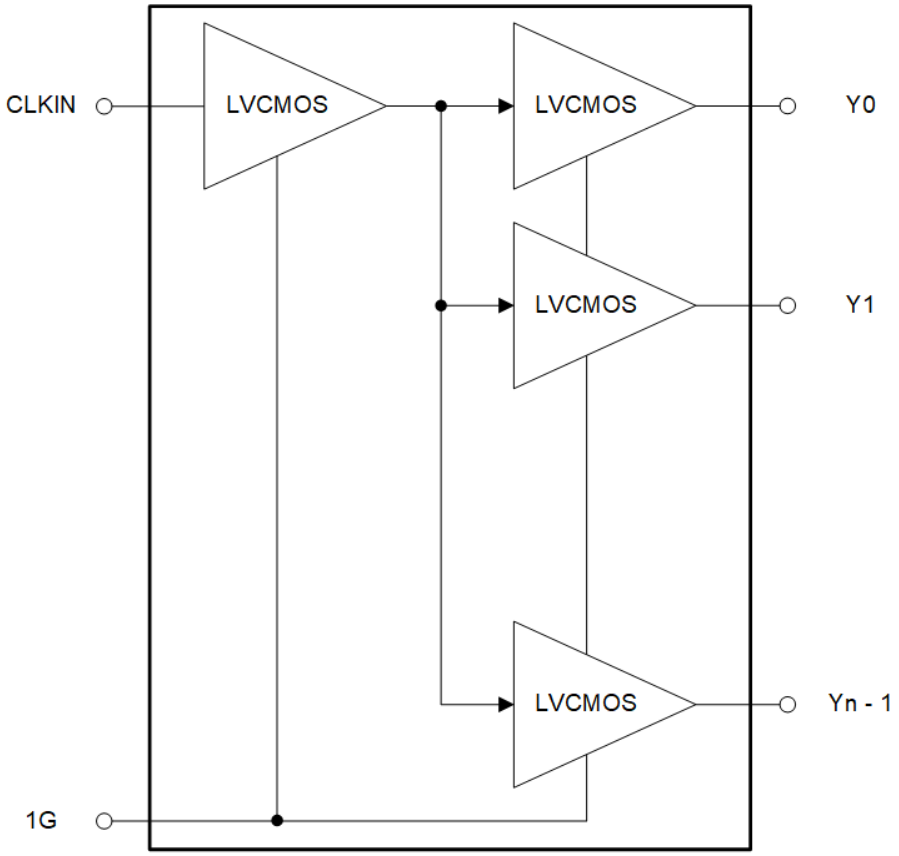
8 Detailed Description

8.1 Overview

The LMK1C110x-Q1 family of devices is part of a low-jitter and low-skew LVCMOS fan-out buffer solution. Matching the characteristic impedance of the LMK1C110x-Q1 output driver with the characteristic impedance of the transmission driver is important for the best signal integrity.

8.2 Functional Block Diagram



n = number of output channels

8.3 Feature Description

The outputs of the LMK1C110x-Q1 can be disabled by driving the synchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. Supply and ground pins must be connected to V_{DD} and GND, respectively.

8.3.1 Fail-Safe Inputs

The LMK1C110x-Q1 family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to *Absolute Maximum Ratings* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis that prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

8.3.2 Synchronous Output Enable

Synchronous output enable makes sure that all the output clocks are synchronized before the output is enabled. For high speed clock inputs, adding delays for glitches due to asynchronous output enable is difficult. Synchronous output enable provides glitchless output enable by synchronizing the outputs with clock input. See Section 4 for available output enable options from TI.

8.4 Device Functional Modes

The LMK1C110x-Q1 operates from 1.8V, 2.5V, or 3.3V supplies. Table 8-1shows the output logics of the LMK1C110x-Q1. Synchronous output enable pin requires a clock edge for the outputs to follow the "L" and "H" logic of the input.

Table 8-1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK1C110x-Q1 family is a low additive jitter LVCMOS buffer design that can operate up to 250MHz at V_{DD} = 3.3V and 200MHz at V_{DD} = 2.5V, 1.8V. Low output skew as well as the ability for synchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

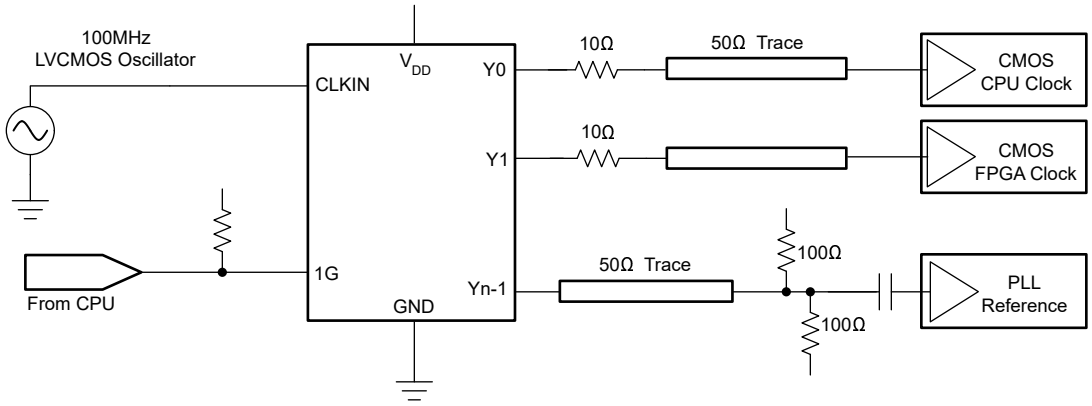


Figure 9-1. System Configuration Example

9.2.1 Design Requirements

The LMK1C110x-Q1 shown in Figure 9-1 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor R_S is placed near the LMK1C110x-Q1 to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the LMK1C110x-Q1.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination (pull up to VDD and pull down to GND) is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

9.2.2 Detailed Design Procedure

Unused outputs can be left floating. See *Power Supply Recommendations* for recommended filtering techniques.

9.2.3 Application Curves

The low additive jitter of the LMK1C110x-Q1 is shown in Figure 9-2.

Figure 9-3 shows the low-noise 156.25-MHz reference source with 25.6fs RMS jitter driving the LMK1C110x-Q1, resulting in 26.7fs RMS jitter when integrated from 12kHz to 20MHz at 3.3V supply. The resultant additive jitter measured is a low 7.6fs RMS for this configuration.

ADVANCE INFORMATION

Figure 9-4 shows the low-noise 156.25-MHz reference source with 25.6fs RMS jitter driving the LMK1C110x-Q1, resulting in 27.5fs RMS jitter when integrated from 12kHz to 20MHz at 2.5V supply. The resultant additive jitter measured is a low 10fs RMS for this configuration.

Figure 9-5 shows the low-noise 156.25-MHz reference source with 25.6fs RMS jitter driving the LMK1C110x-Q1, resulting in 32fs RMS jitter when integrated from 12kHz to 20MHz at 1.8V supply. The resultant additive jitter measured is a low 19.2fs RMS for this configuration.

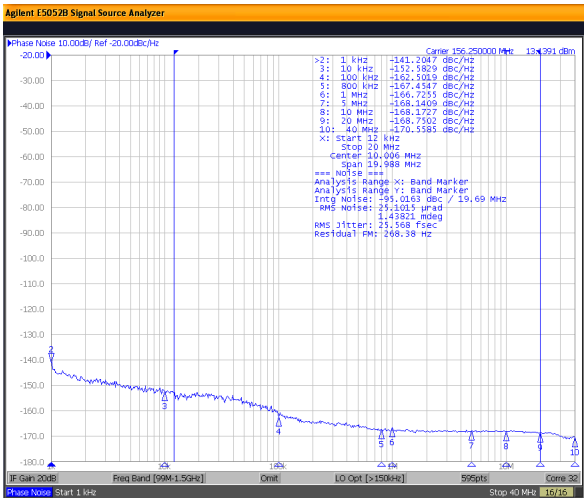


Figure 9-2. LMK1C110x-Q1 Reference Phase Noise 25.6fs (12kHz to 20MHz)

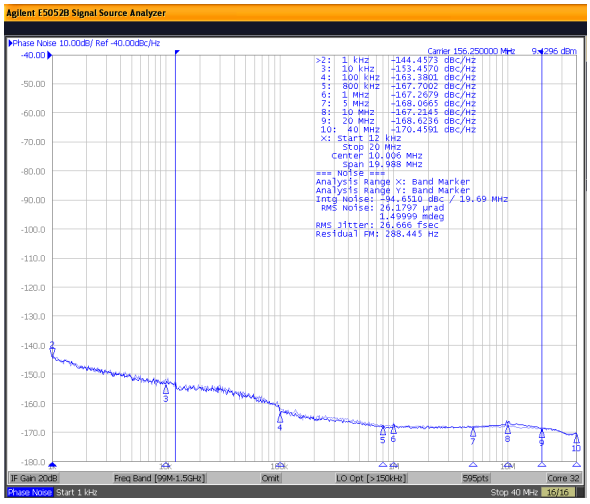


Figure 9-3. LMK1C110x-Q1 3.3V Output Phase Noise 26.7fs (12kHz to 20MHz)

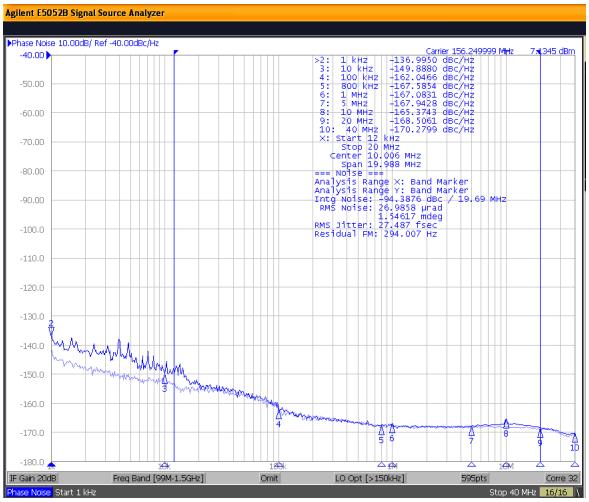


Figure 9-4. LMK1C110x-Q1 2.5V Output Phase Noise 27.5fs (12kHz to 20MHz)

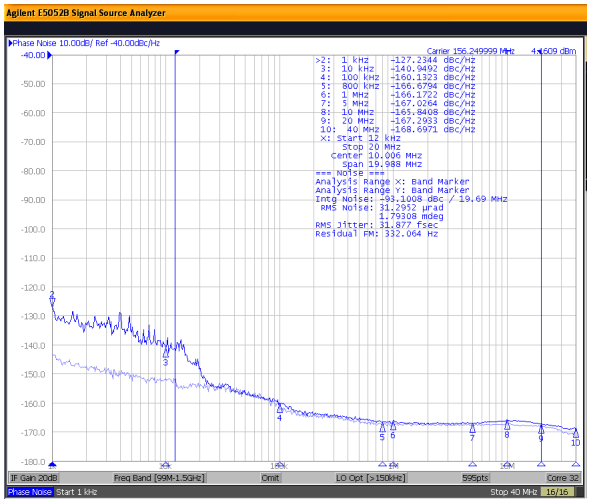


Figure 9-5. LMK1C110x-Q1 1.8V Output Phase Noise 32fs (12kHz to 20MHz)

ADVANCE INFORMATION

9.3 Power Supply Recommendations

High-performance clock buffers can be sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, managing any excessive noise from the system power supply is essential, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling

capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. Select an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 9-6 shows this recommended power supply decoupling method.

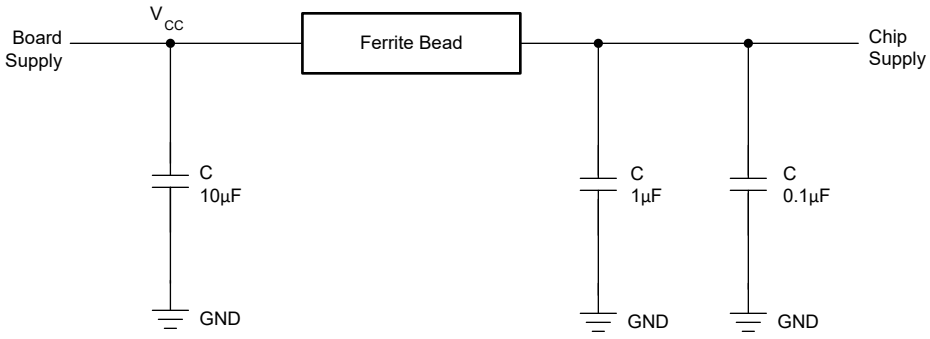


Figure 9-6. Power Supply Decoupling

9.4 Layout

9.4.1 Layout Guidelines

Figure 9-7 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

9.4.2 Layout Example

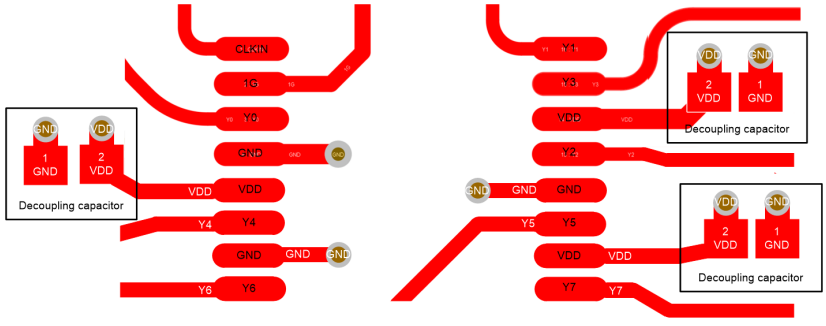


Figure 9-7. Layout Example for 14-Pin and 16-Pin PW Device

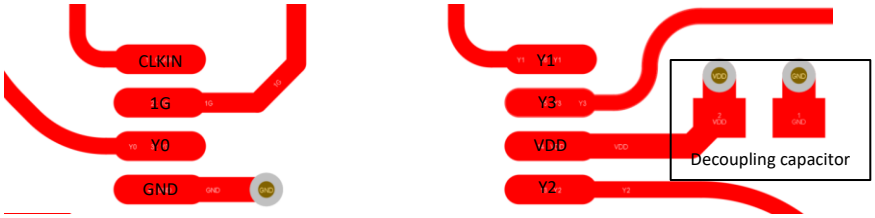


Figure 9-8. Layout Example for 8-Pin PW Device

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMK1C1108EVM*, EVM user's guide

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead finish/ Ball material(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PLMK1C1102Q DQFRQ1	ACTIVE	WSON	DQF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL2Q
PLMK1C1104Q DQFRQ1	ACTIVE	WSON	DQF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL4Q
PLMK1C1106Q PWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P1106Q
PLMK1C1108Q PWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P1108Q

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

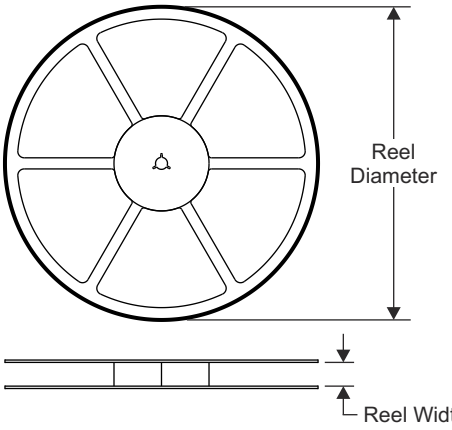
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

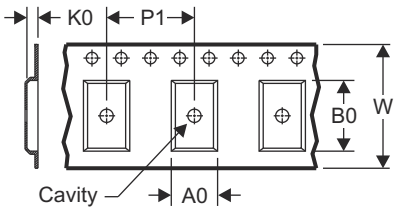
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

12.1 Tape and Reel Information

REEL DIMENSIONS

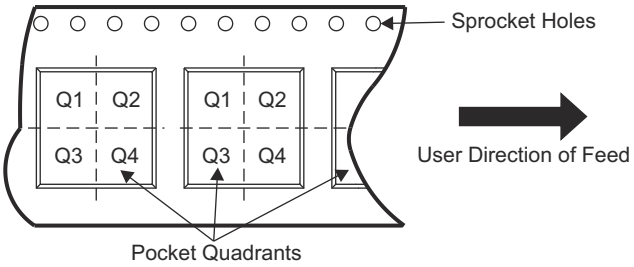


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

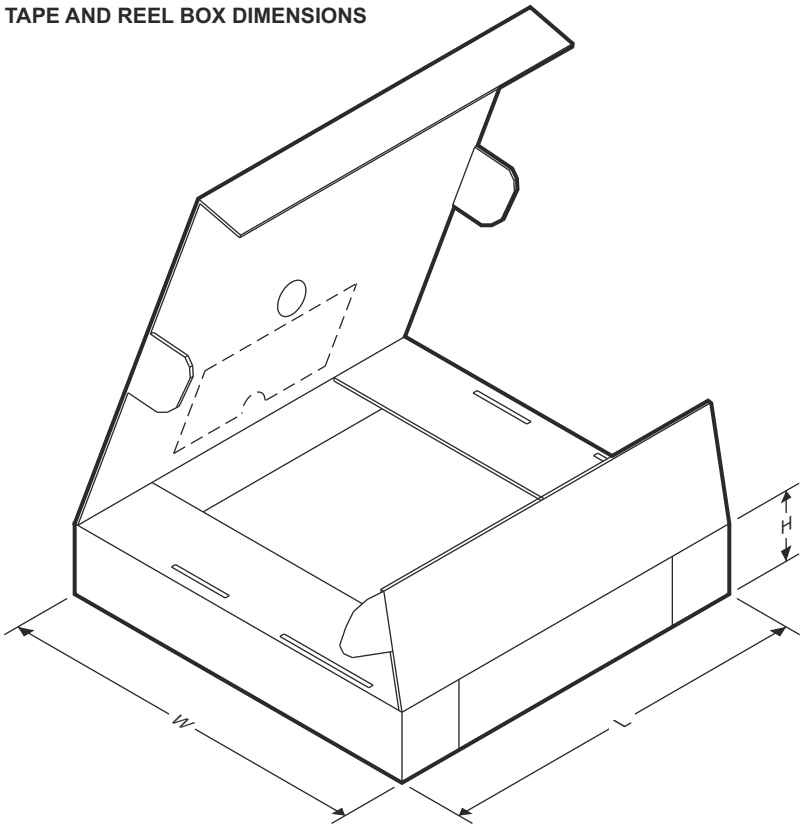
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLMK1C1102QDQFRQ1	WSON	DQF	8	250	178	8.4	2.25	2.25	1.0	4	8	Q2
PLMK1C1104QDQFRQ1	WSON	DQF	8	250	178	8.4	2.25	2.25	1.0	4	8	Q2
PLMK1C1106QPWRQ1	TSSOP	PW	14	2000	330	12.4	6.9	5.6	1.6	8	12	Q1
PLMK1C1108QPWRQ1	TSSOP	PW	16	2000	330	12.4	6.9	5.6	1.6	8	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLMK1C1102QDQFRQ1	WSON	DQF	8	250	205	200	33
PLMK1C1104QDQFRQ1	WSON	DQF	8	250	205	200	33
PLMK1C1106QPWRQ1	TSSOP	PW	14	2000	356	356	35
PLMK1C1108QPWRQ1	TSSOP	PW	16	2000	356	356	35

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLMK1C1106QPWTQ1	Active	Preproduction	TSSOP (PW) | 14	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
PLMK1C1108QPWTQ1	Active	Preproduction	TSSOP (PW) | 16	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LMK1C1106-Q1, LMK1C1108-Q1 :

- Catalog : LMK1C1106, LMK1C1108

NOTE: Qualified Version Definitions:

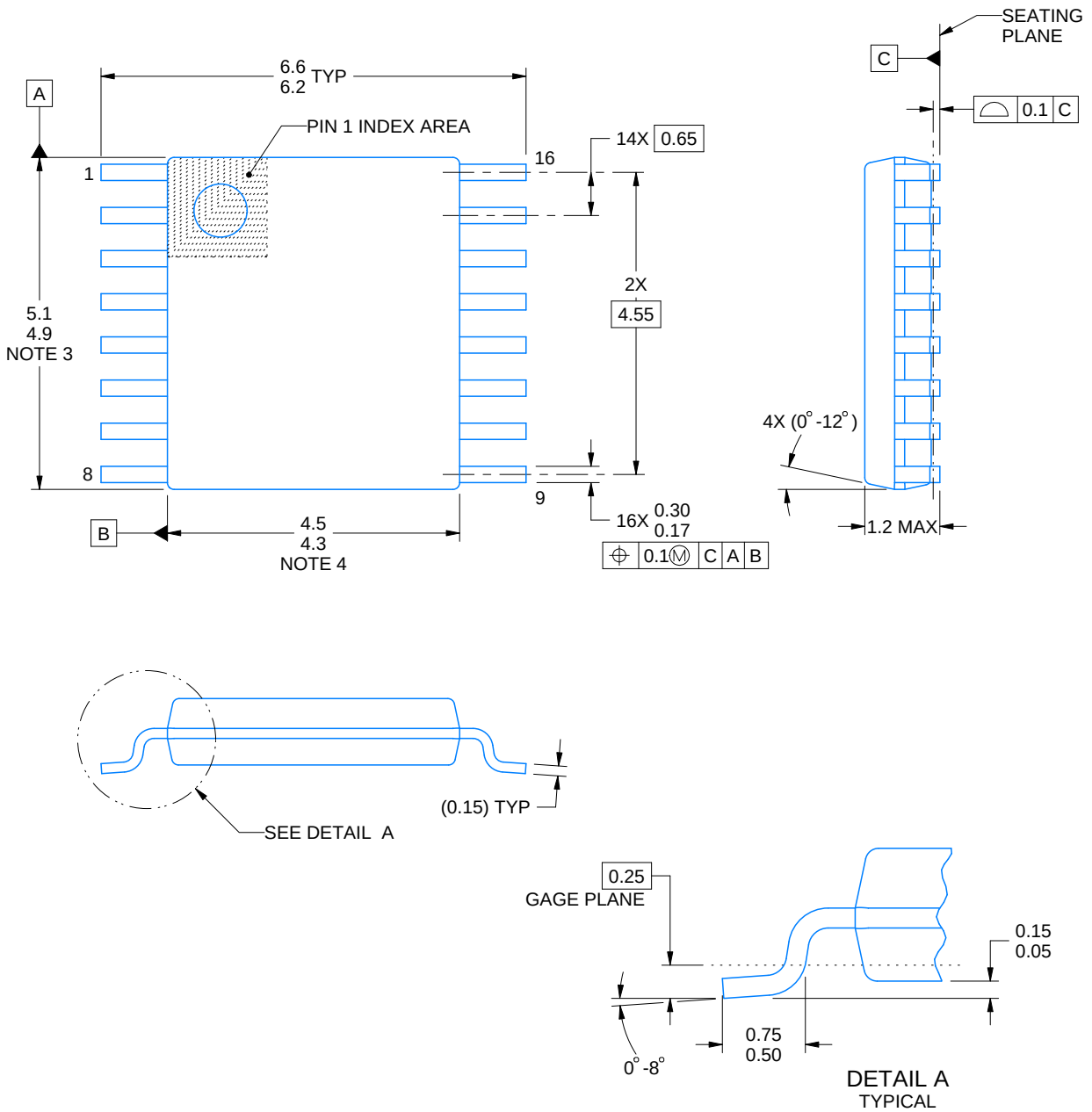
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

PW0016A

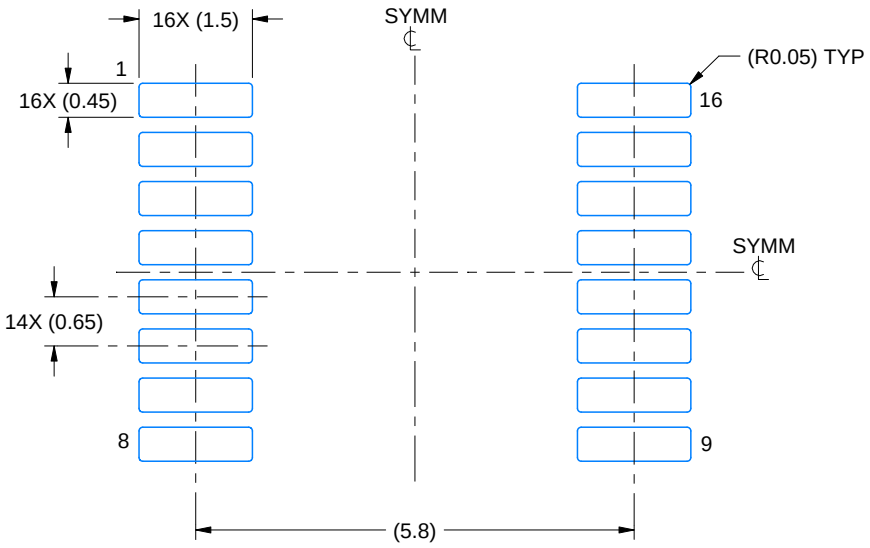
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



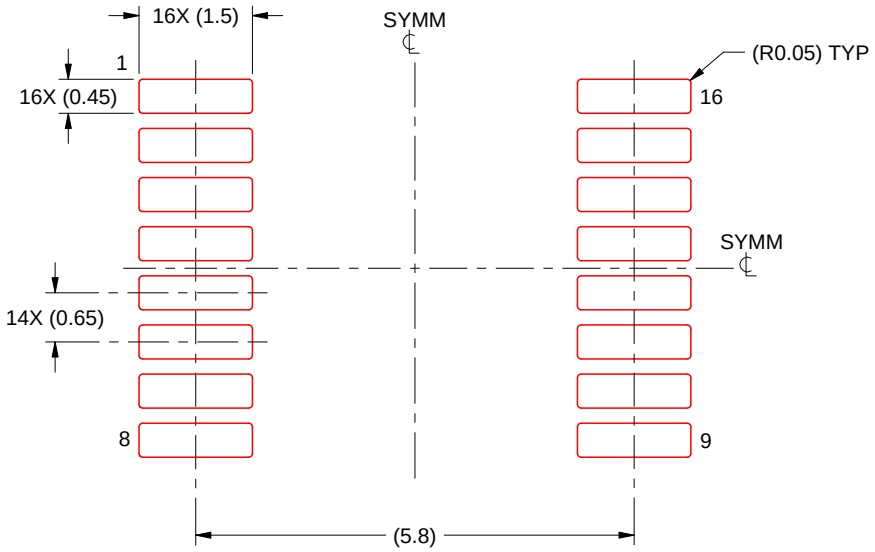
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

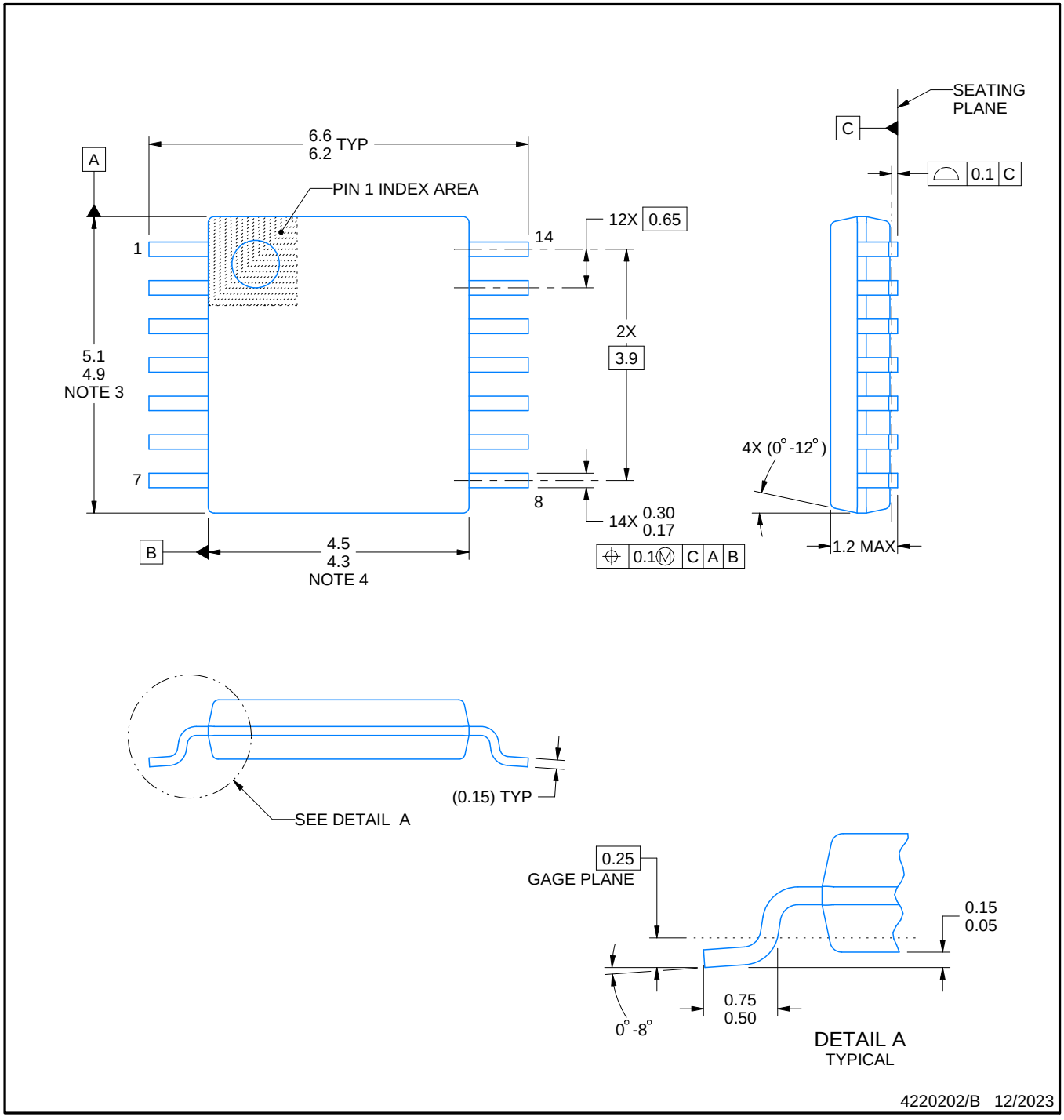
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

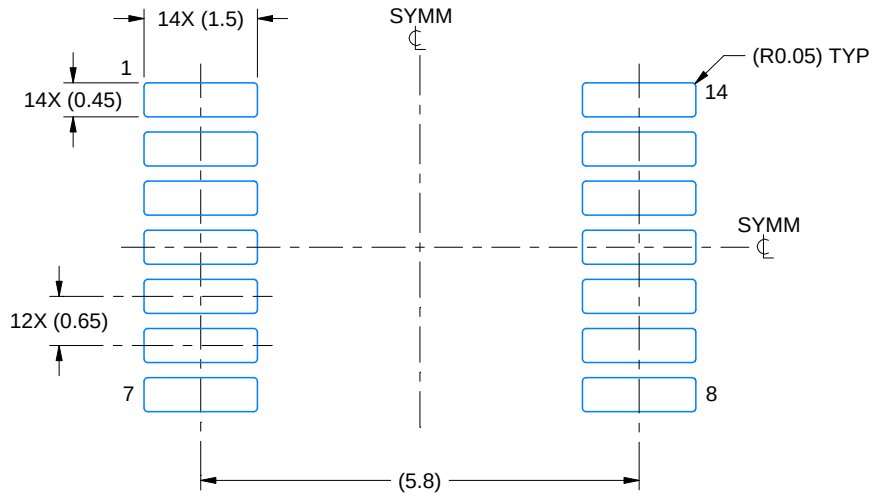
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

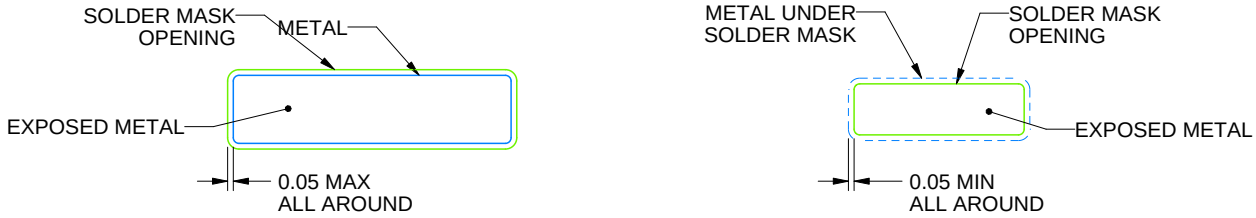


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

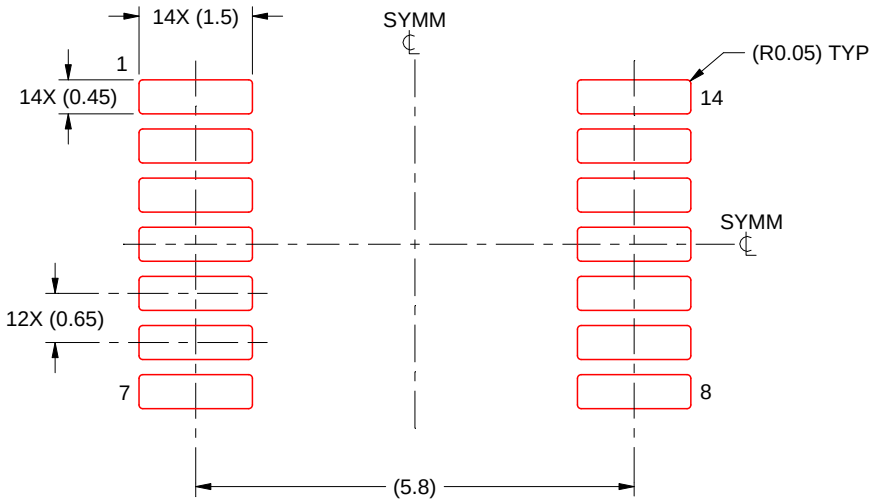


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025