

# INA12x Precision, Low-Power Instrumentation Amplifiers

## 1 Features

- Low offset voltage: 50μV, maximum
- Low drift: 0.5μV/°C, maximum
- Low input bias current:
  - 5nA, maximum (CSO: SHE)
  - 0.7nA, maximum (CSO: FRE)
- Low noise: 8nV/√Hz, 0.2μVpp
- High CMR: 120dB, minimum
- Bandwidth: 1.3MHz (G = 1)
- Inputs protected to ±40V
- Wide supply range: ±2.25V to ±18V
- Low quiescent current: 700μA
- Packages: 8-pin plastic DIP, SO-8

## 2 Applications

- [Pressure transmitter](#)
- [Temperature transmitter](#)
- [Weigh scale](#)
- [Electrocardiogram \(ECG\)](#)
- [Analog input module](#)
- [Data acquisition \(DAQ\)](#)

## 3 Description

The INA128 and INA129 (INA12x) are low-power, general-purpose instrumentation amplifiers that offer excellent accuracy. The versatile three op amp design and small size make these amplifiers an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation with a 50kΩ resistor. The INA129 gain equation uses a 49.4kΩ resistor to allow for drop-in replacements of comparable devices.

The INA12x are available in plastic DIP and surface-mount packages, specified for the –40°C to +85°C temperature range. The INA128 is also available in a dual configuration, the [INA218](#).

The upgraded [INA828](#) offers a lower input bias current (0.6nA, maximum) and lower noise (7nV/√Hz) at the same quiescent current. See the [Device Comparison Table](#) for a selection of precision instrumentation amplifiers from Texas Instruments.

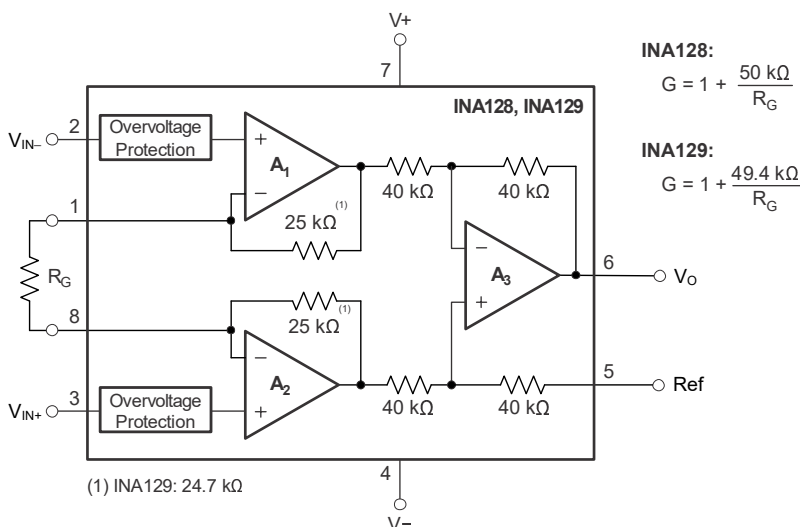
### Device Information

| PART NUMBER <sup>(3)</sup> | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|----------------------------|------------------------|-----------------------------|
| INA128,<br>INA129          | D (SOIC, 8)            | 4.9mm × 6mm                 |
|                            | P (PDIP, 8)            | 9.81mm × 9.43mm             |

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) See the [Device Comparison Table](#).



**Simplified Schematic**



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## 4 Device Comparison Table

| DEVICE                 | DESCRIPTION                                                                                                | GAIN EQUATION                      | RG PINS AT PIN |
|------------------------|------------------------------------------------------------------------------------------------------------|------------------------------------|----------------|
| <a href="#">INA818</a> | 35-μV offset, 0.4-μV/°C $V_{OS}$ drift, 8nV/√Hz noise, low-power, precision instrumentation amplifier      | $G = 1 + 50 \text{ k}\Omega / R_G$ | 1, 8           |
| <a href="#">INA821</a> | 35-μV offset, 0.4-μV/°C $V_{OS}$ drift, 7nV/√Hz noise, high-bandwidth, precision instrumentation amplifier | $G = 1 + 49.4\text{k}\Omega / R_G$ | 2, 3           |
| <a href="#">INA828</a> | 50-μV offset, 0.5-μV/°C $V_{OS}$ drift, 7nV/√Hz noise, low-power, precision instrumentation amplifier      | $G = 1 + 50 \text{ k}\Omega / R_G$ | 1, 8           |
| <a href="#">INA333</a> | 25-μV $V_{OS}$ , 0.1-μV/°C $V_{OS}$ drift, 1.8V to 5V, RRO, 50-μA $I_Q$ , chopper-stabilized INA           | $G = 1 + 100\text{k}\Omega / R_G$  | 1, 8           |
| <a href="#">PGA280</a> | 20mV to ±10V programmable gain IA with 3V or 5V differential output; analog supply up to ±18V              | Digital programmable               | N/A            |
| <a href="#">INA159</a> | $G = 0.2\text{V}$ differential amplifier for ±10V to 3V and 5V conversion                                  | $G = 0.2 \text{ V/V}$              | N/A            |
| <a href="#">PGA112</a> | Precision programmable gain op amp with SPI                                                                | Digital programmable               | N/A            |

## 5 Pin Configuration and Functions

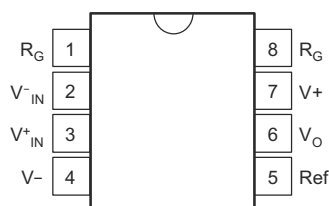


Figure 5-1. D (8-Pin SOIC) and P (8-Pin PDIP) Packages, Top View

Table 5-1. Pin Functions

| PIN       |     | TYPE   | DESCRIPTION                                                                                |
|-----------|-----|--------|--------------------------------------------------------------------------------------------|
| NAME      | NO. |        |                                                                                            |
| REF       | 5   | Input  | Reference input. This pin must be driven by low impedance or connected to ground.          |
| $R_G$     | 1,8 | —      | Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8. |
| $V_-$     | 4   | Power  | Negative supply                                                                            |
| $V_+$     | 7   | Power  | Positive supply                                                                            |
| $V_{IN-}$ | 2   | Input  | Negative input                                                                             |
| $V_{IN+}$ | 3   | Input  | Positive input                                                                             |
| $V_O$     | 6   | Output | Output                                                                                     |

## 6 Specifications

### Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see [Section 9.1.1](#).

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                     |                                           | MIN        | MAX | UNIT |
|------------------|-------------------------------------|-------------------------------------------|------------|-----|------|
| V <sub>S</sub>   | Supply voltage                      | Dual supply, V <sub>S</sub> = (V+) – (V–) |            | ±18 | V    |
|                  |                                     | Single supply, V <sub>S</sub> = (V+) – 0V |            | 36  |      |
|                  | Analog input voltage                |                                           |            | ±40 | V    |
|                  | Output short-circuit <sup>(2)</sup> |                                           | Continuous |     |      |
| T <sub>A</sub>   | Operating temperature               |                                           | –40        | 125 | °C   |
|                  | Junction temperature                |                                           |            | 150 | °C   |
|                  | Lead temperature (soldering, 10s)   |                                           |            | 300 | °C   |
| T <sub>stg</sub> | Storage temperature                 |                                           | –55        | 125 | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to V<sub>S</sub> / 2.

### 6.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±50   |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                                                         |               | MIN      | TYP | MAX      | UNIT |
|----------------|---------------------------------------------------------|---------------|----------|-----|----------|------|
| V <sub>S</sub> | Supply voltage                                          | Single-supply | 4.5      | 30  | 36       | V    |
|                |                                                         | Dual-supply   | ±2.25    | ±15 | ±18      |      |
|                | Input common-mode voltage range for V <sub>O</sub> = 0V |               | (V–) + 2 |     | (V+) – 2 | V    |
| T <sub>A</sub> | Specified temperature                                   |               | –40      |     | 85       | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | INA12x   |          | UNIT |
|-------------------------------|----------------------------------------------|----------|----------|------|
|                               |                                              | D (SOIC) | P (PDIP) |      |
|                               |                                              | 8 PINS   | 8 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 110      | 46.1     | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 57       | 34.1     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 54       | 23.4     | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 11       | 11.3     | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 53       | 23.2     | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.5 Electrical Characteristics

at T<sub>A</sub> = 25°C, V<sub>S</sub> = ±15 V, R<sub>L</sub> = 10 kΩ, V<sub>REF</sub> = 0 V, V<sub>CM</sub> = V<sub>S</sub> / 2, and G = 1, all chips site origins (CSO) (unless otherwise noted)

| PARAMETER       |                                    | TEST CONDITIONS                                           |                    |                    | MIN                            | TYP | MAX           | UNIT  |
|-----------------|------------------------------------|-----------------------------------------------------------|--------------------|--------------------|--------------------------------|-----|---------------|-------|
| INPUT           |                                    |                                                           |                    |                    |                                |     |               |       |
| V <sub>OS</sub> | Offset voltage (RTI)               | 1 ≤ G ≤ 10000                                             | CSO: SHE           | INA12xP, INA12xU   | ±10 ±100 / G                   |     | ±50 ±500 / G  | μV    |
|                 |                                    |                                                           |                    | INA12xPA, INA12xUA | ±25 ±100 / G    ±125 ±1000 / G |     |               |       |
|                 |                                    |                                                           | CSO: FRE           | INA12xU            | ±20 ±50 / G                    |     | ±50 ±500 / G  |       |
|                 |                                    |                                                           |                    | INA12xUA           | ±20 ±50 / G    ±125 ±1000 / G  |     |               |       |
|                 | Offset voltage drift (RTI)         | T <sub>A</sub> = −40°C to +85°C                           | INA12xP, INA12xU   |                    | ±0.2 ±2 / G                    |     | ±0.5 ±20 / G  | μV/°C |
|                 |                                    |                                                           | INA12xPA, INA12xUA |                    | ±0.2 ±5 / G    ±1 ±20 / G      |     |               |       |
| PSRR            | Power-supply rejection ratio (RTI) | V <sub>S</sub> = ±2.25V to ±18V                           | CSO: SHE           | INA12xP, INA12xU   | ±0.2 ±20 / G                   |     | ±1 ±100 / G   | μV/V  |
|                 |                                    |                                                           |                    | INA12xPA, INA12xUA | ±2 ±200 / G                    |     |               |       |
|                 |                                    |                                                           | CSO: FRE           | INA12xU            | ±0.1 ±1 / G                    |     | ±0.4 ±3.2 / G |       |
|                 |                                    |                                                           |                    | INA12xUA           | ±0.8 ±6.4 / G                  |     |               |       |
|                 | Long-term stability                | CSO: SHE                                                  |                    |                    | ±0.1 ±3 / G                    |     | μV/mo         |       |
|                 |                                    | CSO: FRE                                                  |                    |                    | ±0.2 ±3 / G                    |     |               |       |
|                 | Input impedance                    | Differential                                              |                    |                    | 10    2                        |     | GΩ    pF      |       |
|                 |                                    | Common-mode                                               |                    |                    | 100    9                       |     |               |       |
| V <sub>CM</sub> | Common-mode voltage <sup>(2)</sup> | V <sub>O</sub> = 0V                                       |                    |                    | (V−) + 2                       |     | (V+) − 2      | V     |
|                 | Safe input voltage                 | R <sub>S</sub> = 0Ω                                       |                    |                    |                                |     | ±40           | V     |
| CMRR            | Common-mode rejection ratio        | ΔR <sub>S</sub> = 1 kΩ, V <sub>CM</sub> = ±13 V, CSO: SHE | G = 1              | INA12xP, INA12xU   | 80                             | 86  | dB            |       |
|                 |                                    |                                                           |                    | INA12xPA, INA12xUA | 73                             |     |               |       |
|                 |                                    |                                                           | G = 10             | INA12xP, INA12xU   | 100                            | 106 |               |       |
|                 |                                    |                                                           |                    | INA12xPA, INA12xUA | 93                             |     |               |       |
|                 |                                    |                                                           | G = 100            | INA12xP, INA12xU   | 120                            | 125 |               |       |
|                 |                                    |                                                           |                    | INA12xPA, INA12xUA | 110                            |     |               |       |
|                 |                                    |                                                           | G = 1000           | INA12xP, INA12xU   | 120                            | 130 |               |       |
|                 |                                    |                                                           |                    | INA12xPA, INA12xUA | 110                            |     |               |       |
|                 |                                    | ΔR <sub>S</sub> = 1 kΩ, V <sub>CM</sub> = ±13 V, CSO: FRE | G = 1              | INA12xU            | 90                             | 100 |               |       |
|                 |                                    |                                                           |                    | INA12xUA           | 83                             |     |               |       |
|                 |                                    |                                                           | G = 10             | INA12xU            | 110                            | 120 |               |       |
|                 |                                    |                                                           |                    | INA12xUA           | 103                            |     |               |       |
|                 |                                    |                                                           | G = 100            | INA12xU            | 130                            | 140 |               |       |
|                 |                                    |                                                           |                    | INA12xUA           | 120                            |     |               |       |
|                 |                                    |                                                           | G = 1000           | INA12xU            | 140                            | 145 |               |       |
|                 |                                    |                                                           |                    | INA12xUA           | 130                            |     |               |       |

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)

| PARAMETER          |                            | TEST CONDITIONS                 |                                | MIN      | TYP   | MAX              | UNIT   |
|--------------------|----------------------------|---------------------------------|--------------------------------|----------|-------|------------------|--------|
| INPUT BIAS CURRENT |                            |                                 |                                |          |       |                  |        |
| I <sub>B</sub>     | Input bias current         | CSO: SHE                        | INA12xP, INA12xU               |          | ±2    | ±5               | nA     |
|                    |                            |                                 | INA12xPA, INA12xUA             |          |       | ±10              |        |
|                    |                            | CSO: FRE                        | INA12xU                        |          | ±0.15 | ±0.6             |        |
|                    |                            |                                 | INA12xUA                       |          |       | ±1.2             |        |
|                    | Input bias current drift   | T <sub>A</sub> = −40°C to +85°C |                                |          | ±30   |                  | pA/°C  |
| I <sub>OS</sub>    | Input offset current       | CSO: SHE                        | INA12xP, INA12xU               |          | ±1    | ±5               | nA     |
|                    |                            |                                 | INA12xPA, INA12xUA             |          |       | ±10              |        |
|                    |                            | CSO: FRE                        | INA12xU                        |          | ±0.15 | ±0.6             |        |
|                    |                            |                                 | INA12xUA                       |          |       | ±1.2             |        |
|                    | Input offset current drift | T <sub>A</sub> = −40°C to +85°C |                                |          | ±30   |                  | pA/°C  |
| NOISE              |                            |                                 |                                |          |       |                  |        |
| e <sub>N</sub>     | Voltage noise (RTI)        | G = 1000, R <sub>S</sub> = 0Ω   | f = 10Hz                       | CSO: SHE |       | 10               | nV/√Hz |
|                    |                            |                                 |                                | CSO: FRE |       | 7                |        |
|                    |                            |                                 | f = 100Hz                      | CSO: SHE |       | 8                |        |
|                    |                            |                                 |                                | CSO: FRE |       | 6.9              |        |
|                    |                            |                                 | f = 1kHz                       | CSO: SHE |       | 8                |        |
|                    |                            |                                 |                                | CSO: FRE |       | 6.9              |        |
|                    |                            |                                 | f <sub>B</sub> = 0.1Hz to 10Hz |          |       | 0.2              |        |
| I <sub>n</sub>     | Current noise              | f = 10Hz                        |                                |          | 0.9   | pA/√Hz           |        |
|                    |                            |                                 | f = 1kHz                       | CSO: SHE |       |                  | 0.3    |
|                    |                            | CSO: FRE                        |                                |          | 0.17  |                  |        |
|                    |                            | f <sub>B</sub> = 0.1Hz to 10Hz  | CSO: SHE                       |          | 30    | pA <sub>PP</sub> |        |
|                    |                            |                                 | CSO: FRE                       |          | 4.7   |                  |        |

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{\text{REF}} = 0\text{ V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)

| PARAMETER       |                                  | TEST CONDITIONS                  |                                          |                    | MIN                             | TYP | MAX    | UNIT     |
|-----------------|----------------------------------|----------------------------------|------------------------------------------|--------------------|---------------------------------|-----|--------|----------|
| GAIN            |                                  |                                  |                                          |                    |                                 |     |        |          |
|                 | Gain equation                    | INA128                           |                                          |                    | 1 + (50 kΩ / R <sub>G</sub> )   |     |        | V/V      |
|                 |                                  | INA129                           |                                          |                    | 1 + (49.4 kΩ / R <sub>G</sub> ) |     |        |          |
| G               | Gain                             |                                  |                                          |                    | 1                               |     | 10000  | V/V      |
|                 | Gain error                       | G = 1                            | CSO: SHE                                 | INA12xP, INA12xU   | ±0.01                           |     | ±0.024 | %        |
|                 |                                  |                                  |                                          | INA12xPA, INA12xUA |                                 |     | ±0.1   |          |
|                 |                                  |                                  | CSO: FRE                                 | INA12xU            | ±0.005                          |     | ±0.025 |          |
|                 |                                  |                                  |                                          | INA12xUA           |                                 |     | ±0.1   |          |
|                 |                                  | G = 10                           | CSO: SHE                                 | INA12xP, INA12xU   | ±0.02                           |     | ±0.4   |          |
|                 |                                  |                                  |                                          | INA12xPA, INA12xUA |                                 |     | ±0.5   |          |
|                 |                                  |                                  | CSO: FRE                                 | INA12xU            | ±0.025                          |     | ±0.15  |          |
|                 |                                  |                                  |                                          | INA12xUA           |                                 |     | ±0.2   |          |
|                 |                                  | G = 100                          | CSO: SHE                                 | INA12xP, INA12xU   | ±0.05                           |     | ±0.5   |          |
|                 |                                  |                                  |                                          | INA12xPA, INA12xUA |                                 |     | ±0.7   |          |
|                 |                                  |                                  | CSO: FRE                                 | INA12xU            | ±0.025                          |     | ±0.15  |          |
|                 |                                  |                                  |                                          | INA12xUA           |                                 |     | ±0.25  |          |
|                 |                                  | G = 1000                         | CSO: SHE                                 | INA12xP, INA12xU   | ±0.5                            |     | ±1     |          |
|                 |                                  |                                  |                                          | INA12xPA, INA12xUA |                                 |     | ±2     |          |
|                 |                                  |                                  | CSO: FRE                                 | INA12xU            | ±0.05                           |     | ±1     |          |
|                 |                                  |                                  |                                          | INA12xUA           |                                 |     | ±2     |          |
|                 | Gain drift <sup>(4)</sup>        | T <sub>A</sub> = −40°C to +85°C  | CSO: SHE                                 |                    | ±1                              |     | ±10    | ppm/°C   |
|                 |                                  |                                  | CSO: FRE                                 |                    |                                 |     | ±5     |          |
|                 |                                  |                                  | 50kΩ or 49.4kΩ resistance <sup>(3)</sup> | CSO: SHE           | ±25                             |     | ±100   |          |
|                 |                                  |                                  |                                          | CSO: FRE           |                                 |     | ±50    |          |
|                 | Gain nonlinearity <sup>(1)</sup> | G = 1, V <sub>O</sub> = ±13.6V   | INA12xP, INA12xU                         |                    | ±0.0001                         |     | ±0.001 | % of FSR |
|                 |                                  |                                  | INA12xPA, INA12xUA                       |                    |                                 |     | ±0.002 |          |
|                 |                                  | G = 10                           | INA12xP, INA12xU                         |                    | ±0.0003                         |     | ±0.002 |          |
|                 |                                  |                                  | INA12xPA, INA12xUA                       |                    |                                 |     | ±0.004 |          |
|                 |                                  | G = 100                          | INA12xP, INA12xU                         |                    | ±0.0005                         |     | ±0.002 |          |
|                 |                                  |                                  | INA12xPA, INA12xUA                       |                    |                                 |     | ±0.004 |          |
|                 |                                  | G = 1000                         |                                          |                    | ±0.001                          |     |        |          |
|                 |                                  |                                  |                                          |                    |                                 |     |        |          |
| OUTPUT          |                                  |                                  |                                          |                    |                                 |     |        |          |
|                 | Positive output voltage swing    | CSO: SHE                         |                                          |                    | (V+) − 1.4                      |     |        | V        |
|                 |                                  | CSO: FRE                         |                                          |                    | (V+) − 0.15                     |     |        |          |
|                 | Negative output voltage swing    | CSO: SHE                         |                                          |                    | (V−) + 1.4                      |     |        | V        |
|                 |                                  | CSO: FRE                         |                                          |                    | (V−) + 0.15                     |     |        |          |
| C <sub>L</sub>  | Load capacitance                 | Stable operation                 |                                          |                    | 1000                            |     |        | pF       |
| I <sub>SC</sub> | Short-circuit current            | Continuous to V <sub>S</sub> / 2 | CSO: SHE                                 |                    | +6/−15                          |     |        | mA       |
|                 |                                  |                                  | CSO: FRE                                 |                    | +18/−18                         |     |        |          |

## 6.5 Electrical Characteristics (continued)

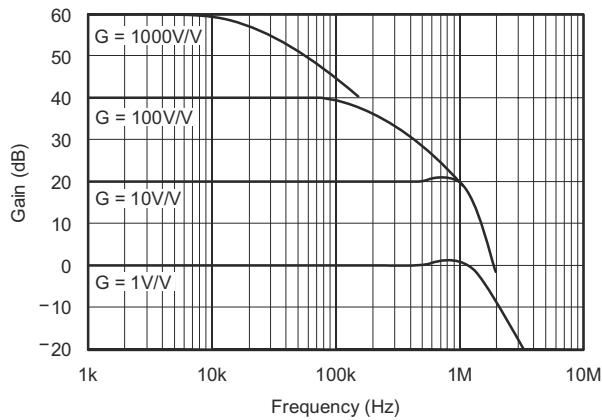
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| PARAMETER          |                   | TEST CONDITIONS              |          | MIN      | TYP | MAX  | UNIT |    |
|--------------------|-------------------|------------------------------|----------|----------|-----|------|------|----|
| FREQUENCY RESPONSE |                   |                              |          |          |     |      |      |    |
| BW                 | Bandwidth, −3dB   | G = 1                        |          | 1.3      |     |      | MHz  |    |
|                    |                   | G = 10                       |          | 640      |     |      | kHz  |    |
|                    |                   | G = 100                      |          | 200      |     |      |      |    |
|                    |                   | G = 1000                     | CSO: SHE | 20       |     |      |      |    |
|                    |                   |                              | CSO: FRE | 33       |     |      |      |    |
| SR                 | Slew rate         | G = 5, V <sub>O</sub> = ±10V | CSO: SHE | 4        |     |      | V/μs |    |
|                    |                   |                              | CSO: FRE | 1.2      |     |      |      |    |
| t <sub>s</sub>     | Settling time     | To 0.01%                     | G = 1    | CSO: SHE | 7   |      |      | μs |
|                    |                   |                              |          | CSO: FRE | 12  |      |      |    |
|                    |                   |                              | G = 10   | CSO: SHE | 7   |      |      |    |
|                    |                   |                              |          | CSO: FRE | 12  |      |      |    |
|                    |                   |                              | G = 100  | CSO: SHE | 9   |      |      |    |
|                    |                   |                              |          | CSO: FRE | 12  |      |      |    |
|                    |                   |                              | G = 1000 |          | 80  |      |      |    |
|                    | Overload recovery | 50% input overload           |          | 4        |     |      | μs   |    |
| POWER SUPPLY       |                   |                              |          |          |     |      |      |    |
| I <sub>Q</sub>     | Quiescent current | V <sub>IN</sub> = 0V         |          | ±700     |     | ±750 | μA   |    |

- (1) Nonlinearity measurements in  $G = 1000$  are dominated by noise. Typical nonlinearity is  $\pm 0.001\%$
- (2) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
- (3) Temperature coefficient of the  $50\text{-k}\Omega$  or  $49.4\text{-k}\Omega$  term in the gain equation.
- (4) Specified by wafer test.

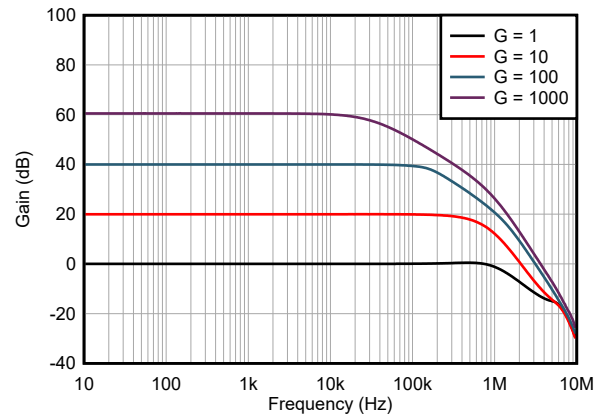
## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)



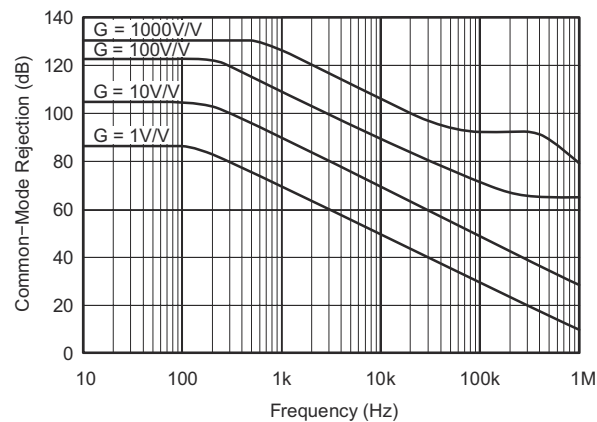
CSO: SHE

**Figure 6-1. Gain vs Frequency**



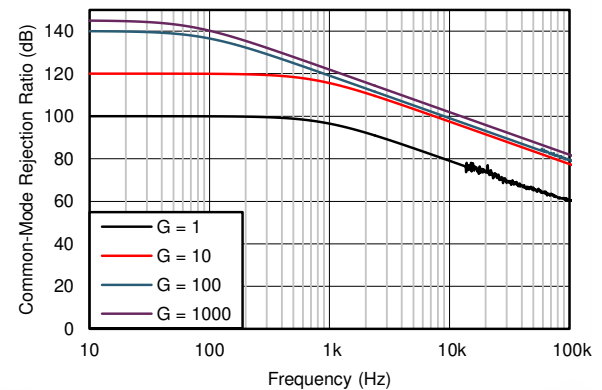
CSO: FRE

**Figure 6-2. Gain vs Frequency**



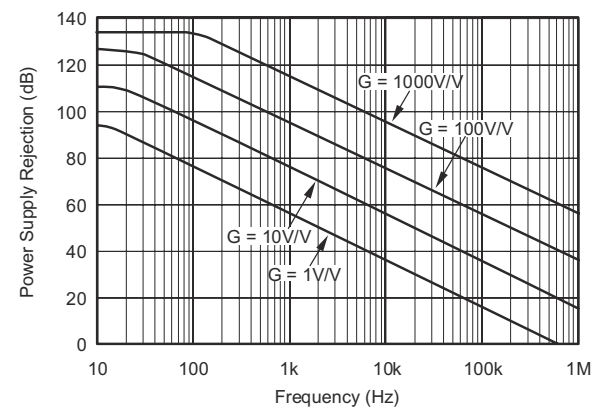
CSO: SHE

**Figure 6-3. Common-Mode Rejection vs Frequency**



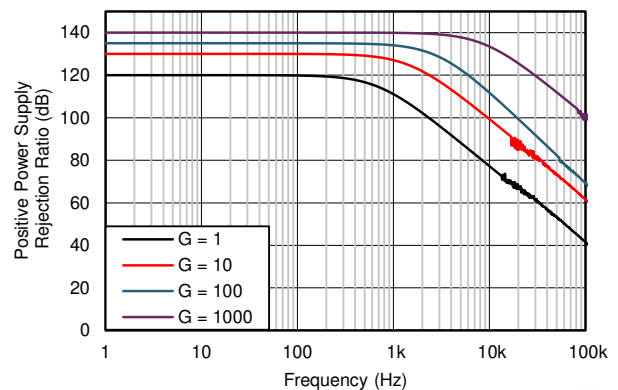
CSO: FRE

**Figure 6-4. Common-Mode Rejection vs Frequency**



CSO: SHE

**Figure 6-5. Positive Power Supply Rejection vs Frequency**

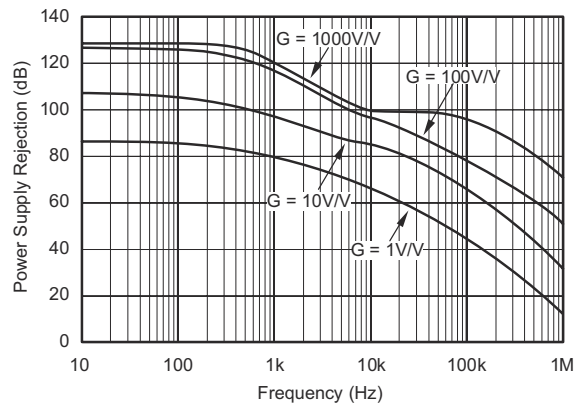


CSO: FRE

**Figure 6-6. Positive Power Supply Rejection vs Frequency**

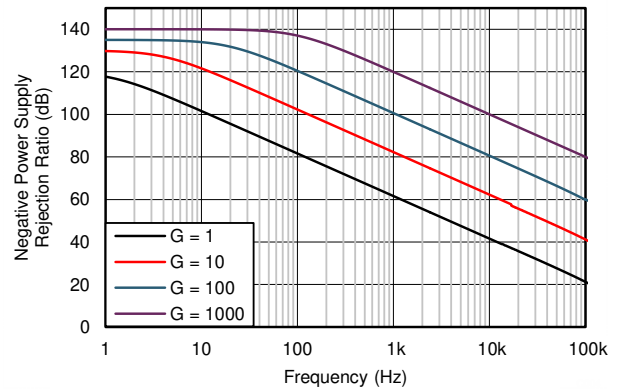
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)



CSO: SHE

Figure 6-7. Negative Power Supply Rejection vs Frequency



CSO: FRE

Figure 6-8. Negative Power Supply Rejection vs Frequency

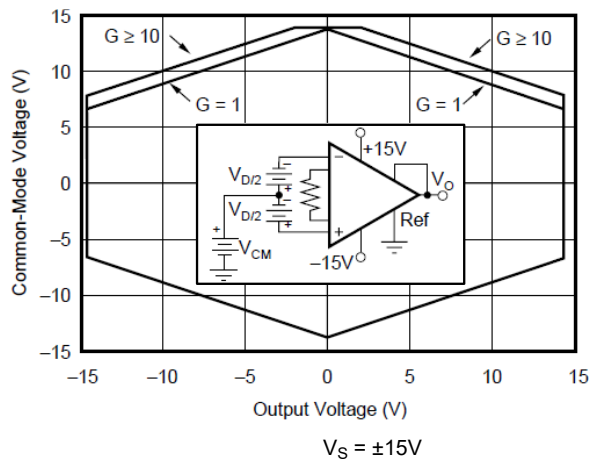


Figure 6-9. Input Common-Mode Range vs Output Voltage

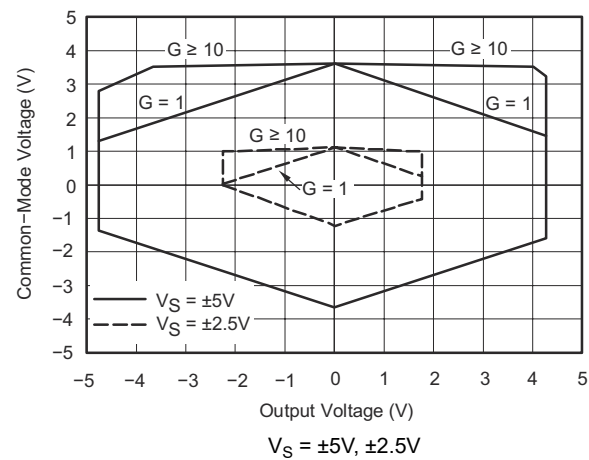
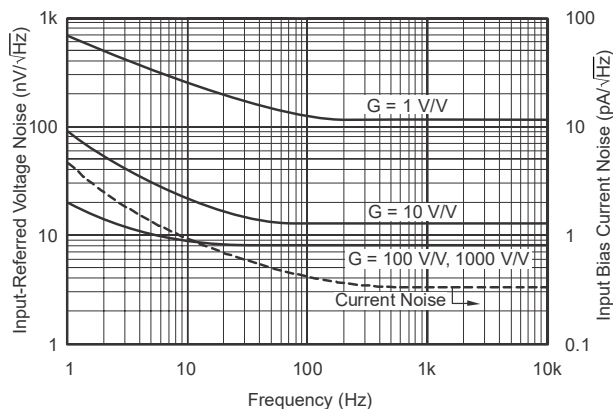
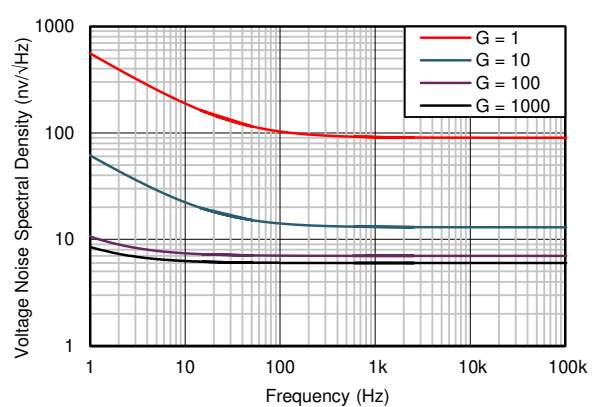


Figure 6-10. Input Common-Mode Range vs Output Voltage



CSO: SHE

Figure 6-11. Input-Referred Noise vs Frequency

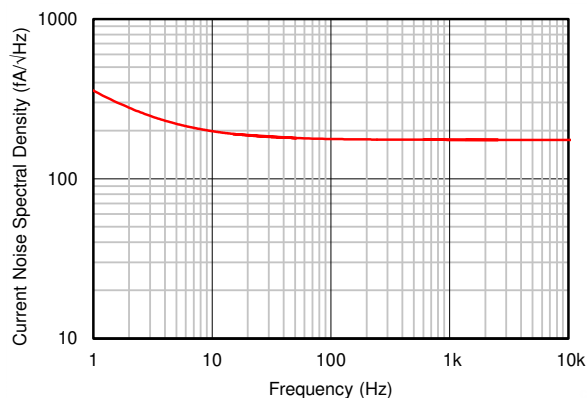


CSO: FRE

Figure 6-12. Input-Referred Voltage Noise vs Frequency

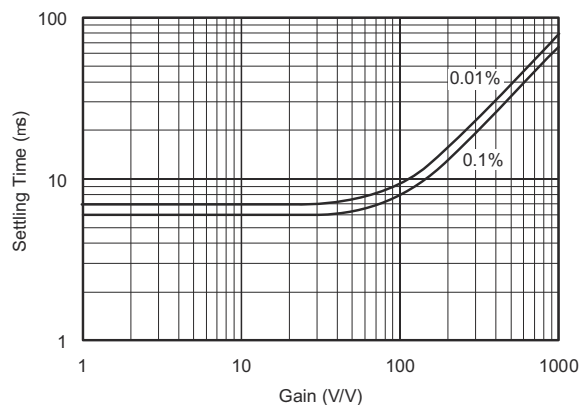
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)



CSO: FRE

Figure 6-13. Input-Referred Current Noise vs Frequency



CSO: SHE

Figure 6-14. Settling Time vs Gain

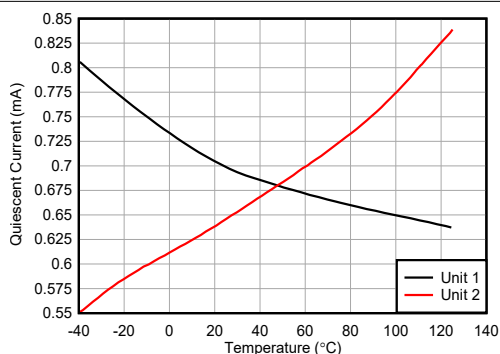
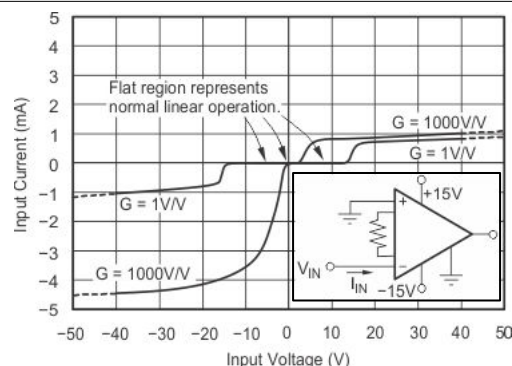
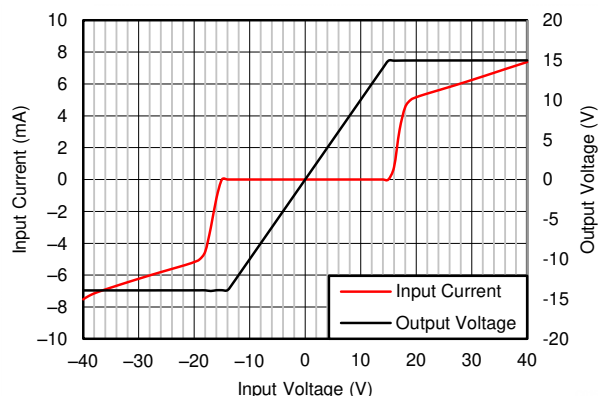


Figure 6-15. Quiescent Current vs Temperature



CSO: SHE

Figure 6-16. Input Overvoltage V/I Characteristics



CSO: FRE

Figure 6-17. Input Overvoltage V/I Characteristics

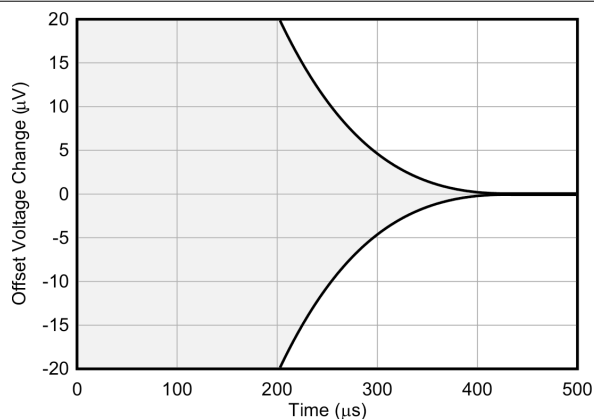
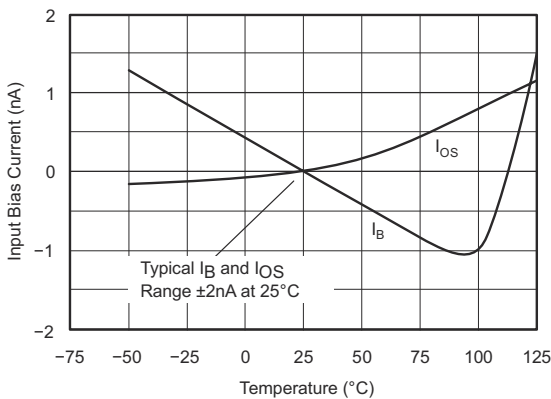


Figure 6-18. Input Offset Voltage Warm-Up

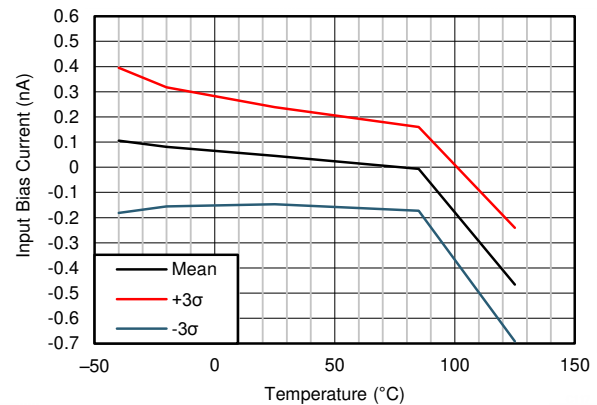
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)



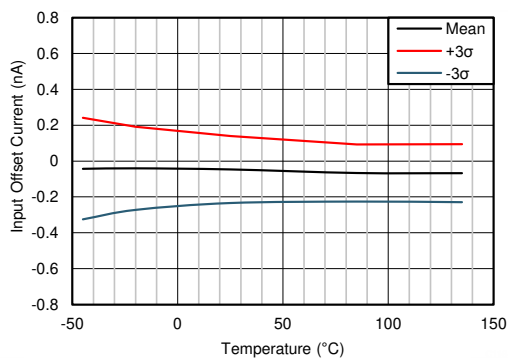
CSO: SHE

Figure 6-19. Input Bias Current vs Temperature



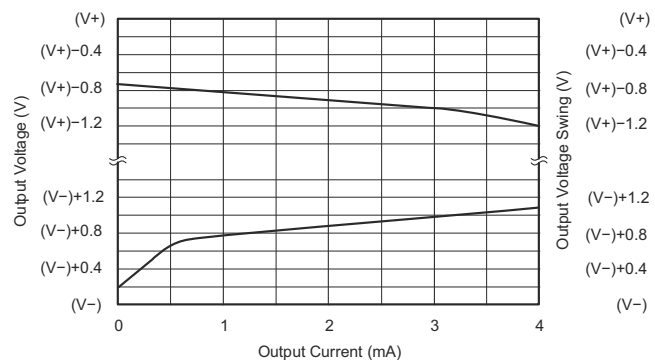
CSO: FRE

Figure 6-20. Input Bias Current vs Temperature



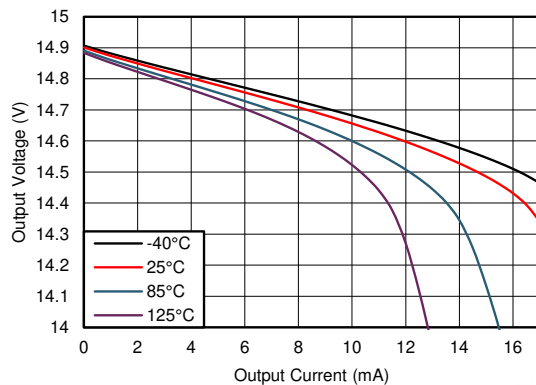
CSO: FRE

Figure 6-21. Input Offset Current vs Temperature



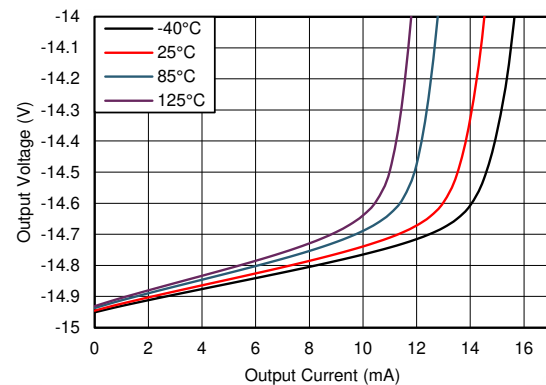
CSO: SHE

Figure 6-22. Output Voltage Swing vs Output Current



CSO: FRE

Figure 6-23. Positive Output Voltage Swing vs Output Current

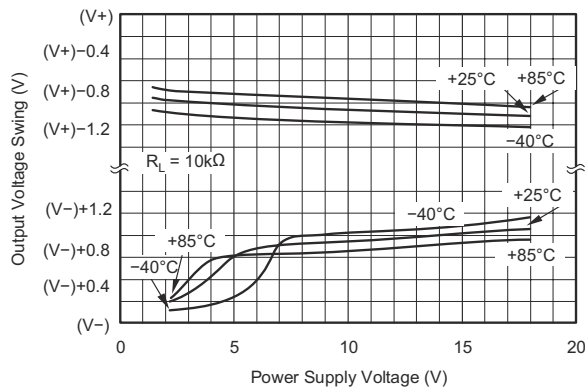


CSO: FRE

Figure 6-24. Negative Output Voltage Swing vs Output Current

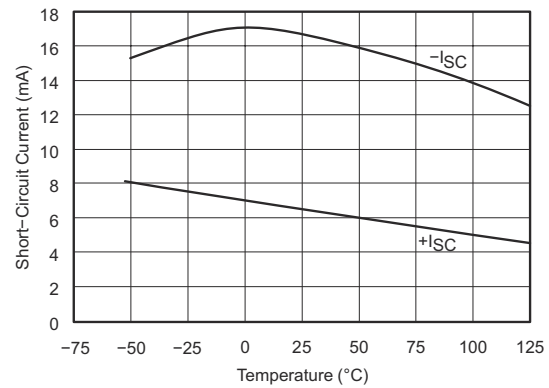
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)



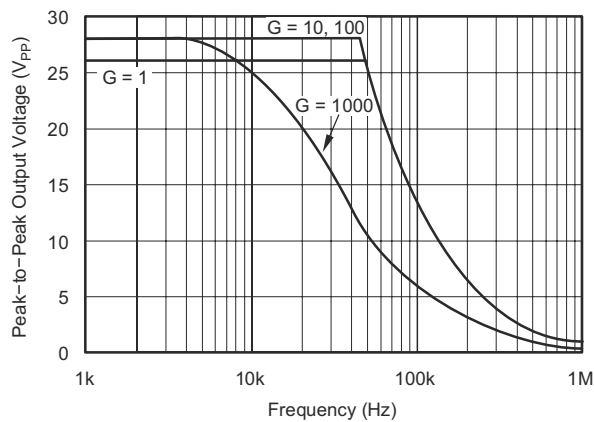
CSO: SHE

Figure 6-25. Output Voltage Swing vs Power Supply Voltage



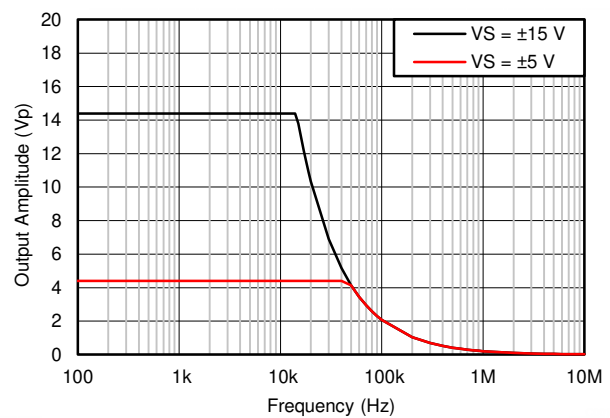
CSO: SHE

Figure 6-26. Short Circuit Output Current vs Temperature



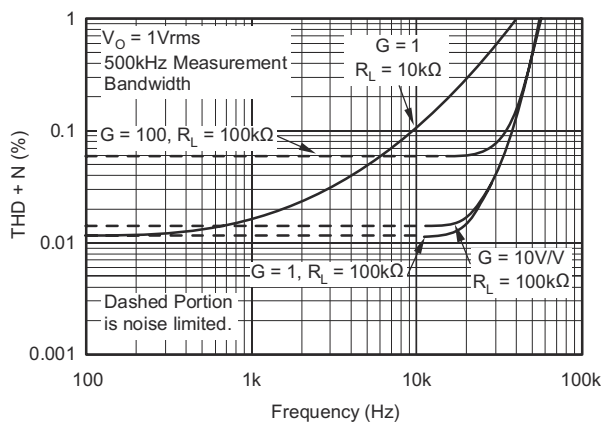
CSO: SHE

Figure 6-27. Maximum Output Voltage vs Frequency



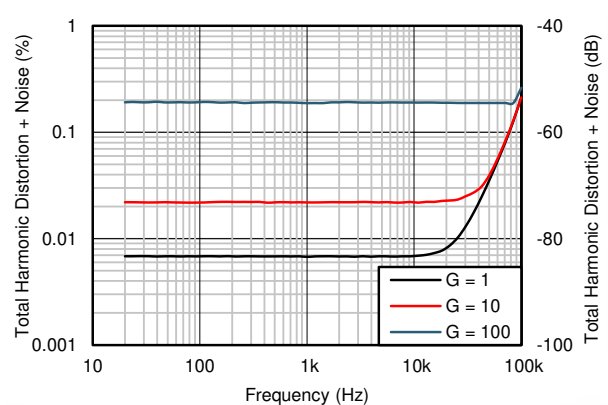
CSO: FRE

Figure 6-28. Maximum Output Voltage vs Frequency



CSO: SHE

Figure 6-29. Total Harmonic Distortion + Noise vs Frequency



CSO: FRE

Figure 6-30. Total Harmonic Distortion + Noise vs Frequency

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)

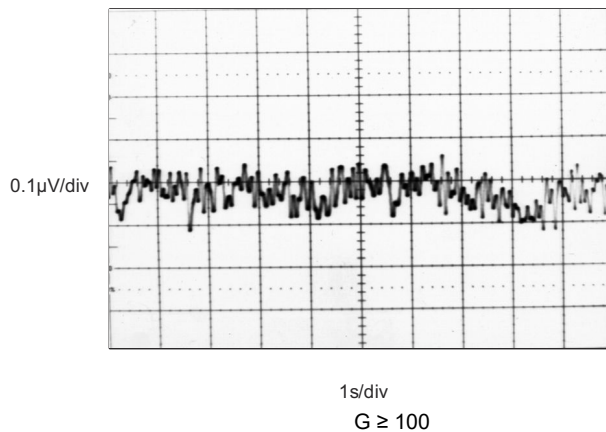


Figure 6-31. 0.1 to 10Hz Input-Referred Voltage Noise

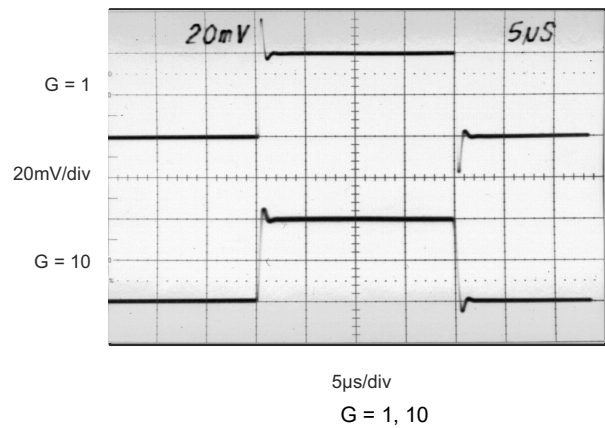


Figure 6-32. Small Signal

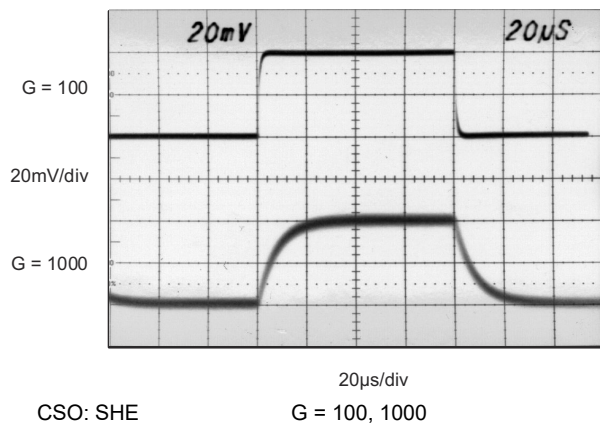


Figure 6-33. Small Signal

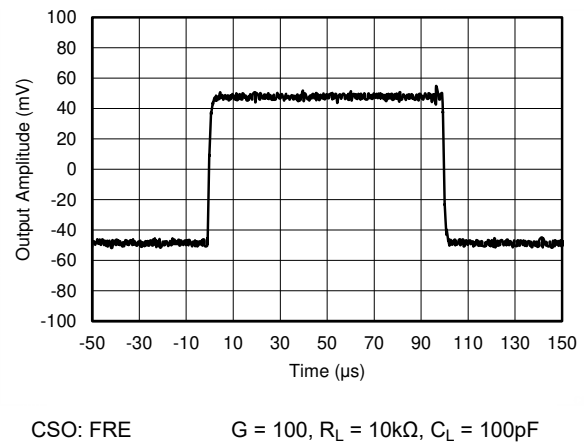


Figure 6-34. Small Signal

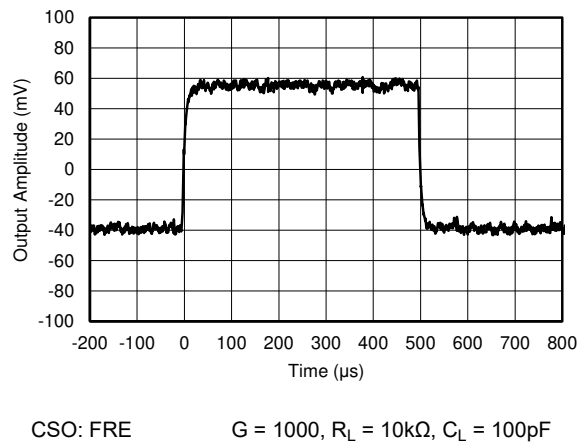


Figure 6-35. Small Signal

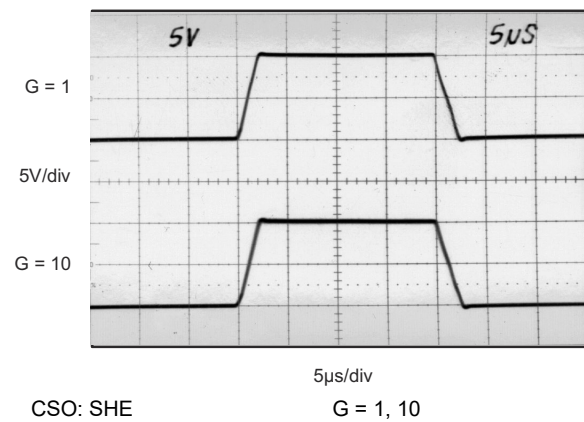


Figure 6-36. Large Signal

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $V_{\text{CM}} = V_S / 2$ , and  $G = 1$ , all chips site origins (CSO) (unless otherwise noted)

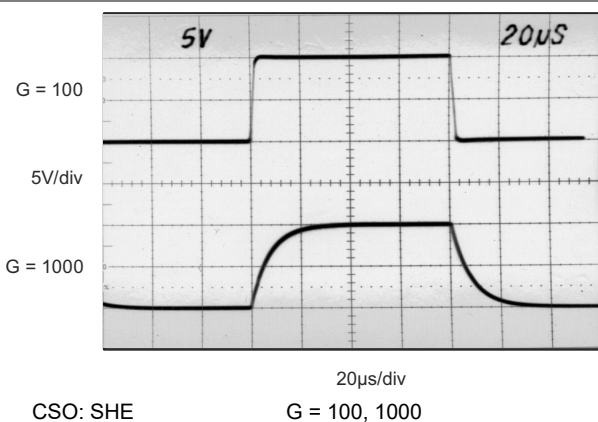


Figure 6-37. Large Signal

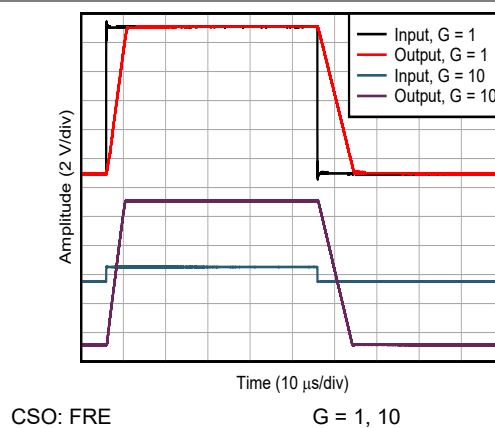


Figure 6-38. Large Signal

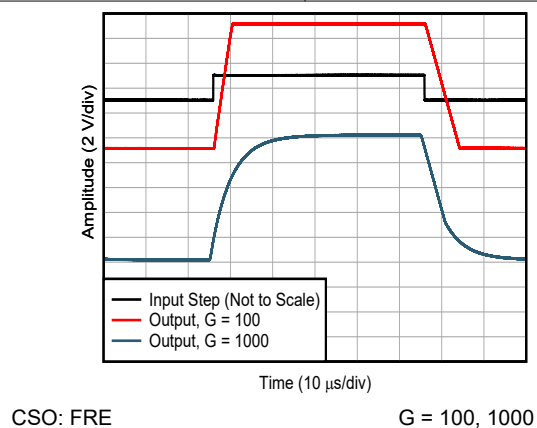


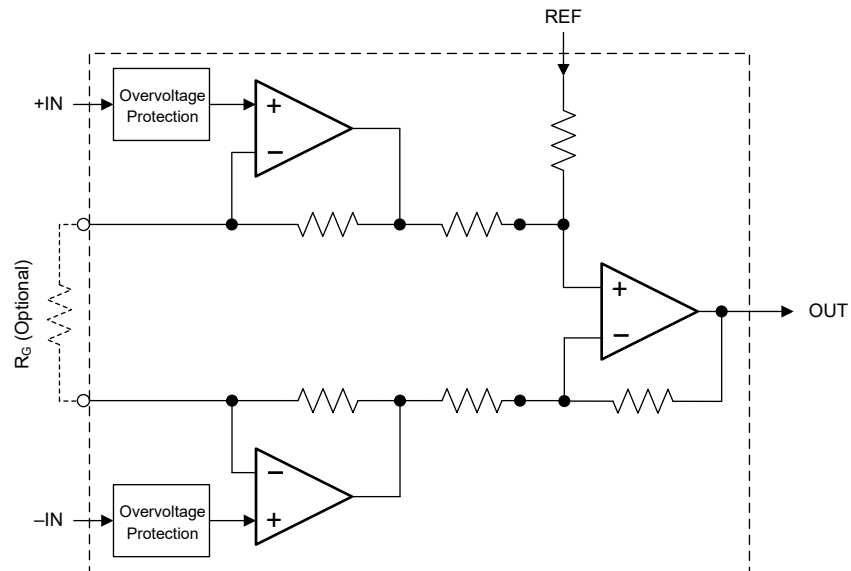
Figure 6-39. Large Signal

## 7 Detailed Description

### 7.1 Overview

The INA128 and INA129 (INA12x) instrumentation amplifiers are outfitted with an input protection circuit and input buffer amplifiers. These features eliminate the need for input impedance matching and make the amplifier an excellent choice for use in measurement and test equipment. Additional characteristics of the INA12x include a very-low dc offset, low drift, low noise, very-high open-loop gain, very-high common-mode rejection ratio, and very-high input impedances. The INA12x is used where great accuracy and stability of the circuit, both short and long term, are required.

### 7.2 Functional Block Diagram

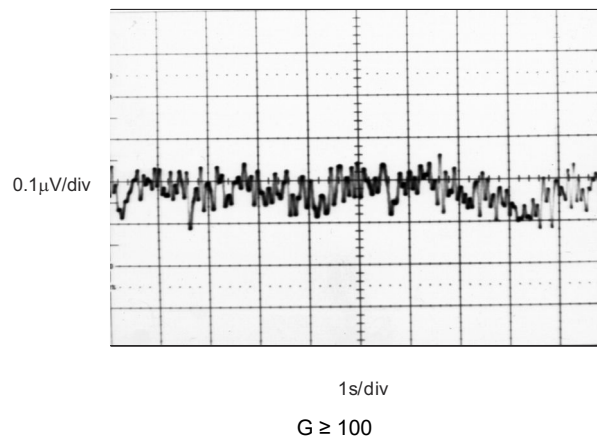


## 7.3 Feature Description

The INA12x are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-op-amp design and small size make the amplifiers an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA12x are laser trimmed for very low offset voltage (25 $\mu$ V typical) and high common-mode rejection (93dB at  $G \geq 100$ ). These devices operate with power supplies as low as  $\pm 2.25$ V, and a quiescent current of 2mA, typically. The internal input protection can withstand up to  $\pm 40$ V without damage, as shown in [Figure 6-17](#).

### 7.3.1 Noise Performance

The INA12x provide very low noise in most applications. Low-frequency noise is approximately 0.2 $\mu$ V<sub>PP</sub> measured from 0.1 to 10Hz ( $G \geq 100$ ). This feature provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.



**Figure 7-1. 0.1Hz to 10Hz Input-Referred Voltage Noise**

## 7.4 Device Functional Modes

The INA12x have a single functional mode and operate when the power-supply voltage is greater than 4.5V ( $\pm 2.25$ V). The maximum power-supply voltage for the INA12x is 36V ( $\pm 18$ V).

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 8.1 Application Information

The INA12x measure a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The high input-voltage protection circuit in conjunction with high input impedance make the INA12x an excellent choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

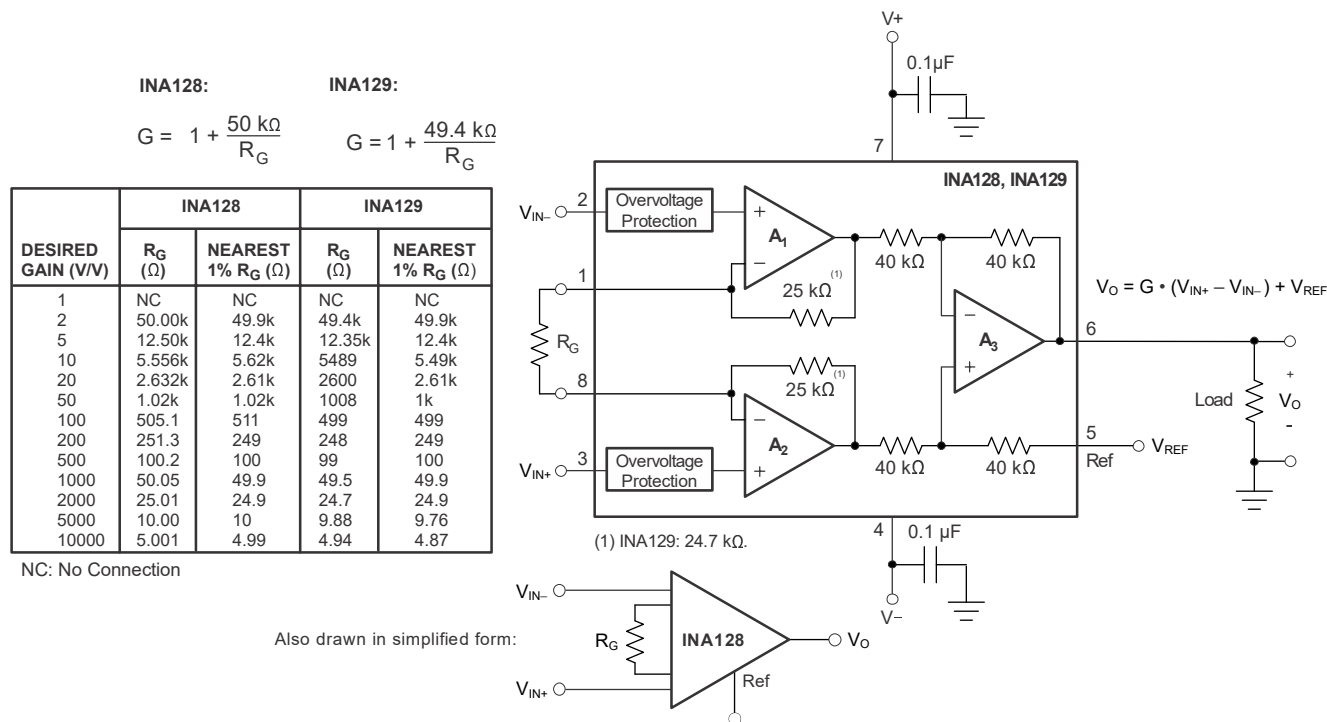
#### 8.1.1 Input Common-Mode Range

The linear input voltage range of the INA12x input circuitry ranges from approximately 2V less than the positive supply voltage to 2V greater than the negative supply. A differential input voltage causes the output voltage to increase; however, the linear input range is limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on the supply voltage (see [Figure 6-10](#)).

Input overload can produce an output voltage that appears normal. For example, if an input-overload condition drives both input amplifiers to the positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of  $A_3$  is near 0V even though both inputs are overloaded.

## 8.2 Typical Application

Figure 8-1 shows the basic connections required for operation of the INA12x. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 8Ω in series with the REF pin causes a typical device to degrade to approximately 80 dB CMR ( $G = 1$ ).



**Figure 8-1. Basic Connections**

### 8.2.1 Design Requirements

The devices are configured to monitor the input differential voltage when the input signal gain is set by the external resistor,  $R_G$ . The output signal is developed with respect to the voltage on the reference pin, REF. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground, as Figure 8-1 shows. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5V in a 5V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level shift the output so that the device can drive a single-supply ADC.

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider is used to generate a reference voltage, the voltage must be buffered by an op amp to avoid CMRR degradation.

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Setting the Gain

The gain (G) is set by connecting a single external resistor,  $R_G$ , between pins 1 and 8:

$$\text{INA128: } G = 1 + 50\text{k}\Omega / R_G \quad (1)$$

$$\text{INA129: } G = 1 + 49.4\text{k}\Omega / R_G \quad (2)$$

Commonly used gains and resistor values are shown in [Figure 8-1](#).

The 50k $\Omega$  term in [Equation 1](#) and the 49.4k $\Omega$  term in [Equation 2](#) come from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip metal film resistors are laser trimmed to accurate, absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications in the *Electrical Characteristics* table.

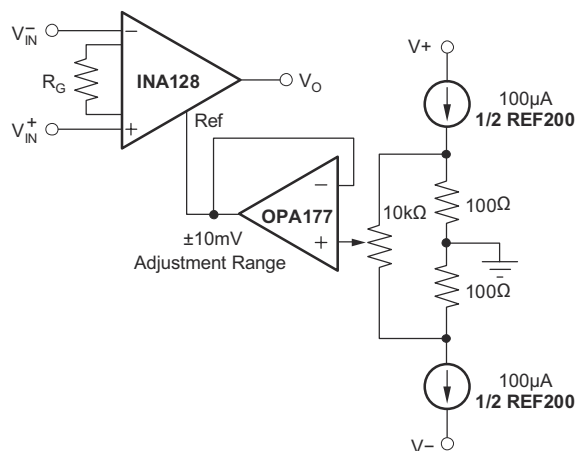
The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The contribution of  $R_G$  to gain accuracy and drift can be directly inferred from [Equation 1](#) and [Equation 2](#). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

### 8.2.2.2 Dynamic Performance

The typical performance curve in [Figure 6-2](#) shows that despite low quiescent current, the INA12x achieve wide bandwidth even at high gain. This performance is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

### 8.2.2.3 Offset Trimming

The INA12x is laser trimmed for low-offset voltage and low offset voltage drift. Most applications require no external offset adjustment. [Figure 8-2](#) shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed with the output. The op-amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.



**Figure 8-2. Optional Trimming of Output Offset Voltage**

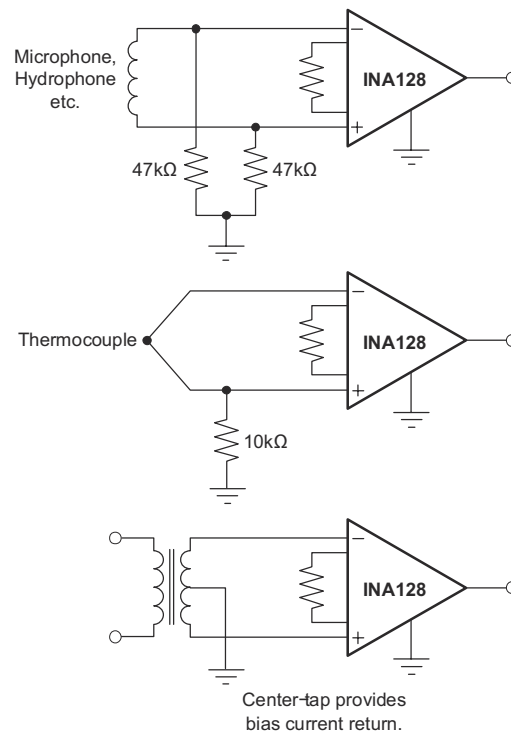
#### 8.2.2.4 Input Bias Current Return Path

The input impedance of the INA12x is extremely high: approximately 10GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 8-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range, and the input amplifiers saturate.

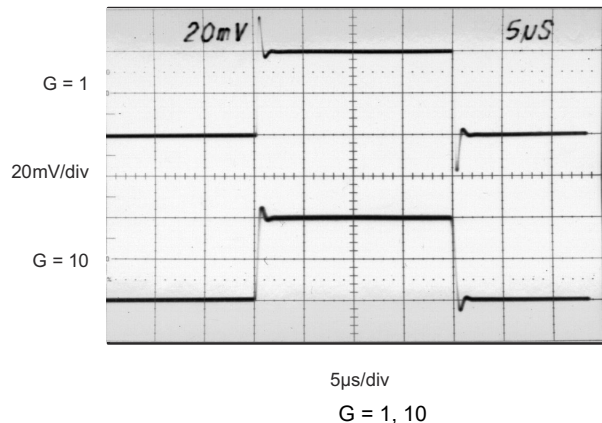
If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 8-3). With higher source impedance, use two equal resistors to provide a balanced input, with possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

For more details about why a valid input bias current return path is necessary, see the [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications](#) application note.

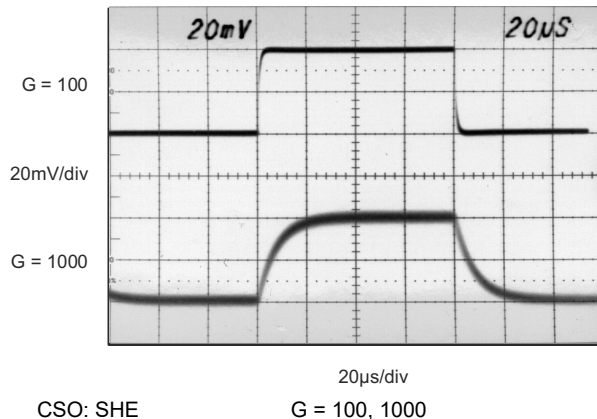


**Figure 8-3. Providing an Input Common-Mode Current Path**

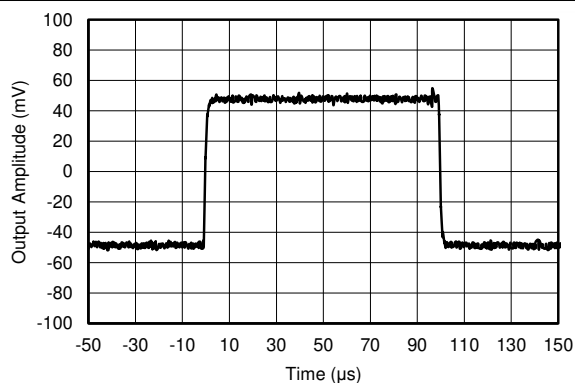
## 8.2.3 Application Curves



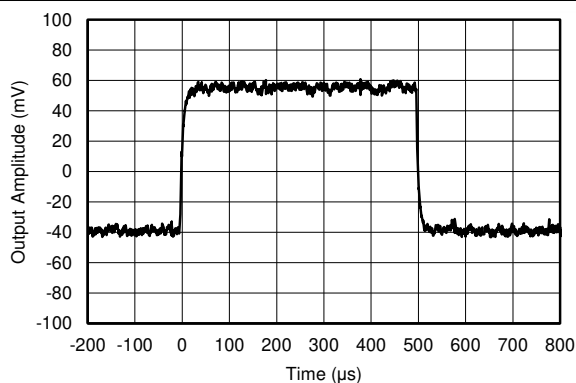
**Figure 8-4. Small Signal**



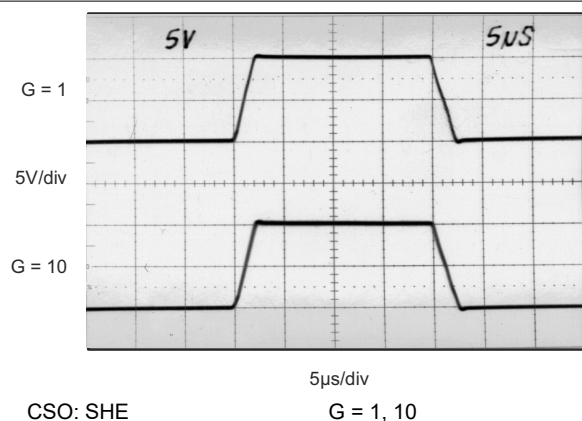
**Figure 8-5. Small Signal**



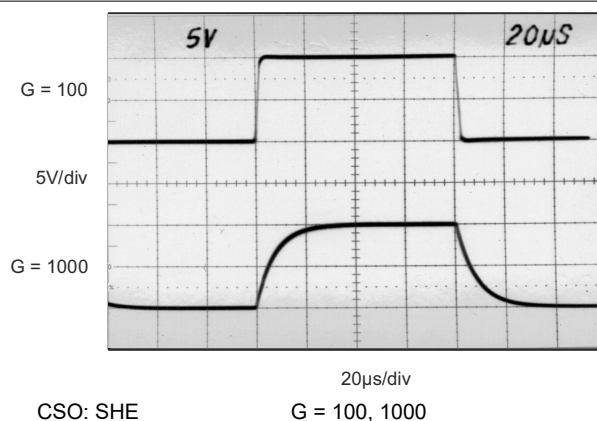
**Figure 8-6. Small Signal**



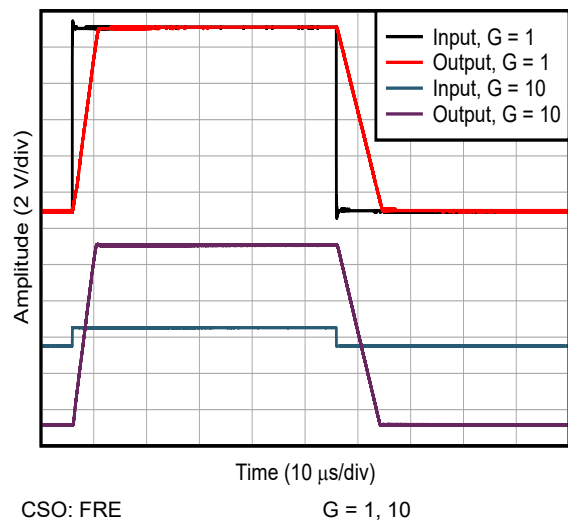
**Figure 8-7. Small Signal**



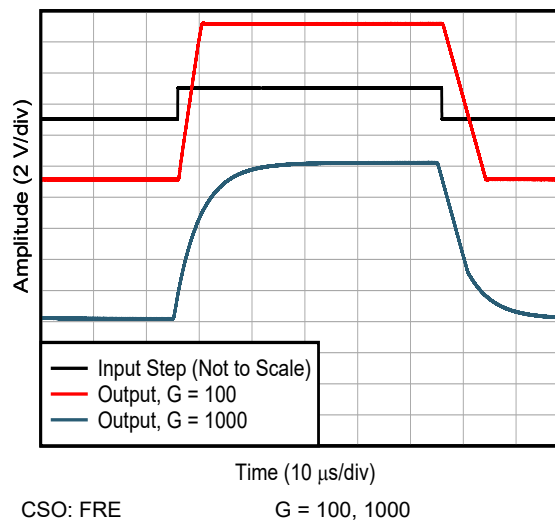
**Figure 8-8. Large Signal**



**Figure 8-9. Large Signal**

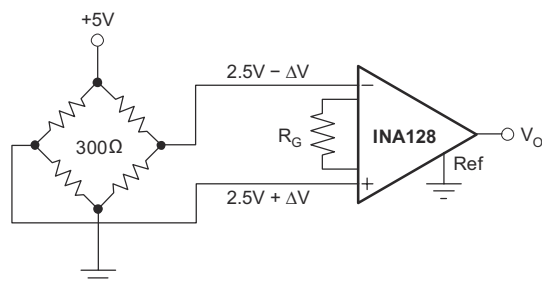


**Figure 8-10. Large Signal**

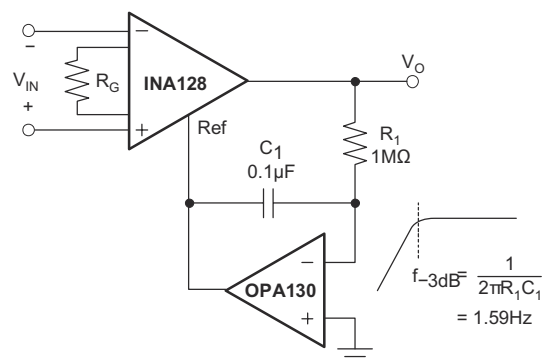


**Figure 8-11. Large Signal**

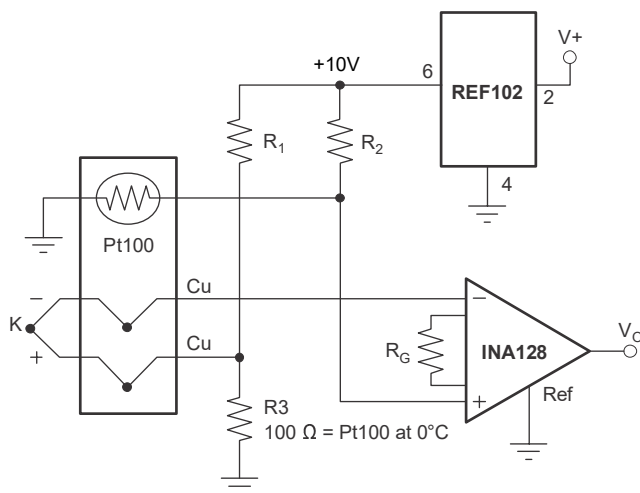
## 8.3 System Examples



**Figure 8-12. Bridge Amplifier**



**Figure 8-13. AC-Coupled Instrumentation Amplifier**



| ISA TYPE | MATERIAL                  | SEEBECK COEFFICIENT (μV/°C) | R1, R2  |
|----------|---------------------------|-----------------------------|---------|
| E        | + Chromel<br>- Constantan | 58.5                        | 66.5 kΩ |
| J        | + Iron<br>- Constantan    | 50.2                        | 76.8 kΩ |
| K        | + Chromel<br>- Alumel     | 39.4                        | 97.6 kΩ |
| T        | + Copper<br>- Constantan  | 38.0                        | 102 kΩ  |

**Figure 8-14. Thermocouple Amplifier With RTD Cold-Junction Compensation**

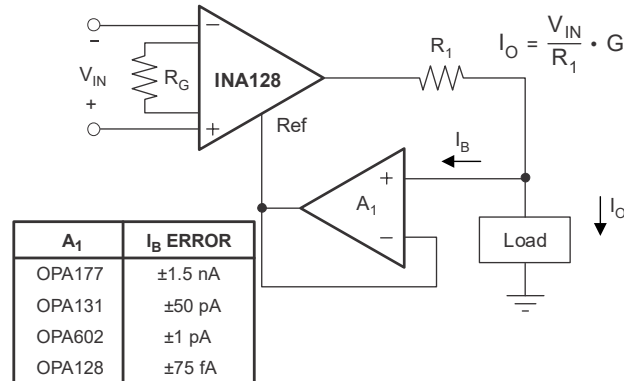


Figure 8-15. Differential Voltage to Current Converter

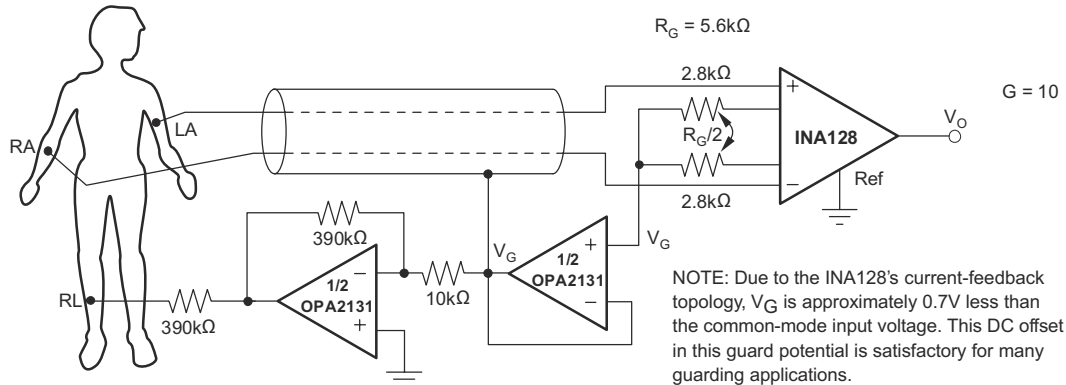


Figure 8-16. ECG Amplifier With Right-Leg Drive

## 8.4 Power Supply Recommendations

The minimum power supply voltage for INA12x is  $\pm 2.25\text{V}$  and the maximum power supply voltage is  $\pm 18\text{V}$ . This minimum and maximum range covers a wide range of power supplies; but for optimum performance,  $\pm 15\text{V}$  is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

### 8.4.1 Low-Voltage Operation

The INA12x operate on power supplies as low as  $\pm 2.25\text{V}$ . Performance remains excellent with power supplies ranging from  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$ . Most parameters vary only slightly throughout this supply voltage range; see [Section 6.6](#).

Operation at very-low supply voltages requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. [Figure 6-10](#) shows the range of linear operation for  $\pm 15\text{V}$ ,  $\pm 5\text{V}$ , and  $\pm 2.5\text{V}$  supplies.

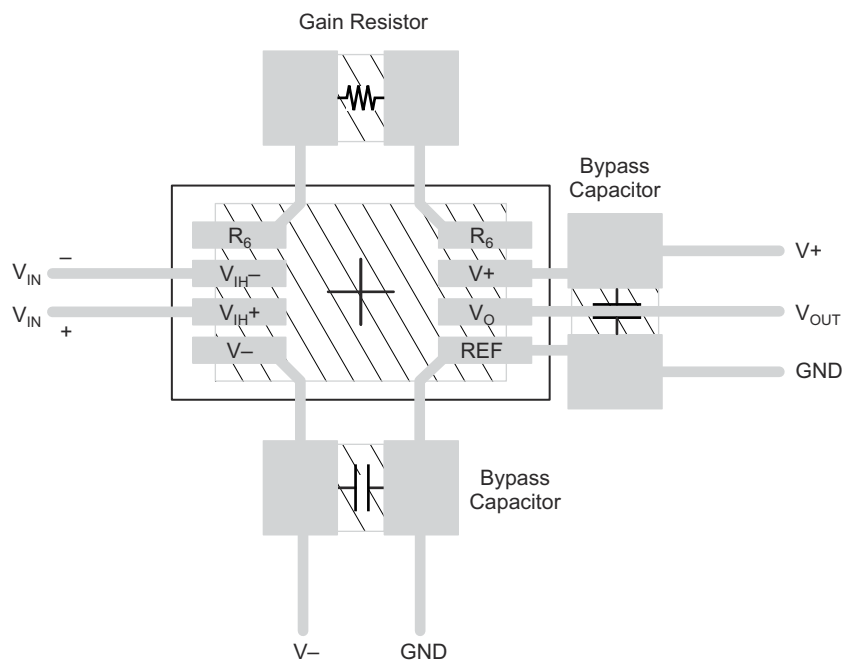
## 8.5 Layout

### 8.5.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is  $0.1\mu\text{F}$  to  $1\mu\text{F}$ . If necessary, add more decoupling capacitance to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x devices.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the devices.

## 8.5.2 Layout Example



**Figure 8-17. Recommended Layout**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

| PART NUMBER                                                          | DEFINITION                                       |
|----------------------------------------------------------------------|--------------------------------------------------|
| INA12xU<br>INA12xU/2K5<br>INA12xU/2K51G4<br>INA12xUA<br>INA12xUA/2K5 | The die is manufactured in CSO: SHE or CSO: FRE. |
| INA12xP<br>INA12xPA                                                  | The die is manufactured in CSO: SHE.             |

#### 9.1.2 Development Support

##### 9.1.2.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

##### 9.1.2.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design and simulation tools](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

#### Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers application note](#)
- Texas Instruments, [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications application note](#)

## 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 9.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

All trademarks are the property of their respective owners.

## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (May 2022) to Revision G (January 2026)                                                                                                                                                                                                                                                                                                                                                                                                                  | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added different fabrication process specifications for Input bias current in the <i>Features</i> section.....                                                                                                                                                                                                                                                                                                                                                                  | 1    |
| • Added description of device flow information in the <i>Specifications</i> .....                                                                                                                                                                                                                                                                                                                                                                                                | 4    |
| • Added all chips site origins (CSO) condition to the typical test conditions in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                     | 5    |
| • Added different fabrication process specifications for Offset voltage (RTI) in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                     | 5    |
| • Added different fabrication process specifications for Power-supply rejection ratio (RTI) in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                       | 5    |
| • Added different fabrication process specifications for Long-term stability in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                      | 5    |
| • Added different fabrication process specifications for Common-mode rejection ratio in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                              | 5    |
| • Added different fabrication process specifications for Input bias current in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                       | 5    |
| • Added different fabrication process specifications for Input offset current in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                     | 5    |
| • Added different fabrication process specifications for Voltage noise (RTI) in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                      | 5    |
| • Added different fabrication process specifications for Current noise in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                            | 5    |
| • Added different fabrication process specifications for Gain error in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                               | 5    |
| • Added different fabrication process specifications for Gain drift in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                               | 5    |
| • Added different fabrication process specifications for Positive output voltage swing in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                            | 5    |
| • Added different fabrication process specifications for Negative output voltage swing in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                            | 5    |
| • Added different fabrication process specifications for Short-circuit current in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                    | 5    |
| • Added different fabrication process specifications for Bandwidth, –3dB in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                          | 5    |
| • Added different fabrication process specifications for Slew rate in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                                | 5    |
| • Added different fabrication process specifications for Settling time in the <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                            | 5    |
| • Added all <i>chips site origins</i> (CSO) condition to the typical test conditions in the <i>Typical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                 | 9    |
| • Added CSO: SHE to <i>Common-Mode Rejection vs Frequency</i> , <i>Positive Power Supply Rejection vs Frequency</i> , <i>Input-Referred Noise vs Frequency</i> , <i>Settling Time vs Gain</i> , <i>Input Bias Current vs Temperature</i> , <i>Output Voltage Swing vs Output Current</i> , <i>Output Voltage Swing vs Power Supply Voltage</i> , <i>Short Circuit Output Current vs Temperature</i> , and <i>Small Signal</i> curves in the <i>Typical Characteristics</i> ..... | 9    |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| • Added CSO: FRE to <i>Gain vs Frequency</i> , <i>Negative Power Supply Rejection vs Frequency</i> , <i>Input Overvoltage V/I Characteristics</i> , <i>Maximum Output Voltage vs Frequency</i> , <i>Total Harmonic Distortion + Noise vs Frequency</i> , and <i>Large Signal</i> curves in the <i>Typical Characteristics</i> .....                                                                                                                                                                               | 9  |
| • Added <i>Gain vs Frequency</i> , <i>Input-Referred Noise vs Frequency</i> , <i>Positive Power Supply Rejection vs Frequency</i> , <i>Negative Power Supply Rejection vs Frequency</i> , <i>Input Overvoltage V/I Characteristics</i> , <i>Maximum Output Voltage vs Frequency</i> , <i>Total Harmonic Distortion + Noise vs Frequency</i> , and <i>Large Signal</i> curves for CSO: SHE in the <i>Typical Characteristics</i> .....                                                                             | 9  |
| • Added <i>Common-Mode Rejection vs Frequency</i> , <i>Positive Power Supply Rejection vs Frequency</i> , <i>Input-Referred Voltage Noise vs Frequency</i> , <i>Input-Referred Current Noise vs Frequency</i> , <i>Input Bias Current vs Temperature</i> , <i>Input Offset Current vs Temperature</i> , <i>Positive Output Voltage Swing vs Output Current</i> , <i>Negative Output Voltage Swing vs Output Current</i> , and <i>Small Signal</i> curves for CSO: FRE in the <i>Typical Characteristics</i> ..... | 9  |
| • Updated the <i>Gain vs Frequency</i> curve for CSO: FRE in the <i>Typical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                                                                             | 9  |
| • Updated the <i>Positive Power Supply Rejection vs Frequency</i> curve for CSO: SHE in the <i>Typical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                                                  | 9  |
| • Added CSO: SHE to <i>Small Signal</i> curves in the <i>Application Curves</i> .....                                                                                                                                                                                                                                                                                                                                                                                                                             | 22 |
| • Added CSO: FRE to <i>Large Signal</i> curves in the <i>Application Curves</i> .....                                                                                                                                                                                                                                                                                                                                                                                                                             | 22 |
| • Added <i>Large Signal</i> curves for CSO: SHE in the <i>Application Curves</i> .....                                                                                                                                                                                                                                                                                                                                                                                                                            | 22 |
| • Added <i>Small Signal</i> curves for CSO: FRE in the <i>Application Curves</i> .....                                                                                                                                                                                                                                                                                                                                                                                                                            | 22 |
| • Added part number flow information table to the <i>Device Nomenclature</i> .....                                                                                                                                                                                                                                                                                                                                                                                                                                | 27 |

| <b>Changes from Revision E (April 2019) to Revision F (May 2022)</b>                                                                                                                                                                                  | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....                                                                                                                                                 | 1           |
| • Added bandwidth and noise specifications in <i>Features</i> .....                                                                                                                                                                                   | 1           |
| • Changed <i>Applications</i> to link to latest end-equipment solutions on ti.com.....                                                                                                                                                                | 1           |
| • Changed reference from INA819 to INA818 in <i>Device Comparison Table</i> .....                                                                                                                                                                     | 3           |
| • Added single supply specification to <i>Absolute Maximum Ratings</i> .....                                                                                                                                                                          | 4           |
| • Added note clarifying output short-circuit "to ground" in <i>Absolute Maximum Ratings</i> refers to short-circuit to $V_S / 2$ .....                                                                                                                | 4           |
| • Added single supply specification to <i>Recommended Operating Conditions</i> .....                                                                                                                                                                  | 4           |
| • Changed input common-mode voltage range specification from $V - 2$ to $(V-) + 2$ in <i>Recommended Operating Conditions</i> .....                                                                                                                   | 4           |
| • Deleted INA128-HT and INA129-HT operating temperature specifications from <i>Recommended Operating Conditions</i> .....                                                                                                                             | 4           |
| • Added specified temperature range to <i>Recommended Operating Conditions</i> .....                                                                                                                                                                  | 4           |
| • Added $V_{REF} = 0\text{ V}$ , $V_{CM} = V_S / 2$ , and $G = 1$ to "unless otherwise noted" conditions in <i>Electrical Characteristics</i> and <i>Typical Characteristics</i> for clarity.....                                                     | 5           |
| • Changed test condition for offset voltage drift specification in <i>Electrical Characteristics</i> from " $T_A = T_{MIN}$ to $T_{MAX}$ " to " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " for clarity.....                                   | 5           |
| • Changed typical long-term stability specification from $\pm 0.1 \pm 3/G\text{ }\mu\text{V/mo}$ to $\pm 0.2 \pm 3/G\text{ }\mu\text{V/mo}$ in <i>Electrical Characteristics</i> .....                                                                | 5           |
| • Changed common-mode voltage specification from $(V-) + 2\text{ V}$ minimum and $(V+) - 2\text{ V}$ minimum across two rows to $(V-) + 2\text{ V}$ minimum and $(V+) - 2\text{ V}$ maximum across one row in <i>Electrical Characteristics</i> ..... | 5           |
| • Deleted typical common-mode voltage specifications in <i>Electrical Characteristics</i> .....                                                                                                                                                       | 5           |
| • Added test condition of " $R_S = 0\Omega$ " to safe input voltage specification in <i>Electrical Characteristics</i> for clarity....                                                                                                                | 5           |
| • Added test condition of " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " to input bias current drift specification in <i>Electrical Characteristics</i> for clarity.....                                                                        | 5           |
| • Added test condition of " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " to input offset current drift specification in <i>Electrical Characteristics</i> for clarity.....                                                                      | 5           |
| • Changed maximum gain error specification for INA128PA/UA and INA129PA/UA with $G = 1$ from $\pm 0.01\%$ to $\pm 0.1\%$ in <i>Electrical Characteristics</i> .....                                                                                   | 5           |
| • Added test condition of " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " for gain drift in <i>Electrical Characteristics</i> for clarity.....                                                                                                   | 5           |

|                                                                                                                                                                                                                                  |    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| • Changed parameter names from "Voltage - Positive" to "Positive output voltage swing" and from "Voltage - Negative" to "Negative output voltage swing" in <i>Electrical Characteristics</i> .....                               | 5  |
| • Deleted typical positive and negative output voltage swing specifications in <i>Electrical Characteristics</i> .....                                                                                                           | 5  |
| • Added test condition of "Continuous to $V_S / 2$ " to short-circuit current specification in <i>Electrical Characteristics</i> for clarity.....                                                                                | 5  |
| • Changed typical bandwidth specification for $G = 10$ from 700kHz to 640kHz in <i>Electrical Characteristics</i> .....                                                                                                          | 5  |
| • Changed typical slew rate specification from 4V/ $\mu$ s to 1.2V/ $\mu$ s in <i>Electrical Characteristics</i> .....                                                                                                           | 5  |
| • Changed typical settling time specification for $G = 1$ , $G = 10$ , and $G = 100$ from 7 $\mu$ s, 7 $\mu$ s, and 9 $\mu$ s respectively to 12 $\mu$ s, 12 $\mu$ s, and 12 $\mu$ s, in <i>Electrical Characteristics</i> ..... | 5  |
| • Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from <i>Electrical Characteristics</i> .....                                                                  | 5  |
| • Changed Figures 7-1, 7-3, 7-4, 7-9, 7-10, 7-11, 7-16, 7-17, 7-20, 7-21.....                                                                                                                                                    | 9  |
| • Changed values discussed in <i>Input Common-Mode Range</i> from typical input common-mode voltage range values to maximum and minimum values.....                                                                              | 18 |
| • Changed Figure 9-1 to fix missing text and include reference voltage.....                                                                                                                                                      | 19 |
| • Added more detailed guidance concerning REF pin in <i>Design Requirements</i> .....                                                                                                                                            | 19 |
| • Changed Figures 9-6, 9-7.....                                                                                                                                                                                                  | 22 |
| • Changed Figures 9-10 and 9-11 to fix missing text.....                                                                                                                                                                         | 24 |
| • Added <i>Related Documentation</i> links to <i>Device and Documentation Support</i> .....                                                                                                                                      | 27 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)    | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|-----------------|---------------------|
| <a href="#">INA128P</a>      | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -               | INA128P             |
| INA128P.A                    | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -40 to 125      | INA128P             |
| <a href="#">INA128PA</a>     | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -               | INA128P<br>A        |
| INA128PA.A                   | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -40 to 125      | INA128P<br>A        |
| INA128PG4                    | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | See INA128P     | INA128P             |
| <a href="#">INA128U</a>      | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -               | INA<br>128U         |
| INA128U.B                    | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125      | INA<br>128U         |
| <a href="#">INA128U/2K5</a>  | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -               | INA<br>128U         |
| INA128U/2K5.B                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -40 to 125      | INA<br>128U         |
| INA128U/2K51G4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -40 to 125      | INA<br>128U         |
| INA128U/2K51G4.B             | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -40 to 125      | INA<br>128U         |
| INA128U/2K5G4                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Call TI                           | See INA128U/2K5 |                     |
| <a href="#">INA128UA</a>     | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125      | INA<br>128U<br>A    |
| INA128UA.B                   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125      | INA<br>128U<br>A    |
| <a href="#">INA128UA/2K5</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125      | INA<br>128U<br>A    |
| INA128UA/2K5.B               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125      | INA<br>128U<br>A    |
| INA128UA/2K5G4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Call TI                           | -40 to 125      |                     |

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| INA128UAG4                   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | -           | Call TI                              | Call TI                           | -40 to 125   |                     |
| <a href="#">INA129P</a>      | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -            | INA129P             |
| INA129P.A                    | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -40 to 125   | INA129P             |
| <a href="#">INA129PA</a>     | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -            | INA129P<br>A        |
| INA129PA.A                   | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | Call TI                              | N/A for Pkg Type                  | -40 to 125   | INA129P<br>A        |
| <a href="#">INA129U</a>      | Active        | Production           | SOIC (D)   8   | 75   TUBE             | -           | Call TI                              | Level-3-260C-168 HR               | -            | INA<br>129U<br>S    |
| INA129U.B                    | Active        | Production           | SOIC (D)   8   | 75   TUBE             | -           | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | INA<br>129U<br>S    |
| <a href="#">INA129U/2K5</a>  | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -            | INA<br>129U<br>S    |
| INA129U/2K5.B                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | -           | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | INA<br>129U<br>S    |
| INA129U/2K5G4                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA<br>129U<br>S    |
| INA129U/2K5G4.B              | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | INA<br>129U<br>S    |
| <a href="#">INA129UA</a>     | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | INA<br>129U<br>A    |
| INA129UA.B                   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | INA<br>129U<br>A    |
| <a href="#">INA129UA/2K5</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | INA<br>129U<br>A    |

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| INA129UA/2K5.B        | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | INA<br>129U<br>A    |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## OTHER QUALIFIED VERSIONS OF INA128, INA129 :

- Enhanced Product : [INA129-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INA128U/2K5    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| INA128U/2K51G4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| INA128UA/2K5   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| INA129U/2K5    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| INA129U/2K5G4  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| INA129UA/2K5   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| INA128U/2K5    | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| INA128U/2K51G4 | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| INA128UA/2K5   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| INA129U/2K5    | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| INA129U/2K5G4  | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| INA129UA/2K5   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

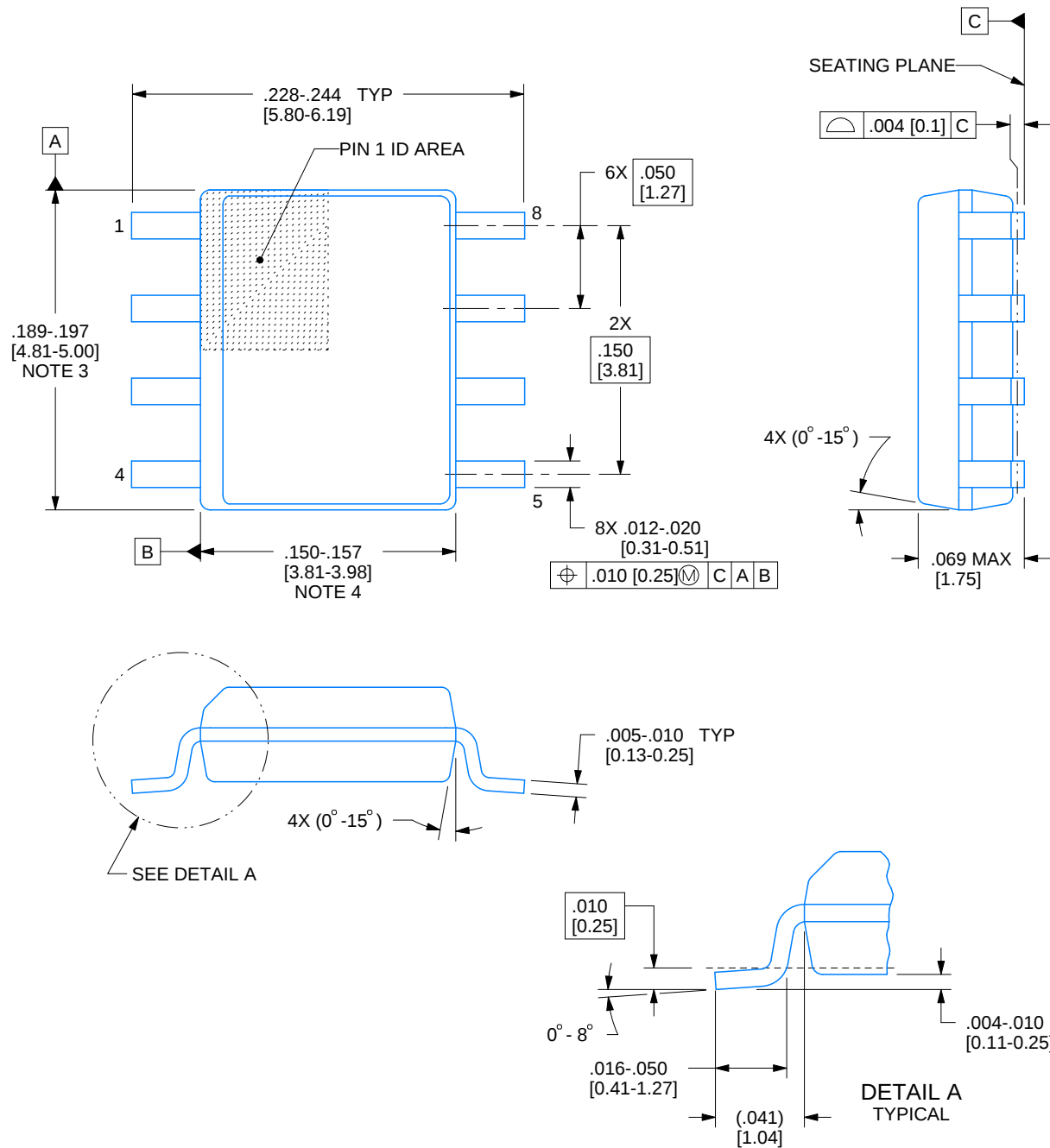
| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| INA128P    | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128P    | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128P.A  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128P.A  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128PA   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128PA   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128PA.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128PA.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128PG4  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128PG4  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA128U    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA128U.B  | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA128UA   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA128UA.B | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA129P    | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA129P.A  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA129PA   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA129PA.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| INA129U    | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA129U.B  | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA129UA   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| INA129UA.B | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |

**D0008A**

## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

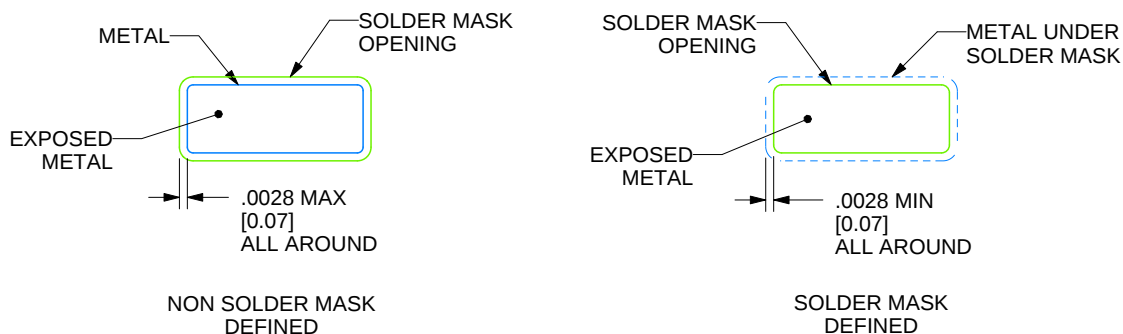
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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