

# CSD87334Q3D Synchronous Buck NexFET™ Power Block

## 1 Features

- Half-Bridge Power Block
- Optimized for High-Duty Cycle
- Up to 24 V<sub>in</sub>
- 96.1% System Efficiency at 12 A
- 1.6-W P<sub>LOSS</sub> at 12 A
- Up to 20-A Operation
- High-Frequency Operation (up to 1.5 MHz)
- High-Density SON 3.3 mm × 3.3 mm Footprint
- Optimized for 5-V Gate Drive
- Low-Switching Losses
- Ultra-Low-Inductance Package
- RoHS Compliant
- Halogen-Free
- Lead-Free Terminal Plating

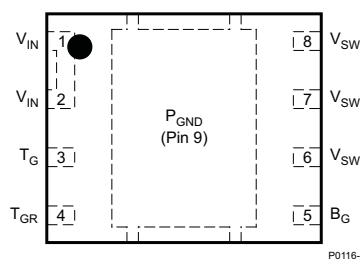
## 2 Applications

- Synchronous Buck Converters
  - High-Frequency Applications
  - High-Duty Cycle Applications
- Synchronous Boost Converters
- POL DC-DC Converters

## 3 Description

The CSD87334Q3D NexFET™ power block is an optimized design for synchronous buck and boost applications offering high-current, high-efficiency, and high-frequency capability in a small 3.3 mm × 3.3 mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution in high-duty cycle applications when paired with an external controller or driver.

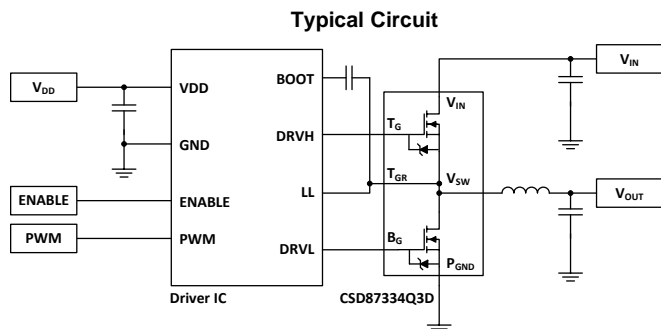
TOP VIEW



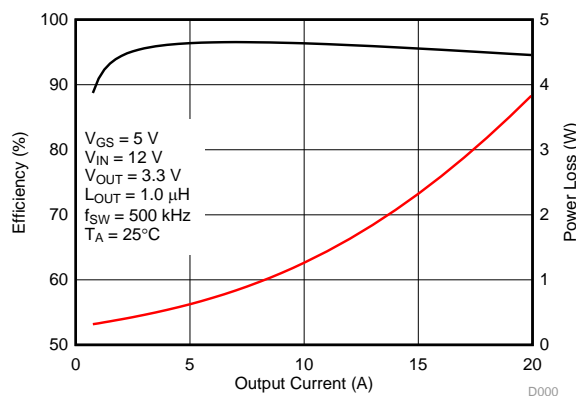
Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD87334Q3D	2500	13-Inch Reel	SON	Tape and Reel
CSD87334Q3DT	250	7-Inch Reel	3.30-mm × 3.30-mm Plastic Package	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Power Block Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>7 Layout</b> .....	<b>12</b>
<b>2 Applications</b> .....	<b>1</b>	7.1 Layout Guidelines .....	12
<b>3 Description</b> .....	<b>1</b>	7.2 Layout Example .....	13
<b>4 Revision History</b> .....	<b>2</b>	7.3 Thermal Considerations .....	13
<b>5 Specifications</b> .....	<b>3</b>	<b>8 Device and Documentation Support</b> .....	<b>14</b>
5.1 Absolute Maximum Ratings .....	3	8.1 Receiving Notification of Documentation Updates..	14
5.2 Recommended Operating Conditions .....	3	8.2 Community Resources .....	14
5.3 Power Block Performance .....	3	8.3 Trademarks .....	14
5.4 Thermal Information .....	3	8.4 Electrostatic Discharge Caution .....	14
5.5 Electrical Characteristics .....	4	8.5 Glossary .....	14
5.6 Typical Power Block Device Characteristics .....	5	<b>9 Mechanical, Packaging, and Orderable</b>	
5.7 Typical Power Block MOSFET Characteristics .....	7	<b>Information</b> .....	<b>15</b>
<b>6 Application and Implementation</b> .....	<b>9</b>	9.1 Q3D Package Dimensions .....	15
6.1 Application Information .....	9	9.2 Land Pattern Recommendation .....	16
6.2 Typical Application .....	9	9.3 Stencil Recommendation .....	17
6.3 System Example .....	9	9.4 Q3D Tape and Reel Information .....	17

## 4 Revision History

Changes from Original (August 2015) to Revision A	Page
• Changed $T_G$ to $T_{GR}$ minimum voltage, from $-8\text{ V}$ : to $-0.3\text{ V}$ in <i>Absolute Maximum Ratings</i> table .....	3
• Changed $B_G$ to $P_{GND}$ minimum voltage, from $-8\text{ V}$ : to $-0.3\text{ V}$ in <i>Absolute Maximum Ratings</i> table .....	3
• Changed $I_{GSS}$ test condition for $V_{GS}$ , from $+10 / -8\text{ V}$ : to $10\text{ V}$ in <i>Electrical Characteristics</i> table .....	4
• Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section to <i>Device and Documentation Support</i> section .....	14

## 5 Specifications

### 5.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$  (unless otherwise noted) (see <sup>(1)</sup>)

		MIN	MAX	UNIT
Voltage	$V_{IN}$ to $P_{GND}$		30	V
	$V_{SW}$ to $P_{GND}$		30	
	$V_{SW}$ to $P_{GND}$ (10 ns)		32	
	$T_G$ to $T_{GR}$	-0.3	10	
	$B_G$ to $P_{GND}$	-0.3	10	
$I_{DM}$	Pulsed current rating		60	A
$P_D$	Power dissipation		6	W
$E_{AS}$	Avalanche energy	Sync FET, $I_D = 31$ A, $L = 0.1$ mH	48	mJ
		Control FET, $I_D = 31$ A, $L = 0.1$ mH	48	
$T_J$	Operating junction temperature	-55	150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		MIN	MAX	UNIT
$V_{GS}$	Gate drive voltage	3.3	8	V
$V_{IN}$	Input supply voltage		24	V
$f_{SW}$	Switching frequency	$C_{BST} = 0.1$ $\mu\text{F}$ (min)	1500	kHz
	Operating current		20	A
$T_J$	Operating temperature		125	$^\circ\text{C}$

### 5.3 Power Block Performance

 $T_A = 25^\circ\text{C}$  (unless otherwise noted) (see <sup>(1)</sup>)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{LOSS}$	Power loss <sup>(1)</sup>	$V_{IN} = 12$ V, $V_{GS} = 5$ V, $V_{OUT} = 3.3$ V, $I_{OUT} = 12$ A, $f_{SW} = 500$ kHz, $L_{OUT} = 1$ $\mu\text{H}$ , $T_J = 25^\circ\text{C}$		1.6		W
$I_{QVIN}$	$V_{IN}$ quiescent current	$T_G$ to $T_{GR} = 0$ V $B_G$ to $P_{GND} = 0$ V			10	$\mu\text{A}$

(1) Measurement made with six 10- $\mu\text{F}$  (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across  $V_{IN}$  to  $P_{GND}$  pins and using a high current 5-V driver IC.

### 5.4 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) <sup>(1)</sup>			130	$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance (max Cu) <sup>(1)(2)</sup>			75	
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) <sup>(1)</sup>			21	$^\circ\text{C}/\text{W}$
	Junction-to-case thermal resistance ( $P_{GND}$ pin) <sup>(1)</sup>			2.1	

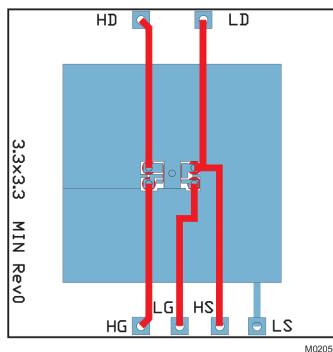
(1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in  $\times$  1.5-in (3.81-cm  $\times$  3.81-cm), 0.06-in (1.52-mm) thick FR4 board.  $R_{\theta JC}$  is specified by design while  $R_{\theta JA}$  is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>) Cu.

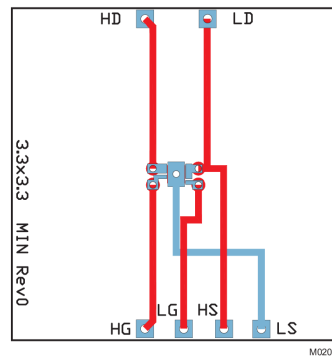
## 5.5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER	TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>STATIC CHARACTERISTICS</b>									
$V_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$			30			V	
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1			$\mu\text{A}$	
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 10\text{ V}$			100			nA	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$			0.75	0.90	1.20	V	
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 3.5\text{ V}, I_{DS} = 12\text{ A}$			6.3	8.3	6.3	8.3	
		$V_{GS} = 4.5\text{ V}, I_{DS} = 12\text{ A}$			5.6	7.0	5.6	7.0	
		$V_{GS} = 8\text{ V}, I_{DS} = 12\text{ A}$			4.9	6.0	4.9	6.0	
$g_{fs}$	Transconductance	$V_{DS} = 15\text{ V}, I_{DS} = 12\text{ A}$			62			S	
<b>DYNAMIC CHARACTERISTICS</b>									
$C_{ISS}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$			971	1260	971	1260	pF
$C_{OSS}$	Output capacitance				453	589	453	589	pF
$C_{RSS}$	Reverse transfer capacitance				16	21	16	21	pF
$R_G$	Series gate resistance	$V_{DS} = 15\text{ V}, I_{DS} = 12\text{ A}$			1.0	2.0	1.0	2.0	$\Omega$
$Q_g$	Gate charge total (4.5 V)				6.4	8.3	6.4	8.3	nC
$Q_{gd}$	Gate charge gate-to-drain				1.0		1.0		nC
$Q_{gs}$	Gate charge gate-to-source	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 12\text{ A}, R_G = 2\ \Omega$			1.9		1.9		nC
$Q_{g(th)}$	Gate charge at $V_{th}$				0.9		0.9		nC
$Q_{OSS}$	Output charge	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$			10.5			nC	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 12\text{ A}, R_G = 2\ \Omega$			4			ns	
$t_r$	Rise time				7			ns	
$t_{d(off)}$	Turnoff delay time				11			ns	
$t_f$	Fall time				17			ns	
<b>DIODE CHARACTERISTICS</b>									
$V_{SD}$	Diode forward voltage	$I_{DS} = 12\text{ A}, V_{GS} = 0\text{ V}$			0.8	1.0	0.8	1.0	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 15\text{ V}, I_F = 12\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$			23			nC	
$t_{rr}$	Reverse recovery Time	$V_{DS} = 15\text{ V}, I_F = 12\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$			18			ns	



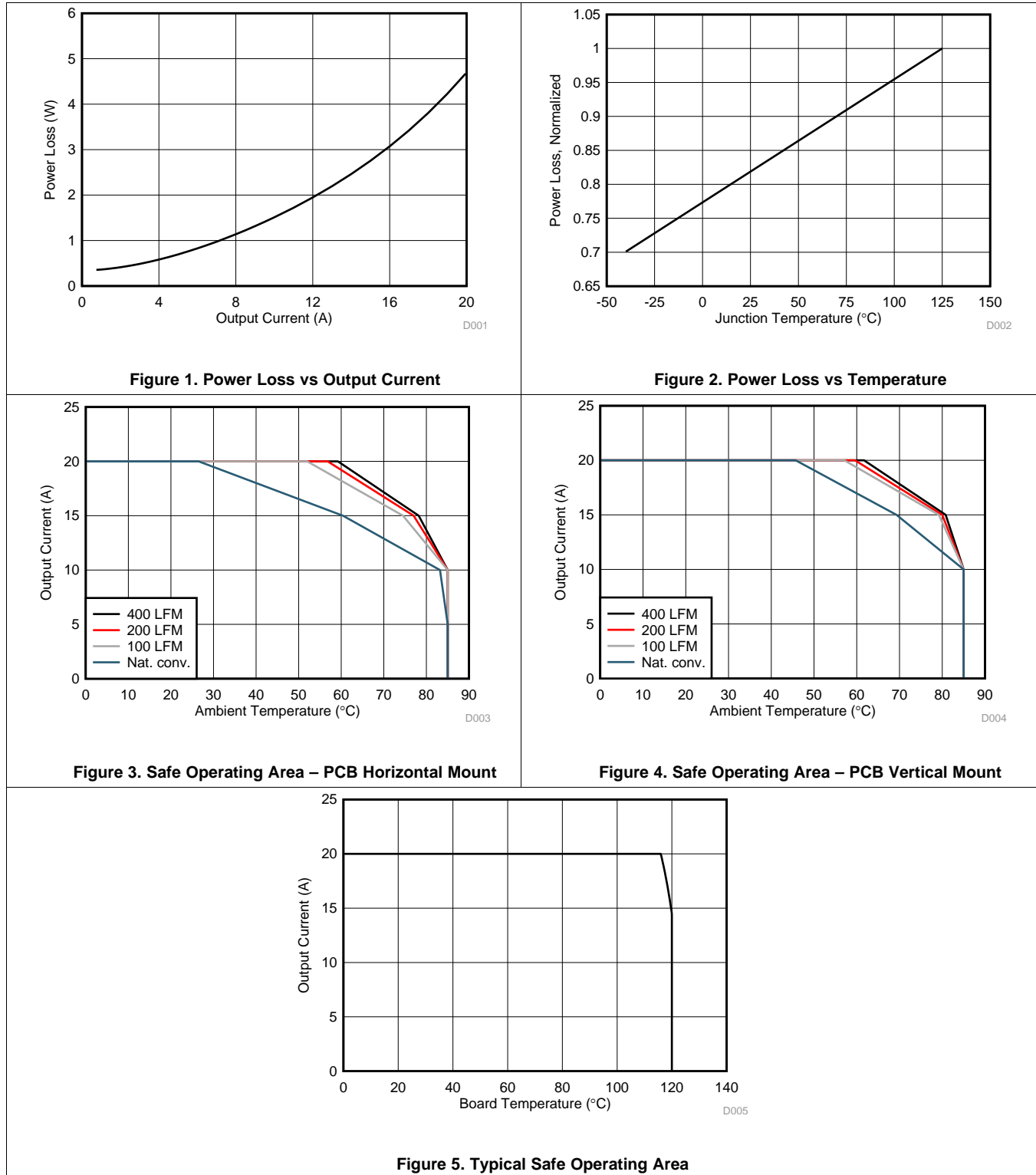
Max  $R_{\theta JA} = 75^\circ\text{C}/\text{W}$   
when mounted on 1 in<sup>2</sup>  
(6.45 cm<sup>2</sup>) of 2-oz  
(0.071-mm) thick Cu.



Max  $R_{\theta JA} = 130^\circ\text{C}/\text{W}$   
when mounted on  
minimum pad area of  
2-oz (0.071-mm) thick  
Cu.

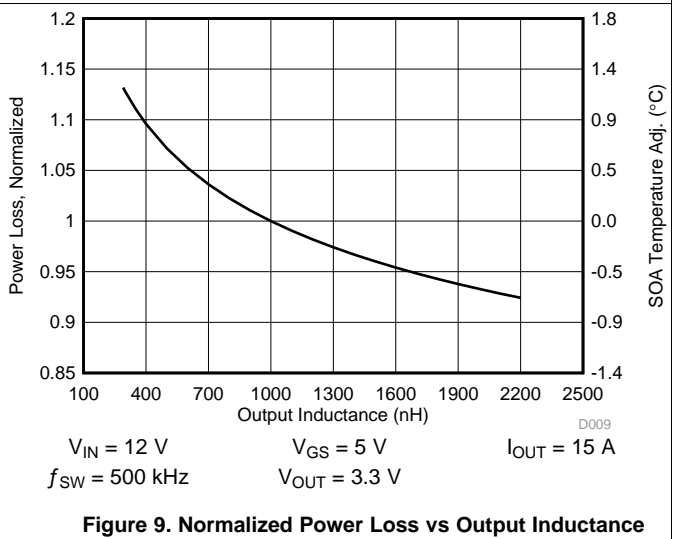
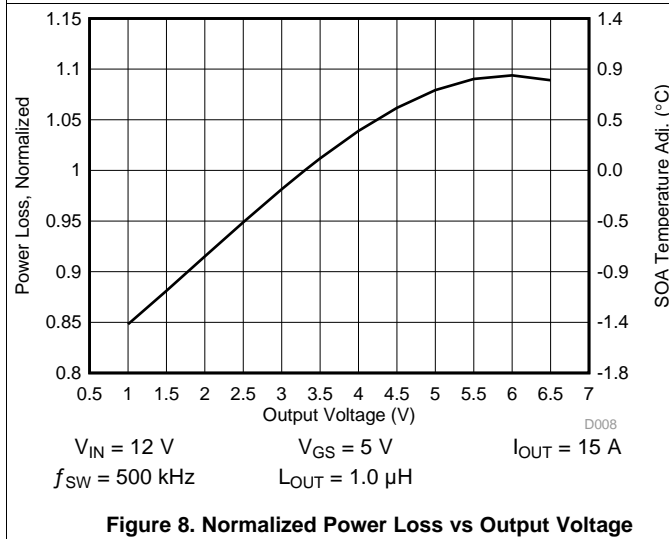
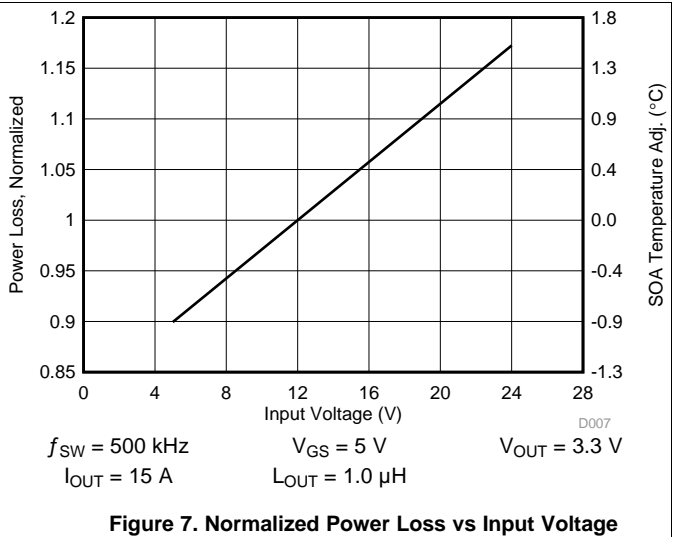
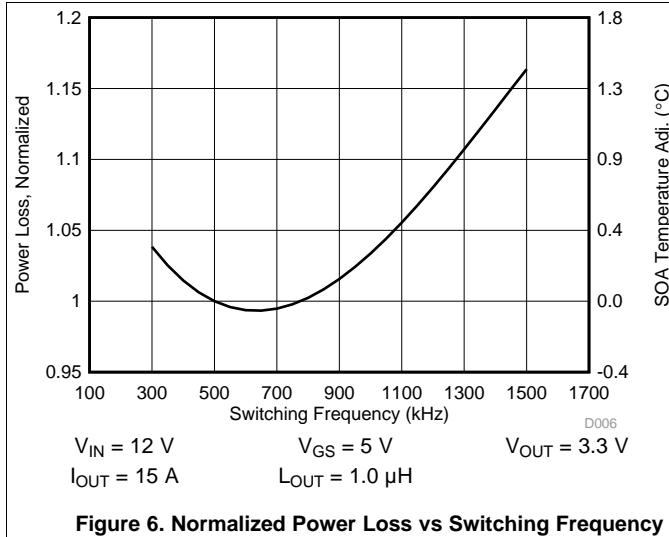
## 5.6 Typical Power Block Device Characteristics

The typical power block system characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See [Application and Implementation](#) for detailed explanation. Conditions for Figure 1 through Figure 5 are given by the following;  $V_{IN} = 12\text{ V}$ ,  $V_{GS} = 5\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 500\text{ kHz}$ ,  $L_{OUT} = 1\text{ }\mu\text{H}$ .  $T_A = 125^\circ\text{C}$ , unless stated otherwise.



### Typical Power Block Device Characteristics (continued)

The typical power block system characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See [Application and Implementation](#) for detailed explanation. Conditions for Figure 1 through Figure 5 are given by the following;  $V_{IN} = 12\text{ V}$ ,  $V_{GS} = 5\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 500\text{ kHz}$ ,  $L_{OUT} = 1\text{ }\mu\text{H}$ ,  $T_A = 125^\circ\text{C}$ , unless stated otherwise.



### 5.7 Typical Power Block MOSFET Characteristics

$T_A = 25^\circ\text{C}$ , unless stated otherwise.

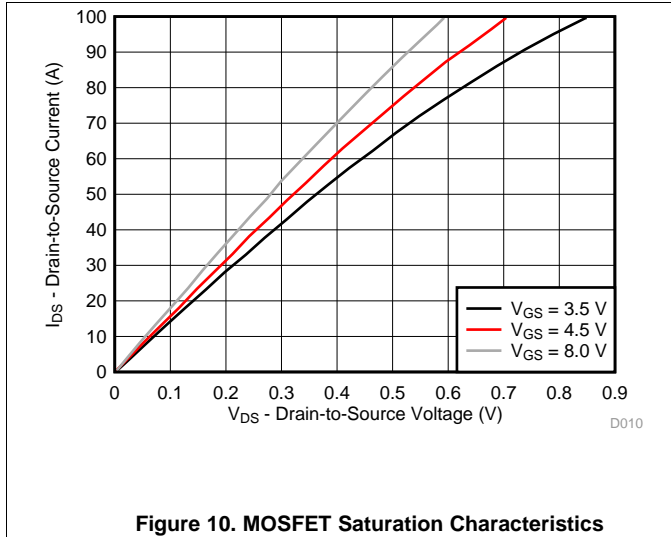


Figure 10. MOSFET Saturation Characteristics

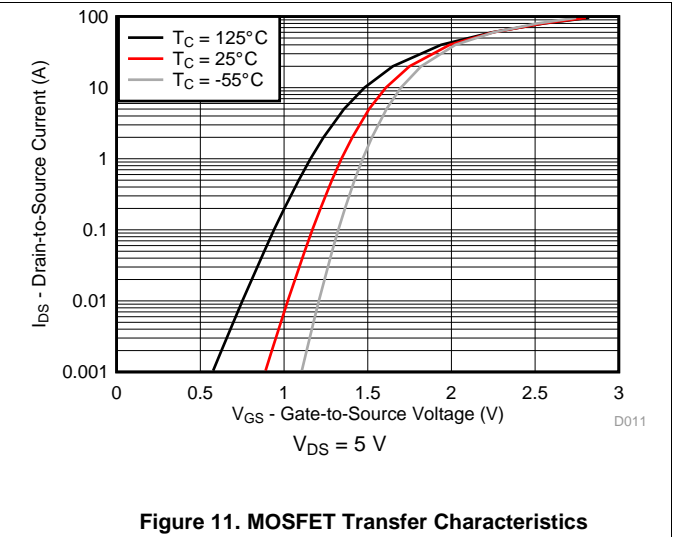


Figure 11. MOSFET Transfer Characteristics

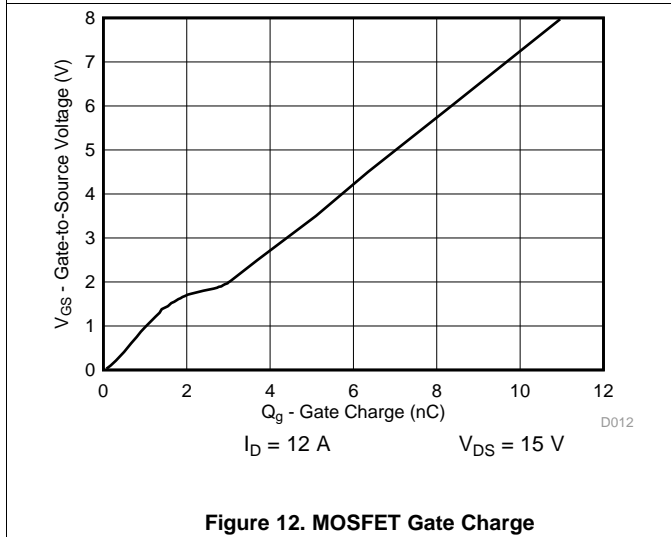


Figure 12. MOSFET Gate Charge

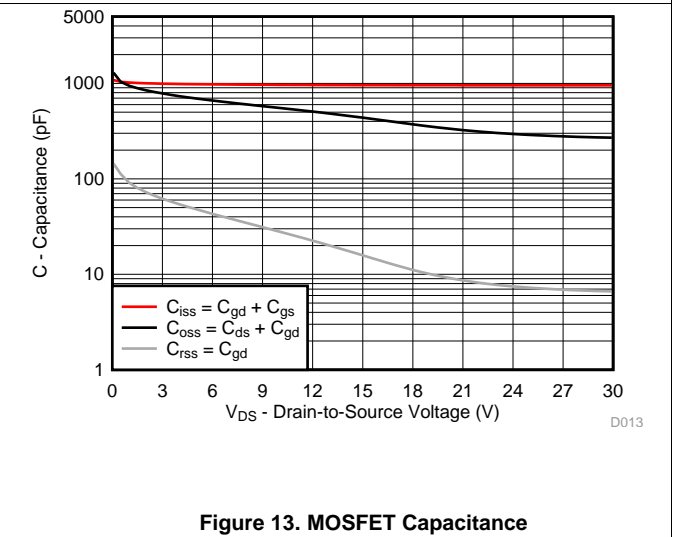


Figure 13. MOSFET Capacitance

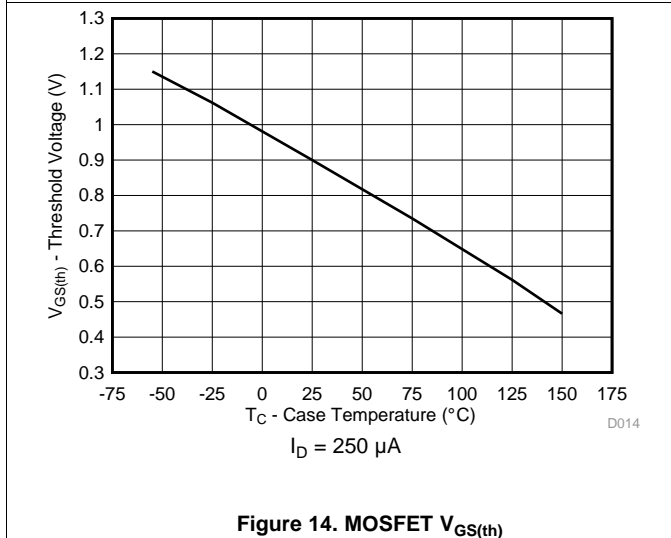


Figure 14. MOSFET  $V_{GS(th)}$

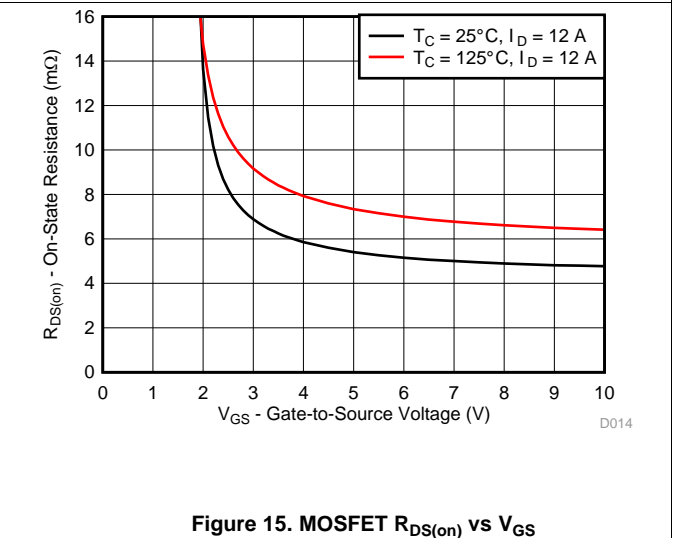


Figure 15. MOSFET  $R_{DS(on)}$  vs  $V_{GS}$

Typical Power Block MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ , unless stated otherwise.

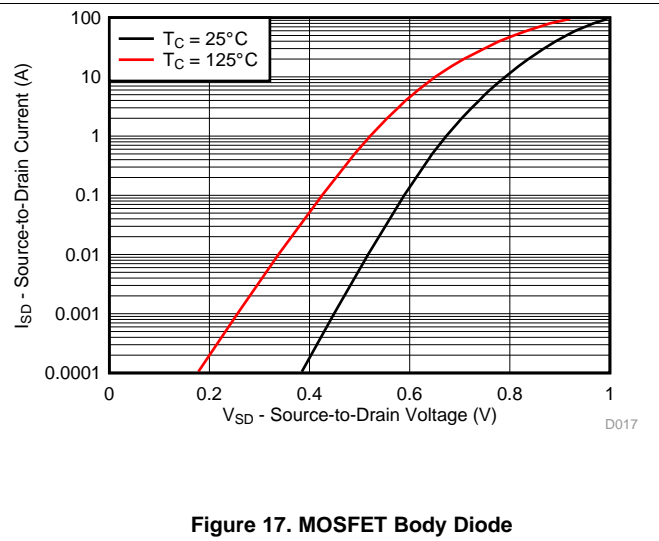
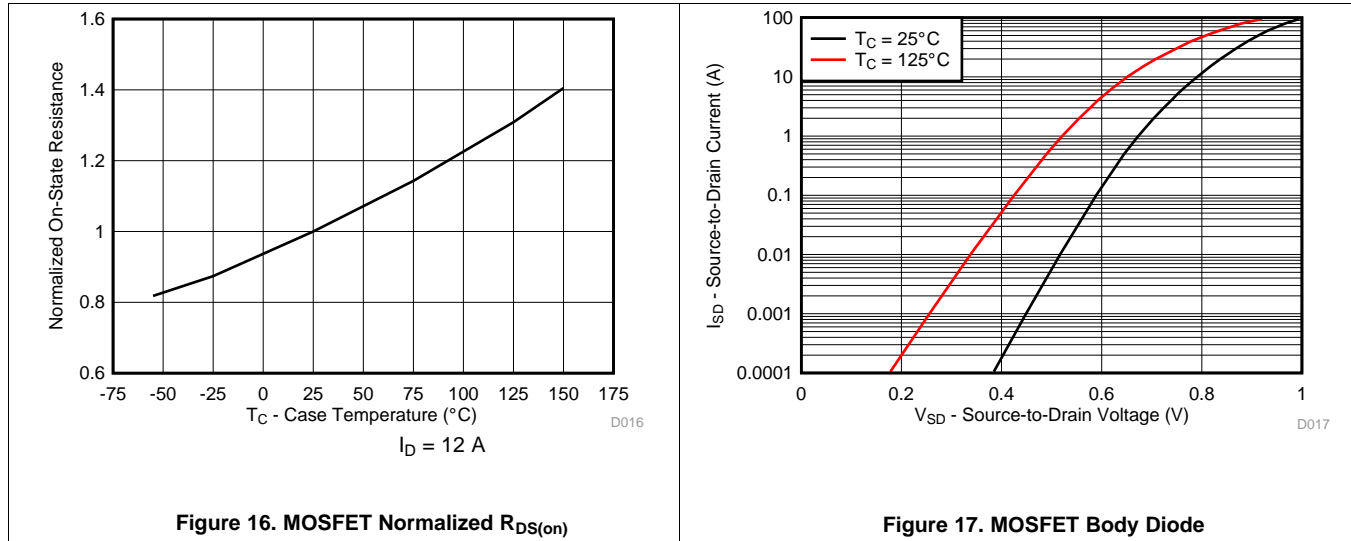


Figure 16. MOSFET Normalized  $R_{DS(on)}$

Figure 17. MOSFET Body Diode

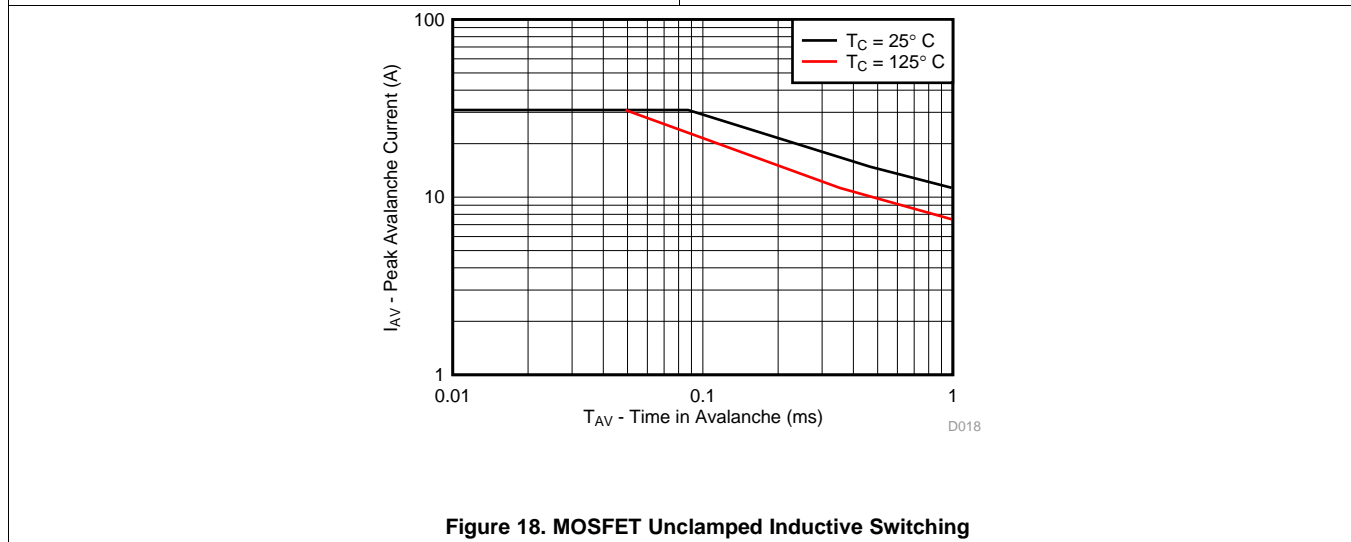


Figure 18. MOSFET Unclamped Inductive Switching



## 6 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 6.1 Application Information

The CSD87334Q3D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

### 6.2 Typical Application

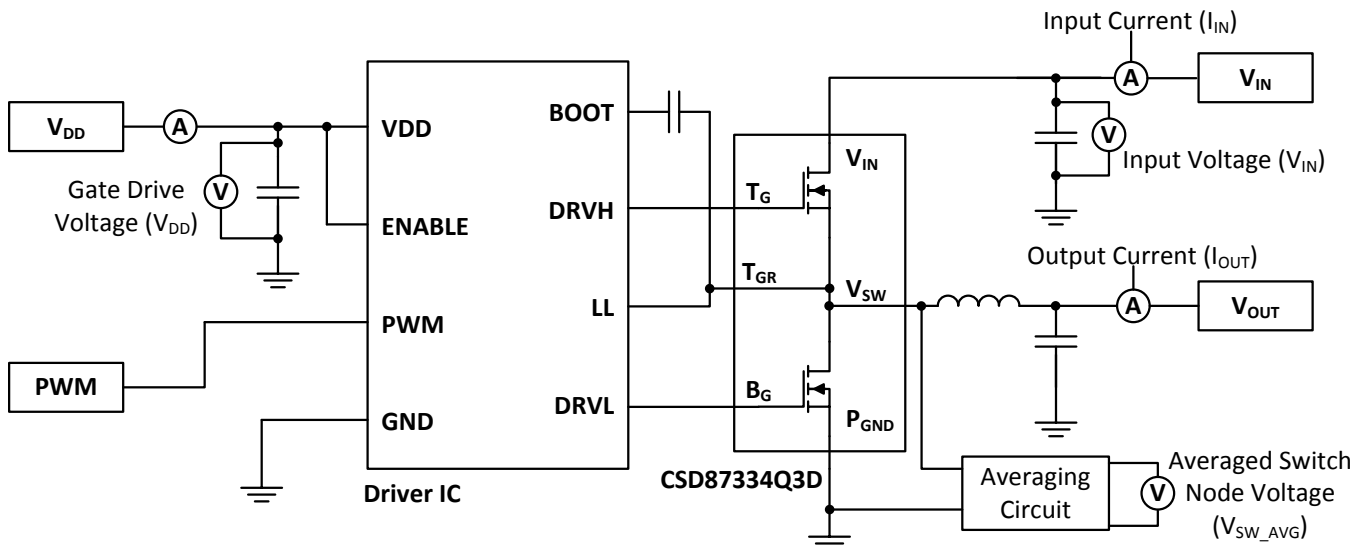


Figure 19. Typical Circuit Application

### 6.3 System Example

#### 6.3.1 Power Loss Curves

MOSFET centric parameters such as  $R_{DS(ON)}$  and  $Q_{gd}$  are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87334Q3D as a function of load current. This curve is measured by configuring and running the CSD87334Q3D as it would be in the final application (see Figure 19). The measured power loss is the CSD87334Q3D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

## System Example (continued)

### 6.3.2 Safe Operating Area (SOA) Curves

The SOA curves in the CSD87334Q3D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. [Figure 3](#) to [Figure 5](#) outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the SOA. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

### 6.3.3 Normalized Curves

The normalized curves in the CSD87334Q3D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss, and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

### 6.3.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see [Design Example](#) section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

#### 6.3.4.1 Design Example

Operating conditions:

- Output current = 15 A
- Input voltage = 16 V
- Output voltage = 5 V
- Switching frequency = 1000 kHz
- Inductor = 0.6 μH

#### 6.3.4.2 Calculating Power Loss

- Power loss at 15 A = 2.8 W ([Figure 1](#))
- Normalized power loss for input voltage ≈ 1.05 ([Figure 7](#))
- Normalized power loss for output voltage ≈ 1.08 ([Figure 8](#))
- Normalized power loss for switching frequency ≈ 1.03 ([Figure 6](#))
- Normalized power loss for output inductor ≈ 1.05 ([Figure 9](#))
- **Final calculated power loss = 2.8 W × 1.05 × 1.08 × 1.03 × 1.05 ≈ 3.4 W**

#### 6.3.4.3 Calculating SOA Adjustments

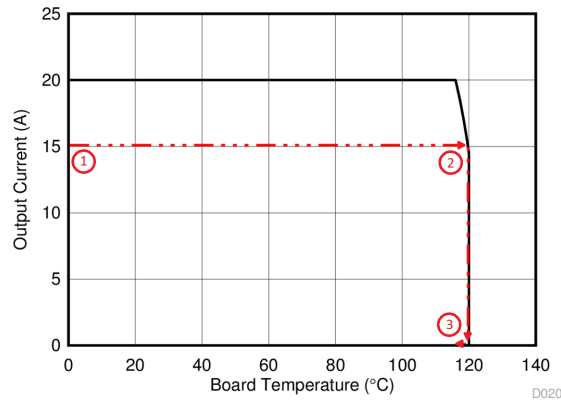
- SOA adjustment for input voltage ≈ 0.5°C ([Figure 7](#))
- SOA adjustment for output voltage ≈ 0.7°C ([Figure 8](#))
- SOA adjustment for switching frequency ≈ 0.3°C ([Figure 6](#))
- SOA adjustment for output inductor ≈ 0.5°C ([Figure 9](#))
- **Final calculated SOA adjustment = 0.5 + 0.7 + 0.3 + 0.5 ≈ 2°C**

In the design example, the estimated power loss of the CSD87334Q3D would increase to 3.4 W. In addition, the maximum allowable board or ambient temperature, or both, would have to decrease by 2°C. [Figure 20](#) graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board or ambient temperature by subtracting the temperature adjustment value.

**System Example (continued)**

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 2°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.



**Figure 20. Power Block SOA**

## 7 Layout

### 7.1 Layout Guidelines

#### 7.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is provided.

#### 7.1.2 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/μs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's  $V_{IN}$  and  $P_{GND}$  pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the  $V_{IN}$  and  $P_{GND}$  pins (see [Figure 21](#)). The example in [Figure 21](#) uses six 10-μF ceramic capacitors (TDK C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins.  $T_G$  and  $B_G$  should connect to the outputs of the driver IC. The  $T_{GR}$  pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, and so forth). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block  $V_{SW}$  pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.<sup>(1)</sup> In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R, and from 330 pf to 2200 pF for the C. Please refer to [Snubber Circuits: Theory, Design and Application](#) (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the  $V_{SW}$  node and  $P_{GND}$  (see [Figure 21](#)).<sup>(1)</sup>

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

## 7.2 Layout Example

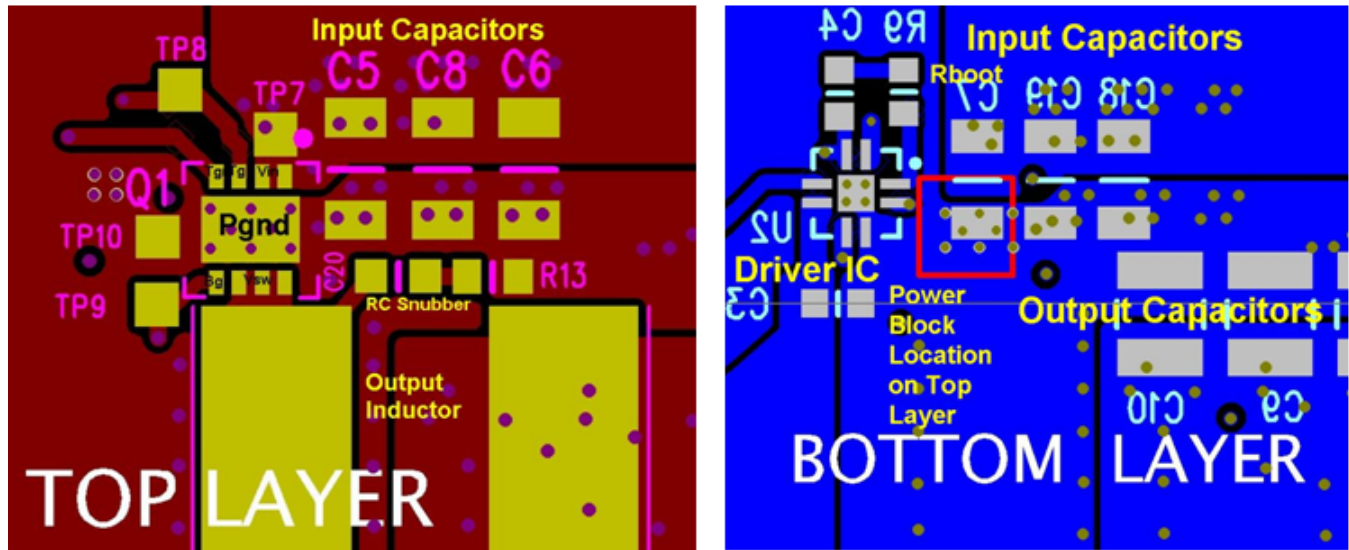


Figure 21. Recommended PCB Layout (Top Down)

## 7.3 Thermal Considerations

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in [Figure 21](#) uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the PCB design rules and manufacturing capabilities of the end user.

## 8 Device and Documentation Support

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 8.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 8.5 Glossary

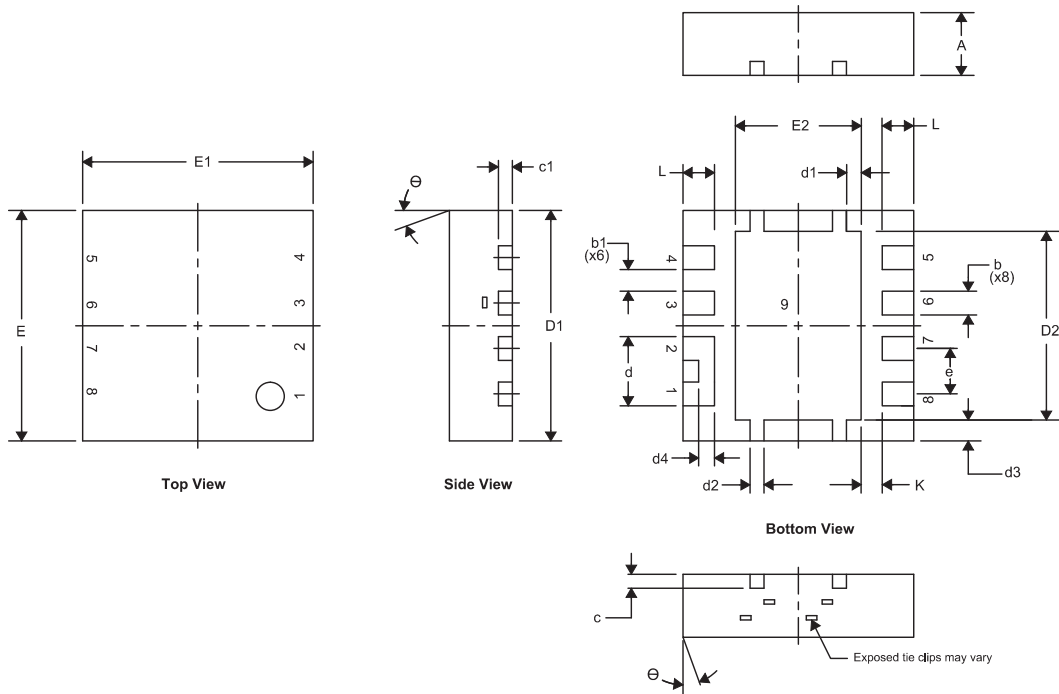
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 9.1 Q3D Package Dimensions

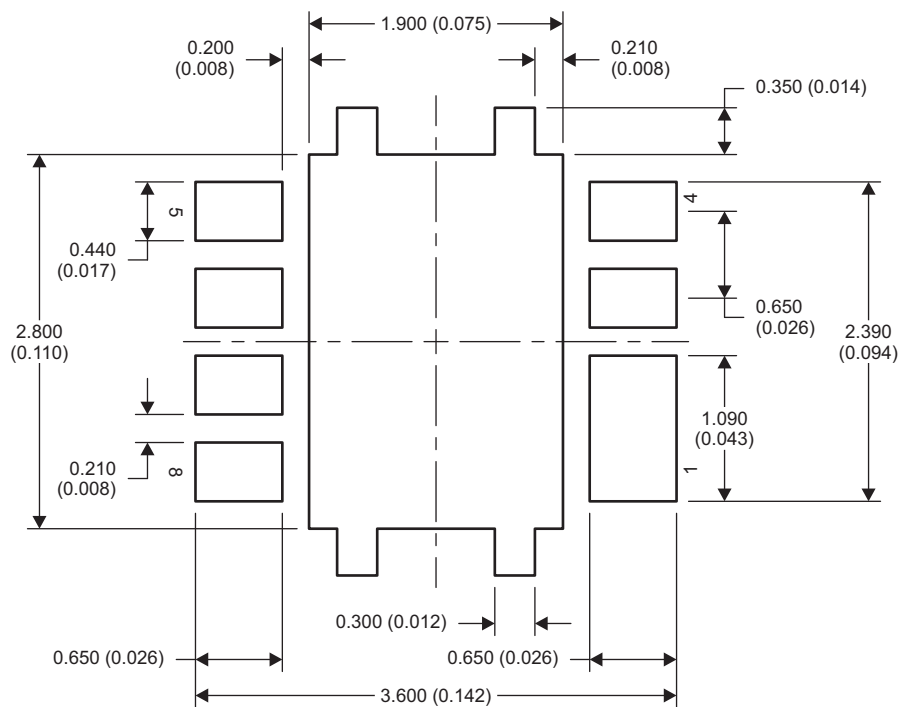


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.850		1.050	0.033		0.041
b	0.280		0.400	0.011		0.016
b1		0.310			0.012	
c	0.150		0.250	0.006		0.010
c1	0.150		0.250	0.006		0.010
d	0.940		1.040	0.037		0.041
d1	0.160		0.260	0.006		0.010
d2	0.150		0.250	0.006		0.010
d3	0.250		0.350	0.010		0.014
d4	0.175		0.275	0.007		0.011
D1	3.200		3.400	0.126		0.134
D2	2.650		2.750	0.104		0.108
E	3.200		3.400	0.126		0.134
E1	3.200		3.400	0.126		0.134
E2	1.750		1.850	0.069		0.073
e		0.650 TYP			0.026 TYP	
L	0.400		0.500	0.016		0.020
θ	0.000		—	—		—
K		0.300 TYP			0.012 TYP	

**Table 1. Pinout Configuration**

POSITION	DESIGNATION
Pin 1	$V_{IN}$
Pin 2	$V_{IN}$
Pin 3	$T_G$
Pin 4	$T_{GR}$
Pin 5	$B_G$
Pin 6	$V_{SW}$
Pin 7	$V_{SW}$
Pin 8	$V_{SW}$
Pin 9	$P_{GND}$

## 9.2 Land Pattern Recommendation

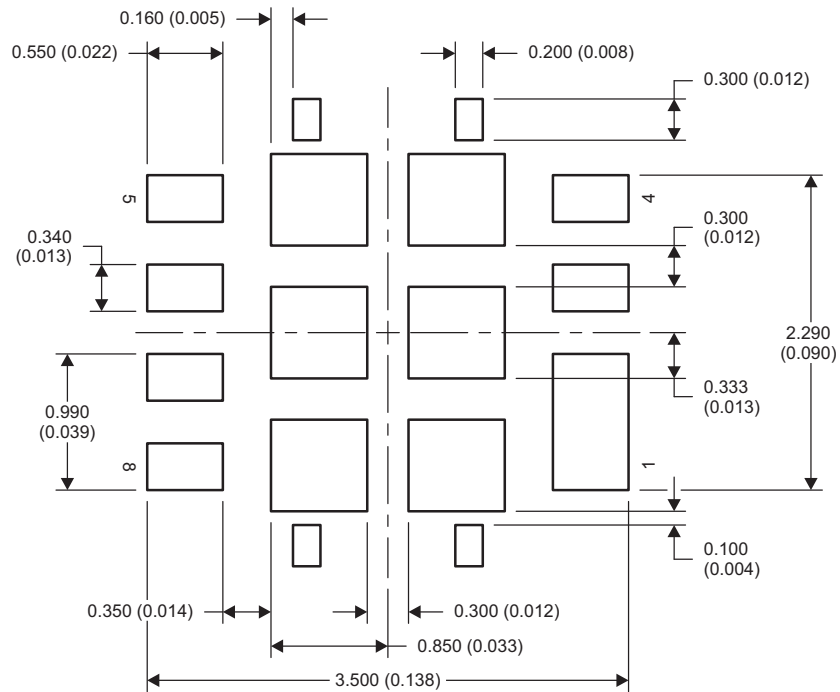


M0193-01

NOTE: Dimensions are in mm (in).



### 9.3 Stencil Recommendation

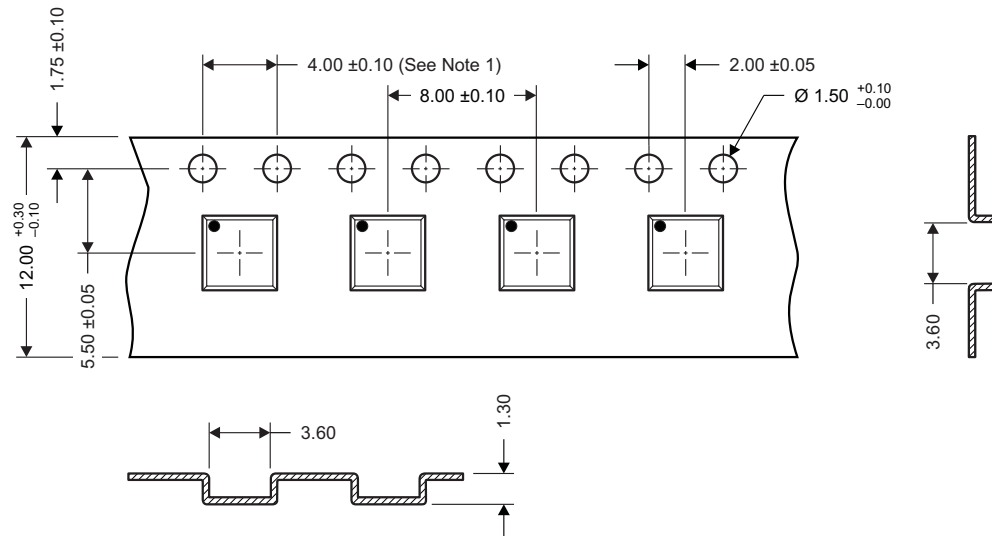


M0207-01

NOTE: Dimensions are in mm (in).

For recommended circuit layout for PCB designs, see [Reducing Ringing Through PCB Layout Techniques \(SLPA005\)](#).

### 9.4 Q3D Tape and Reel Information



M0144-01

- NOTES:
- 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$ .
  - Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
  - Material: black static-dissipative polystyrene.
  - All dimensions are in mm, unless otherwise specified.
  - Thickness:  $0.3 \pm 0.05$  mm.
  - MSL1 260°C (IR and convection) PbF reflow compatible.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD87334Q3D</a>	Active	Production	VSON-CLIP (DPB)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3D.B	Active	Production	VSON-CLIP (DPB)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DG4	Active	Production	VSON-CLIP (DPB)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DG4.B	Active	Production	VSON-CLIP (DPB)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D
<a href="#">CSD87334Q3DT</a>	Active	Production	VSON-CLIP (DPB)   8	250   SMALL T&R	ROHS Exempt	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DT.B	Active	Production	VSON-CLIP (DPB)   8	250   SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87334Q3D	VSON-CLIP	DPB	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87334Q3DG4	VSON-CLIP	DPB	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87334Q3DT	VSON-CLIP	DPB	8	250	180.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87334Q3D	VSON-CLIP	DPB	8	2500	346.0	346.0	33.0
CSD87334Q3DG4	VSON-CLIP	DPB	8	2500	346.0	346.0	33.0
CSD87334Q3DT	VSON-CLIP	DPB	8	250	182.0	182.0	20.0

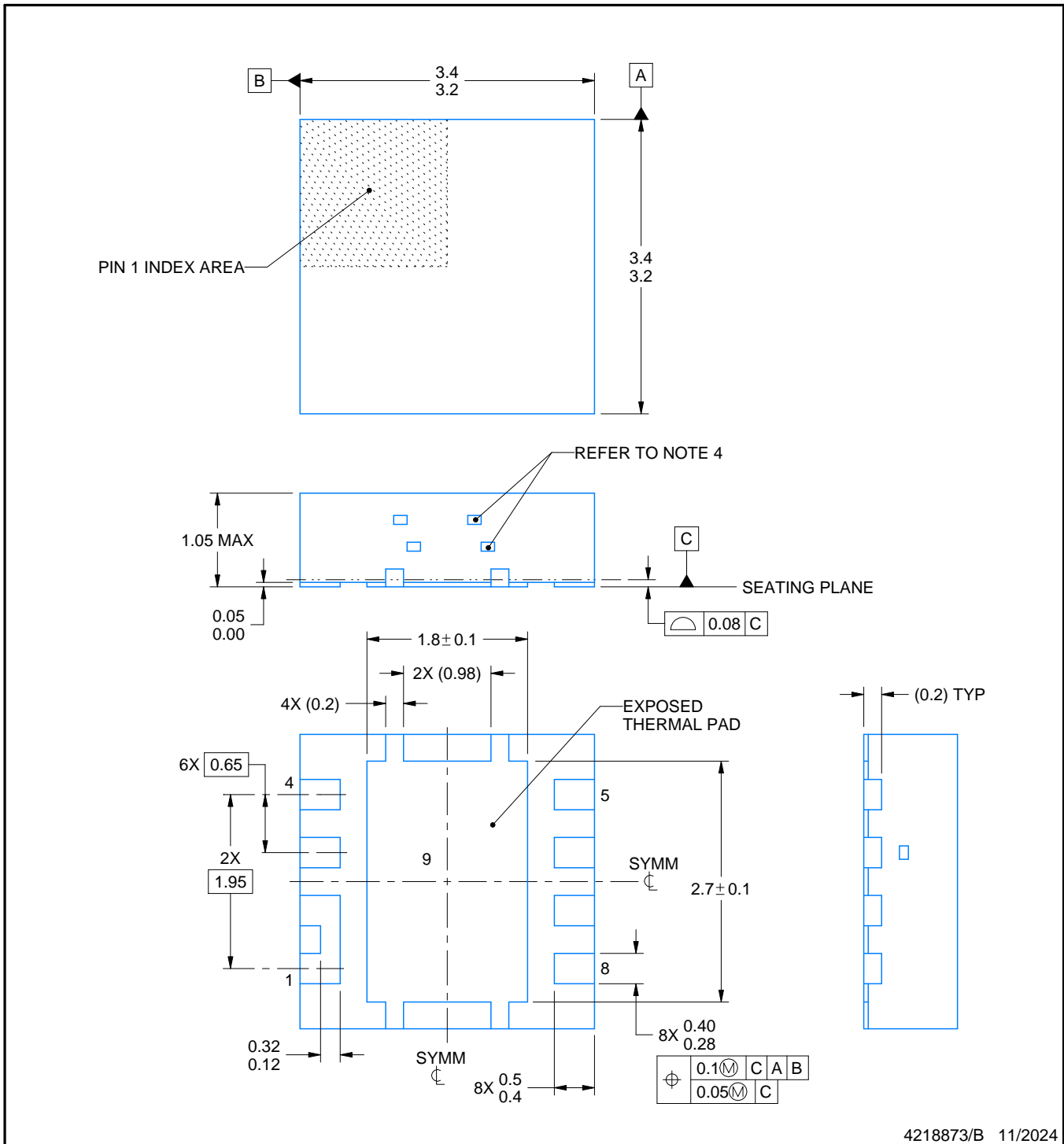


# DPB0008A

# PACKAGE OUTLINE

VSON - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218873/B 11/2024

### NOTES:

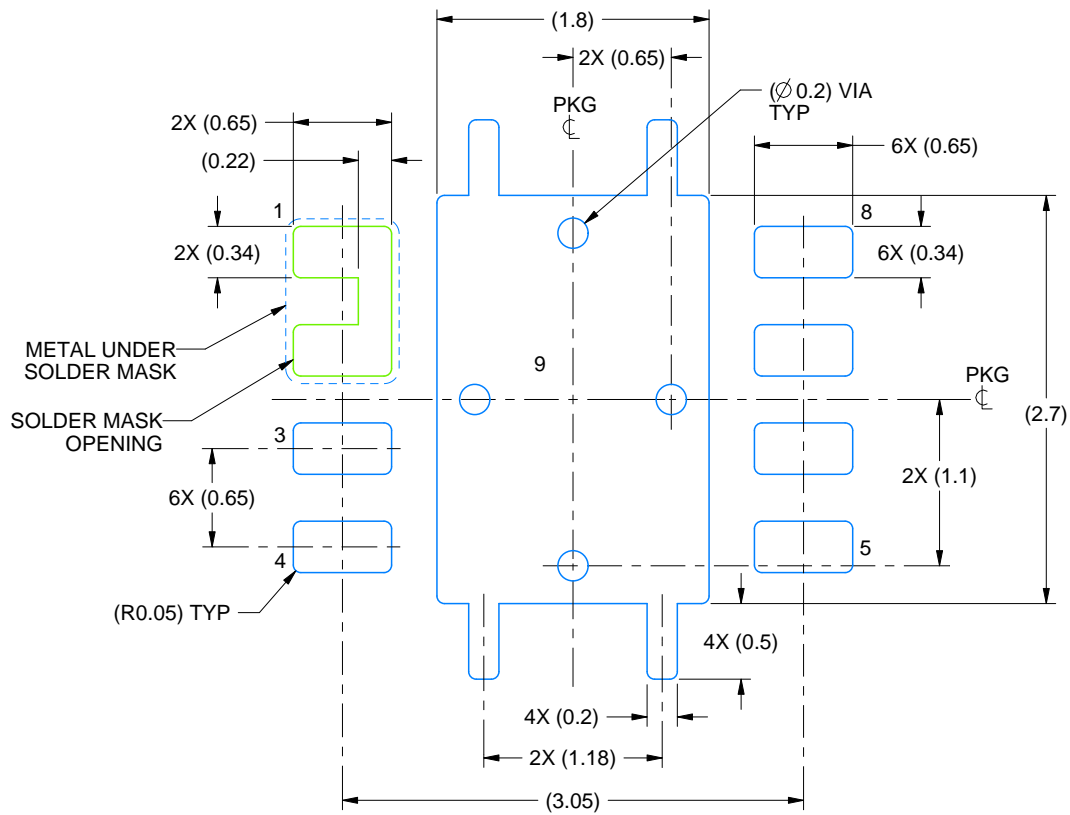
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance
4. Exposed metals on side wall may vary & not visible.

# EXAMPLE BOARD LAYOUT

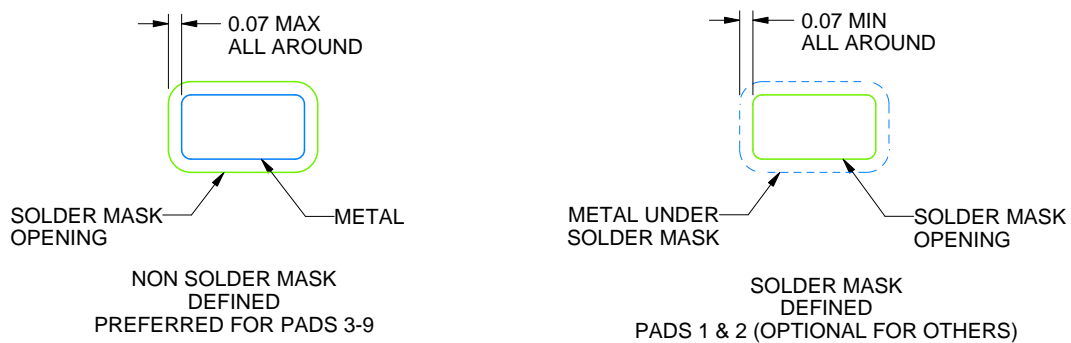
DPB0008A

VSON - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218873/B 11/2024

NOTES: (continued)

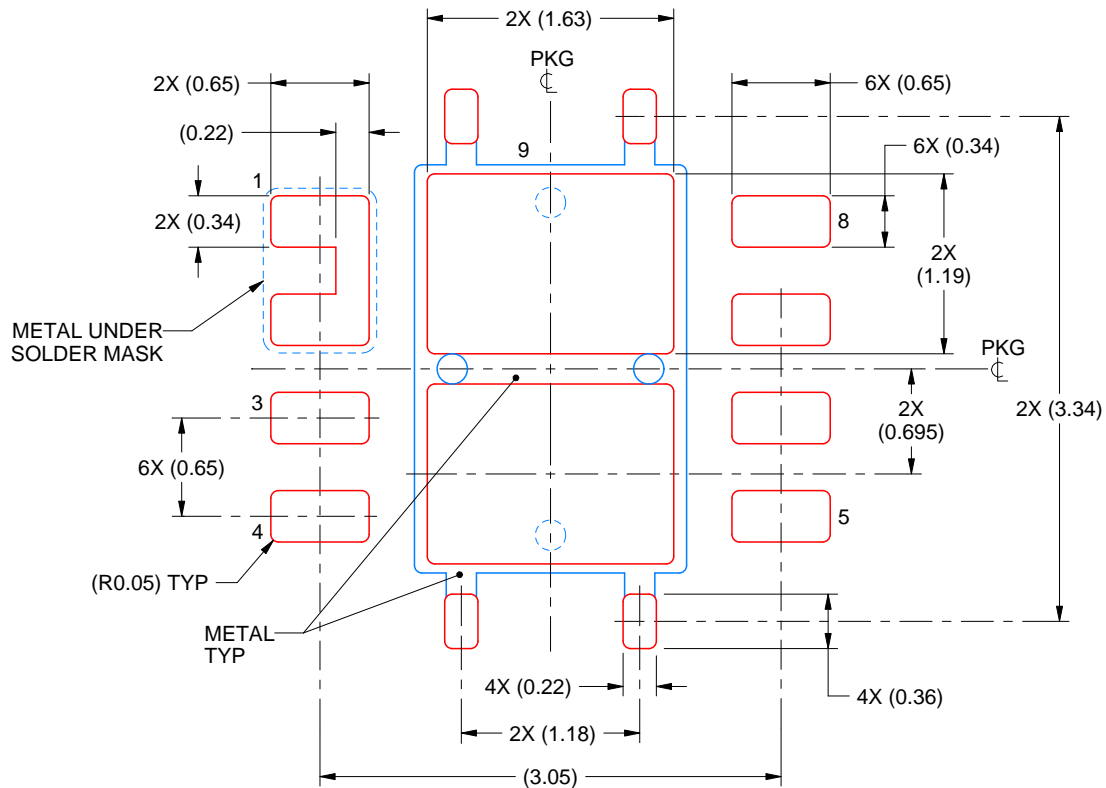
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DPB0008A

VSON - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9  
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4218873/B 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025