



## 30V, N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD17553Q5A](#)

### FEATURES

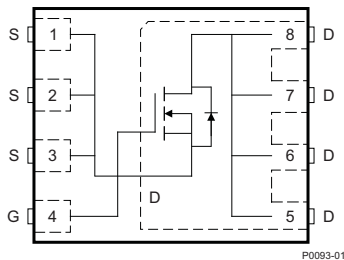
- **Ultralow  $Q_g$  and  $Q_{gd}$**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm x 6-mm Plastic Package**

### APPLICATIONS

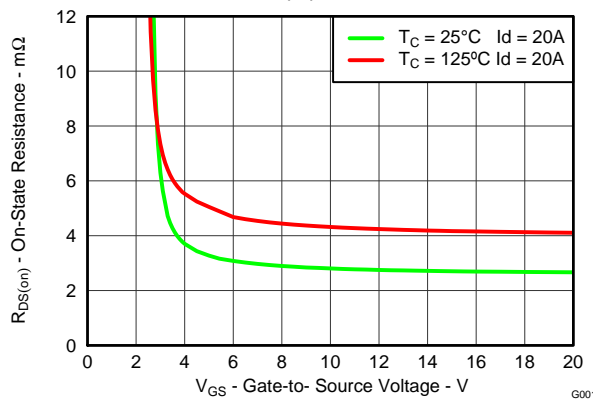
- **Point of load Synchronous Buck in Networking, Telecom and Computing Systems**
- **Optimized for Control and Synchronous FET Applications**

### DESCRIPTION

The NexFET power MOSFET has been designed to minimize losses in power conversion applications.

**Top View**


P0093-01

 **$R_{DS(on)}$  vs  $V_{GS}$** 


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### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5V)	17.5	nC
$Q_{gd}$	Gate Charge Gate to Drain	4.7	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	3.5 mΩ
		$V_{GS} = 10V$	2.7 mΩ
$V_{GS(th)}$	Threshold Voltage	1.5	V

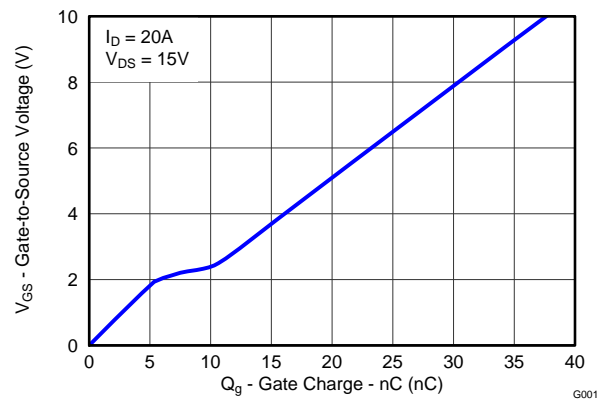
### ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17553Q5A	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	+/-20	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	23.5	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	151	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 45A, L = 0.1mH, R_G = 25\Omega$	101	mJ

- (1) Typical  $R_{\theta JA} = 40.5^\circ\text{C/W}$  on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

**GATE CHARGE**


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

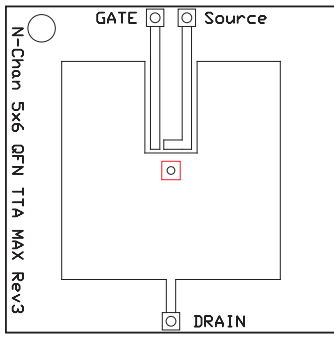
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$V_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	1.9	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 20A$		3.5	4	$m\Omega$
		$V_{GS} = 10V, I_D = 20A$		2.7	3.1	$m\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 20A$		106		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1\text{MHz}$		2710	3252	pF
$C_{oss}$	Output Capacitance			635	762	pF
$C_{rss}$	Reverse Transfer Capacitance			48	60	pF
$R_G$	Series Gate Resistance	$V_{DS} = 15V, I_D = 20A$		0.7	0.9	$\Omega$
$Q_g$	Gate Charge Total (4.5V)			17.5	21.5	nC
$Q_{gd}$	Gate Charge Gate to Drain			4.7		nC
$Q_{gs}$	Gate Charge Gate to Source			5.8		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			4.1		nC
$Q_{oss}$	Output Charge	$V_{DS} = 15V, V_{GS} = 0V$		19.6		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 20A, R_G = 0.75\Omega$		9.7		ns
$t_r$	Rise Time			17		ns
$t_{d(off)}$	Turn Off Delay Time			14.8		ns
$t_f$	Fall Time			5.2		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{DS} = 20A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 14V, I_F = 20A, di/dt = 300A/\mu s$		23.8		nC
$t_{rr}$	Reverse Recovery Time			23.1		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

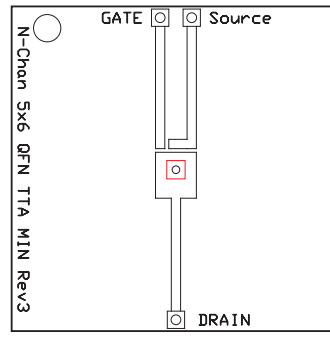
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			50.6	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



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Max  $R_{\theta JA} = 50.6^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45-cm<sup>2</sup>) of 2-  
oz. (0.071-mm thick)  
Cu.



M0137-02

Max  $R_{\theta JA} = 122.4^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

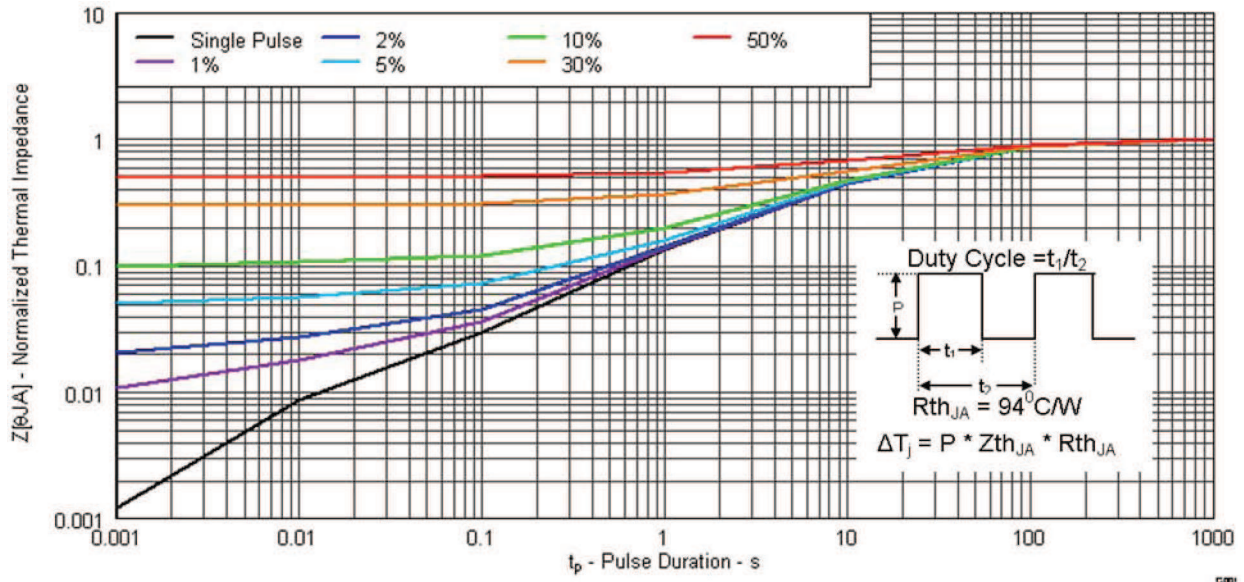
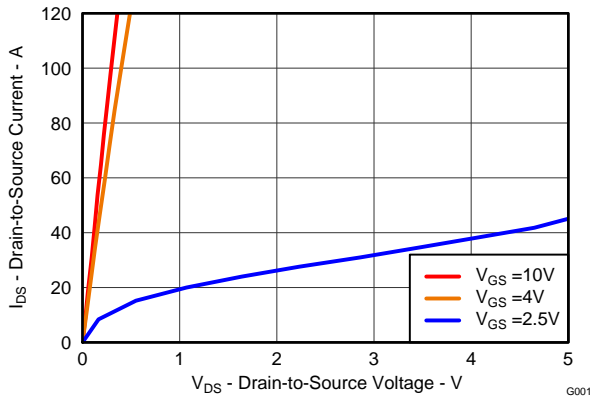


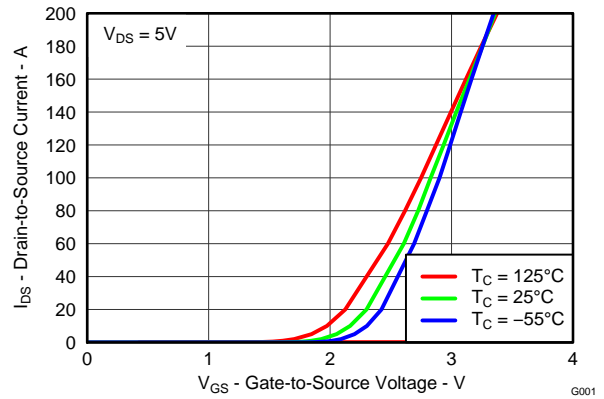
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

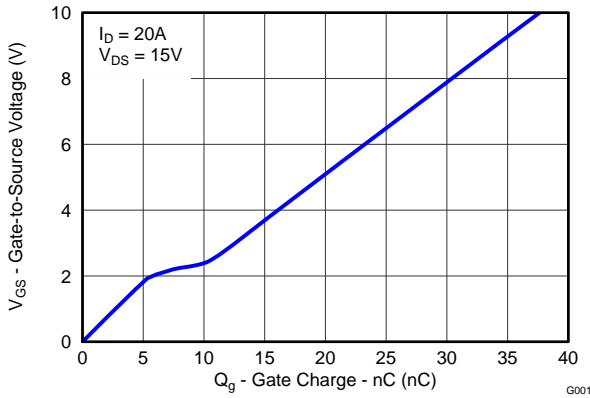
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



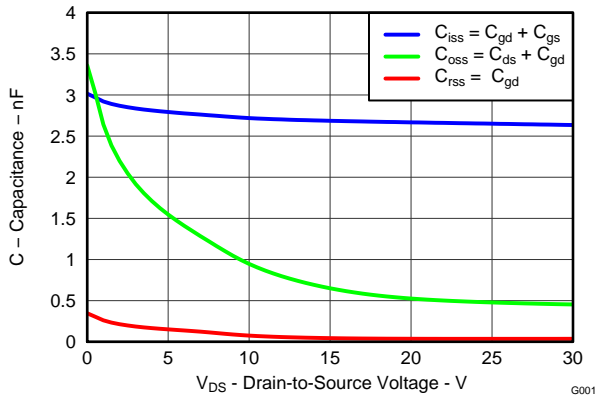
**Figure 2. Saturation Characteristics**



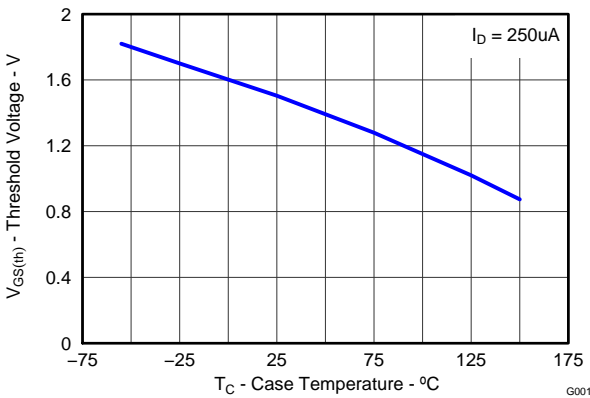
**Figure 3. Transfer Characteristics**



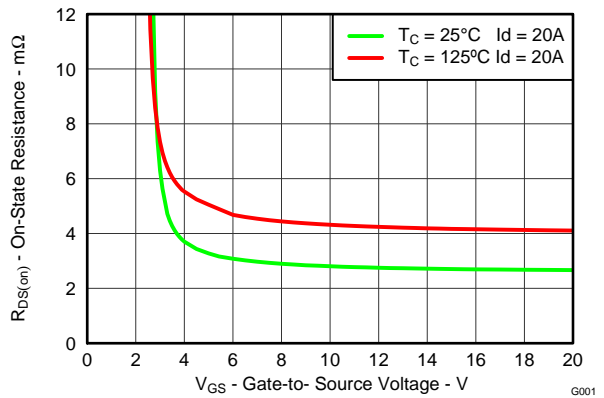
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

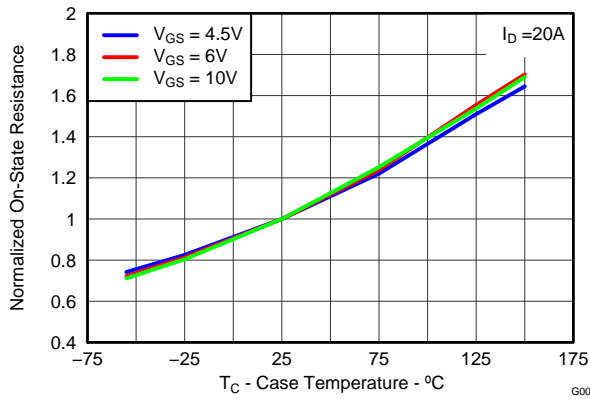


Figure 8. Normalized On-State Resistance vs. Temperature

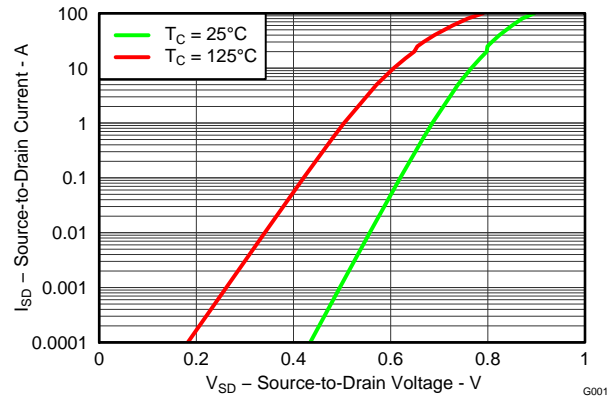


Figure 9. Typical Diode Forward Voltage

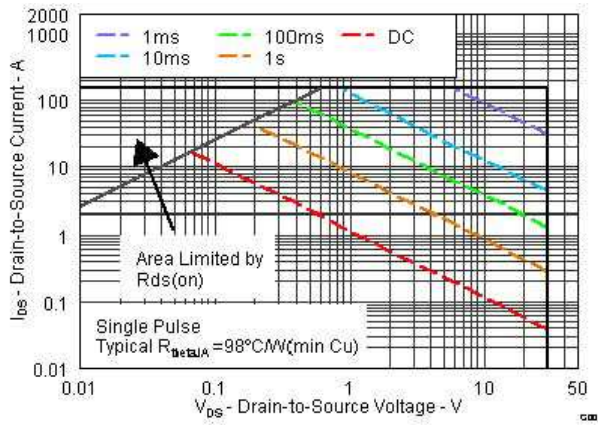


Figure 10. Maximum Safe Operating Area

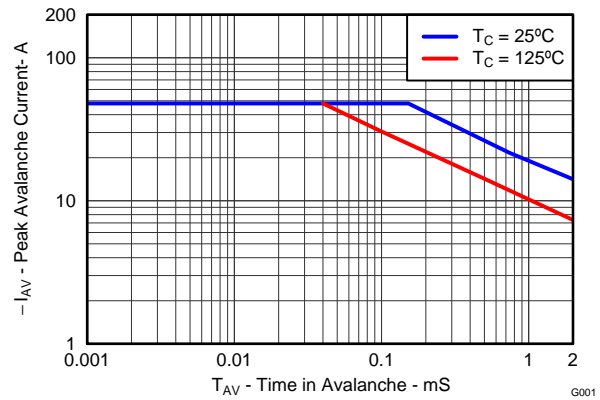


Figure 11. Single Pulse Unclamped Inductive Switching

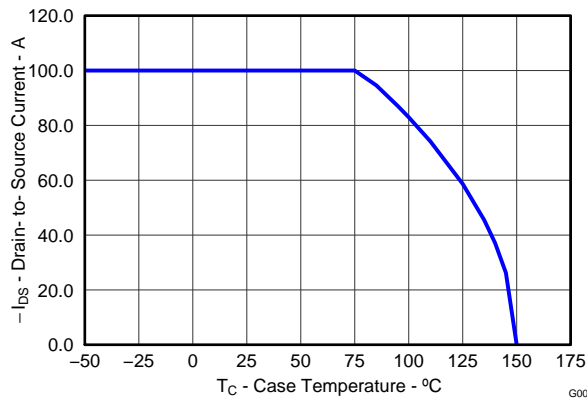


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

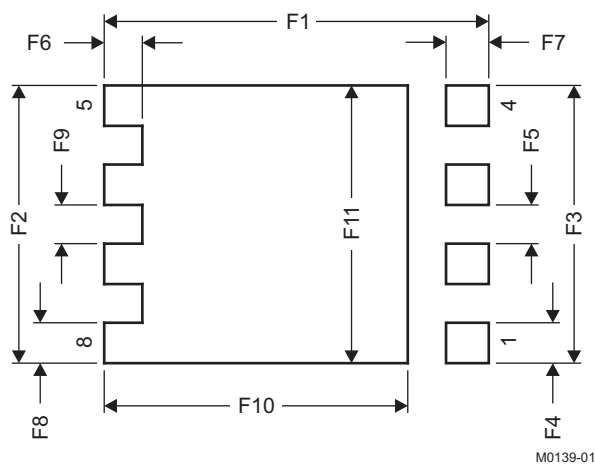
**Q5A Package Dimensions**



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°		12°

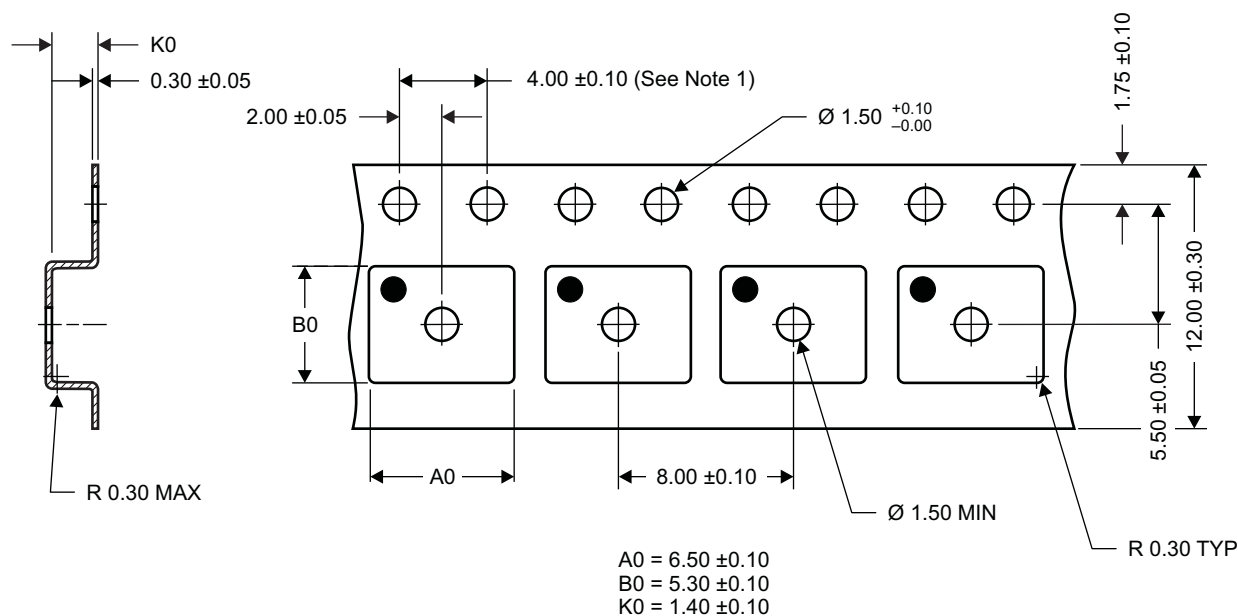
Figure 13. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Q5A Tape and Reel Information



M0138-01

### Notes:

- 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD17553Q5A</a>	Active	Production	VSONP (DQJ)   8	2500   LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17553
CSD17553Q5A.B	Active	Production	VSONP (DQJ)   8	2500   LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17553

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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