N-Channel NexFET™ Power MOSFET

1 Features

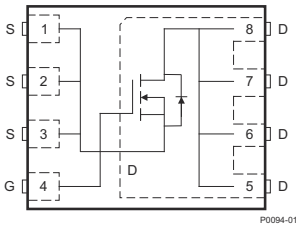
- Optimized for 5 V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

2 Applications

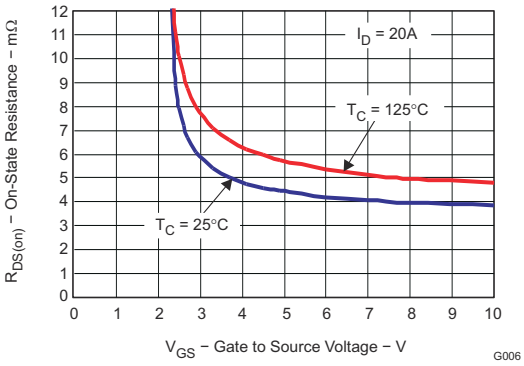
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Synchronous or Control FET Applications

3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5 V gate drive applications.



Top View



$R_{DS(on)}$ vs V_{GS}

Product Summary

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	6.8		nC
Q_{gd}	Gate Charge Gate to Drain	1.3		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3 V	5.4	mΩ
		V_{GS} = 4.5 V	4.6	mΩ
		V_{GS} = 8 V	3.9	mΩ
$V_{GS(th)}$	Threshold Voltage	1.1		V

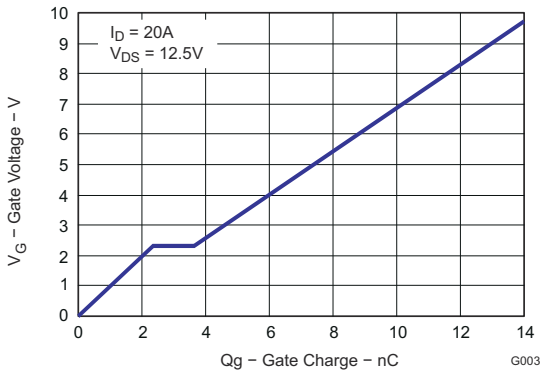
Ordering Information

Device	Package	Media	Qty	Ship
CSD16322Q5	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	97	A
	Continuous Drain Current(1)	21	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	136	A
P_D	Power Dissipation(1)	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 50 A, L = 0.1 mH, R_G = 25 Ω	125	mJ

(1) Typical $R_{\theta JA}$ = 39°C/W on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
(2) Pulse duration ≤300 µs, duty cycle ≤2%



GATE CHARGE

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2010) to Revision C (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	7

Changes from Revision A (April 2010) to Revision B (May 2010)	Page
• Changed $R_{DS(on)}$, V_{GS} = 3 V in the Electrical Characteristics table From: 7 To: 7.2 in the max column	3

Changes from Revision * (August 2009) to Revision A (April 2010)	Page
• Changed Note1 of the ABSOLUTE MAXIMUM RATINGS From: $R_{\theta JA}$ = 39°C/W To: Typical $R_{\theta JA}$ = 39°C/W	1
• Changed Figure 7-1 text From: $R_{\theta JA}$ = 99°C/W To: Typical $R_{\theta JA}$ = 98°C/W	4
• Changed Figure 7-10 text From: $R_{\theta JA}$ = 99°C/W To: Typical $R_{\theta JA}$ = 98°C/W	4
• Changed Figure 7-11 X-axis values	4

5 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0 V, I_D = 250 µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0 V, V_{GS} = +10/–8 V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3 V, I_D = 20 A		5.4	7.2	mΩ
		V_{GS} = 4.5 V, I_D = 20 A		4.6	5.8	mΩ
		V_{GS} = 8 V, I_D = 20 A		3.9	5	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 20 A		106		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		1050	1365	pF
C_{oss}	Output Capacitance			740	950	pF
C_{rss}	Reverse Transfer Capacitance			55	70	pF
R_G	Series Gate Resistance			1.1	2.2	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 12.5 V, I_D = 20 A		6.8	9.7	nC
Q_{gd}	Gate Charge Gate to Drain			1.3		nC
Q_{gs}	Gate Charge Gate to Source			2.4		nC
$Q_{g(th)}$	Gate Charge at Vth			1.3		nC
Q_{oss}	Output Charge	V_{DS} = 13 V, V_{GS} = 0 V		17		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 20 A, R_G = 2 Ω		6.1		ns
t_r	Rise Time			10.7		ns
$t_{d(off)}$	Turn Off Delay Time			12.3		ns
t_f	Fall Time			3.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 20 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 13 V, I_F = 20 A, di/dt = 300 A/µs		19		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 13 V, I_F = 20 A, di/dt = 300 A/µs		21		ns

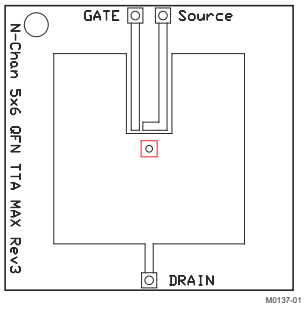
6 Thermal Characteristics

(T_A = 25°C unless otherwise stated)

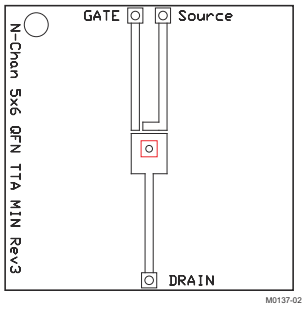
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			2.4	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 123°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

7 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

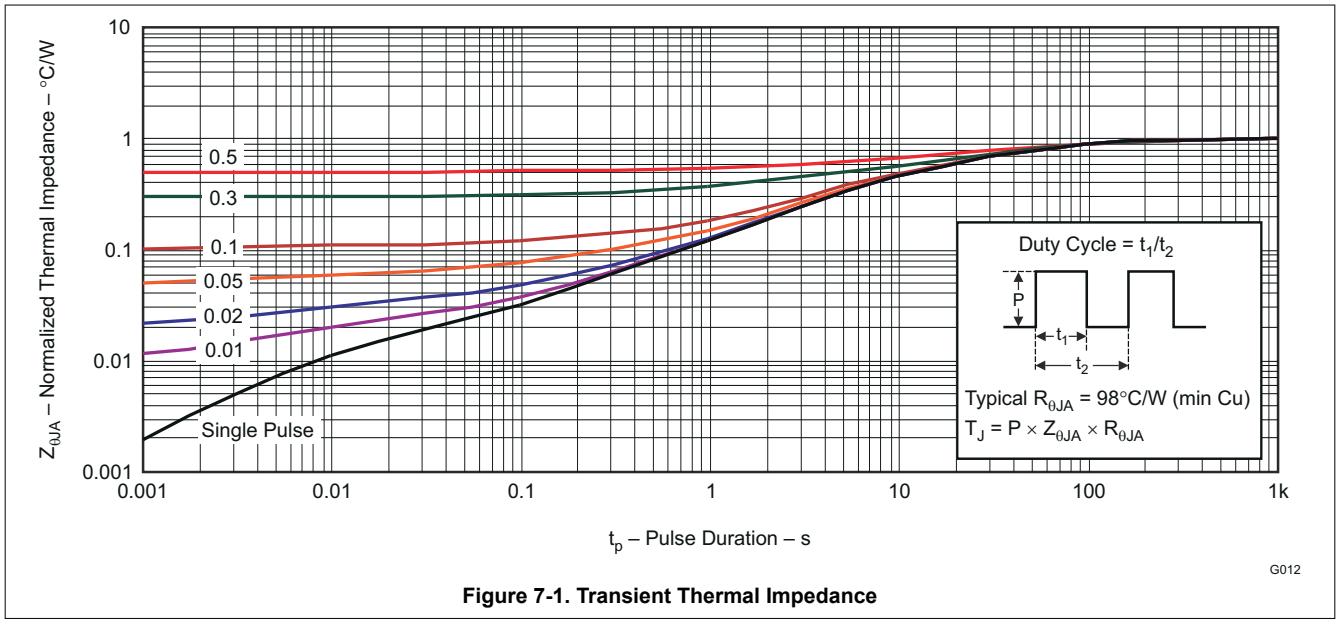


Figure 7-1. Transient Thermal Impedance

7 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

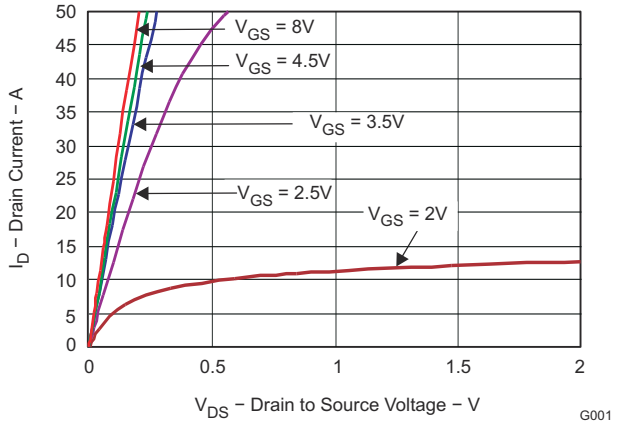


Figure 7-2. Saturation Characteristics

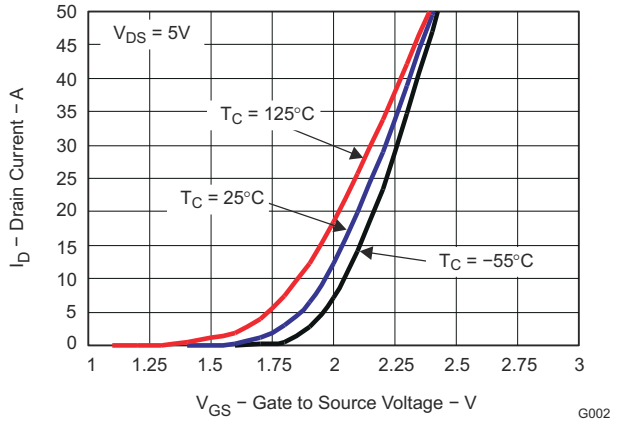


Figure 7-3. Transfer Characteristics

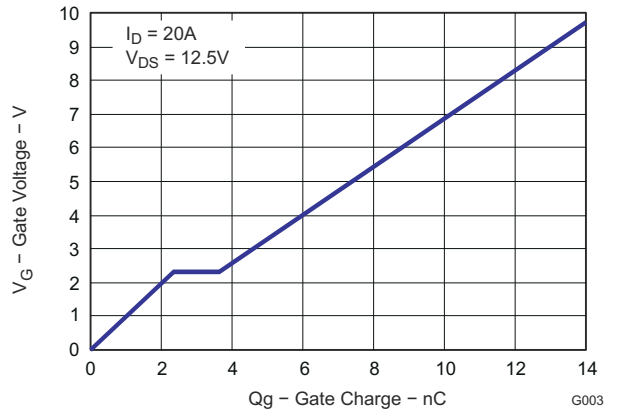


Figure 7-4. Gate Charge

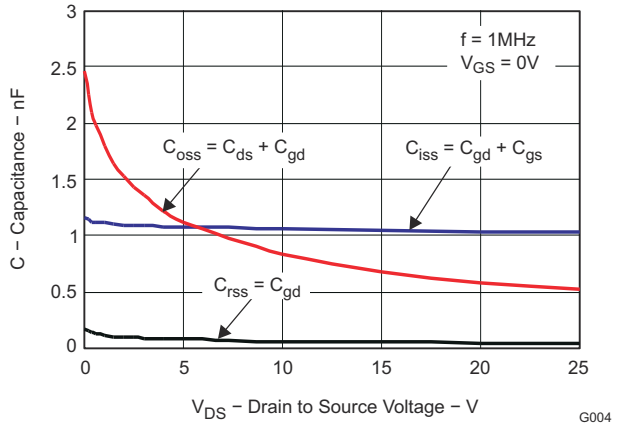


Figure 7-5. Capacitance

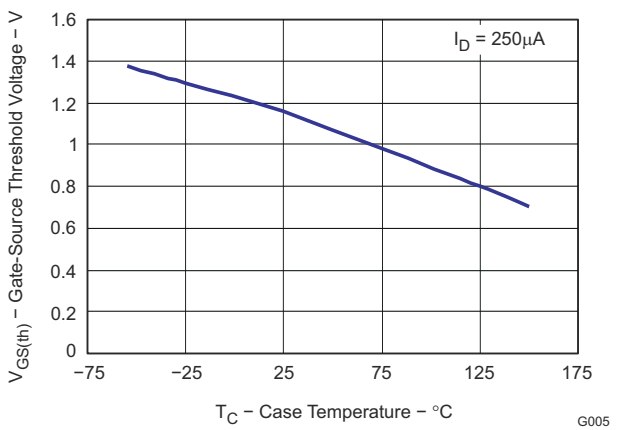


Figure 7-6. Threshold Voltage vs. Temperature

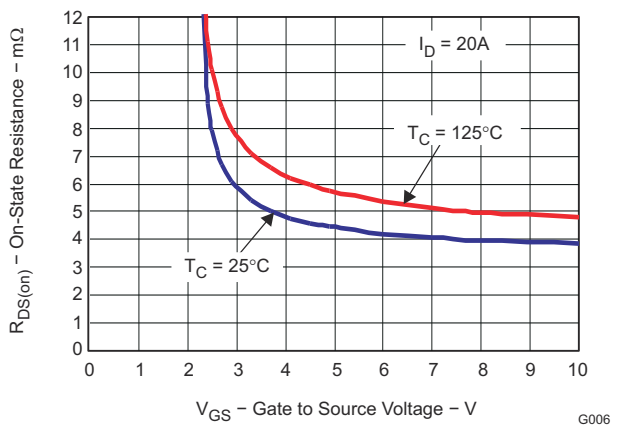


Figure 7-7. On-State Resistance vs. Gate to Source Voltage

7 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

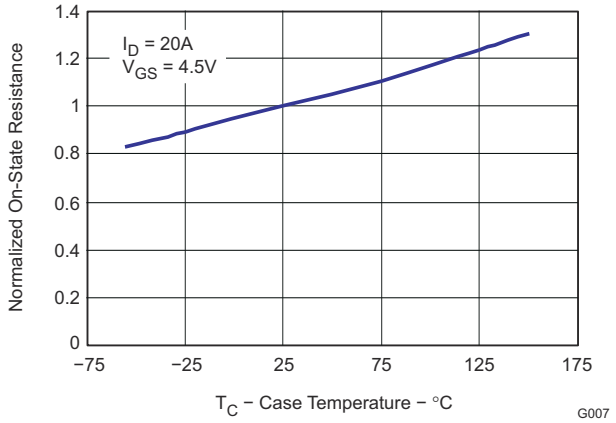


Figure 7-8. Normalized On-State Resistance vs. Temperature

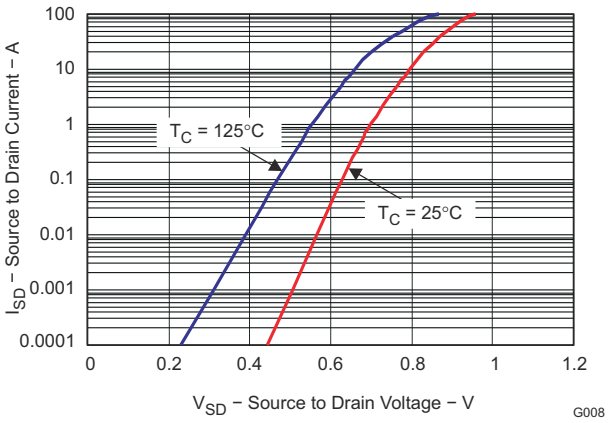


Figure 7-9. Typical Diode Forward Voltage

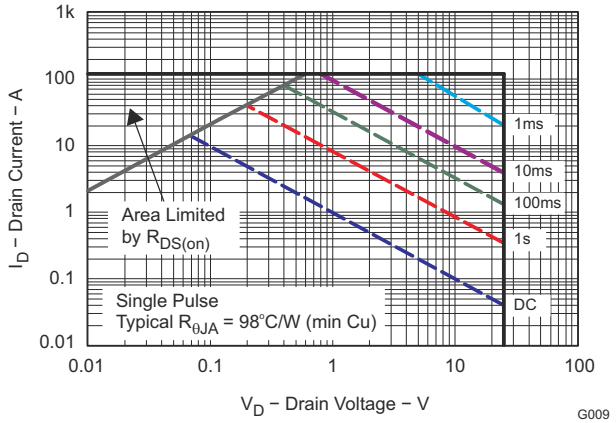


Figure 7-10. Maximum Safe Operating Area

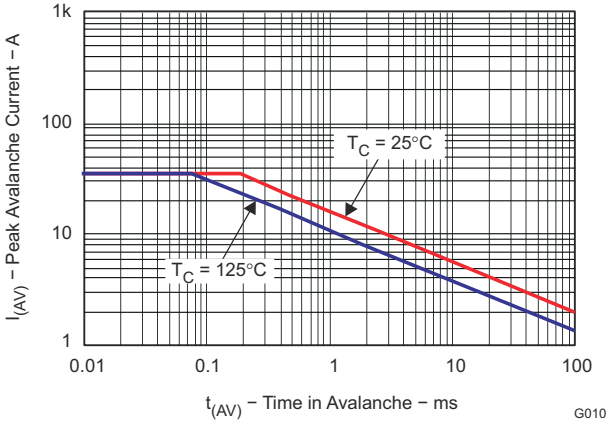


Figure 7-11. Single Pulse Unclamped Inductive Switching

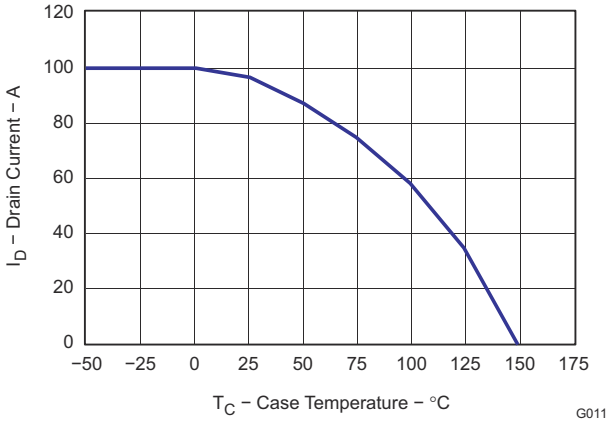


Figure 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16322Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16322
CSD16322Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16322

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

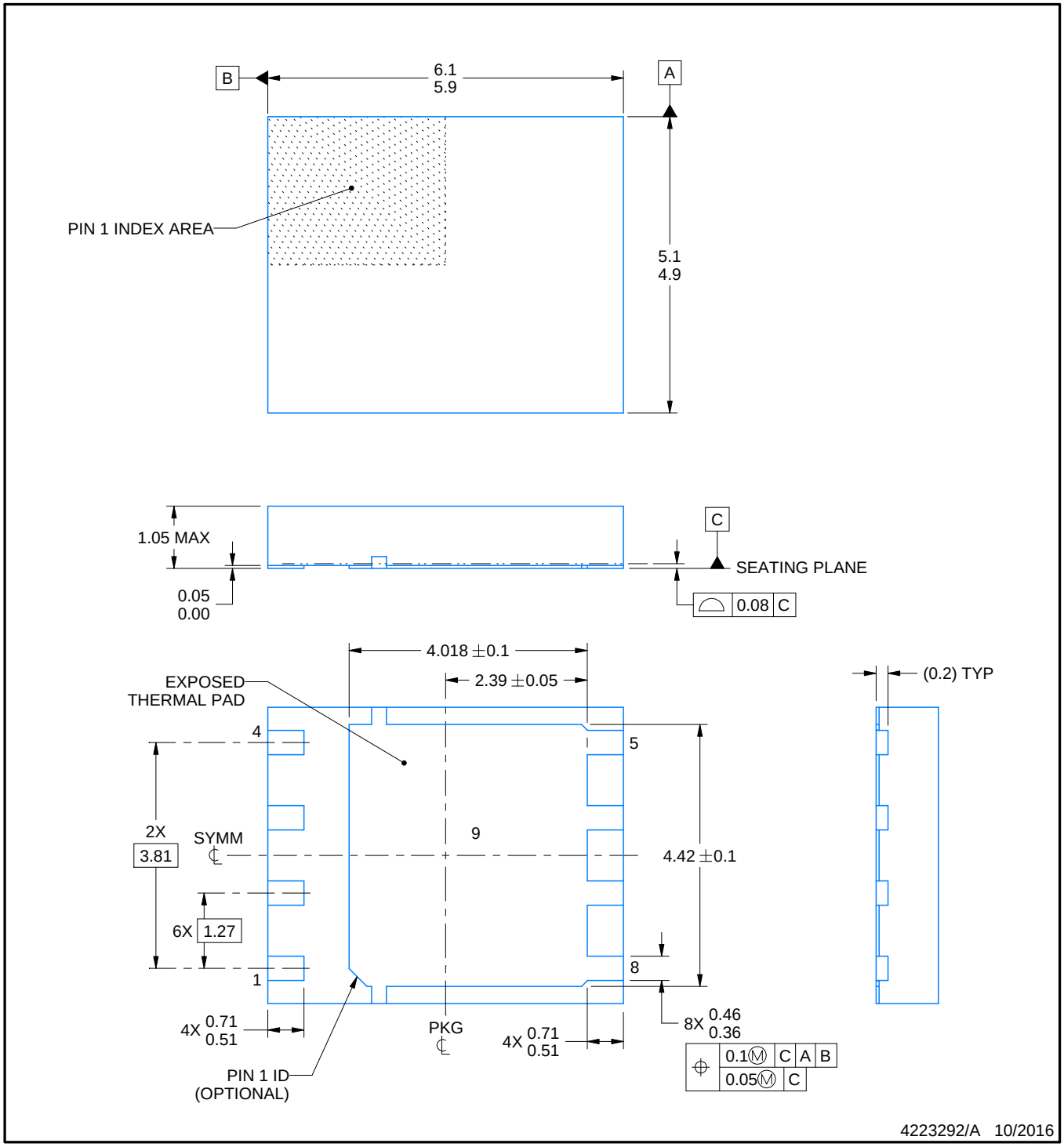
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DQH0008A

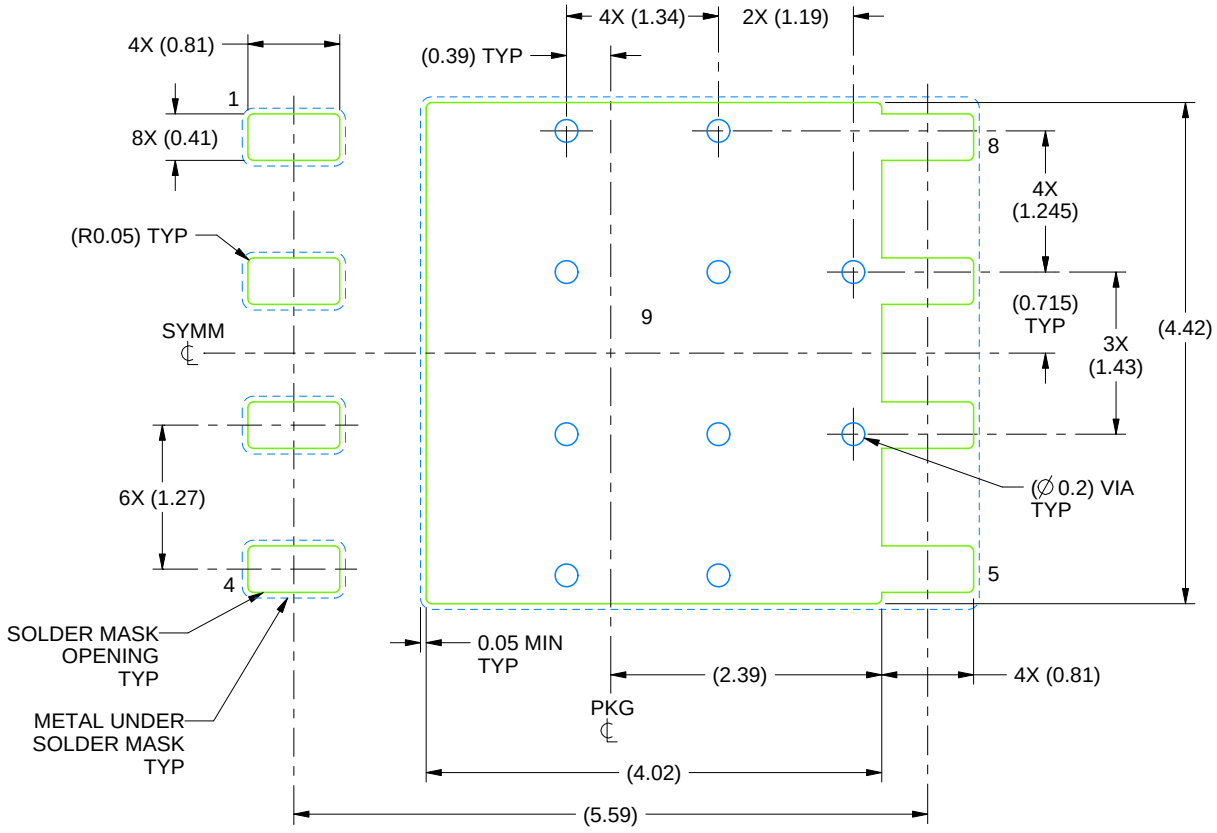
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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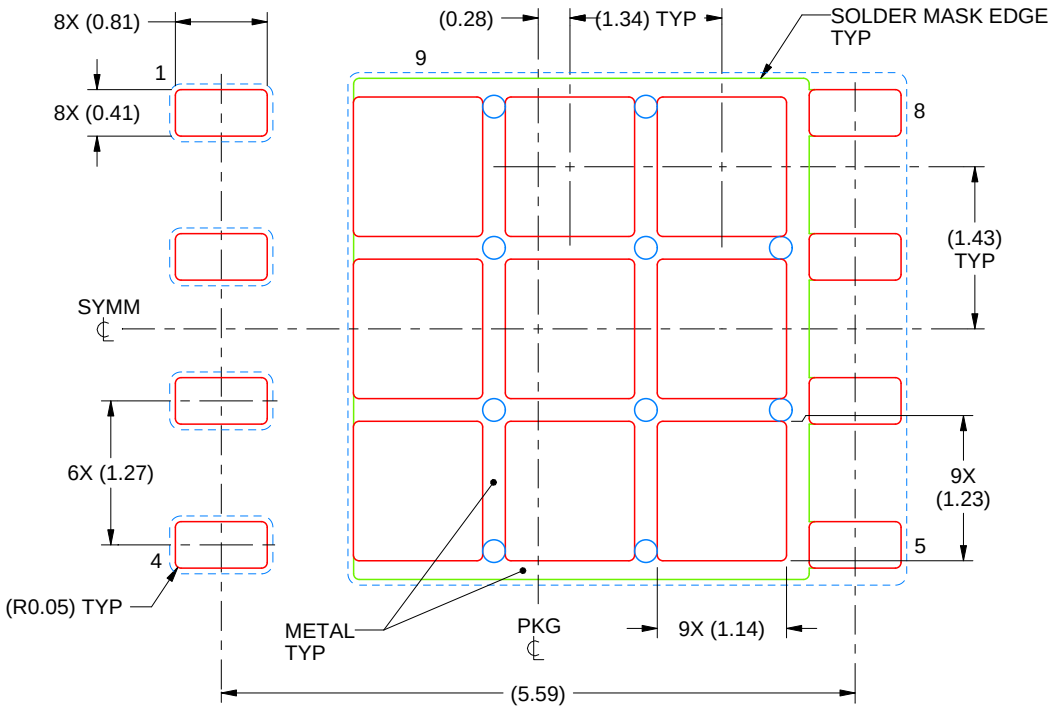
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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