CC355xE SimpleLink™ 2.4GHz and 5GHz Dual-Band Wi-Fi 6 and Bluetooth® Low Energy Wireless MCU

1 Features

Microcontroller

- Powerful 160MHz Arm® Cortex®-M33 processor with FPU, TrustZone®, and AI acceleration
- High-speed quad-SPI and octal-SPI for XiP flash with on-the-fly decryption
- Flexible configuration of low-latency TCM (up to 32KB) and Cache (32KB or 64KB) for improved code execution performance
- 1.1MB embedded SRAM including 128KB TCM for Wi-Fi™, Bluetooth® Low Energy, networking, and application data

Peripherals

- Up to 36 I/Os with flexible multiplexing options
- 8 × general-purpose timers and pulse-width modulation (PWM)
- 3 × universal asynchronous receiver-transmitter (UART)
- 2 × Serial Peripheral Interface (SPI)
- 2 × inter-integrated circuit (I^2C)
- Inter-IC sound (I^2S)
- Pulse density modulation (PDM)
- Secure digital and multimedia card (SD/MMC)
- Secure digital input output (SDIO) 2.0
- Controller area network (CAN) 2.0
- 8-channel, 12-bit analog-to-digital converter (ADC)

System Services

- Direct memory access (DMA)
- One-time-programmable memory (OTP)
- Real-time clock (RTC) and watchdog timer (WDT)

Radio

- Wi-Fi 6 (802.11ax)
  - 2.4GHz and 5GHz, single-stream 20MHz channels with application throughput up to 20Mbps (UDP)
  - Compatible with IEEE 802.11 a/b/g/n/ax
    - Orthogonal frequency-division multiple access (OFDMA)
    - Target wake time (TWT)
    - Trigger frames
    - Basic service set (BSS) color
  - Integrated PA for a complete WLAN system with up to 20.5dBm output power at 1 DSSS
  - Role support: STA, softAP , Wi-Fi direct, multi-role AP + STA
  - Support for personal and enterprise Wi-Fi security: WPA and WPA2 PSK, WPA2 Enterprise, WPA3 personal or enterprise
  - Wi-Fi TX Power:
    - 20.5dBm at 1DSSS
    - 17.8dBm at 54OFDM
  - Wi-Fi RX Sensitivity:
    - –98.7dBm at 1DSSS
    - –76.6dBm at 54OFDM
- Bluetooth® low energy
  - Bluetooth low energy 5.4 certified stack
  - Supports long-range and high-speed PHYs (up to 2Mbps)

Security Features

- ARM TrustZone
- Hardware security module supporting all of the following:
  - ECC, RSA, AES, SHA2/3, MD5, CRC 16/32, and TRNG
  - Secure key storage
- Initial secure programming
- Secure boot
- Software IP and cloning protection
- Debug security through JTAG and debug port lock
- OTP with ability to program root-of-trust public key
- Secure over-the-air (OTA) updates
- Anti-rollback protection

Clock Source

- Fast clock: 52MHz XTAL
- Slow clock: Internal low-frequency oscillator, 32.768kHz XTAL, or external slow clock source

Power Management

- Support for 3.3V and 1.8V on multiple I/O domains
- Supplies: VPA: 3.3V, VMAIN: 1.8V, VIO: 1.8/3.3V

Key Benefits

- Complete software development kit with open-source TCP/IP and TLS stacks
- Operating temperature: –40°C to +105°C
- Support for 3-wire PTA coexistence interface for use with external 2.4GHz radios (for example Thread or Zigbee®)
- Antenna selection capability

Package

- Easy to design with 56-pin, 7mm × 7mm quad flat no leaded (QFN) package

2 Applications

- Building Automation
  - Thermostat
  - HVAC motor control
  - Wireless security camera
  - Video Doorbell
  - Garage door system
- Appliances
  - Refrigerator and freezer
  - Oven
  - Washer and dryer
  - Residential water heater
  - Air conditioner indoor unit
  - Coffee machine
  - Vacuum robot
  - Robotic lawn mower
- Grid Infrastructure
  - Electricity meter
  - String Inverter
  - Micro Inverter
  - Battery energy storage systems
  - EV charging infrastructure
- Medical
  - Infusion pump
  - Electronic hospital bed and bed control
  - Multiparameter patient monitor
  - CPAP machine
  - Telehealth systems
  - Ultrasound scanner
  - Ultrasound smart probe
  - Electric toothbrush
- Retail automation and payment
- Connected peripherals and printers
- Factory automation and control
- Asset tracking

3 Description

The SimpleLink™ Wi-Fi system-on-chip CC35xx family is where affordability meets reliability, enabling engineers to connect more applications with confidence. CC35xx are single-chip Wi-Fi 6 and Bluetooth Low Energy 5.4 wireless microcontrollers (MCUs). The CC3550E and CC3551E are the first dual-band devices in this pin-to-pin compatible family.

- CC3550E: 2.4GHz and 5GHz Wi-Fi 6 wireless MCU
- CC3551E: 2.4GHz and 5GHz Wi-Fi 6 and Bluetooth low energy 5.4 wireless MCU

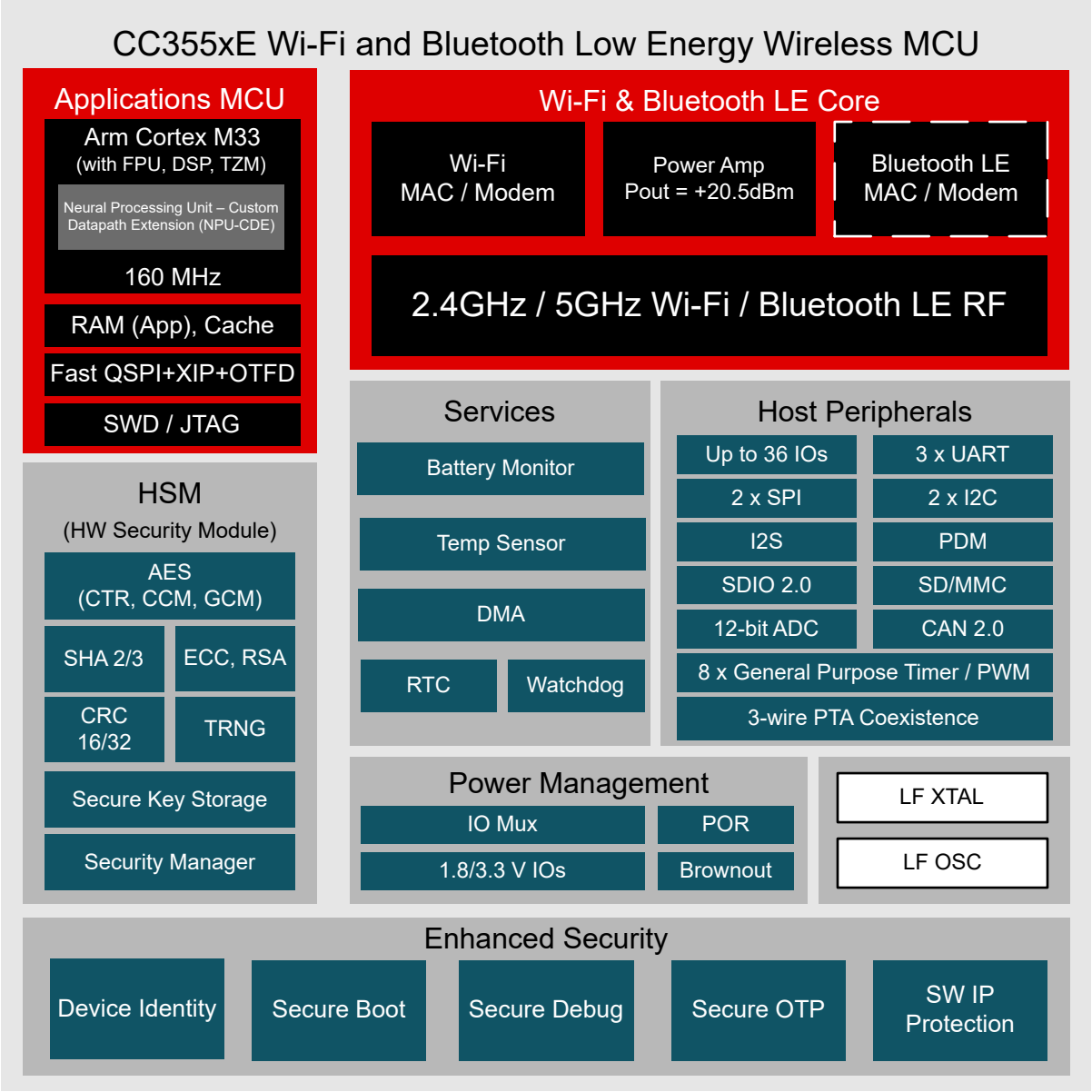
The CC355xE offers the latest standards from Wi-Fi and Bluetooth Low Energy while maintaining compatibility with Wi-Fi 4 (802.11 a/b/g/n) and Wi-Fi 5 (802.11 ac). These CC355xE are the 10th-generation connectivity combo chip from Texas Instruments. As such, the CC355xE is based on proven technology. These devices are an excellent choice to use in cost-sensitive embedded applications with RTOS software. CC355xE brings the efficiency of Wi-Fi 6 to embedded device applications for the Internet of Things (IoT), with a small PCB footprint and highly optimized bill of materials. Device flavors with in-package PSRAM for additional runtime memory are also available, see the table below.

Table 3-1. Device Information

PART NUMBER	FLASH	EXPANSION PSRAM	WI-FI 6 2.4GHz AND 5GHz SISO	BLUETOOTH LOW ENERGY	STATUS
CC3550ENJARSHR			✓		Production
CC3551ENJARSHR			✓	✓	Production
CC3551ESIARSHR		2MB	✓	✓	Preview
CC3551ETIARSHR		8MB	✓	✓	Production
CC3551EFIARSHR	4MB		✓	✓	Preview
CC3551EGIARSHR	8MB		✓	✓	Preview

4 Functional Block Diagram

The figure below shows a functional block diagram of the CC355xE.



– – – – CC3551E only

Figure 4-1. CC355xE High-Level System Diagram

Table of Contents

5 Pin Configuration and Functions

5.1 Pin Diagram

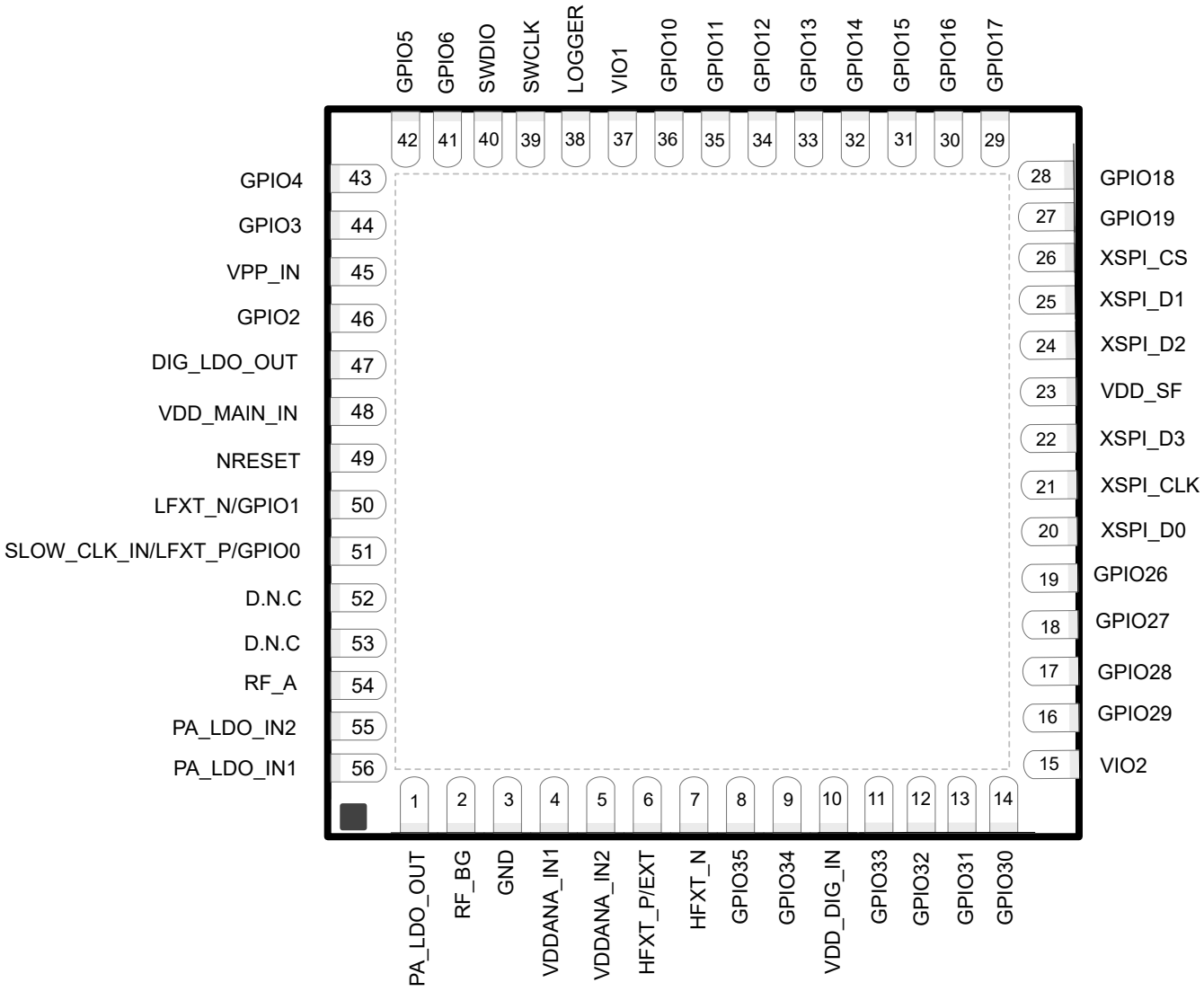


Figure 5-1. CC355xE Pin Diagram

5.2 Pin Attributes

Table 5-1. Pin Attributes

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
1	-	PA_LDO_OUT	Power	N/A	N/A	N/A	N/A
2	-	RF_BG	RF	N/A	N/A	N/A	N/A
3	-	GND	GND	N/A	N/A	N/A	N/A
4	-	VDDANA_IN1	Power	N/A	N/A	N/A	N/A
5	-	VDDANA_IN2	Power	N/A	N/A	N/A	N/A
6	-	HFXT_P/EXT	Analog	N/A	N/A	N/A	N/A
7	-	HFXT_N	Analog	N/A	N/A	N/A	N/A
8	GPIO35	SPI1_CLK	I/O	VIO2	3	PU	Hi-Z, Pull, Drive
		UART1_RX			5		
		I2C0_DATA			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT0_1			9		
		DCAN_RX			10		
		I2C1_DATA			11		
		SPI0_CS4			16		
		SPI0_CS3			17		
		GPT0_2_N			18		
		GPT1_2_N			19		
		COEX_PRIORITY			20		
		ANT_SEL_0			23		
		GPT1_PRE_EVENT			24		
		COEX_REQ			29		
		SDIO_CMD			30		
		UART2_RX			31		
9	GPIO34	SPI1_PICO	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART1_CTS			5		
		I2C1_DATA			6		
		I2S_BCLK			7		
		PDM_DATA1			8		
		GPT1_3			9		
		DCAN_RX			10		
		SPI0_CS2			16		
		GPT1_1_N			18		
		GPT0_3_N			19		
		COEX_REQ			20		
		SDIO_CLK			30		
		UART2_RX			31		
10	-	VDD_DIG_IN	Power	N/A	N/A	N/A	N/A

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
11	GPIO33	SPI1_POCI	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART1_RX			5		
		I2C0_CLK			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT1_2			9		
		DCAN_TX			10		
		SPI0_CS4			16		
		GPT1_0_N			18		
		GPT0_2_N			19		
		COEX_GRANT			20		
		GPT1_PRE_EVENT			24		
		SDIO_D0			30		
		UART2_CTS			31		
12	GPIO32	SPI1_CS1	I/O	VIO2	3	PU	Hi-Z, Pull, Drive
		SPI1_CLK			4		
		UART1_TX			5		
		I2C0_DATA			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT1_1			9		
		DCAN_RX			10		
		SPI0_CS3			16		
		GPT1_0_N			18		
		GPT0_1_N			19		
		COEX_REQ			20		
		SDIO_D1			30		
		UART2_RTS			31		
13	GPIO31	SPI1_CS1	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART1_RTS			5		
		I2C1_CLK			6		
		I2S_WCLK			7		
		PDM_BCLK			8		
		GPT1_0			9		
		DCAN_TX			10		
		SPI0_CS3			16		
		GPT1_1_N			18		
		GPT0_0_N			19		
		COEX_GRANT			20		
		ANT_SEL_0			23		
		GPT_INFRARED			24		
		SDIO_D2			30		
		UART2_TX			31		

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
14	GPIO30	I2C1_CLK	I/O	VIO2	5	PU	Hi-Z, Pull, Drive
		I2C0_CLK			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT1_1			9		
		DCAN_TX			10		
		SPI0_CS2			16		
		GPT0_2_N			18		
		COEX_GRANT			19		
		COEX_REQ			20		
		ANT_SEL_0			23		
		CCA			24		
		GPT1_PRE_EVENT			28		
		GPT0_PRE_EVENT			29		
		SDIO_D3			30		
		UART2_TX			31		
15	-	VIO2	Power	N/A	N/A	N/A	N/A
16	GPIO29	SPI0_PICO	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART0_CTS			5		
		I2C1_DATA			6		
		I2S_BCLK			7		
		PDM_DATA1			8		
		GPT0_3			9		
		DCAN_RX			10		
		I2S_MCLK			12		
		SPI1_CS4			16		
		GPT0_1_N			18		
		GPT1_3_N			19		
		COEX_GRANT			20		
		SDIO_OOB_IRQ			30		
		UART2_RX			31		
17	GPIO28	SPI0_POCI	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART0_RX			5		
		I2C0_CLK			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT0_2			9		
		SPI1_CS4			16		
		GPT0_0_N			18		
		GPT1_2_N			19		
		COEX_PRIORITY			20		
		GPT0_PRE_EVENT			24		
		UART2_CTS			31		

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
18	GPIO27	SPI0_CLK	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART0_TX			5		
		I2C0_DATA			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT0_1			9		
		SPI1_CS3			16		
		GPT0_0_N			18		
		GPT1_1_N			19		
		COEX_REQ			20		
		UART2_RTS			31		
19	GPIO26	SPI0_CS1	I/O	VIO2	4	PU	Hi-Z, Pull, Drive
		UART0_RTS			5		
		I2C1_CLK			6		
		I2S_WCLK			7		
		PDM_BCLK			8		
		GPT0_0			9		
		DCAN_TX			10		
		SPI1_CS2			16		
		GPT0_1_N			18		
		GPT1_0_N			19		
		COEX_GRANT			20		
		COEX_REQ			21		
		ANT_SEL_0			23		
		GPT_INFRARED			24		
		SDIO_OOB_IRQ			30		
		UART2_TX			31		
20	-	xSPI D0	I/O	VDD_SF	N/A	PU	Hi-Z, Pull, Drive
21	-	xSPI CLK	O	VDD_SF	N/A	PU	Hi-Z, Pull, Drive
22	-	xSPI D3	I/O	VDD_SF	N/A	PU	Hi-Z, Pull, Drive
23	-	VDD_SF	Power	N/A	N/A	N/A	N/A
24	-	xSPI D2	I/O	VDD_SF	N/A	PU	Hi-Z, Pull, Drive
25	-	xSPI D1	I/O	VDD_SF	N/A	PU	Hi-Z, Pull, Drive
26	-	xSPI CS	O	VDD_SF	N/A	PU	1

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
27	GPIO19	SPI0_PICO	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
		UART0_CTS			5		
		I2C1_CLK			6		
		I2S_BCLK			7		
		PDM_DATA0			8		
		GPT0_3			9		
		DCAN_RX			10		
		GPT0_PRE_EVENT			16		
		SDIO_OOB_IRQ			17		
		GPT0_1_N			18		
		SDIO_D3			19		
		COEX_PRIORITY			20		
		GPT1_3_N			21		
		GPT_INFRARED			22		
		UART2_RX			30		
28	GPIO18	SPI0_POCI	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
		UART0_RX			5		
		I2C0_DATA			6		
		I2S_DATA0			7		
		PDM_DATA1			8		
		GPT0_2			9		
		DCAN_TX			10		
		SPI1_CS4			16		
		SDIO_OOB_IRQ			17		
		GPT0_0_N			18		
		COEX_REQ			20		
		GPT1_2_N			21		
29	GPIO17	SDMMC_WP	I/O	VIO1	1	PU	Hi-Z, Pull, Drive
		SPI0_CLK			4		
		UART0_TX			5		
		I2C0_CLK			6		
		I2S_DATA1			7		
		PDM_DATA0			8		
		GPT0_1			9		
		SPI1_CS3			16		
		SDIO_OOB_IRQ			17		
		GPT0_0_N			18		
		COEX_GRANT			20		
		GPT1_1_N			21		

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
30	GPIO16	SPI0_CS1	I/O	VIO1	4	PU	Hi-Z, Pull, Drive
		UART0_RTS			5		
		I2C1_DATA			6		
		I2S_WCLK			7		
		PDM_BCLK			8		
		GPT0_0			9		
		SPI1_CS2			16		
		GPT0_1_N			18		
		SDIO_D2			19		
		GPT1_0_N			21		
		GPT_INFRARED			22		
		ANT_SEL_0			23		
		UART2_TX			30		
31	GPIO15	SDMMC_CMD	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_POCI			4		
		UART1_RX			5		
		UART0_CTS			6		
		GPT1_1			9		
		SPI0_CS2			16		
		GPT0_PRE_EVENT			17		
		GPT1_0_N			18		
		SDIO_D1			19		
		COEX_REQ			20		
32	GPIO14	SDMMC_CLK	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_CLK			4		
		UART1_TX			5		
		UART0_RX			6		
		GPT1_0			9		
		SPI0_CS2			16		
		GPT1_PRE_EVENT			17		
		GPT1_1_N			18		
		SDIO_D0			19		
		COEX_GRANT			20		

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
33	GPIO13	SDMMC_DATA_0	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_PICO			4		
		UART1_CTS			5		
		UART0_TX			6		
		I2S_BCLK			7		
		I2S_MCLK			8		
		GPT1_3			9		
		GPT1_2_N			18		
		SDIO_CMD			19		
		COEX_PRIORITY			20		
		ANT_SEL_0			23		
		UART2_RX			31		
34	GPIO12	SDMMC_DATA_1	I/O	VIO1	3	PU	Hi-Z, Pull, Drive
		SPI1_CS1			4		
		UART1_RTS			5		
		UART0_RTS			6		
		I2S_WCLK			7		
		GPT1_2			9		
		GPT0_PRE_EVENT			16		
		GPT1_PRE_EVENT			17		
		GPT1_3_N			18		
		SDIO_CLK			19		
		UART2_TX			31		
35	GPIO11	ADC0	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_RX			1		
		SDMMC_DATA_2			3		
		SPI1_CS1			4		
		UART1_CTS			5		
		I2C1_CLK			6		
		I2S_DATA0			7		
		PDM_DATA0			8		
		GPT1_1			9		
		DCAN_TX			10		
		SPI0_CS2			16		
		GPT1_2_N			18		
		SDIO_D2			19		
		COEX_REQ			20		
		CCA			24		
		UART2_CTS			30		
		UART2_RX			31		

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
36	GPIO10	ADC1	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_TX			1		
		SDMMC_DATA_3			3		
		SPI1_CLK			4		
		UART1_RTS			5		
		I2C1_DATA			6		
		I2S_DATA1			7		
		PDM_DATA1			8		
		GPT1_0			9		
		DCAN_RX			10		
		SPI0_CS3			16		
		GPT1_3_N			18		
		SDIO_D3			19		
		COEX_PRIORITY			20		
		COEX_GRANT			21		
		CCA			24		
		UART2_RTS			30		
		UART2_TX			31		
37	-	VIO1	Power	N/A	N/A	N/A	N/A
38	-	Logger [(3)]	O	VIO1	N/A	PU	Hi-Z, Pull, Drive
39	-	SWCLK	I	VIO1	N/A	PD	Hi-Z, Pull, Drive
40	-	SWDIO	I/O	VIO1	N/A	PU	Hi-Z, Pull, Drive

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
41	GPIO6	ADC2	I/O	VIO1		PU	Hi-Z, Pull, Drive
		SDMMC_POW1			3		
		SPI1_PICO			4		
		UART1_RX			5		
		I2C0_DATA			6		
		I2S_WCLK			7		
		PDM_DATA0			8		
		GPT1_3			9		
		DCAN_RX			10		
		SDMMC_WP			11		
		SPI0_CS4			16		
		I2S_BCLK			17		
		GPT1_1_N			18		
		SDIO_D1			19		
		COEX_PRIORITY			20		
		GPT0_3_N			21		
		GPT1_PRE_EVENT			22		
		ANT_SEL_0			23		
		CCA			24		
		COEX_GRANT			26		
		I2C1_CLK			28		
		SDMMC_POW2			29		
		UART2_CTS			30		
42	GPIO5	ADC3	I/O	VIO1		PU	Hi-Z, Pull, Drive
		SDMMC_POW2			3		
		SPI1_POCI			4		
		UART1_TX			5		
		I2C0_CLK			6		
		I2S_MCLK			7		
		PDM_BCLK			8		
		GPT1_2			9		
		DCAN_TX			10		
		SPI0_CS4			16		
		GPT1_0_N			18		
		SDIO_D0			19		
		COEX_REQ			20		
		GPT0_2_N			21		
		I2C1_DATA			28		
		UART2_RTS			30		

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
43	GPIO4	ADC4	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_RX			1		
		SDMMC_CD			3		
		SPI1_CS1			4		
		UART1_CTS			5		
		I2S_BCLK			6		
		I2S_DATA1			7		
		PDM_BCLK			8		
		GPT1_1			9		
		DCAN_TX			10		
		SPI0_CS2			16		
		GPT1_0_N			18		
		SDIO_CMD			19		
		COEX_PRIORITY			20		
		GPT0_1_N			21		
		I2C1_CLK			28		
		UART2_RX			30		
44	GPIO3	ADC5	I/O	VIO1		PU	Hi-Z, Pull, Drive
		UART1_TX			1		
		SDMMC_WP			3		
		SPI1_CLK			4		
		UART1_RTS			5		
		I2S_MCLK			6		
		I2S_DATA0			7		
		PDM_DATA1			8		
		GPT1_0			9		
		DCAN_RX			10		
		SPI0_CS3			16		
		GPT1_1_N			18		
		SDIO_CLK			19		
		COEX_REQ			20		
		GPT0_0_N			21		
		GPT_INFRARED			22		
		I2C1_DATA			28		
		UART2_TX			30		
45	-	VPP_IN	Power	N/A	N/A	N/A	N/A

Table 5-1. Pin Attributes (continued)

PIN No.	GPIO No.	SIGNAL NAME	SIGNAL TYPE [1]	IO RING	PIN MUX ENCODING	PAD STATES	
						RESET	LPDS [2]
46	GPIO2	ADC6	I/O	VIO1		PU	Hi-Z, Pull, Drive
		SDMMC_CD			3		
		I2C1_CLK			6		
		GPT1_3			9		
		DCAN_TX			10		
		SPI0_CS4			16		
		GPT1_PRE_EVENT			18		
		SDIO_OOB_IRQ			19		
		COEX_GRANT			20		
		COEX_REQ			21		
		CCA			24		
47	-	DIG_LDO_OUT	Power	N/A	N/A	N/A	N/A
48	-	VDD_MAIN_IN	Power	N/A	N/A	N/A	N/A
49	-	nRESET	I	N/A	N/A	N/A	N/A
50	GPIO1	LFXTAL_N	I/O	VIO1	0	PD	Hi-Z, Pull, Drive
		ADC7					
		GPT1_PRE_EVENT			7		
		GPT0_PRE_EVENT			8		
		GPT1_0			9		
		GPT0_0			10		
		GPT_INFRARED			11		
		SDIO_OOB_IRQ			19		
		COEX_GRANT			20		
		COEX_REQ			21		
		ANT_SEL_0			23		
51	GPIO0	LFXTAL_P	I/O	VIO1		PD	Hi-Z, Pull, Drive
		SLOW_CLK_IN			1		
		GPT1_1			9		
		GPT0_1			10		
		COEX_REQ			21		
52	D.N.C [3]	Do Not Connect					
53	D.N.C	Do Not Connect					
54	-	RF_A	RF	N/A	N/A	N/A	N/A
55	-	PA_LDO_IN2	Power	N/A	N/A	N/A	N/A
56	-	PA_LDO_IN1	Power	N/A	N/A	N/A	N/A

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.
(2) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
(3) Pin 52 and Logger are sensed by the device during boot, contact TI for more information.

5.3 Signal Descriptions

Table 5-2. Signal Descriptions

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR (1)	DESCRIPTION
ADC	ADC0	GPIO11	35	VIO1	I	ADC channel 0 input
	ADC1	GPIO10	36			ADC channel 1 input
	ADC2	GPIO6	41			ADC channel 2 input
	ADC3	GPIO5	42			ADC channel 3 input
	ADC4	GPIO4	43			ADC channel 4 input
	ADC5	GPIO3	44			ADC channel 5 input
	ADC6	GPIO2	46			ADC channel 6 input
	ADC7	GPIO1	50			ADC channel 7 input
Antenna Select	ANT_SEL_0	GPIO1	50	VIO1	O	Antenna Selection Control
		GPIO6	41			
		GPIO13	33			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
		GPIO35	8			
Clear Channel Assesment	CCA	GPIO2	46	VIO1	O	Clear Channel Assesment Flag
		GPIO10	36			
		GPIO11	35			
		GPIO30	14	VIO2		
Clocks	HFXT_P/External Input	-	6	N/A	N/A	52MHz crystal, HFXTAL_P pin
	HFXT_N	-	7	N/A	N/A	52MHz crystal, HFXTAL_N pin
	SLOW_CLOCK_IN	GPIO0	51	VIO1	I	32.768kHz oscillator clock input or crystal LFXTAL_P pin
	LFXT_N	GPIO1	50	VIO1	N/A	32.768kHz crystal LFXTAL_N pin

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR (1)	DESCRIPTION
Coexistence	COEX_REQ	GPIO0	51	VIO1	I	External Coexistence Interface - Request
		GPIO1	50			
		GPIO2	45			
		GPIO3	44			
		GPIO5	42			
		GPIO11	35			
		GPIO15	31			
		GPIO18	28			
		GPIO26	19	VIO2		
		GPIO27	18			
		GPIO30	14			
		GPIO32	12			
		GPIO34	9			
		GPIO35	8			
	COEX_GRANT	GPIO0	51	VIO1	O	External Coexistence Interface - Grant
		GPIO1	50			
		GPIO2	45			
		GPIO10	36			
		GPIO14	32			
		GPIO17	29			
		GPIO6	41			
		GPIO26	19	VIO2		
		GPIO29	16			
		GPIO30	14			
		GPIO31	13			
		GPIO33	11			
	COEX_PRIORITY	GPIO4	43	VIO1	I	External Coexistence Interface - Priority
		GPIO41	6			
		GPIO10	36			
		GPIO13	33			
		GPIO19	27			
		GPIO28	17	VIO2		
		GPIO35	8			

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
DCAN	DCAN_TX	GPIO2	46	VIO1	O	Controller Area Network - TX
		GPIO4	43			
		GPIO5	42			
		GPIO11	35			
		GPIO18	28			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
		GPIO33	11			
	DCAN_RX	GPIO3	44	VIO1	I	Controller Area Network - RX
		GPIO6	41			
		GPIO10	36			
		GPIO19	27			
		GPIO29	16	VIO2		
		GPIO32	12			
		GPIO34	9			
		GPIO35	8			
GPIO	GPIO0		51	VIO1	I/O	General Purpose Inputs or Outputs
	GPIO1		50			
	GPIO2		45			
	GPIO3		44			
	GPIO4		43			
	GPIO5		42			
	GPIO6		41			
	GPIO10		36			
	GPIO11		35			
	GPIO12		34			
	GPIO13		33			
	GPIO14		32			
	GPIO15		31			
	GPIO16		30			
	GPIO17		29			
	GPIO18		28			
	GPIO19		27			
	GPIO26		19	VIO2		
	GPIO27		18			
	GPIO28		17			
	GPIO29		16			
	GPIO30		14			
	GPIO31		13			
	GPIO32		12			
	GPIO33		11			
	GPIO34		9			
	GPIO35		8			

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR (1)	DESCRIPTION
I²C	I2C0_CLK	GPIO5	42	VIO1	I/O	I²C0 Clock SCL
		GPIO17	29			
		GPIO28	17	VIO2		
		GPIO30	14			
		GPIO33	11			
	I2C0_DATA	GPIO6	41	VIO1	I/O	I²C0 Data SDA
		GPIO18	28			
		GPIO27	18	VIO2		
		GPIO32	12			
		GPIO35	8			
	I2C1_CLK	GPIO2	45	VIO1	I/O	I²C1 Clock SCL
		GPIO4	43			
		GPIO6	41			
		GPIO11	35			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
	I2C1_DATA	GPIO3	44	VIO1	I/O	I²C1 Data SDA
		GPIO5	42			
		GPIO10	36			
		GPIO16	30			
		GPIO29	16	VIO2		
		GPIO34	9			
		GPIO35	8			

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
I²S	I2S_DATA0	GPIO3	44	VIO1	I/O	I²S Audio Port Data 0
		GPIO11	35			
		GPIO18	28			
		GPIO27	18	VIO2		
		GPIO33	11			
	I2S_DATA1	GPIO4	43	VIO1	I/O	I²S Audio Port Data 1
		GPIO10	36			
		GPIO17	29			
		GPIO28	17	VIO2		
		GPIO32	12			
		GPIO35	8			
	I2S_WCLK	GPIO6	41	VIO1	I/O	I²S Audio Port Word Transfer Clock
		GPIO12	34			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO31	13			
	I2S_BCLK	GPIO4	43	VIO1	I/O	I²S Audio Port Bit Clock
		GPIO13	33			
		GPIO19	27			
		GPIO29	16	VIO2		
		GPIO34	9			
	I2S_MCLK	GPIO3	44	VIO1	O	I²S Audio Port Controller Clock
		GPIO5	42			
		GPIO6	41			
		GPIO13	33			
		GPIO29	16	VIO2		
Logger		-	38	VIO1	O	Tracer (UART TX Debug Logger)
xSPI	xSPI_CLK	-	21	VDDSF	O	Clock to xSPI Flash/RAM
	xSPI_DATA_0	-	20		I/O	Data 0 to xSPI Flash/RAM
	xSPI_DATA_1	-	25		I/O	Data 1 to xSPI Flash/RAM
	xSPI_DATA_2	-	24		I/O	Data 2 to xSPI Flash/RAM
	xSPI_DATA_3	-	22		I/O	Data 3 to xSPI Flash/RAM
	xSPI_CS_FLASH	-	26	VDDSF	O	Chip select to xSPI Flash

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
PDM	PDM_Data0	GPIO6	41	VIO1	I	Pulse Density Modulation Data 0
		GPIO11	35			
		GPIO17	29			
		GPIO19	27			
		GPIO27	18	VIO2		
		GPIO30	14			
		GPIO33	11			
	PDM_Data1	GPIO3	44	VIO1	I	Pulse Density Modulation Data 1
		GPIO10	36			
		GPIO18	28			
		GPIO29	16	VIO2		
		GPIO34	9			
	PDM_BCLK	GPIO4	43	VIO1	O	Pulse Density Modulation Clock
		GPIO5	42			
		GPIO16	30			
		GPIO28	17	VIO2		
		GPIO31	13			
		GPIO32	12			
		GPIO35	8			
Power	VDDMAIN_IN	-	48	N/A	N/A	1.8V Supply Input for SRAM and Digital
	VDD_DIG_IN	-	10	N/A	N/A	Internal Digital Core Voltage - Must be Shorted to DIG_LDO_OUT
	VDD_ANA_IN1	-	4	N/A	N/A	1.8V supply to Analog Domain
	VDD_ANA_IN2	-	5	N/A	N/A	1.8V supply to Analog Domain
	VPP_IN	-	45	N/A	N/A	1.8V OTP Programming Input Supply
	PA_LDO_IN1	-	56	N/A	N/A	3.3V supply for PA
	PA_LDO_IN2	-	55	N/A	N/A	3.3V supply for PA
	VIO1	-	17	N/A	N/A	1.8/3.3V IO supply for IO Ring 1
	VIO2	-	15	N/A	N/A	1.8/3.3V IO supply for IO Ring 2
	VDDSF	-	23	N/A	N/A	1.8/3.3V IO supply for IO Ring VDD_SF
	DIG_LDO_OUT	-	47	N/A	N/A	Digital LDO output to VDD_DIG_IN
	PA_LDO_OUT	-	1	N/A	N/A	PA LDO output
nReset		-	49	N/A	N/A	Reset line for enabling or disabling device (active low)
RF	RF_BG	-	2	N/A	N/A	Bluetooth Low Energy and WLAN 2.4GHz RF port
	RF_A	-	54	N/A	N/A	WLAN 5GHz RF port

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
SDIO	SDIO_CLK	GPIO3	44	VIO1	I	SDIO Clock
		GPIO12	34			
		GPIO34	9	VIO2		
	SDIO_CMD	GPIO4	43	VIO1	I/O	SDIO Command
		GPIO13	33			
		GPIO35	8	VIO2		
	SDIO_D0	GPIO5	42	VIO1	I/O	SDIO Data 0
		GPIO14	32			
		GPIO33	11	VIO2		
	SDIO_D1	GPIO6	41	VIO1	I/O	SDIO Data 1
		GPIO15	31			
		GPIO32	12	VIO2		
	SDIO_D2	GPIO11	35	VIO1	I/O	SDIO Data 2
		GPIO16	30			
		GPIO31	13	VIO2		
	SDIO_D3	GPIO10	36	VIO1	I/O	SDIO Data 3
		GPIO19	27			
		GPIO30	14	VIO2		
	SDIO_OOB_IRQ	GPIO1	51	VIO1	O	SDIO out of band interrupt
		GPIO2	45			
		GPIO17	29			
		GPIO18	28			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO29	16			
SDMMC	SDMMC_CLK	GPIO14	32	VIO1	O	SDMMC Clock
	SDMMC_CMD	GPIO15	31	VIO1	I/O	SDMMC Command
	SDMMC_DATA_0	GPIO13	33	VIO1	I/O	SDMMC Data 0
	SDMMC_DATA_1	GPIO12	34	VIO1	I/O	SDMMC Data 1
	SDMMC_DATA_2	GPIO11	35	VIO1	I/O	SDMMC Data 2
	SDMMC_DATA_3	GPIO10	36	VIO1	I/O	SDMMC Data 3
	SDMMC_CD	GPIO2	45	VIO1	I	SDMMC Card Detect
		GPIO4	43			
	SDMMC_WP	GPIO3	43	VIO1	I	SDMMC Write Protect
		GPIO6	41			
		GPIO11	41			
		GPIO17	29			
	SDMMC_POW1	GPIO6	41	VIO1	O	SDMMC power supply control 1
	SDMMC_POW2	GPIO5	42	VIO1	O	SDMMC power supply control 2

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
SPI	SPI0_CLK	GPIO17	29	VIO1	I/O	General SPI0 Clock
		GPIO27	18	VIO2		
	SPI0_POCI	GPIO18	28	VIO1	I/O	General SPI0 POCI
		GPIO28	17	VIO2		
	SPI0_PICO	GPIO19	27	VIO1	I/O	General SPI0 PICO
		GPIO29	16	VIO2		
	SPI0_CS1	GPIO16	30	VIO1	I/O	General SPI0 Chip select 1
		GPIO26	19	VIO2		
	SPI0_CS2	GPIO4	43	VIO1	I/O	General SPI0 Chip select 2
		GPIO11	35			
		GPIO14	32			
		GPIO30	14	VIO2		
		GPIO34	9			
	SPI0_CS3	GPIO3	34	VIO1	I/O	General SPI0 Chip select 3
		GPIO10	36			
		GPIO31	13	VIO2		
		GPIO32	12			
	SPI0_CS4	GPIO2	45	VIO1	I/O	General SPI0 Chip select 4
		GPIO5	42			
		GPIO6	41			
		GPIO33	11	VIO2		
		GPIO35	8			
	SPI1_CLK	GPIO3	44	VIO1	I/O	General SPI1 Clock
		GPIO10	36			
		GPIO14	32			
		GPIO32	12	VIO2		
		GPIO35	8			
	SPI1_POCI	GPIO5	42	VIO1	I/O	General SPI1 POCI
		GPIO15	31			
		GPIO33	11	VIO2		
	SPI1_PICO	GPIO6	41	VIO1	I/O	General SPI1 PICO
		GPIO13	33			
		GPIO34	19	VIO2		
	SPI1_CS1	GPIO4	43	VIO1	I/O	General SPI1 Chip select 1
		GPIO11	35			
		GPIO12	34			
		GPIO31	13	VIO2		
		GPIO32	12			
	SPI1_CS2	GPIO15	32	VIO1	I/O	General SPI1 Chip select 2
		GPIO16	30			
		GPIO26	19	VIO2		
	SPI1_CS3	GPIO17	29	VIO1	I/O	General SPI1 Chip select 3
		GPIO27	18	VIO2		

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
SPI	SPI1_CS4	GPIO18	28	VIO1	I/O	General SPI1 Chip select 4
		GPIO28	17	VIO2		
		GPIO29	16			
SWD	SWDIO	-	40	VIO1	I/O	Serial Wire Debug I/O
	SWCLK	-	39		I	Serial Wire Debug Clock
Timers_0	GPT0_0	GPIO1	50	VIO1	I/O	General Purpose Timer 0 Channel 0
		GPIO16	30			
		GPIO26	19	VIO2		
	GPT0_1	GPIO0	51	VIO1	I/O	General Purpose Timer 0 Channel 1
		GPIO17	29			
		GPIO27	18	VIO2		
		GPIO35	8			
	GPT0_2	GPIO18	28	VIO1	I/O	General Purpose Timer 0 Channel 2
		GPIO28	17	VIO2		
	GPT0_3	GPIO19	27	VIO1	I/O	General Purpose Timer 0 Channel 3
		GPIO29	16	VIO2		
	GPT0_0_N	GPIO3	44	VIO1	I/O	General Purpose Timer 0 Channel 0 Negative
		GPIO17	29			
		GPIO18	28			
		GPIO27	18	VIO2		
		GPIO28	17			
		GPIO31	13			
	GPT0_1_N	GPIO4	43	VIO1	I/O	General Purpose Timer 0 Channel 1 Negative
		GPIO16	30			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO29	16			
		GPIO32	12			
	GPT0_2_N	GPIO5	42	VIO1	I/O	General Purpose Timer 0 Channel 2 Negative
		GPIO30	14	VIO2		
		GPIO33	11			
		GPIO35	8			
	GPT0_3_N	GPIO6	41	VIO1	I/O	General Purpose Timer 0 Channel 3 Negative
		GPIO34	9	VIO2		
	GPT0_PRE_EVENT	GPIO1	50	VIO1	O	General Purpose Timer 0 PreEvent Signal
		GPIO12	34			
		GPIO15	31			
		GPIO19	27			
		GPIO28	17	VIO2		
		GPIO30	14			

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
Timers_1	GPT1_0	GPIO1	50	VIO1	I/O	General Purpose Timer 1 Channel 0
		GPIO3	44			
		GPIO10	35			
		GPIO14	32			
		GPIO31	13	VIO2		
	GPT1_1	GPIO0	51	VIO1	I/O	General Purpose Timer 1 Channel 1
		GPIO4	43			
		GPIO11	35			
		GPIO15	31			
		GPIO30	14	VIO2		
		GPIO32	12			
	GPT1_2	GPIO5	42	VIO1	I/O	General Purpose Timer 1 Channel 2
		GPIO12	34			
		GPIO33	11	VIO2		
	GPT1_3	GPIO2	45	VIO1	I/O	General Purpose Timer 1 Channel 3
		GPIO6	41			
		GPIO13	33			
		GPIO34	9	VIO2		
	GPT1_0_N	GPIO4	43	VIO1	I/O	General Purpose Timer 1 Channel 0 Negative
		GPIO5	42			
		GPIO15	31			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO32	12			
		GPIO33	11			
	GPT1_1_N	GPIO3	44	VIO1	I/O	General Purpose Timer 1 Channel 1 Negative
		GPIO6	41			
		GPIO14	32			
		GPIO17	29			
		GPIO27	18	VIO2		
		GPIO31	13			
		GPIO34	9			
	GPT1_2_N	GPIO11	35	VIO1	I/O	General Purpose Timer 1 Channel 2 Negative
		GPIO13	33			
		GPIO18	28			
		GPIO28	17	VIO2		
		GPIO35	8			
	GPT1_3_N	GPIO10	36	VIO1	I/O	General Purpose Timer 1 Channel 3 Negative
		GPIO12	34			
		GPIO19	27			
		GPIO29	16	VIO2		

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR [1]	DESCRIPTION
Timers_1	GPT1_PRE_EVENT	GPIO1	50	VIO1	O	General Purpose Timer 1 PreEvent Signal
		GPIO2	45			
		GPIO6	41			
		GPIO12	34			
		GPIO14	32			
		GPIO33	11	VIO2		
		GPIO35	8			
Timers_Infrared	GPT_INFRARED	GPIO1	50	VIO1	O	General Purpose Timer Infrared Signal
		GPIO3	44			
		GPIO16	30			
		GPIO19	27			
		GPIO26	19	VIO2		
		GPIO31	13			
UART	UART0_TX	GPIO13	33	VIO1	O	UART0 TX
		GPIO17	29			
		GPIO27	18	VIO2		
	UART0_RX	GPIO14	32	VIO1	I	UART0 RX
		GPIO18	28			
		GPIO28	17	VIO2		
	UART0_RTS	GPIO12	34	VIO1	O	UART0 request to send
		GPIO16	30			
		GPIO26	19	VIO2		
	UART0_CTS	GPIO15	31	VIO1	I	UART0 clear to send
		GPIO19	27			
		GPIO29	16	VIO2		
	UART1_TX	GPIO3	44	VIO1	O	UART1 TX
		GPIO5	42			
		GPIO10	36			
		GPIO14	32			
		GPIO32	12	VIO2		
	UART1_RX	GPIO4	43	VIO1	I	UART1 RX
		GPIO6	41			
		GPIO11	35			
		GPIO15	31			
		GPIO33	11	VIO2		
		GPIO35	8			
	UART1_RTS	GPIO3	44	VIO1	O	UART1 request to send
		GPIO10	36			
		GPIO12	34			
		GPIO31	13	VIO2		
	UART1_CTS	GPIO4	43	VIO1	I	UART1 clear to send
		GPIO11	35			
		GPIO13	33			
		GPIO34	9	VIO2		

Table 5-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	GPIO NO.	PIN NO.	IO RING	DIR (1)	DESCRIPTION
UART	UART2_TX	GPIO3	44	VIO1	O	UART2 TX
		GPIO10	36			
		GPIO12	34			
		GPIO16	30			
		GPIO26	19	VIO2		
		GPIO30	14			
		GPIO31	13			
	UART2_RX	GPIO4	43	VIO1	I	UART2 RX
		GPIO11	35			
		GPIO13	33			
		GPIO19	27			
		GPIO29	16	VIO2		
		GPIO34	9			
		GPIO35	8			
	UART2_RTS	GPIO5	42	VIO1	O	UART2 request to send
		GPIO10	36			
		GPIO27	18	VIO2		
		GPIO32	12			
	UART2_CTS	GPIO6	41	VIO1	I	UART2 clear to send
		GPIO11	35			
		GPIO28	17	VIO2		
		GPIO33	11			

(1) Drive strength for GPIO's can be user defined.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		PINS	MIN	MAX	UNIT
V_{PA}	V_{DD} PA Voltage	55,56	–0.5	4.2	V
V_{MAIN}	Main supply voltage for analog and digital - VDD_MAIN_IN, VDD_ANA_IN1, VDD_ANA_IN2	48,4,5	–0.5	2.1	V
V_{IO}	VDD IO Voltage	37,15	–0.5	3.6	V
	Input Voltage to all digital pins		–0.5	V_{IO} + 0.5	V
	HFXT_P Input Voltage	6	–0.5	2.1	V
V_{PP}	VPP OTP Voltage	45	–0.5	2.1	V
T_A	Operating Ambient Temperature	N/A	–40	105	°C
T_{stg}	Storage temperature	N/A	–55	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	RF pins	±1000	V
			Other pins	±2000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	RF pins	±250	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	MIN	TYP	MAX	UNIT
V_{MAIN}	Main supply voltage digital and analog - VDD_MAIN_IN, VDD_ANA_IN1, VDD_ANA_IN2	48,4,5	1.71	1.8	1.98	V
V_{PA}	DC supply rail for PA	55,56	3	3.3	3.6	
V_{IO} (2) (3)	DC supply rail for input/output	37,15, 23	1.71/3	1.8/3.3	1.98/3.6	
V_{PP}	DC supply rail for OTP memory	45	1.71	1.8	1.98	
T_A	Operating ambient temperature	N/A	–40		85/105(1)	°C
	Maximum power dissipation	N/A			2	W

(1) The CC35xxE devices may operate at temperatures of up to 105°C. This allows the device to be used reliably in applications that may be exposed to higher ambient temperature over certain periods of the product's life. At temperatures higher than 85°C, the WLAN/Bluetooth LE performance may degrade.
(2) VIO pins can be set to either 1.8 or 3.3 V.
(3) VIO2 and VDDSF must be set to 1.8V for CC35x1ES and CC35x1ET devices

6.4 Electrical Characteristics

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
GPIO pullup current	Input mode, pullup enabled, Vpad = 0V	VIO = 1.8V	9	20	42	µA
		VIO = 3.3V	45	86	155	
GPIO pulldown current	Input mode, pullup enabled, Vpad = 0V	VIO = 1.8V	9	20	43	
		VIO = 3.3V	39	80	151	
V_{IH}	High Level Input Voltage		0.7 x V_{IO}		V_{IO}	V
V_{IL}	Low Level Input Voltage		0		0.3 x V_{IO}	
V_{OH}	High Level Output Voltage	at 4mA	V_{IO} – 0.4		V_{IO}	
V_{OL}	Low Level Output Voltage	at 4mA(1)	0		0.4	

(1) Low drive GPIO in low drive mode tested at 2mA.

6.5 Thermal Resistance Characteristics

THERMAL METRIC(1)	DESCRIPTION		UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (According to JEDEC EIA/JESD 51 document)	22.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	
Ψ_{JT}	Junction-to-top characterization parameter	0.2	
Ψ_{JB}	Junction-to-board characterization parameter	6.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 WLAN Performance: 2.4-GHz Receiver Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		2412		2472	MHz
Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 Mbps DSSS		-98.7		dBm
	2 Mbps DSSS		-96.3		
	11 Mbps CCK		-90.7		
	6 Mbps OFDM		-94		
	54 Mbps OFDM		-76.6		
	HT MCS0 MM 4K		-93.7		
	HT MCS7 MM 4K		-74.5		
	HE MCS0 4K		-93.7		
	HE MCS7 4K		-74.7		
Maximum input level: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 DSSS		0		dBm
	OFDM6, HT MCS0, HE MCS0		0		
	OFDM54, HT MCS7, HE MCS7		-10		

6.6 WLAN Performance: 2.4-GHz Receiver Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Adjacent Channel Rejection	1 Mbps DSSS		45		dB
	11 Mbps CCK		39		
	6 Mbps OFDM		25		
	54 Mbps OFDM		10		
	HT MCS0		23		
	HT MCS7		5		
	HE MCS0		16		
	HE MCS7		-1		
RSSI Accuracy	-90 dBm to -30dBm	-3		3	dB

6.7 WLAN Performance: 2.4-GHz Transmitter Power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		2412		2472	MHz
Maximum output power at V_{PA} > 3.0 V	1 Mbps DSSS		20.5		dBm
	6 Mbps OFDM		20.2		
	54 Mbps OFDM		17.8		
	HT MCS0 MM		20.2		
	HT MCS7 MM		17.7		
	HE MCS0		20.2		
	HE MCS7		17.6		

6.8 WLAN Performance: 5-GHz Receiver Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		5180		5845	MHz
Sensitivity (10% PER for 11a/n/ax rates)	6Mbps OFDM		-93.7		dBm
	54Mbps OFDM		-76.2		
	HT MCS0 MM 4K		-93.4		
	HT MCS7 MM 4K		-74		
	HE MCS0 4K		-93.4		
	HE MCS7 4K		-74.2		
Maximum input level (10% PER for 11a/n/ax rates)	6OFDM, HT MCS0, HE MCS0		-8.5		dBm
	54OFDM, HT MCS7, HE MCS7		-17.5		
Adjacent Channel Rejection	6Mbps OFDM		20		dB
	54Mbps OFDM		3		
	HT MCS0		18		
	HT MCS7		0		
	HE MCS0		16		
	HE MCS7		1		
RSSI Accuracy	-90dBm to -30dBm	-3		3	dB

6.9 WLAN Performance: 5-GHz Transmitter Power

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		5180		5845	MHz
Maximum output power at V_{PA} > 3.0 V	6 Mbps OFDM		19.7		dBm
	54 Mbps OFDM		15.4		
	HT MCS0 MM		19.9		
	HT MCS7 MM		15.3		
	HE MCS0 20 MHz		19.7		
	HE MCS7 20 MHz		14.3		

6.10 Bluetooth LE Performance: Receiver Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Bluetooth LE 125Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity	PER <30.2%		-104.4		dBm
Receiver saturation	PER <30.2%		0		dBm
Co-channel rejection(1)	Wanted signal at -79 dBm, modulated interferer in channel		10		dB
Selectivity, ±1 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±1 MHz.		2/2(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±2 MHz.		-40 / -30(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±3 MHz.		-45 / -40(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±4 MHz.		-48 / -43(2)		dB
RSSI Accuracy	Dynamic range of -90 to -20dBm	-4		4	dB
Bluetooth LE 500Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity	PER <30.2%		-101.3		dBm
Receiver saturation	PER <30.2%		0		dBm
Co-channel rejection(1)	Wanted signal at -72 dBm, modulated interferer in channel.		9		dB
Selectivity, ±1 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±1 MHz.		2/2(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±2 MHz.		-40 / -30(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±3 MHz.		-45 / -40(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±4 MHz.		-48 / -43(2)		dB
RSSI Accuracy	Dynamic range of -90 to -20dBm	-4		4	dB
Bluetooth LE 1Mbps (LE 1M) Receiver Characteristics					
Receiver sensitivity(3)	PER <30.2%, 37-byte packets		-99.9		dBm
Receiver sensitivity(3)	PER <30.2%, 255 byte-packets		-98.6		dBm
Receiver saturation	PER <30.2%		0		dBm
Co-channel rejection(1)	Wanted signal at -67 dBm, modulated interferer in channel		8		dB
Selectivity, ±1 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±1 MHz		-5 / -5(2)		dB

6.10 Bluetooth LE Performance: Receiver Characteristics (continued)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Selectivity, ±2 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±2 MHz.		-40 / -30(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±3 MHz		-45 / -40(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±4 MHz		-48 / -43		dB
Out-of-band blocking	30 MHz to 2000 MHz, Wanted signal at -67 dBm		–23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	2484 MHz to 2997 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	3000 MHz to 6 GHz, Wanted signal at -67 dBm		–21		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–40		dBm
RSSI accuracy	Dynamic range of -90 to -20dBm	-4		4	dB
Bluetooth LE 2Mbps (LE 2M) Receiver Characteristics					
Receiver sensitivity(4)	PER <30.2%		-95.8		dBm
Receiver saturation	PER <30.2%		0		dBm
Co-channel rejection(1)	Wanted signal at -67 dBm, modulated interferer in channel		8		dB
Selectivity, ±2 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±2 MHz.		-5 / -4(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±4 MHz		-40 / -30(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±6 MHz		-40 / -38(2)		dB
Alternate channel rejection, ±8 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±8 MHz		-45 / -40(2)		dB
Out-of-band blocking	30 MHz to 2000 MHz, Wanted signal at -67 dBm		–23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	2484 MHz to 2997 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	3000 MHz to 6 GHz, Wanted signal at -67 dBm		–21		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–44		dBm
RSSI Accuracy	Dynamic range of -90 to -20dBm	-4		4	dB

(1) Numbers given as C/I dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Bluetooth LE 1M and coded PHY sensitivity on channel 19 may degrade by up to 2.5 dB
(4) Bluetooth LE 2M PHY sensitivity on channel 19 may degrade by up to 1.5 dB

6.11 Bluetooth LE Performance - Transmitter Characteristics

The CC355XE devices support Bluetooth LE TX setting 0,5,10, or 20 dBm

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Output Power, highest setting			20		dBm

6.12 Current Consumption - 2.4GHz WLAN Static Modes

All results are based on measurements taken using the RadioTool evaluation application (typ values are taken with nominal devices at room temp).

PARAMETER	TEST CONDITIONS		V_{MAIN}		V_{PA}		UNIT
			TYP	MAX	TYP	MAX	
TX (Continuous)(1)	1 DSSS	TX Power = 20.5 dBm	120	195	310	335	mA
	6 OFDM	TX Power = 20.2 dBm	134	210	298	342	
	54 OFDM	TX Power = 17.8 dBm	141		242		
	HT MCS0	TX Power = 20.2 dBm	136		305		
	HT MCS7	TX Power = 17.7 dBm	141		242		
	HE MCS0	TX Power = 20.2 dBm	134		304		
	HE MCS7	TX Power = 17.6 dBm	139		240		
RX	Continuous Listen (for Beacon)		60		0		mA
	Active RX		64		0.4		

(1) Peak current V_{PA} can reach up to 495mA during device calibration.
Peak current V_{MAIN} is 400mA including peripherals and internal cortex

6.13 Current Consumption - 5GHz WLAN Static Modes

All results are based on measurements taken using the RadioTool evaluation application (typ values are taken with nominal devices at room temp).

PARAMETER	TEST CONDITIONS		V_{MAIN}		V_{PA}		UNIT
			TYP	MAX	TYP	MAX	
TX (Continuous)(1)	6 OFDM	TX Power = 19.7 dBm	193	275	295	348	mA
	54 OFDM	TX Power = 15.4 dBm	196		224		
	HT MCS0	TX Power = 19.9 dBm	195		305		
	HT MCS7	TX Power = 15.3 dBm	196		224		
	HE MCS0	TX Power = 19.7 dBm	193		302		
	HE MCS7	TX Power = 14.3 dBm	194		214		
RX	Continuous Listen (for Beacon)		96		0		mA
	Active RX		117		0.4		

(1) Peak current V_{PA} can reach up to 495mA during device calibration.
Peak current V_{MAIN} is 400mA including peripherals and internal cortex

6.14 Current Consumption - 2.4GHz WLAN Use Cases

MODE	DESCRIPTION	TYP(1) (2)	UNIT
System with 3.3V to Ext. DC/DC at 85% Efficiency			
DTIM = 1	WLAN beacon reception every DTIM=1 (~102ms)	975	µA
DTIM = 3	WLAN beacon reception every DTIM=3 (~306ms)	570	
DTIM = 10	WLAN beacon reception every DTIM=10 (~1020ms)	430	
System with 1.8V			
DTIM = 1	WLAN beacon reception every DTIM=1 (~102ms)	1520	µA
DTIM = 3	WLAN beacon reception every DTIM=3 (~306ms)	890	
DTIM = 10	WLAN beacon reception every DTIM=10 (~1020ms)	670	

(1) Current referenced to V_{Main} supply
(2) These are target values, measured values reflecting ongoing optimization can be found in SDK documentation.

6.15 Current Consumption - Bluetooth LE Static Modes

All results are based on measurements taken using the RadioTool evaluation application (typ values are taken with nominal devices at room temp).

PARAMETER	TEST CONDITIONS	V_{MAIN}		V_{PA}		UNIT
		TYP	MAX	TYP	MAX	
TX (Continuous)	TX Power = 0dBm	110		58		mA
	TX Power = 10dBm	111		135		
	TX Power = 20dBm	113		315		
RX		64		0.4		

6.16 Current Consumption - MCU Modes

PARAMETER		TEST CONDITIONS	V_{MAIN}	V_{PA}	UNIT
			TYP	TYP	
MCU Sleep	Memory Retention Sleep	Full Memory Retention	520		µA
Host MCU Active, Wireless Core Sleep	Host MCU 160MHz running, Wi-Fi/Bluetooth LE Core sleep		22		mA
Host MCU Shutdown		External supplies are available, device held in reset (nReset is low)	14	4	µA

6.17 Timing and Switching Characteristics

6.17.1 Clock Specifications

The CC355xE device uses two clocks for operation:

- A fast clock running at 52 MHz for active MCU functions and peripherals, as well as WLAN/Bluetooth LE.
- A slow clock running at 32.768 kHz for low power modes. The slow clock can be generated internally or externally.

6.17.1.1 Fast Clock Using an External Crystal (XTAL)

The CC355xE device supports a crystal-based fast clock (XTAL). The crystal is fed directly between HFXT_P and HFXT_M pins with compatible loading capacitors, and must meet the requirements below.

6.17.1.1.1 External Fast Clock XTAL Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported frequencies			52		MHz
Frequency accuracy	Initial + temperature + aging	-20		+20	ppm
Load Capacitance, C_L (1)		5		13	pF
Equivalent series resistance, ESR				40	Ω
Drive level			100		uW

(1) Load capacitance, C_L= [C1*C2] / [C1 + C2] + C_P, where C1, C2 are the capacitors connected on HFXT_P and HFXT_M, respectively, and C_P is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and C_P = 2pF, then C_L = 5pF.

6.17.1.2 Slow Clock Using Internal Oscillator

In order to minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less accurate and consumes more power than sourcing the slow clock externally.

6.17.1.3 Slow Clock Using an External Oscialltor

For optimal power consumption, the slow clock can be generated externally by an oscillator, XTAL, or sourced from elsewhere in the system. If using an oscialltor, the external source must meet the requirements listed below. This clock should be fed into the CC355xE pin Slow_CLK_IN/ GPIO0 and should be stable before nReset is deasserted and device is enabled. The clock signal logic high should be the same voltage as VIO1 IO Ring.

6.17.1.3.1 External Slow Clock Oscillator Specifications

PARAMETER		Description	MIN	TYP	MAX	UNIT
	Input slow clock frequency	Square wave		32.768		kHz
	Frequency accuracy	Inital + temperature + aging	-250		+250	ppm
	Input Duty cycle		30	50	70	%
T_r/T_f	Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
	Input impedence		1			MΩ
	Input capacitance				5	pF

6.17.1.4 Slow Clock Using an External Crystal (XTAL)

For optimal power consumption, the slow clock can be generated externally by an oscillator, XTAL, or sourced from elsewhere in the system. If using an XTAL, the external source must meet the requirements listed below. The crystal pins should be fed into the CC355xE pins LFXT_P/ GPIO0 and LFXT_N/GPIO1.

6.17.1.4.1 External Slow Clock XTAL Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported frequencies			32.768		kHz
Frequency accuracy	Initial + temperature + aging	-250		+250	ppm
Load Capacitance, C_L (1)		3		12.5	pF
Equivalent series resistance, ESR				100	kΩ

(1) Load capacitance, C_L= [C1*C2] / [C1 + C2] + C_P, where C1, C2 are the capacitors connected on LFXT_P and LFXT_M, respectively, and C_P is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and C_P = 2pF, then C_L = 5pF.

6.17.2 Peripheral Characteristics

6.17.2.1 ADC

The CC355xE supports eight ADC channels, 12-bit, with the following specifications.

6.17.2.1.1 ADC Electrical Specifications

Over operating free-air temperature range (unless otherwise noted).

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions						
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins, VIO1 = 3.3V	0		3.2	V
		All ADC analog input pins, VIO1 = 1.8V	0		1.8	
V_{R+}	Positive ADC reference voltage	ADC reference sourced from external reference pin (VeREF+)		1.8		V
ADC Switching Characteristics						
F_S ADCREF	ADC sampling frequency when using the internal ADC reference voltage				1	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage				2	Msps
ADC Linearity Parameters						
E_I	Integral linearity error (INL)		-2	+/ -1	2	LSB
E_D	Differential linearity error (DNL)		-1	+/- 0.5	1	LSB
E_O	Offset error - even channel		-3	+/- 2	3	LSB
E_G	Gain error		-100	+/- 3	100	LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits			11		bit
SINAD	Signal-to-noise and distortion ratio	External Reference		66		dB
		Internal Reference		63		

6.17.2.2.1 I²C Timing Parameters

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		Standard Mode		Fast Mode		Fast Mode Plus		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START	4		0.6		0.26		µs
t_{LOW}	LOW period of the SCL clock	4.7		1.3		0.5		µs
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	4.7		0.6		0.26		µs
$t_{HD,DAT}$	Data hold time	0		0		0		µs
$t_{SU,DAT}$	Data setup time	250		100		50		µs
$t_{SU,STO}$	Setup time for STOP	4		0.6		0.26		µs
t_{buf}	bus free time between a STOP and START condition	4.7		1.3		0.5		µs
$t_{VD,DAT}$	data valid time		3.45		0.9		0.45	µs
$t_{VD,ACK}$	data valid acknowledge time		3.45		0.9		0.45	µs

6.17.2.2.2 I²C Timing Diagram

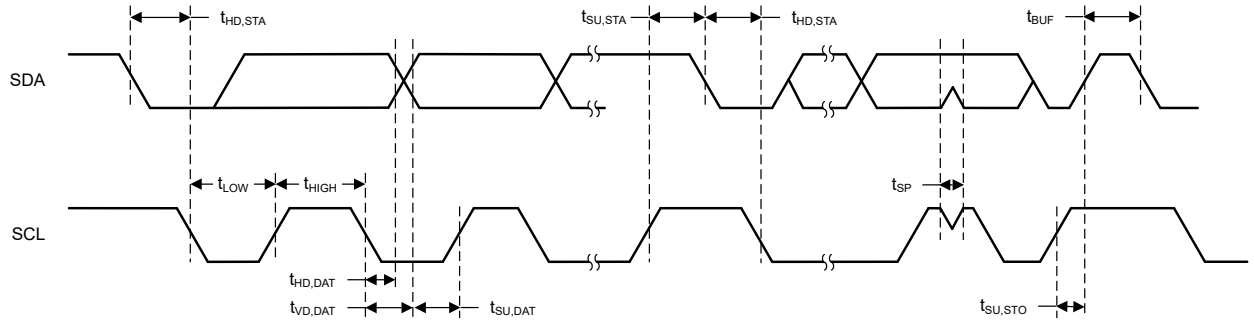


Figure 6-1. I²C Timing Diagram

6.17.2.3 SPI

6.17.2.3.1 SPI Timing Parameters - Controller Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	SPI clock frequency	Controller Mode			40	MHz
DC_{SCLK}	SCLK Duty Cycle		47.5	50	52.5	%
$t_{CS.LEAD}$	CS lead-time, CS active to clock	Motorola Clock Phase 0, National Semiconductor (Microwire)	1			SCLK
$t_{CS.LEAD}$	CS lead-time, CS active to clock	Motorola Clock Phase 1	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 0, National Semiconductor (Microwire)	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 1	1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1	SCLK
$t_{SU.CI}$	POCI input data setup time(3)		15.9			ns
$t_{HD.CI}$	POCI input data hold time		0			ns
$t_{VALID.CO}$	PICO output data valid time(1)	SCLK edge to PICO valid, C_L = 20pF			2.2	ns
$t_{HD.CO}$	PICO output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge
(3) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.

6.17.2.3.2 SPI Timing Diagrams - Controller Mode

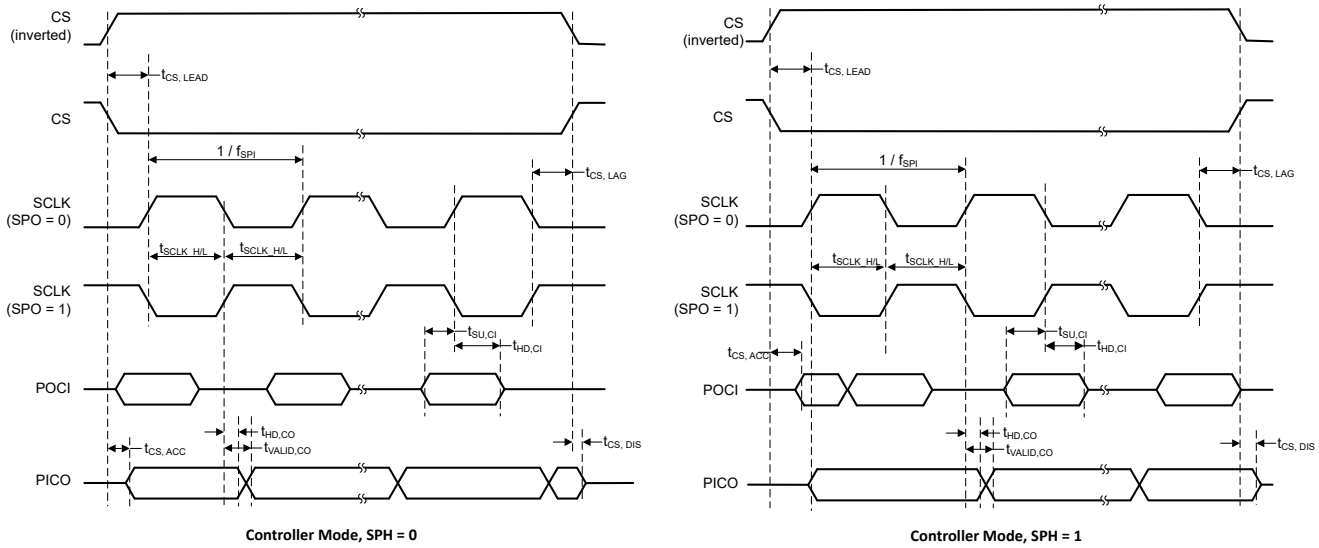


Figure 6-2. SPI Timing Diagram - Controller Mode

6.17.2.3.3 SPI Timing Parameters - Peripheral Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted),

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	SPI clock frequency	Peripheral Mode			30	MHz
DC_{SCLK}	SCLK Duty Cycle		45	50	55	%
$t_{CS.LEAD}$	CS lead-time, CS active to clock	Motorola Clock Phase 0, National Semiconductor (Microwire)	1			SCLK
$t_{CS.LEAD}$	CS lead-time, CS active to clock	Motorola Clock Phase 1	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 0, National Semiconductor (Microwire)	0.5			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	Motorola Clock Phase 1	1			SCLK
$t_{CS.ACC}$	CS access time, CS active to POCI data out				15	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance				15	ns
$t_{SU.PI}$	PICO input data setup time		2.8			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid, C_L = 20pF			10.2	ns
$t_{HD.PO}$	POCI output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

6.17.2.3.4 SPI Timing Diagrams - Peripheral Mode

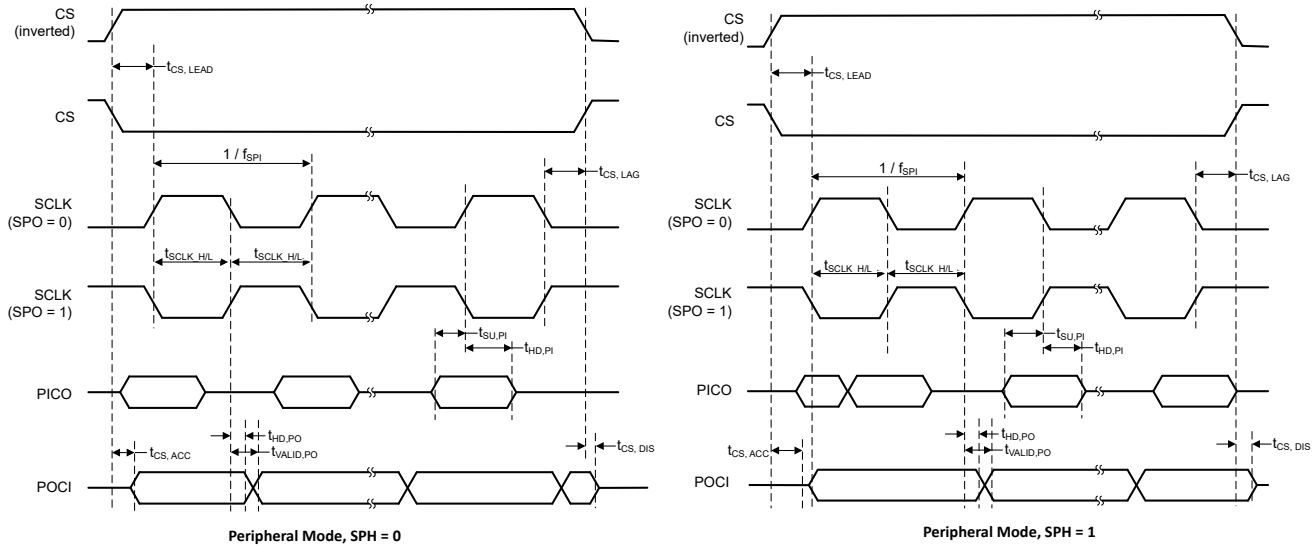


Figure 6-3. SPI Timing Diagram - Peripheral Mode

6.17.2.4 xSPI

The CC355xE device requires external serial flash for application code. The interface to the flash can be with Quad SPI (QSPI) interface.

6.17.2.4.1 QSPI Timing Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Q_{CLK}	QSPI Clock frequency, CLK		80	MHz

6.17.2.5 UART

6.17.2.5.1 UART Timing Parameters

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baud rate		37.5		4364	kbps

6.17.2.6 I^2S

6.17.2.6.1 I^2S Timing Parameters - Controller Mode

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	clock frequency, BCLK	Controller Mode			3.072	MHz
DC_{SCLK}	Clock Duty Cycle		40	50	60	%
$t_{SDIN.setup}$	SD data input setup time (before rising edge of SCLK)		9			ns
$t_{SDIN.hold}$	SD data input hold time (after rising edge of SCLK)		5			ns
$t_{WS.valid}$	WS data output valid time (Falling edge of SCLK to WS data valid)		42		49	ns
$t_{SDOUT.valid}$	SD data output valid time (Falling edge of SCLK to SD data valid)		37		62	ns

6.17.2.6.2 I^2S Timing Parameters - Peripheral Mode

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sclk}	clock frequency, BCLK	Peripheral Mode			3.072	MHz
DC_{SCLK}	Clock Duty Cycle		40	50	60	%
$t_{SDIN.setup}$	SD data input setup time (before rising edge of SCLK)		9			ns
$t_{SDIN.hold}$	SD data input hold time (after rising edge of SCLK)		5			ns
$t_{WS.setup}$	WS data input setup time (before rising edge of SCLK)		15			ns
$t_{WS.hold}$	WS data input hold time (after rising edge of SCLK)		0			ns
$t_{SDOUT.valid}$	SD data output valid time (Falling edge of SCLK to SD data valid)		26		47	ns

6.17.2.7 PDM

6.17.2.7.1 PDM Timing Parameters

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	PDM clock output Frequency		0.016		6.144	MHz
Tr	PDM Clock Rise time				5	ns
t_{DC}	PDM Clock duty Cycle		40	50	60	%
t_{delay}	Decimation filter Delay				5	ms
t_{is}	Left/Right Data Setup Time	Left/Right	20			ns
t_{ih}	Left/Right Data Hold Time	Left/Right	0			ns

6.17.2.8 CAN

6.17.2.8.1 CAN Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CAN_TX_LOAD	DCAN TX load capacitance		4	10	pF
CAN_RX_t_R CAN_RX_t_F	DCAN RX rise and fall times		10	75	ns
$t_{p(CAN\_TX)}$	Propagation delay	Transmit shift register to CAN_TX pin		10	ns
$t_{p(CAN\_RX)}$	Propagation delay	CAN_RX pin to receive shift register		5	ns

6.17.2.9 SDMMC

6.17.2.9.1 SDMMC Timing Parameters - Default Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		20	MHz
DC_{clock}	Clock Duty cycle	47.5	52.5	%
t_{TLH}	Rise time, CLK		3	ns
t_{THL}	Fall time, CLK		3	ns
t_{ISU}	Setup time, input valid before CLK ↑	2.5		ns
t_{IH}	Hold time, input valid after CLK ↑	0		ns
t_{ODLY}	Delay time, CLK ↓ to output valid	0	4	ns
C_L	Capacitive load on outputs		35	pF

6.17.2.9.2 SDMMC Timing Parameters - High Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		40	MHz
DC_{clock}	Clock Duty cycle	47.5	52.5	%
t_{TLH}	Rise time, CLK		3	ns
t_{THL}	Fall time, CLK		3	ns
t_{ISU}	Setup time, input valid before CLK ↑	2.5		ns
t_{IH}	Hold time, input valid after CLK ↑	2.15		ns
t_{ODLY}	Delay time, CLK ↑ to output valid	0	4	ns
C_L	Capacitive load on outputs		35	pF

6.17.2.10 SDIO

6.17.2.10.1 SDIO Timing Parameters - Default Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		26	MHz
t_{WH}	High Period	10		ns
t_{WL}	Low Period	10		
t_{TLH}	Rise time, CLK		10	
t_{THL}	Fall time, CLK		10	
t_{ISU}	Setup time, input valid before CLK ↑	5		
t_{IH}	Hold time, input valid after CLK ↑	5		
t_{ODLY}	Delay time, CLK ↓ to output valid. *15pF (Min); 40pF (Max)	2.5	14	
C_L	Capacitive load on outputs		40	pF

6.17.2.10.2 SDIO Default Timing

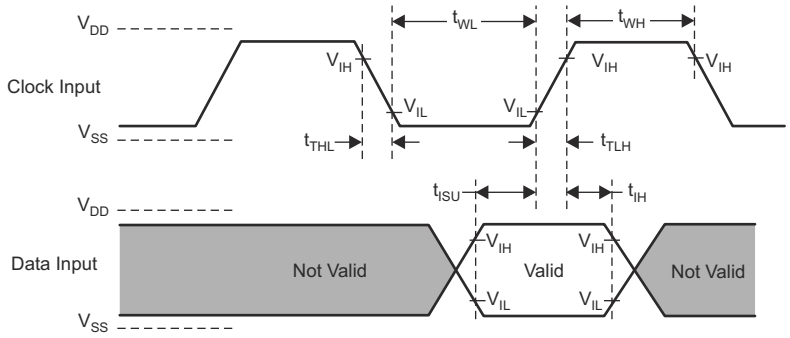


Figure 6-4. SDIO Default Input Timing

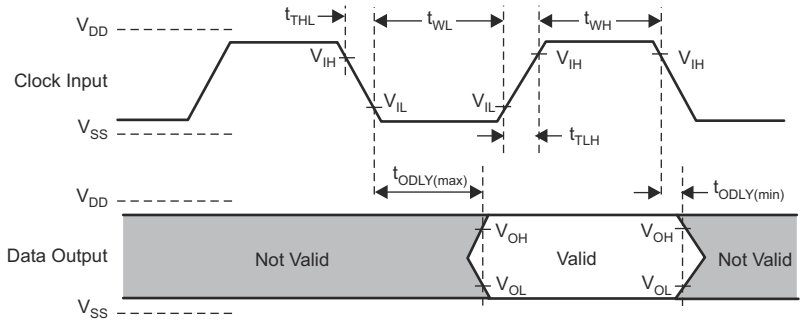


Figure 6-5. SDIO Default Output Timing

6.17.2.10.3 SDIO Timing Parameters - High Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		52	MHz
t_{WH}	High Period	7		ns
t_{WL}	Low Period	7		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{ISU}	Setup time, input valid before CLK ↑	6		
t_{IH}	Hold time, input valid after CLK ↑	2		
t_{ODLY}	Delay time, CLK ↑ to output valid. *15pF (Min); 40pF (Max)	2.5	14	
C_L	Capacitive load on outputs		40	pF

6.17.2.10.4 SDIO High Speed Timing

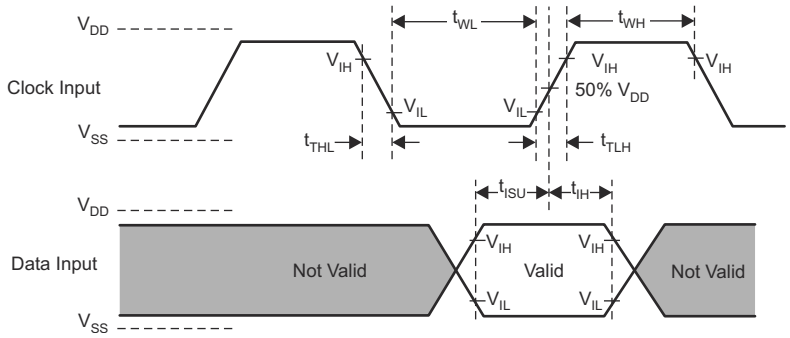


Figure 6-6. SDIO High Speed Input Timing

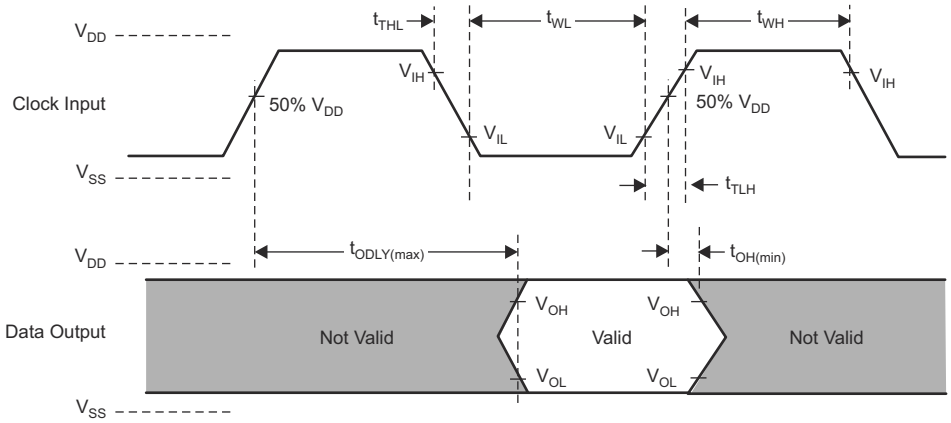


Figure 6-7. SDIO High Speed Output Timing

7 Detailed Description

7.1 Overview

The CC35xx Wi-Fi 6 and Bluetooth Low Energy wireless MCU family has a rich set of peripherals for diverse application requirements. Section 4 shows the core modules of the CC355xE device.

For more information, see CC35xx Wireless MCU TRM.

7.2 Arm Cortex-M33 Processor

The CC35xx SimpleLink Wireless MCU contains an Arm Cortex-M33 system CPU, which runs the application, the protocol stacks, and the wireless subsystem. The Cortex-M33 processor is a high performance, low gate count, highly configurable, and energy efficient processor. It is intended for microcontroller and embedded applications that require an efficient mix of control capability and signal processing instructions. The processor is based on the Armv8-M architecture and is primarily for use in environments where security is an important consideration.

The following features are included:

- 160 MHz Operation
- Arm TrustZone technology, using the Armv8-M Security Extension supporting Secure and Nonsecure states
- The Floating-point Extension (FPU)
- The Digital Signal Processing (DSP) Extension
- Enhanced system debug with up to 4 watchpoints and 8 breakpoints
- The Memory Protection Unit Extension (MPU)
- Programmable Security Attribution Unit (SAU)
- Micro Trace Buffer (MTB)
- Wakeup interrupt controller (WIC)
- Arm Custom Instructions (ACI)
- The Instruction Trace Macrocell Extension (ITM)
- A Nested Vectored Interrupt Controller (NVIC) that is closely integrated with the processor
- A low-cost debug solution with the ability to implement breakpoints, watchpoints, tracing
- Passing on-chip data through a Trace Port Interface Unit (TPIU) to a Trace Port Analyzer (TPA) using Serial Wire Output (SWO) mode
- A ROM table to allow debuggers to determine which components are implemented in the Cortex-M33 processor
- In-order pipeline processor
- Incorporates the Thumb-2 technology
- Data accesses in little endian
- Harvard architecture characterized by separate buses for instruction and data
- Saturating arithmetic and dedicated hardware division
- Standard trace support
  - ITM
  - TPIU with asynchronous serial wire output (SWO)
  - Full debug with data matching for watchpoint generation
  - DWT
  - SWD (Serial Wire Debug) port

7.3 Wireless Subsystem

7.3.1 WLAN

The WLAN features are as follows:

- Compatible with IEEE 802.11 a/b/g/n/ax
  - Orthogonal frequency-division multiple access (OFDMA)
  - Target wake time (TWT)
  - Trigger frames

  - Basic service set (BSS) color
- Integrated PA for a complete WLAN system with up to 20.5dBm output power at 1 DSSS
- Role support: STA, softAP , Wi-Fi direct, multirole AP + STA
- Support for personal and enterprise Wi-Fi security: WPA and WPA2 PSK, WPA2 Enterprise, WPA3 personal or enterprise
- Wi-Fi TX Power:
  - 20.5dBm at 1DSSS
  - 17.8dBm at 54OFDM
- Wi-Fi RX Sensitivity:
  - -98.7dBm at 1DSSS
  - -76.6dBm at 54OFDM

7.3.2 Bluetooth Low Energy

The Bluetooth Low Energy features are as follows: (CC3551E only)

- Bluetooth Low Energy 5.4
- LE coded PHYs (long range), LE 2M PHY (high speed), and advertising extension

7.4 Memory Subsystem (MEMSS)

The CC35xx device supports on-chip and off-chip memories. The memories are used for execution, data and non volatile memory. The on-chip memory includes SRAM and the off-chip memories supported are serial Flash (connected externally or stacked inside device package) and optional serial PSRAM (stacked inside device package).

The SRAM is used for execution and data. It is divided into instruction and data partitions, as well as secure and non-secure. The instruction memory partition is split into Instruction Tightly Coupled Memory (ITCM) and Instruction Cache memory (I-Cache). I-Cache allows for execution from Flash and the PSRAM (Refer to current software development kit (SDK) for support). Data memory is divided into Data Tightly Coupled Memory (DTCM), Data non-Tightly Coupled Memory (DMEM), and Data Cache Memory (D-Cache). The D-Cache is designed to access the PSRAM.

Flash is non-volatile memory used for execution and for data storage. The PSRAM is used predominantly as data storage.

Each of the memories can be accessed by the M33 MCU, Host DMA and the µDMA. The host DMA is used for data transfer between peripherals and the device on-chip SRAM. The µDMA is used for data transfer between the external Flash/PSRAM and on-chip SRAM.

7.4.1 External Memory Interface

The device supports external Flash/PSRAM interface (XIP) and support the following features:

- High speed Quad/ Octal xSPI interface
- Encrypt/Decrypt external memory data
- Logical to physical address translator
- Secured/Non-Secured partitioning

7.5 Hardware Security Module

The CC35xx devices have an integrated hardware security module (HSM) which act as an on-chip secure element. The HSM supports an isolated environment for cryptographic, key management, secure counters, and random number generation operations. Selected algorithms are protected from differential power analysis (DPA) side channel attacks. Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), the system supports secure and future proof IoT applications to be easily built on the platform.

7.6 Debug Subsystem (DEBUGSS)

The debug subsystem (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. Debugging of processor execution and the device state are supported. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

7.7 General Purpose Timers

The General Purpose Timer (GPT) is used to count or time external or internal events, generate Pulse-Width Modulation (PWM) signals, and generate IR modulated codes. There are two general purpose timers available, each with 4 channels.

7.8 Real Time Clock (RTC)

The RTC can be used to wake the CC35xx device from any state where the RTC is active. The RTC contains one capture and one compare channel, clocked from the in. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32.768 kHz slow clock, and has a recovery mechanism to keep the RTC through software initiated resets.

7.9 Direct Memory Access (DMA)

The CC35xx includes a direct memory access (DMA) controller, known as Host DMA. The Host DMA controller provides a way to offload data transfer tasks from the Arm® Cortex®-M33 processor, allowing for more efficient use of the processor and the available bus bandwidth. The Host DMA controller can perform transfers between on-chip memory (SRAM) and peripherals. The Host DMA includes multiple channels and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

7.10 Serial Peripherals and I/Os

I/O pins offer flexibility for a variety of connections. The CC35xx device supports configurable I/O pins (GPIOx) that can be multiplexed to digital and analog peripherals through the I/O Mux.

- Each pin can be mapped to a specific set of peripherals with wide variety in the pinmux
- GPIOn (GPIO0 to GPIO35) are the logical names of the different I/O pins.
- 8 of these GPIOs also have analog capabilities
- Pins can also be mapped to the digital test bus (DTB) to bring out clocks or physical signals like interrupts

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

Figure 8-1 shows the reference schematic for the CC355xE using an optimized bill of materials.

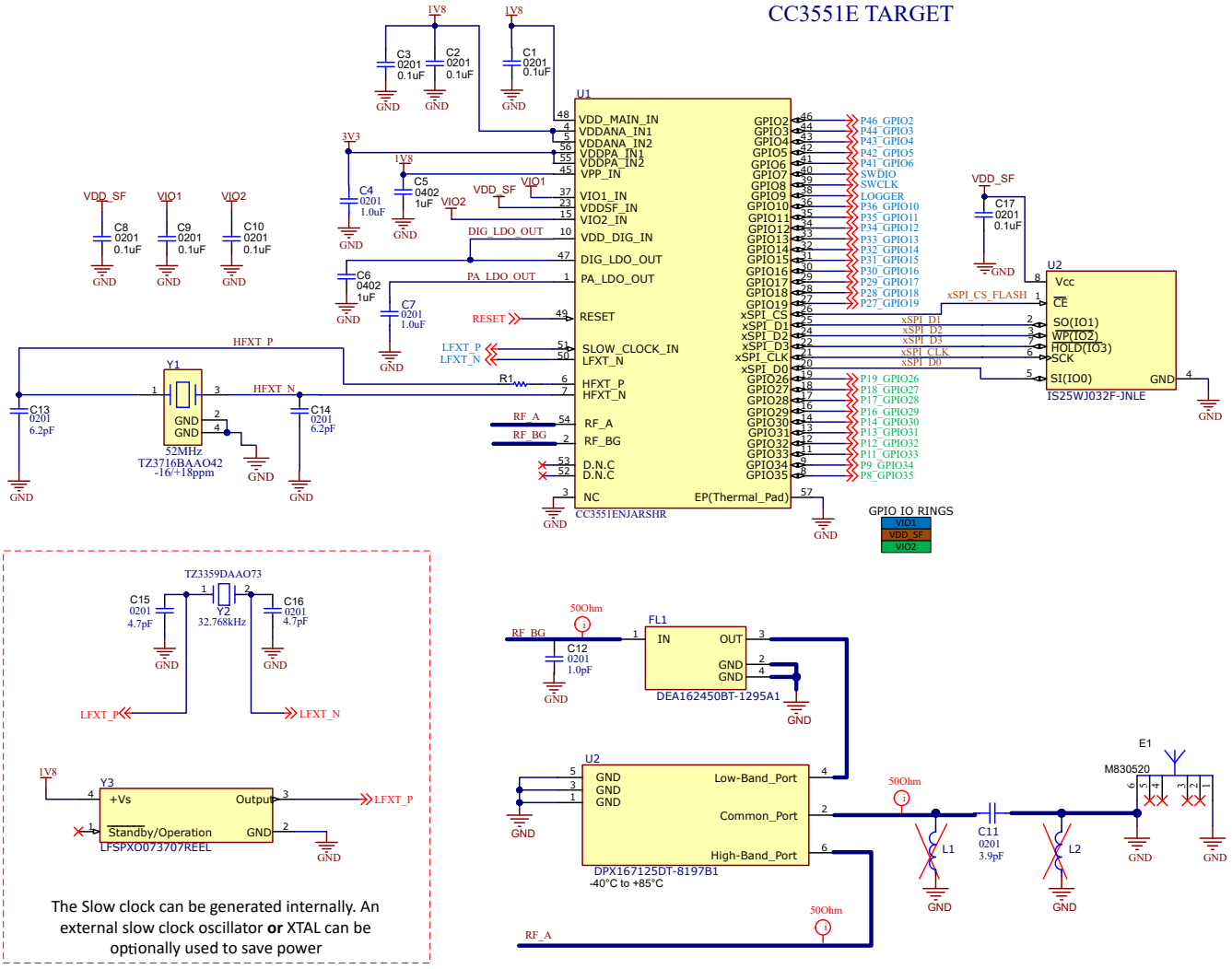


Figure 8-1. CC355xE Reference Schematic

1. The slow clock can be generated internally. An external slow clock oscillator or XTAL can be optionally used to save power.

2. The CC355xE device has three IO rings (VIO1, VIO2, VDD_SF), please see Section 6.3 for IO voltage requirements per device.

3. RF Shield recommended for optimal regulatory compliance.

Table 8-1. Bill of Materials

DESIGNATOR	QUANTITY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
C1, C2, C3, C8, C9,C10, C17	7	0.1µF	GRM033C71A104KE 14D	MuRata	CAP, CERM, 0.1µF, 10V, +/- 10%, X7S, 0201	0201
C4, C7	2	1µF	GRM033D70J105ME 01D	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0µF, X7T, +22%/-33%, 20%, 6.3V	0201
C5, C6	2	1µF	GRM155R70J105MA 12D	Murata	CAP, CERM, 1µF, 6.3V, +/- 20%, X7R, 0402	0402
C11	1	3.9pF	GRM0335C1E3R9BA 01	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 3.9pF, C0G	0201
C12	1	1.0pF	GRM0335C1E1R0CA 01	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0pF, C0G, 25V	0201
C13, C14	2	6.2pF	GRM0335C1E6R2BA 01	Murata	CAP, CERM, 6.2pF, 25V, +/- 2%, C0G/NP0, 0201	0201
R1	1	150Ω	RC0201FR-7D150RL	Yageo America	RES, 150, 1%, 0.05W, 0201	0201
U1	1		CC3551ENJARSHR	Texas Instruments	CC355x 2.4GHz SimpleLink™ Wi-Fi 6 and Bluetooth Low Energy Wireless MCU	VQFN56
U2	1		DPX167125DT-8197 B1	TDK	Multilayer Diplexer For 2.4-2.5GHz W-LAN and Bluetooth / 5-7GHz W-LAN	SMD6
U3	1		IS25WJ032F-JNLE	ISSI	FLASH - NOR Memory IC 32Mbit SPI - Quad I/O, QPI, DTR 133MHz 6ns 8-SOP	SOIC8
Y1	1		TZ3716BAAO42	TAI-SAW TECHNOLOGY	Crystal Unit SMD 2.0x1.6 52.0MHz	SMT_XTAL_ 2MM05_1MM65
FL1	1		DEA162450BT-1295A 1	TDK	2.45GHz Center Frequency Band Pass RF Filter (Radio Frequency) 100MHz Bandwidth 1.8dB 0603 (1608 Metric), 3 PC Pad	SMT_FILTER_ 1MM60_0MM80
E1	1		M830520	Kyocera AVX	WLAN ANTENNA 802.11, SMD	A 802.11, SMD 8x3mm
Optional: Y2	1		TZ3359DAAO73	TAI-SAW Technology	Crystal Unit 1.6x1.0 Tuning Fork 32.768KHz	SMT2_1MM65_ 1MM05
Optional: C15,C16	2	4.7pF	GRM0335C1H4R7BA 01D	Murata	CAP, CERM, 4.7pF, 50V,+/- 3%, C0G/NP0, 0201	0201
Optional: Y3	1		LFSPXO073707REE L	IQD Frequency Products	32.768kHz XO (Standard) CMOS Oscillator 1.8V Enable/ Disable 4- SMD, No Lead	SMT4_2MM0_ 1MM6

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop systems are listed below.

9.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RSH).

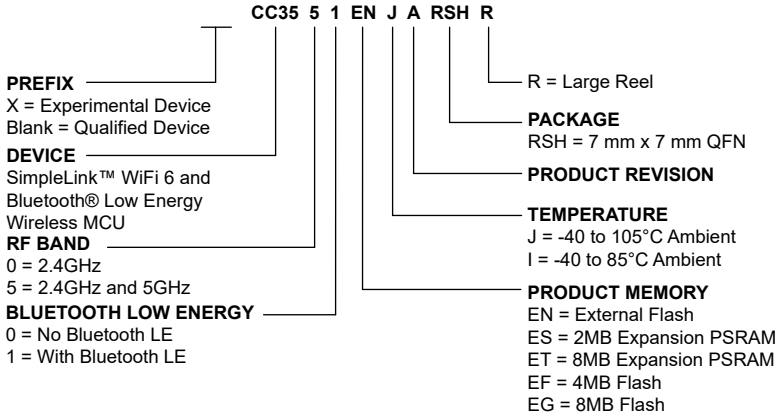


Figure 9-1. Device Nomenclature

9.3 Tools and Software

Design Kits and Evaluation Modules

CC35xxE LaunchPad™ Development Kit	The LP-EM-CC35X1 SimpleLink™ LaunchPad™ development kit highlights the CC3551E Wi-Fi 6 and Bluetooth® Low Energy wireless MCU, providing a test and development board that features on-board sensors, buttons and easy interface options to emulators for a full out-of-the-box experience and rapid development platform. This kit supports software development for the pin-to-pin compatible CC3500E, CC3501E, CC3550E and CC3551E Wi-Fi 6 and Bluetooth Low Energy wireless MCUs helping you bring your Wi-Fi products quickly to market.

Software

SimpleLink™ Wi-Fi Software Development Kit (SDK)	The SimpleLink™ Wi-Fi SDK delivers components that enable engineers to develop applications on the Texas Instruments SimpleLink CC35xx family of wireless microcontroller (MCUs). This powerful software toolkit provides a cohesive and consistent software experience for all SimpleLink CC35xx wireless MCU users by packaging essential software components, such as a Bluetooth® Low Energy (Bluetooth LE) protocol stack supporting Bluetooth 5.4, and Wi-Fi 6 networking stack based on LwIP, as well as the FreeRTOS kernel and TI Drivers in one easy-to-use software package along with example applications and exhaustive documentation.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)	Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.
SimpleLink™ Wi-Fi Toolbox	SimpleLink Wi-Fi Toolbox is a collection of tools to help development and testing of the CC35xx. The Wi-Fi toolbox package provides all the capabilities required to activate and program, debug and monitor WLAN/Bluetooth® Low Energy firmware with a host, perform RF validation tests, run a pretest for regulatory certification testing, and debug hardware and software platform integration issues.

9.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

Errata

CC35xxE Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and describes how to recognize a device revision.

Technical Reference Manual (TRM)

CC35xx Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

9.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.6 Trademarks

SimpleLink™ is a trademark of Texas Instruments.
Wi-Fi™ is a trademark of Wi-Fi Alliance.
TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG.
Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere.
TrustZone® is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
is a registered trademark of Bluetooth SIG, Inc.
is a registered trademark of Bluetooth SIG, Inc..
Zigbee® is a registered trademark of ZigBee Alliance.
All trademarks are the property of their respective owners.

9.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 31, 2026 to June 30, 2026 (from Revision A (March 2026) to Revision B (June 2026))	Page
• Changed Expansion PSRAM 8MB from samples to production	2

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC3550ENJARSHR	Active	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	CC3550 ENJA
CC3551ENJARSHR	Active	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	CC3551 ENJA
CC3551ETIARSHR	Active	Production	VQFN (RSH) | 56	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CC3551 ETIA
XCC3551ENJARSHR.B	Active	Preproduction	VQFN (RSH) | 56	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

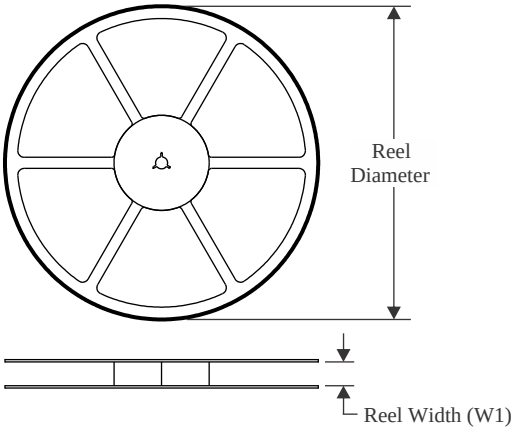
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

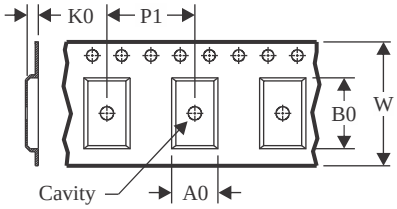
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

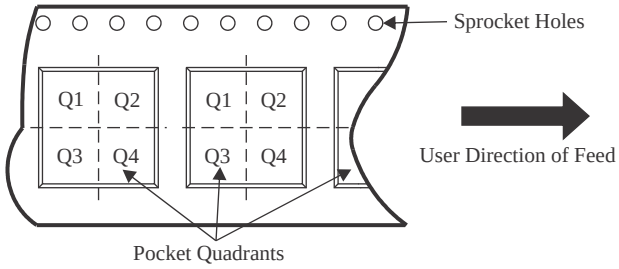


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

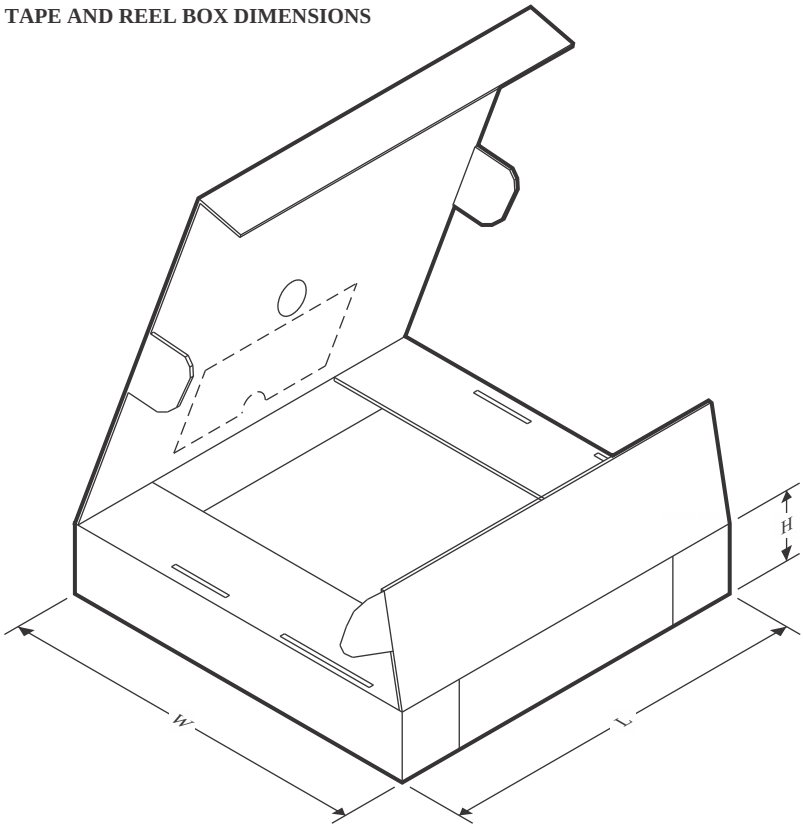
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3550ENJARSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC3551ENJARSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC3551ETIARSHR	VQFN	RSH	56	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

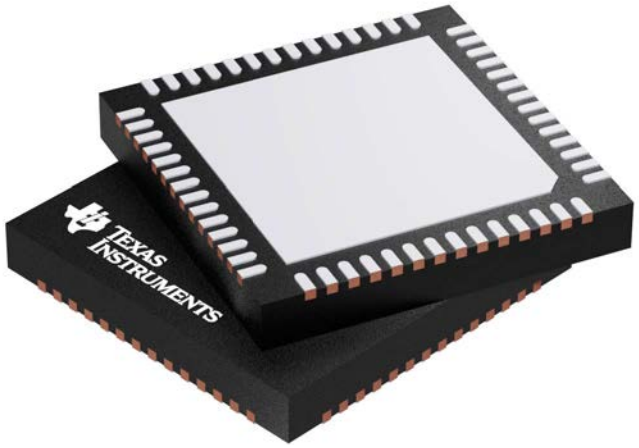
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3550ENJARSHR	VQFN	RSH	56	2500	360.0	360.0	36.0
CC3551ENJARSHR	VQFN	RSH	56	2500	360.0	360.0	36.0
CC3551ETIARSHR	VQFN	RSH	56	4000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

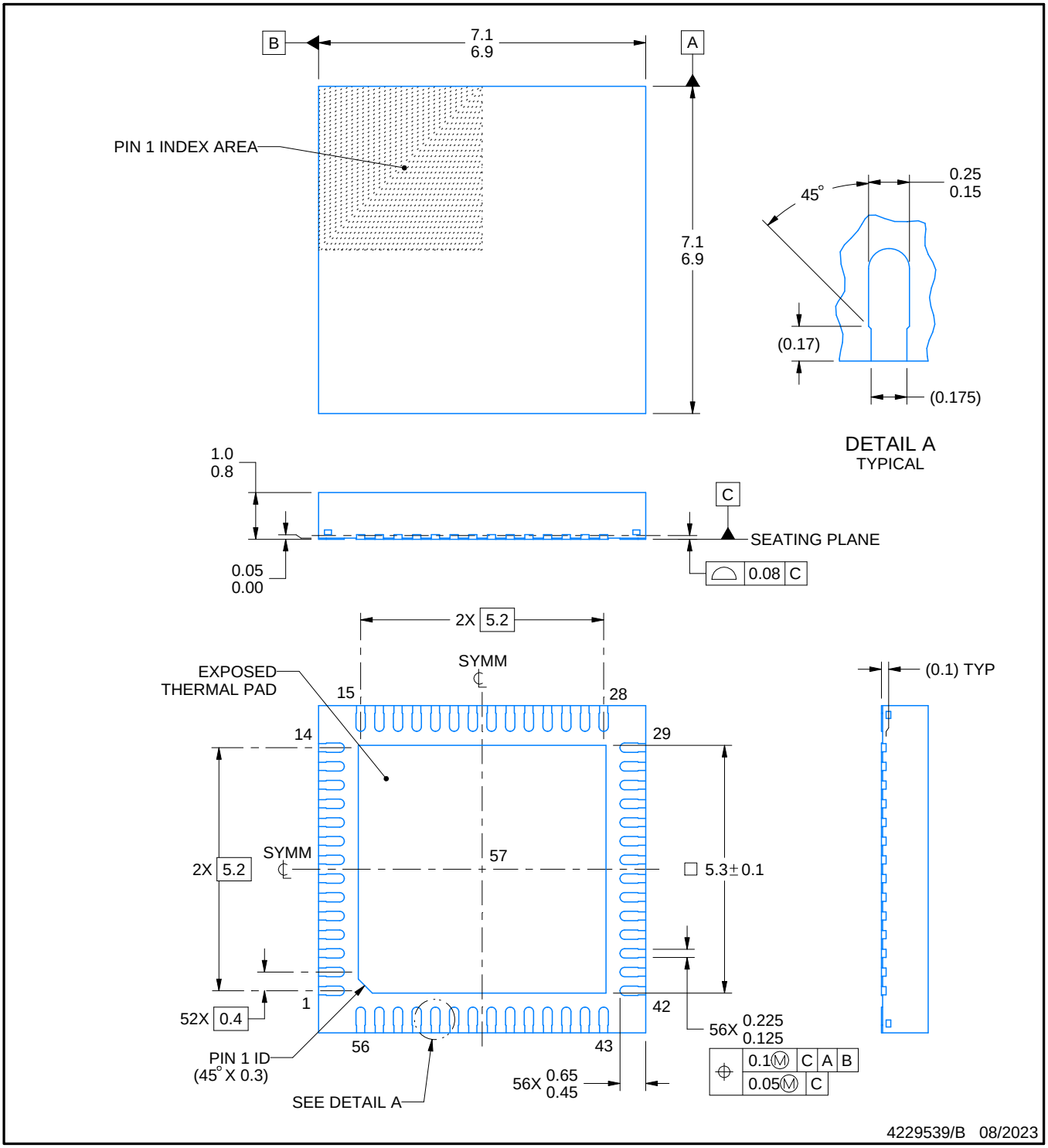
4207513/D

RSH0056G

PACKAGE OUTLINE

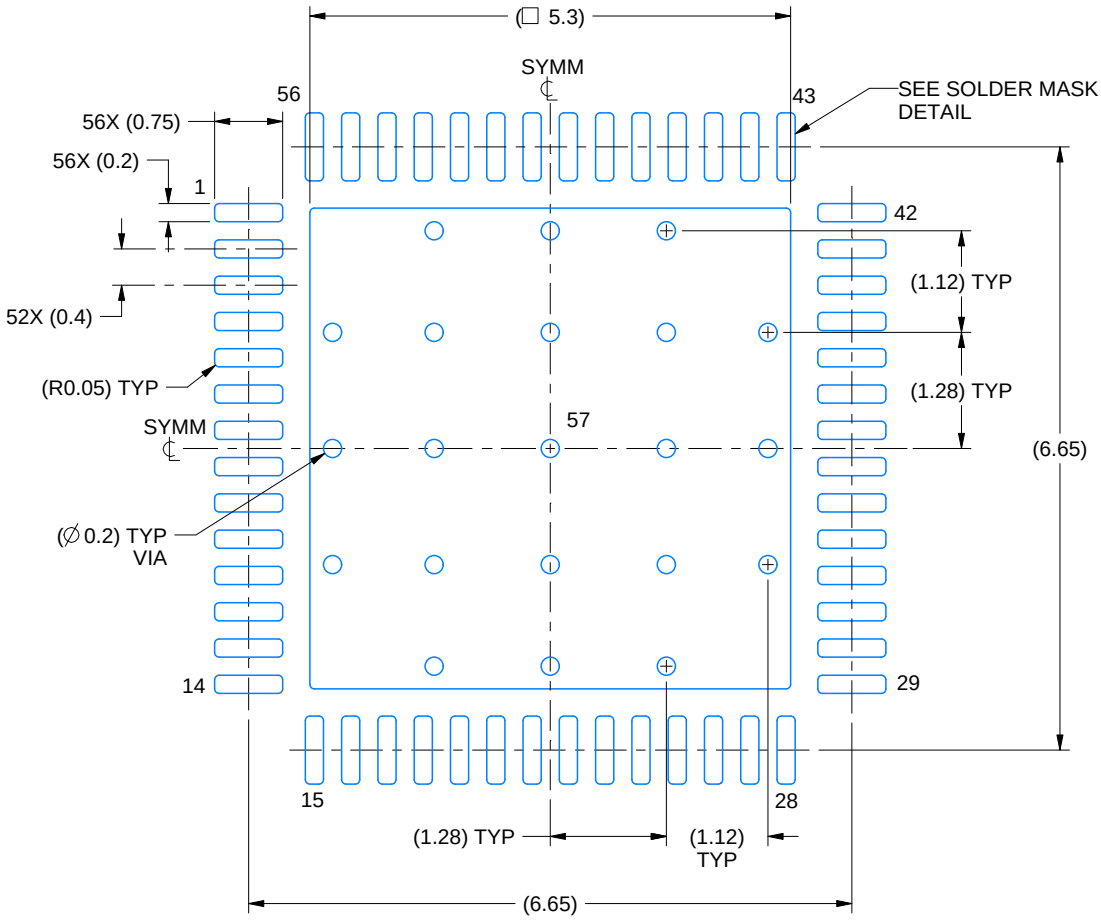
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

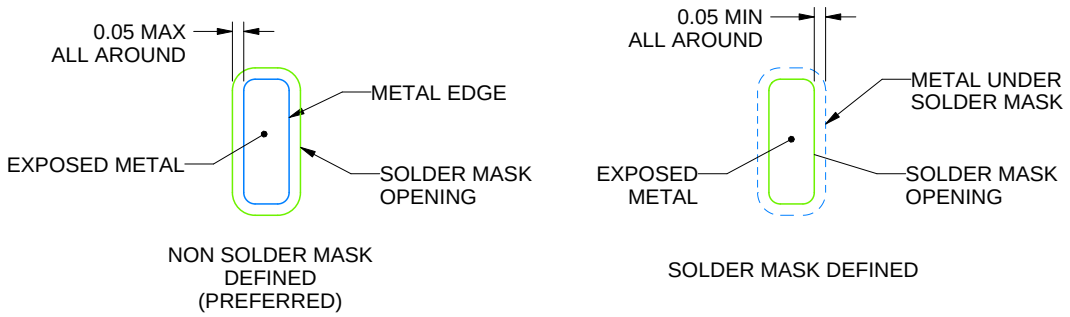


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

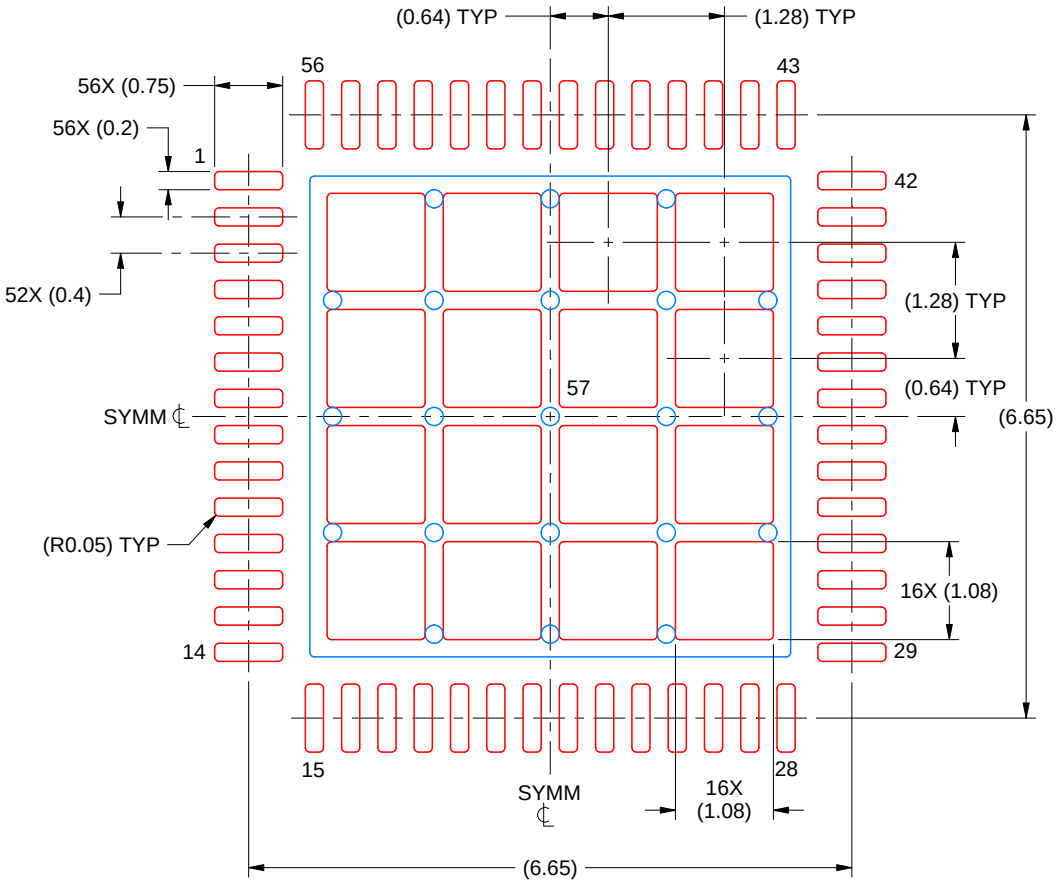


SOLDER MASK DETAILS

4229539/B 08/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.100 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 57
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229539/B 08/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025