

# AMC0x02D-Q1 Automotive, Precision, $\pm 50\text{mV}$ Input, Basic and Reinforced Isolated Amplifiers With Fixed Gain and Differential Output

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $T_A$
- Linear input voltage range:  $\pm 50\text{mV}$
- Supply voltage range:
  - High-side (VDD1): 3.0V to 5.5V
  - Low-side (VDD2): 3.0V to 5.5V
- Fixed gain: 41V/V
- Differential analog output
- Low DC errors:
  - Offset error:  $\pm 50\mu\text{V}$  (maximum)
  - Offset drift:  $\pm 0.9\mu\text{V}/^\circ\text{C}$  (maximum)
  - Gain error:  $\pm 0.2\%$  (maximum)
  - Gain drift:  $\pm 45\text{ppm}/^\circ\text{C}$  (maximum)
  - Nonlinearity: 0.04% (maximum)
- High CMTI: 150V/ns (minimum)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings:
  - AMC0202D-Q1: Basic isolation
  - AMC0302D-Q1: Reinforced Isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577

## 2 Applications

- Traction inverters
- Onboard chargers
- DC/DC converters

## 3 Description

The AMC0x02D-Q1 is a precision, galvanically isolated amplifier with a  $\pm 50\text{mV}$ , differential input and differential output. The input is optimized for direct connection to a shunt resistor or other low-impedance signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to  $5\text{kV}_{\text{RMS}}$  (DWV package) and basic isolation up to  $3\text{kV}_{\text{RMS}}$  (D package) (60s).

The AMC0x02D-Q1 outputs a differential signal proportional to the input voltage. The differential output is insensitive to ground shifts and enables routing the output signal over long distances.

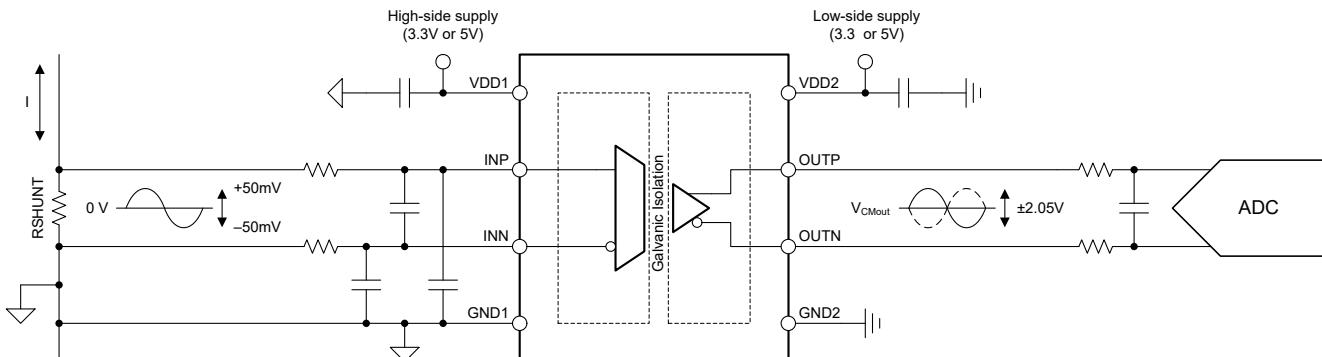
The AMC0x02D-Q1 comes in 8-pin, wide- and narrow-body SOIC packages, and is fully specified over the temperature range from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| AMC0202D-Q1 | D (SOIC, 8)            | 4.9mm $\times$ 6mm          |
| AMC0302D-Q1 | DWV (SOIC, 8)          | 5.85mm $\times$ 11.5mm      |

(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

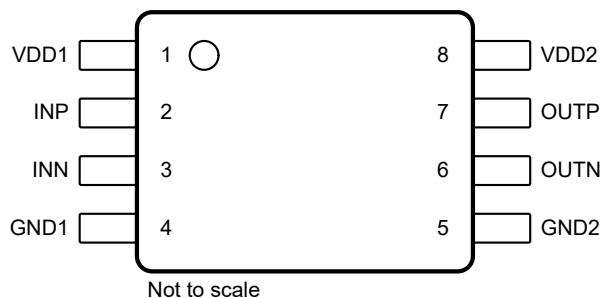
## Table of Contents

|  |          |  |           |
|--|----------|--|-----------|
| <b>1 Features</b> .....  | <b>1</b> | 6.17 Typical Characteristics.....                                | <b>16</b> |
| <b>2 Applications</b> .....                                    | <b>1</b> | <b>7 Detailed Description</b> .....                              | <b>22</b> |
| <b>3 Description</b> .....                                     | <b>1</b> | 7.1 Overview.....  | <b>22</b> |
| <b>4 Device Comparison Table</b> .....                         | <b>3</b> | 7.2 Functional Block Diagram.....                                | <b>22</b> |
| <b>5 Pin Configuration and Functions</b> .....                 | <b>3</b> | 7.3 Feature Description.....                                     | <b>23</b> |
| <b>6 Specifications</b> .....                                  | <b>4</b> | 7.4 Device Functional Modes.....                                 | <b>25</b> |
| 6.1 Absolute Maximum Ratings .....                             | 4        | <b>8 Application and Implementation</b> .....                    | <b>26</b> |
| 6.2 ESD Ratings.....   | 4        | 8.1 Application Information.....                                 | <b>26</b> |
| 6.3 Recommended Operating Conditions .....                     | 4        | 8.2 Typical Application.....                                     | <b>26</b> |
| 6.4 Thermal Information (D Package).....                       | 5        | 8.3 Best Design Practices.....                                   | <b>29</b> |
| 6.5 Thermal Information (DWV Package).....                     | 6        | 8.4 Power Supply Recommendations.....                            | <b>29</b> |
| 6.6 Power Ratings .....  | 6        | 8.5 Layout.....  | <b>30</b> |
| 6.7 Insulation Specifications (Basic Isolation).....           | 7        | <b>9 Device and Documentation Support</b> .....                  | <b>31</b> |
| 6.8 Insulation Specifications (Reinforced Isolation).....      | 8        | 9.1 Documentation Support.....                                   | <b>31</b> |
| 6.9 Safety-Related Certifications (Basic Isolation).....       | 9        | 9.2 Receiving Notification of Documentation Updates.....         | <b>31</b> |
| 6.10 Safety-Related Certifications (Reinforced Isolation)..... | 10       | 9.3 Support Resources.....                                       | <b>31</b> |
| 6.11 Safety Limiting Values (D Package).....                   | 11       | 9.4 Trademarks.....  | <b>31</b> |
| 6.12 Safety Limiting Values (DWV Package).....                 | 12       | 9.5 Electrostatic Discharge Caution.....                         | <b>31</b> |
| 6.13 Electrical Characteristics.....                           | 13       | 9.6 Glossary.....  | <b>31</b> |
| 6.14 Switching Characteristics .....                           | 14       | <b>10 Revision History</b> .....                                 | <b>31</b> |
| 6.15 Timing Diagram.....                                       | 14       | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>31</b> |
| 6.16 Insulation Characteristics Curves.....                    | 15       | 11.1 Mechanical Data.....  | <b>32</b> |

## 4 Device Comparison Table

| PARAMETER                        | AMC0202D-Q1          | AMC0302D-Q1          |
|----------------------------------|----------------------|----------------------|
| Isolation rating per VDE 0884-17 | Basic                | Reinforced           |
| Package                          | Narrow-body SOIC (D) | Wide-body SOIC (DWV) |

## 5 Pin Configuration and Functions



**Figure 5-1. DWV and D Packages, 8-Pin SOIC (Top View)**

**Table 5-1. Pin Functions**

| PIN |      | TYPE             | DESCRIPTION                              |
|-----|------|------------------|--|
| NO. | NAME |                  |  |
| 1   | VDD1 | High-side power  | High-side power supply <sup>(1)</sup>    |
| 2   | INP  | Analog input     | Noninverting analog input <sup>(2)</sup> |
| 3   | INN  | Analog Input     | Inverting analog input <sup>(2)</sup>    |
| 4   | GND1 | High-side ground | High-side analog ground                  |
| 5   | GND2 | Low-side ground  | Low-side analog ground                   |
| 6   | OUTN | Analog output    | Inverting analog output                  |
| 7   | OUTP | Analog output    | Noninverting analog output               |
| 8   | VDD2 | Low-side power   | Low-side power supply <sup>(1)</sup>     |

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

(2) See the [Input Filter Design](#) section for input filter design.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                       |  | MIN        | MAX        | UNIT |
|-----------------------|--|------------|------------|------|
| Power-supply voltage  | High-side VDD1 to GND1                       | –0.3       | 6.5        | V    |
|                       | Low-side VDD2 to GND2                        | –0.3       | 6.5        |      |
| Analog input voltage  | INP, INN to GND1                             | GND1 – 4   | VDD1 + 0.5 | V    |
| Analog output voltage | OUTP, OUTN to GND2                           | GND2 – 0.5 | VDD2 + 0.5 | V    |
| Input current         | Continuous, any pin except power-supply pins | –10        | 10         | mA   |
| Temperature           | Junction, $T_J$                              |            | 150        | °C   |
|                       | Storage, $T_{stg}$                           | –65        | 150        |      |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|             |                         | VALUE   | UNIT       |
|-------------|-------------------------|---|------------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> ,<br>HBM ESD classification level 2 | $\pm 2000$ |
|             |                         | Charged-device model (CDM), per AEC Q100-011,<br>CDM ESD classification level C6            | $\pm 1000$ |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|                          |   | MIN                               | NOM    | MAX | UNIT       |
|--------------------------|---|-----------------------------------|--------|-----|------------|
| <b>POWER SUPPLY</b>      |   |                                   |        |     |            |
| VDD1                     | High-side power supply                                    | VDD1 to GND1                      | 3      | 5.0 | 5.5        |
| VDD2                     | Low-side power supply                                     | VDD2 to GND2                      | 3      | 3.3 | 5.5        |
| <b>ANALOG INPUT</b>      |   |                                   |        |     |            |
| $V_{Clipping}$           | Nominal differential input voltage before clipping output | $V_{IN} = V_{INP} - V_{INN}$      | –64    | 64  | mV         |
| $V_{FSR}$                | Specified linear differential input voltage               | $V_{IN} = V_{INP} - V_{INN}$      | –50    | 50  | mV         |
| $V_{CM}$                 | Operating common-mode input voltage                       | $(V_{INP} + V_{INN}) / 2$ to GND1 | –0.032 | 1   | V          |
| $C_{IN, EXT}$            | Minimum external capacitance connected to the input       | from INP to INN                   |        | 10  | nF         |
| <b>ANALOG OUTPUT</b>     |   |                                   |        |     |            |
| $C_{LOAD}$               | Capacitive load   | OUTP or OUTN to GND2              |        | 500 | pF         |
|                          |   | OUTP to OUTN                      |        | 250 |            |
| $R_{LOAD}$               | Resistive load  | OUTP or OUTN to GND2              | 10     | 1   | k $\Omega$ |
| <b>TEMPERATURE RANGE</b> |   |                                   |        |     |            |
| $T_A$                    | Specified ambient temperature                             |                                   | –40    | 125 | °C         |

## 6.4 Thermal Information (D Package)

| THERMAL METRIC <sup>(1)</sup> |  | D (SOIC) | UNIT |
|-------------------------------|--|----------|------|
|                               |  | 8 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 116.5    | °C/W |
| $R_{\theta JC(\text{top})}$   | Junction-to-case (top) thermal resistance    | 52.8     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 58.9     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 19.4     | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 58.0     | °C/W |
| $R_{\theta JC(\text{bot})}$   | Junction-to-case (bottom) thermal resistance | N/A      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.5 Thermal Information (DWV Package)

| THERMAL METRIC <sup>(1)</sup> |  | DWV (SOIC) | UNIT |
|-------------------------------|--|------------|------|
|                               |  | 8 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 102.8      | °C/W |
| $R_{\theta JC(\text{top})}$   | Junction-to-case (top) thermal resistance    | 45.1       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 63.0       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 14.3       | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 61.1       | °C/W |
| $R_{\theta JC(\text{bot})}$   | Junction-to-case (bottom) thermal resistance | N/A        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

## 6.6 Power Ratings

| PARAMETER |  | TEST CONDITIONS      | VALUE | UNIT |
|-----------|--|----------------------|-------|------|
| $P_D$     | Maximum power dissipation (both sides) | $VDD1 = VDD2 = 5.5V$ | 92    | mW   |
| $P_{D1}$  | Maximum power dissipation (high-side)  | $VDD1 = 5.5V$        | 38    | mW   |
| $P_{D2}$  | Maximum power dissipation (low-side)   | $VDD2 = 5.5V$        | 54    | mW   |

## 6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS   | VALUE         | UNIT             |
|--|---|---|---------------|------------------|
| <b>GENERAL</b>   |   |   |               |                  |
| CLR  | External clearance <sup>(1)</sup>                     | Shortest pin-to-pin distance through air  | $\geq 4$      | mm               |
| CPG  | External creepage <sup>(1)</sup>                      | Shortest pin-to-pin distance across the package surface   | $\geq 4$      | mm               |
| DTI  | Distance through insulation                           | Minimum internal gap (internal clearance) of the insulation   | $\geq 15.4$   | $\mu\text{m}$    |
| CTI  | Comparative tracking index                            | DIN EN 60112 (VDE 0303-11); IEC 60112   | $\geq 600$    | V                |
|  | Material group  | According to IEC 60664-1  | I             |                  |
|  | Overvoltage category per IEC 60664-1                  | Rated mains voltage $\leq 300\text{V}_{\text{RMS}}$   | I-IV          |                  |
|  |   | Rated mains voltage $\leq 600\text{V}_{\text{RMS}}$   | I-III         |                  |
| <b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b> |   |   |               |                  |
| $V_{\text{IORM}}$                                      | Maximum repetitive peak isolation voltage             | At AC voltage   | 1130          | $V_{\text{PK}}$  |
| $V_{\text{IOWM}}$                                      | Maximum-rated isolation working voltage               | At AC voltage (sine wave)   | 800           | $V_{\text{RMS}}$ |
|  |   | At DC voltage   | 1130          | $V_{\text{DC}}$  |
| $V_{\text{IOTM}}$                                      | Maximum transient isolation voltage                   | $V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1\text{s}$ (100% production test)   | 4250          | $V_{\text{PK}}$  |
| $V_{\text{IMP}}$                                       | Maximum impulse voltage <sup>(3)</sup>                | Tested in air, 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1  | 5000          | $V_{\text{PK}}$  |
| $V_{\text{IOSM}}$                                      | Maximum surge isolation voltage <sup>(4)</sup>        | Tested in oil (qualification test),<br>1.2/50 $\mu\text{s}$ waveform per IEC 62368-1  | 10000         | $V_{\text{PK}}$  |
| $q_{\text{pd}}$  | Apparent charge <sup>(5)</sup>                        | Method a, after input/output safety test subgroups 2 and 3,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$ | $\leq 5$      | $\text{pC}$      |
|  |   | Method a, after environmental tests subgroup 1,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.3 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$             | $\leq 5$      |                  |
|  |   | Method b1, at preconditioning (type test) and routine test,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 1\text{s}$ , $V_{\text{pd}(\text{m})} = 1.5 \times V_{\text{IORM}}$ , $t_{\text{m}} = 1\text{s}$   | $\leq 5$      |                  |
|  |   | Method b2, at routine test (100% production) <sup>(7)</sup> ,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}} = V_{\text{pd}(\text{m})}$ , $t_{\text{ini}} = t_{\text{m}} = 1\text{s}$  | $\leq 5$      |                  |
| $C_{\text{IO}}$  | Barrier capacitance, input to output <sup>(6)</sup>   | $V_{\text{IO}} = 0.5V_{\text{PP}}$ at 1MHz  | $\approx 1.5$ | pF               |
| $R_{\text{IO}}$  | Insulation resistance, input to output <sup>(6)</sup> | $V_{\text{IO}} = 500\text{V}$ at $T_A = 25^\circ\text{C}$   | $> 10^{12}$   | $\Omega$         |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$  | $> 10^{11}$   |                  |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $T_S = 150^\circ\text{C}$  | $> 10^9$      |                  |
|  | Pollution degree                                      |   | 2             |                  |
|  | Climatic category                                     |   | 55/125/21     |                  |
| <b>UL1577</b>  |   |   |               |                  |
| $V_{\text{ISO}}$                                       | Withstand isolation voltage                           | $V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1\text{s}$ (100% production test)   | 3000          | $V_{\text{RMS}}$ |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

## 6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS  | VALUE         | UNIT             |
|--|---|--|---------------|------------------|
| <b>GENERAL</b>   |   |  |               |                  |
| CLR  | External clearance <sup>(1)</sup>                     | Shortest pin-to-pin distance through air   | $\geq 8.5$    | mm               |
| CPG  | External creepage <sup>(1)</sup>                      | Shortest pin-to-pin distance across the package surface  | $\geq 8.5$    | mm               |
| DTI  | Distance through insulation                           | Minimum internal gap (internal clearance) of the double insulation   | $\geq 15.4$   | $\mu\text{m}$    |
| CTI  | Comparative tracking index                            | DIN EN 60112 (VDE 0303-11); IEC 60112  | $\geq 600$    | V                |
|  | Material group  | According to IEC 60664-1   | I             |                  |
|  | Overvoltage category per IEC 60664-1                  | Rated mains voltage $\leq 300\text{V}_{\text{RMS}}$  | I-IV          |                  |
|  |   | Rated mains voltage $\leq 6000\text{V}_{\text{RMS}}$   | I-III         |                  |
| <b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b> |   |  |               |                  |
| $V_{\text{IORM}}$                                      | Maximum repetitive peak isolation voltage             | At AC voltage  | 2120          | $V_{\text{PK}}$  |
| $V_{\text{IOWM}}$                                      | Maximum-rated isolation working voltage               | At AC voltage (sine wave)  | 1500          | $V_{\text{RMS}}$ |
|  |   | At DC voltage  | 2120          | $V_{\text{DC}}$  |
| $V_{\text{IOTM}}$                                      | Maximum transient isolation voltage                   | $V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1\text{s}$ (100% production test)  | 7000          | $V_{\text{PK}}$  |
| $V_{\text{IMP}}$                                       | Maximum impulse voltage <sup>(3)</sup>                | Tested in air, 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1   | 7700          | $V_{\text{PK}}$  |
| $V_{\text{IOSM}}$                                      | Maximum surge isolation voltage <sup>(4)</sup>        | Tested in oil (qualification test),<br>1.2/50 $\mu\text{s}$ waveform per IEC 62368-1   | 10000         | $V_{\text{PK}}$  |
| $q_{\text{pd}}$  | Apparent charge <sup>(5)</sup>                        | Method a, after input/output safety test subgroups 2 and 3,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$            | $\leq 5$      | pC               |
|  |   | Method a, after environmental tests subgroup 1,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.6 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$                        | $\leq 5$      |                  |
|  |   | Method b1, at preconditioning (type test) and routine test,<br>$V_{\text{pd}(\text{ini})} = 1.2 \times V_{\text{IOTM}}$ , $t_{\text{ini}} = 1\text{s}$ , $V_{\text{pd}(\text{m})} = 1.875 \times V_{\text{IORM}}$ , $t_{\text{m}} = 1\text{s}$ | $\leq 5$      |                  |
|  |   | Method b2, at routine test (100% production) <sup>(7)</sup><br>$V_{\text{pd}(\text{ini})} = V_{\text{pd}(\text{m})} = 1.2 \times V_{\text{IOTM}}$ , $t_{\text{ini}} = t_{\text{m}} = 1\text{s}$  | $\leq 5$      |                  |
| $C_{\text{IO}}$  | Barrier capacitance, input to output <sup>(6)</sup>   | $V_{\text{IO}} = 0.5\text{V}_{\text{PP}}$ at 1MHz  | $\approx 1.5$ | pF               |
| $R_{\text{IO}}$  | Insulation resistance, input to output <sup>(6)</sup> | $V_{\text{IO}} = 500\text{V}$ at $T_A = 25^\circ\text{C}$  | $> 10^{12}$   | $\Omega$         |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$   | $> 10^{11}$   |                  |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $T_S = 150^\circ\text{C}$   | $> 10^9$      |                  |
|  | Pollution degree                                      |  | 2             |                  |
|  | Climatic category                                     |  | 55/125/21     |                  |
| <b>UL1577</b>  |   |  |               |                  |
| $V_{\text{ISO}}$                                       | Withstand isolation voltage                           | $V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1\text{s}$ (100% production test)  | 5000          | $V_{\text{RMS}}$ |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

## 6.9 Safety-Related Certifications (Basic Isolation)

| VDE   | UL  |
|---|---|
| DIN EN IEC 60747-17 (VDE 0884-17),<br>EN IEC 60747-17,<br>DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ;<br>6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1 | Recognized under 1577 component recognition and<br>CSA component acceptance NO 5 programs |
| Basic insulation  | Single protection   |
| Certificate number: Pending   | File number: Pending  |

## 6.10 Safety-Related Certifications (Reinforced Isolation)

| VDE   | UL  |
|---|---|
| DIN EN IEC 60747-17 (VDE 0884-17),<br>EN IEC 60747-17,<br>DIN EN IEC 62368-1 (VDE 0868-1),<br>EN IEC 62368-1,<br>IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9 | Recognized under 1577 component recognition and<br>CSA component acceptance NO 5 programs |
| Reinforced insulation   | Single protection   |
| Certificate number: Pending   | File number: Pending  |

## 6.11 Safety Limiting Values (D Package)

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER      |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------|---|--|-----|-----|------|------|
| I <sub>S</sub> | Safety input, output, or supply current | R <sub>θJA</sub> = 116.5°C/W, VDDx = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 195  | mA   |
| P <sub>S</sub> | Safety input, output, or total power    | R <sub>θJA</sub> = 116.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C              |     |     | 1070 | mW   |
| T <sub>S</sub> | Maximum safety temperature              |  |     |     | 150  | °C   |

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum junction temperature.

P<sub>S</sub> = I<sub>S</sub> × VDD<sub>max</sub>, where VDD<sub>max</sub> is the maximum supply voltage for high-side and low-side.

## 6.12 Safety Limiting Values (DWV Package)

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER      |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------|---|--|-----|-----|------|------|
| I <sub>S</sub> | Safety input, output, or supply current | R <sub>θJA</sub> = 102.8°C/W, VDDx = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 220  | mA   |
| P <sub>S</sub> | Safety input, output, or total power    | R <sub>θJA</sub> = 102.8°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C              |     |     | 1210 | mW   |
| T <sub>S</sub> | Maximum safety temperature              |  |     |     | 150  | °C   |

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum junction temperature.

P<sub>S</sub> = I<sub>S</sub> × VDD<sub>max</sub>, where VDD<sub>max</sub> is the maximum supply voltage for high-side and low-side.

## 6.13 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $VDD1 = 3.0\text{V}$  to  $5.5\text{V}$ ,  $VDD2 = 3.0\text{V}$  to  $5.5\text{V}$ ,  $V_{INP} = -50\text{mV}$  to  $+50\text{mV}$ , and  $V_{INN} = 0\text{V}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $VDD1 = 5\text{V}$ , and  $VDD2 = 3.3\text{V}$  (unless otherwise noted)

| PARAMETER            | TEST CONDITIONS                             | MIN   | TYP    | MAX        | UNIT             |                              |
|----------------------|---|---|--------|------------|------------------|------------------------------|
| <b>ANALOG INPUT</b>  |   |   |        |            |                  |                              |
| $C_{IN}$             | Effective input sampling capacitance        |   | 8      |            | pF               |                              |
| $R_{IN}$             | Input impedance                             |   | 5.3    | 6.3        | $\text{k}\Omega$ |                              |
| $I_{INP}$            | Input current                               | $V_{IN} = (V_{INP} - V_{INN}) = V_{FSR, MAX}$   | 8      |            | $\mu\text{A}$    |                              |
| $I_{INN}$            | Input current                               | $V_{IN} = (V_{INP} - V_{INN}) = V_{FSR, MAX}$   |        | -8         | $\mu\text{A}$    |                              |
| CMTI                 | Common-mode transient immunity              | $ GND1 - GND2  = 1\text{kV}$  | 150    |            | V/ns             |                              |
| <b>ANALOG OUTPUT</b> |   |   |        |            |                  |                              |
|                      | Nominal gain                                |   | 41     |            | V/V              |                              |
| $V_{CMout}$          | Common-mode output voltage                  |   | 1.39   | 1.44       | 1.50             | V                            |
| $V_{CLIPout}$        | Clipping differential output voltage        | $V_{OUT} = (V_{OUTP} - V_{OUTN})$ ; $ V_{IN}  =  V_{INP} - V_{INN}  >  V_{Clipping} $                 | -2.52  | $\pm 2.49$ | 2.52             | V                            |
| $V_{FAILSAFE}$       | Failsafe differential output voltage        | $VDD1$ missing  | -2.63  | -2.57      | -2.53            | V                            |
| $R_{OUT}$            | Output resistance                           | On OUTP or OUTN   |        | <0.2       | $\Omega$         |                              |
|                      | Output short-circuit current                | On OUTP or OUTN, sourcing or sinking, $INN = INP = GND1$ , outputs shorted to either $GND2$ or $VDD2$ |        | 11         | mA               |                              |
| <b>DC ACCURACY</b>   |   |   |        |            |                  |                              |
| $V_{OS}$             | Offset voltage <sup>(1) (2)</sup>           | $T_A = 25^\circ\text{C}$ , $INP = INN = GND1$   | -50    | $\pm 4$    | 50               | $\mu\text{V}$                |
| $TCV_{OS}$           | Offset drift <sup>(1) (2) (4)</sup>         |   | -0.9   | $\pm 0.1$  | 0.9              | $\mu\text{V}/^\circ\text{C}$ |
| $E_G$                | Gain error <sup>(1)</sup>                   | $T_A = 25^\circ\text{C}$  | -0.2%  | $\pm 0.04$ | 0.2%             |                              |
| $TCE_G$              | Gain drift <sup>(1) (5)</sup>               |   | -45    | $\pm 5$    | 45               | $\text{ppm}/^\circ\text{C}$  |
|                      | Nonlinearity <sup>(1)</sup>                 |   | -0.04% |            | 0.04%            |                              |
|                      | Output noise                                | $INP = INN = GND1$ , $f_{IN} = 0\text{Hz}$ , $BW = 100\text{kHz}$ brickwall filter                    | 410    |            |                  | $\mu\text{V}_{\text{RMS}}$   |
| CMRR                 | Common-mode rejection ratio                 | $f_{IN} = 0\text{Hz}$ , $V_{CM \min} \leq V_{CM} \leq V_{CM \max}$                                    | -100   |            |                  | dB                           |
|                      |   | $f_{IN} = 10\text{kHz}$ , $V_{CM \min} \leq V_{CM} \leq V_{CM \max}$                                  | -100   |            |                  |                              |
| PSRR                 | Power-supply rejection ratio <sup>(2)</sup> | $VDD1$ DC PSRR, $INP = INN = GND1$ , $VDD1$ from $3\text{V}$ to $5.5\text{V}$                         | -113   |            |                  | dB                           |
|                      |   | $VDD1$ AC PSRR, $INP = INN = GND1$ , $VDD1$ with $10\text{kHz}$ / $100\text{mV}$ ripple               | -92    |            |                  |                              |
|                      |   | $VDD2$ DC PSRR, $INP = INN = GND1$ , $VDD2$ from $3\text{V}$ to $5.5\text{V}$                         | -116   |            |                  |                              |
|                      |   | $VDD2$ AC PSRR, $INP = INN = GND1$ , $VDD2$ with $10\text{kHz}$ / $100\text{mV}$ ripple               | -94    |            |                  |                              |
| <b>AC ACCURACY</b>   |   |   |        |            |                  |                              |
| BW                   | Output bandwidth                            |   | 220    | 295        |                  | $\text{kHz}$                 |
| THD                  | Total harmonic distortion <sup>(3)</sup>    | $f_{IN} = 10\text{kHz}$   |        | -80        |                  | dB                           |
| SNR                  | Signal-to-noise ratio                       | $f_{IN} = 1\text{kHz}$ , $BW = 10\text{kHz}$  | 80     | 84         |                  | dB                           |
|                      |   | $f_{IN} = 10\text{kHz}$ , $BW = 100\text{kHz}$  |        | 75         |                  |                              |
| <b>POWER SUPPLY</b>  |   |   |        |            |                  |                              |
| IDD1                 | High-side supply current                    |   |        | 5.6        | 6.9              | mA                           |
| IDD2                 | Low-side supply current                     |   |        | 6.4        | 9.9              | mA                           |
| VDD1 <sub>UV</sub>   | High-side undervoltage detection threshold  | VDD1 rising   | 2.5    | 2.6        | 2.7              | V                            |
|                      |   | VDD1 falling  | 1.9    | 2.0        | 2.1              |                              |

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $\text{VDD1} = 3.0\text{V}$  to  $5.5\text{V}$ ,  $\text{VDD2} = 3.0\text{V}$  to  $5.5\text{V}$ ,  $V_{\text{INP}} = -50\text{mV}$  to  $+50\text{mV}$ , and  $V_{\text{INN}} = 0\text{V}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $\text{VDD1} = 5\text{V}$ , and  $\text{VDD2} = 3.3\text{V}$  (unless otherwise noted)

| PARAMETER          |   | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|--------------------|---|-----------------|-----|------|-----|------|
| VDD2 <sub>UV</sub> | Low-side undervoltage detection threshold | VDD2 rising     | 2.3 | 2.5  | 2.7 | V    |
|                    |   | VDD2 falling    | 1.9 | 2.05 | 2.2 |      |

- (1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:  

$$TCV_{\text{OS}} = (V_{\text{OS,MAX}} - V_{\text{OS,MIN}}) / \text{TempRange}$$
 where  $V_{\text{OS,MAX}}$  and  $V_{\text{OS,MIN}}$  refer to the maximum and minimum  $V_{\text{OS}}$  values measured within the temperature range ( $-40$  to  $125^\circ\text{C}$ ).
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:  

$$TCE_G \text{ (ppm)} = ((E_{\text{G,MAX}} - E_{\text{G,MIN}}) / \text{TempRange}) \times 10^4$$
 where  $E_{\text{G,MAX}}$  and  $E_{\text{G,MIN}}$  refer to the maximum and minimum  $E_{\text{G}}$  values (in %) measured within the temperature range ( $-40$  to  $125^\circ\text{C}$ ).

## 6.14 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER       |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|-----------------|--|--|-----|-----|-----|---------------|
| $t_r$           | Output signal rise time  |  |     | 1.7 |     | $\mu\text{s}$ |
| $t_f$           | Output signal fall time  |  |     | 1.7 |     | $\mu\text{s}$ |
|                 | $V_{\text{INX}}$ to $V_{\text{OUTX}}$ signal delay (50% - 10%) | Unfiltered output  | 0.8 | 1.3 |     | $\mu\text{s}$ |
|                 | $V_{\text{INX}}$ to $V_{\text{OUTX}}$ signal delay (50% - 50%) | Unfiltered output  | 1.6 | 2.1 |     | $\mu\text{s}$ |
|                 | $V_{\text{INX}}$ to $V_{\text{OUTX}}$ signal delay (50% - 90%) | Unfiltered output  | 2.5 | 3   |     | $\mu\text{s}$ |
| $t_{\text{AS}}$ | Analog settling time   | $\text{VDD1}$ step to $3.0\text{V}$ with $\text{VDD2} \geq 3.0\text{V}$ , to $V_{\text{OUTP}}, V_{\text{OUTN}}$ valid, 0.1% settling | 20  | 100 |     | $\mu\text{s}$ |

## 6.15 Timing Diagram

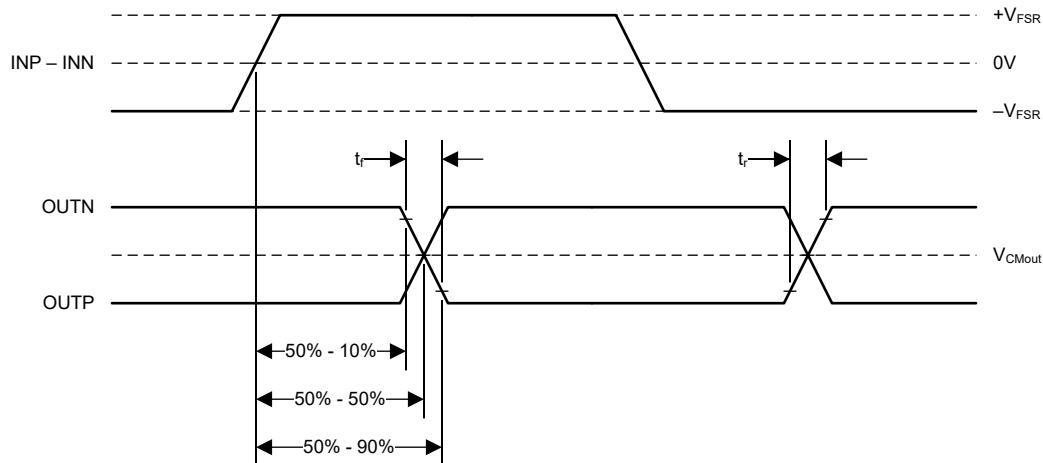


Figure 6-1. Rise, Fall, and Delay Time Waveforms

## 6.16 Insulation Characteristics Curves

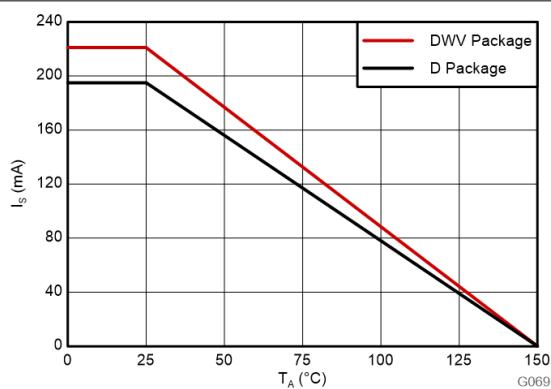


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

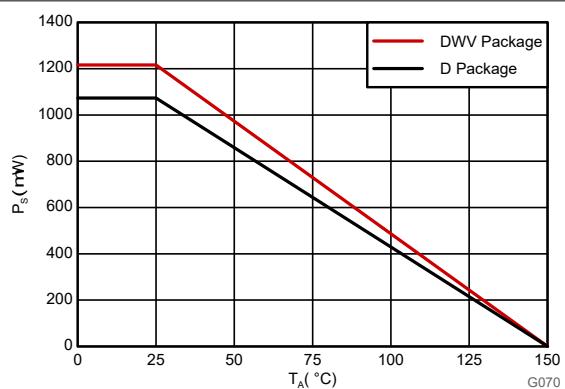
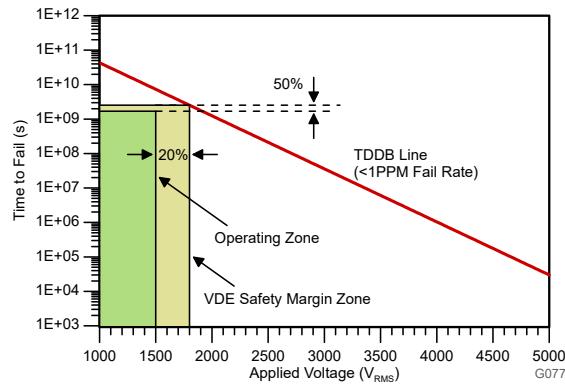
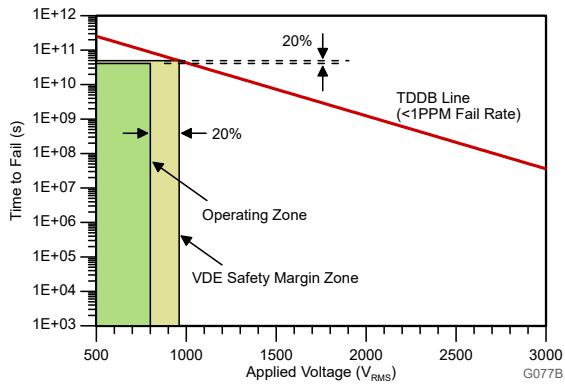


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



$T_A$  up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V<sub>RMS</sub>, projected operating lifetime  $\geq$  50 years

Figure 6-4. Isolation Capacitor Lifetime Projection (Reinforced Isolation)



$T_A$  up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 800V<sub>RMS</sub>, projected operating lifetime  $>> 100$  years

Figure 6-5. Isolation Capacitor Lifetime Projection (Basic Isolation)

## 6.17 Typical Characteristics

at VDD1 = 5V, VDD2 = 3.3V, VINP = -50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

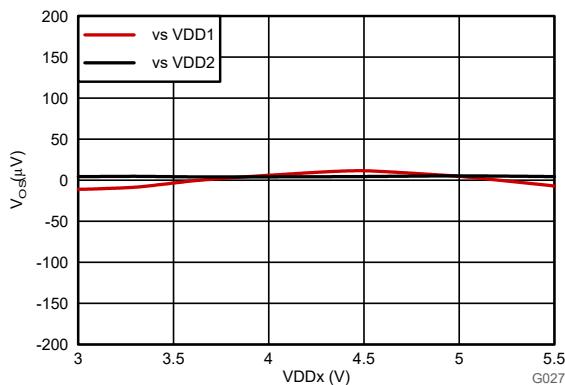


Figure 6-6. Input Offset Voltage vs Supply Voltage

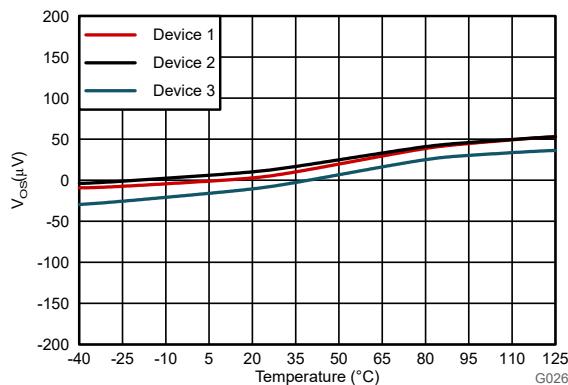


Figure 6-7. Input Offset Voltage vs Temperature

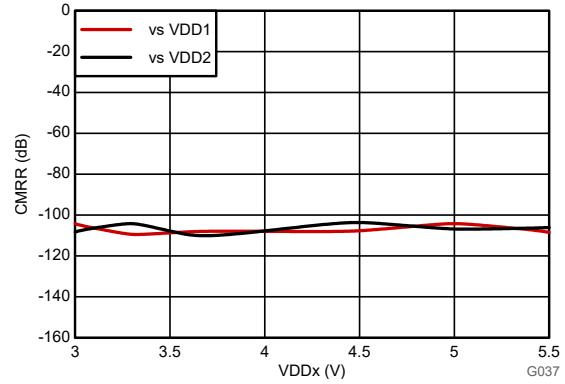


Figure 6-8. Common-Mode Rejection Ratio vs Supply Voltage

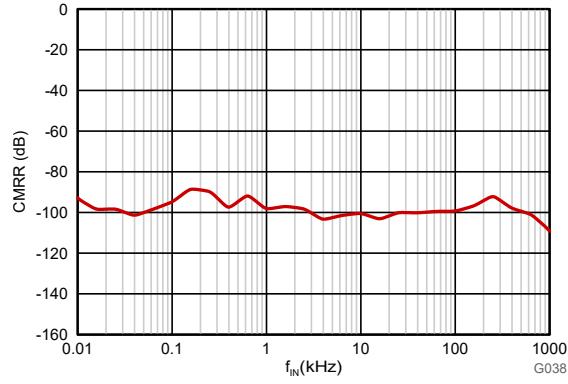


Figure 6-9. Common-Mode Rejection Ratio vs Input Frequency

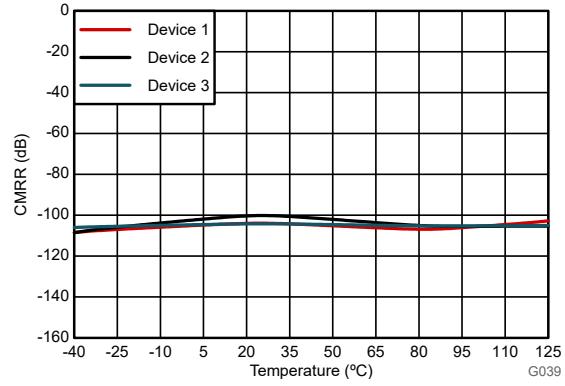


Figure 6-10. Common-Mode Rejection Ratio vs Temperature

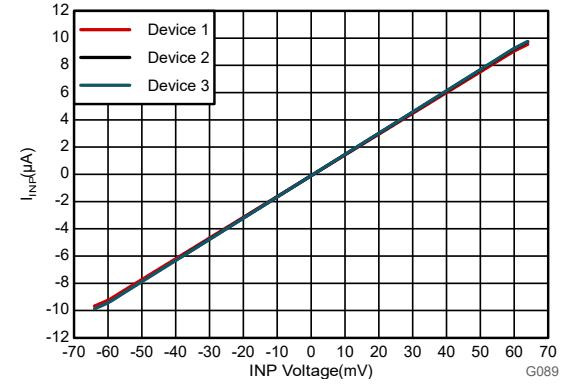
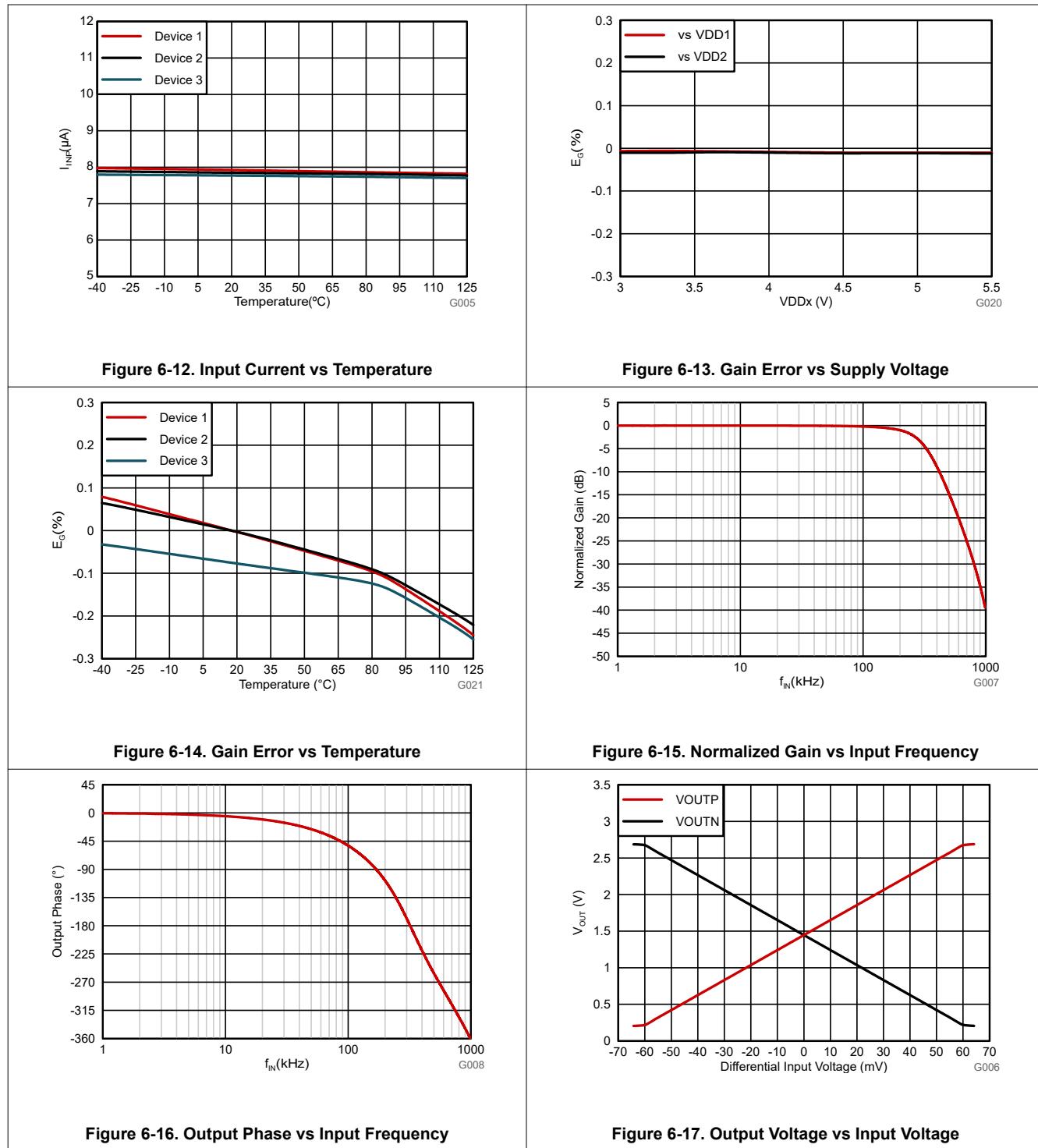


Figure 6-11. Input Current vs Input Voltage

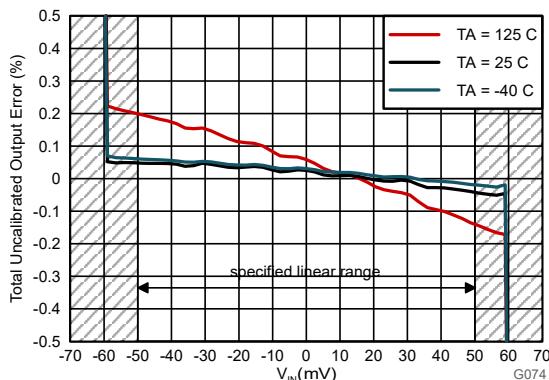
## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = -50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)



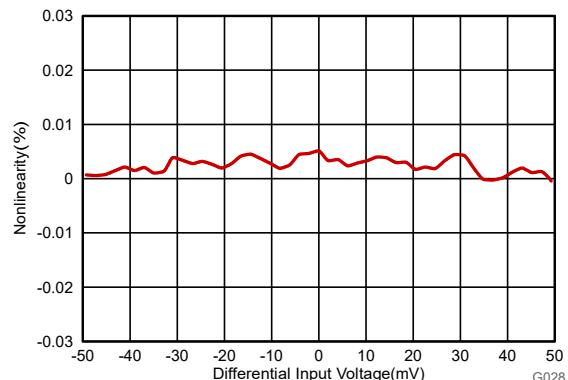
## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = -50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

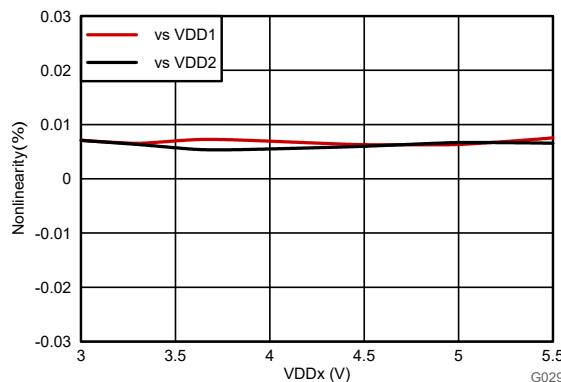


Total uncalibrated output error is defined as:  
 $(V_{OUT} / G - V_{IN}) / (V_{Clipping} \times 100)$ , where G is the nominal gain of the device (41V/V) and V<sub>Clipping</sub> is 0.064V

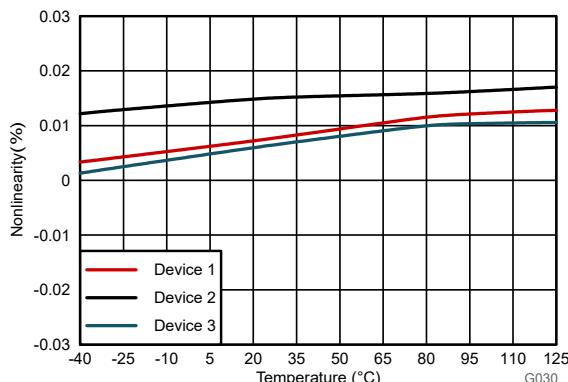
**Figure 6-18. Unadjusted Error vs Input Voltage**



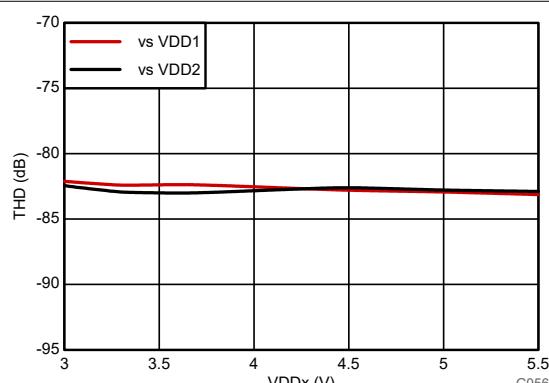
**Figure 6-19. Nonlinearity vs Input Voltage**



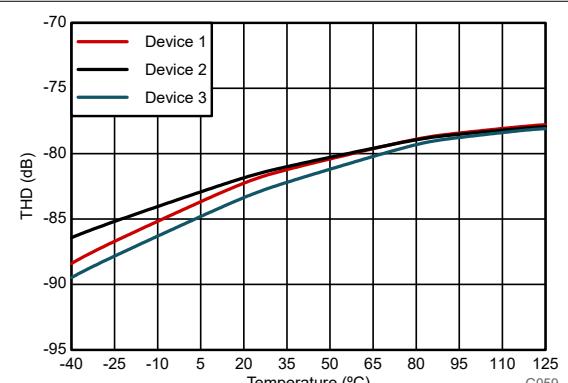
**Figure 6-20. Nonlinearity vs Supply Voltage**



**Figure 6-21. Nonlinearity vs Temperature**



**Figure 6-22. Total Harmonic Distortion vs Supply Voltage**



**Figure 6-23. Total Harmonic Distortion vs Temperature**

## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = -50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

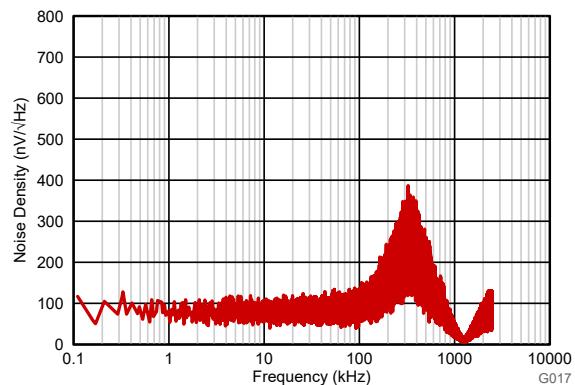


Figure 6-24. Input-Referred Noise Density vs Frequency

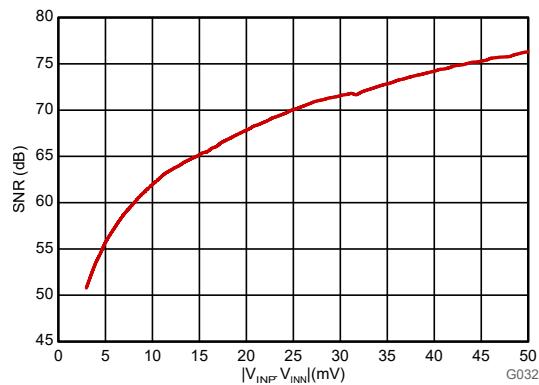


Figure 6-25. Signal-to-Noise Ratio vs Input Voltage

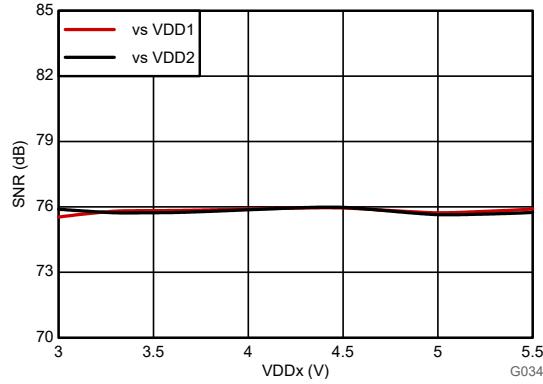


Figure 6-26. Signal-to-Noise Ratio vs Supply Voltage

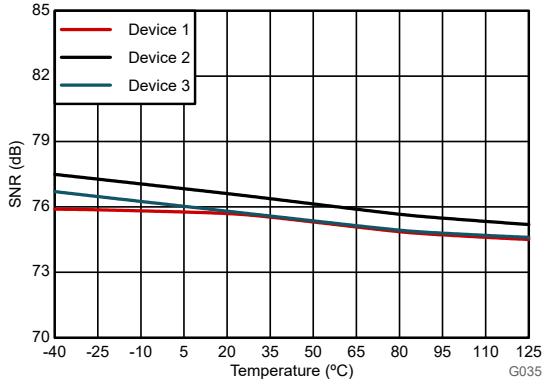


Figure 6-27. Signal-to-Noise Ratio vs Temperature

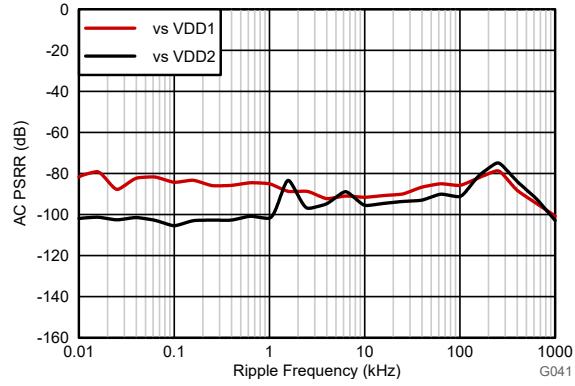


Figure 6-28. Power-Supply Rejection Ratio vs Ripple Frequency

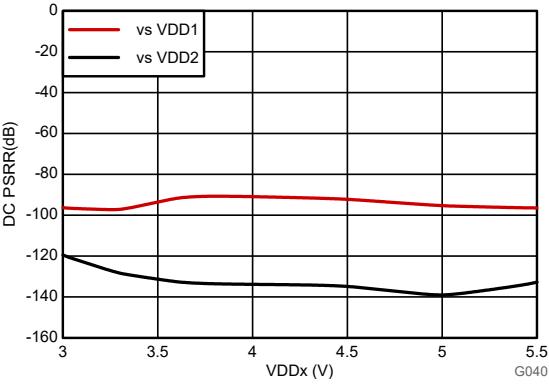


Figure 6-29. Power-Supply Rejection Ratio vs Supply Voltage

## 6.17 Typical Characteristics (continued)

at  $VDD1 = 5V$ ,  $VDD2 = 3.3V$ ,  $VINP = -50mV$  to  $50mV$ ,  $VINN = 0V$ , and  $f_{IN} = 10kHz$  (unless otherwise noted)

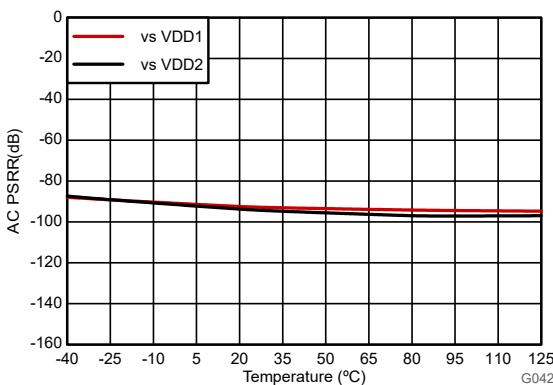


Figure 6-30. Power-Supply Rejection Ratio vs Temperature

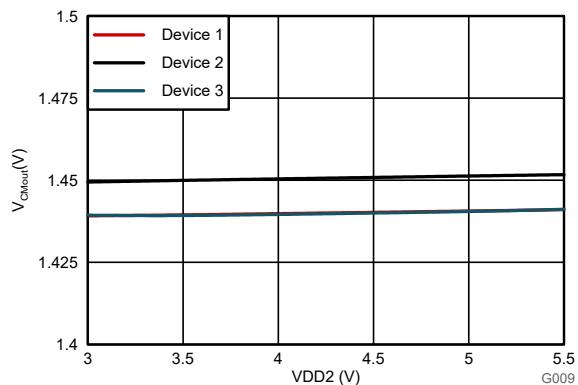


Figure 6-31. Output Common-Mode Voltage vs Low-Side Supply Voltage

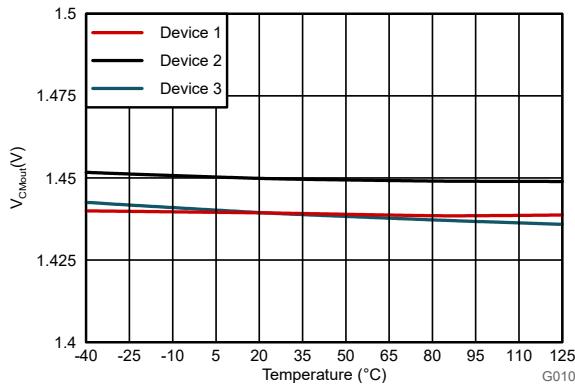


Figure 6-32. Output Common-Mode Voltage vs Temperature

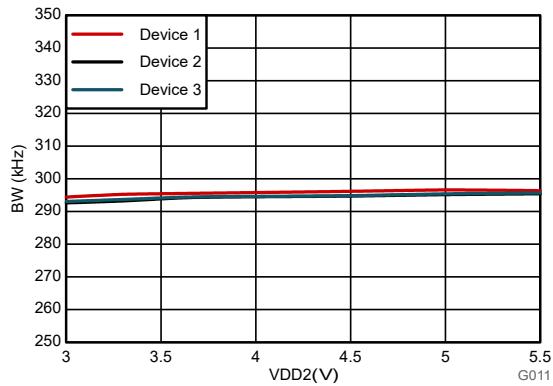


Figure 6-33. Output Bandwidth vs Low-Side Supply Voltage

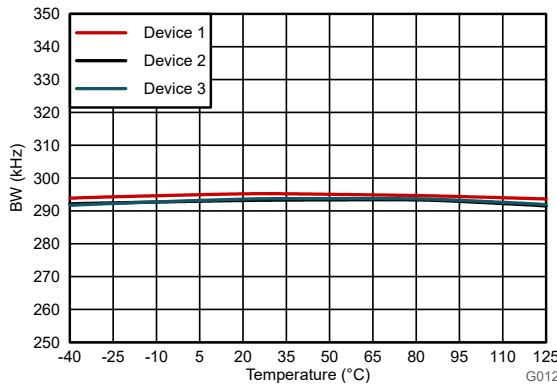


Figure 6-34. Output Bandwidth vs Temperature

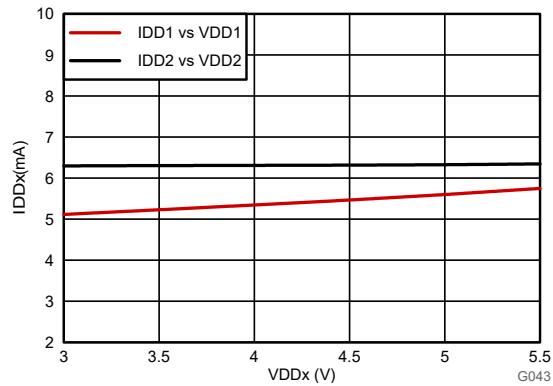


Figure 6-35. Supply Current vs Supply Voltage

## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VINP = -50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

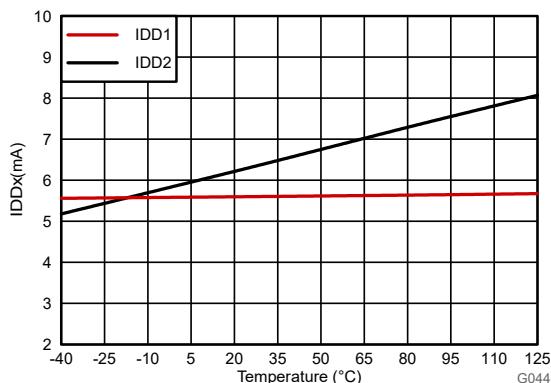


Figure 6-36. Supply Current vs Temperature

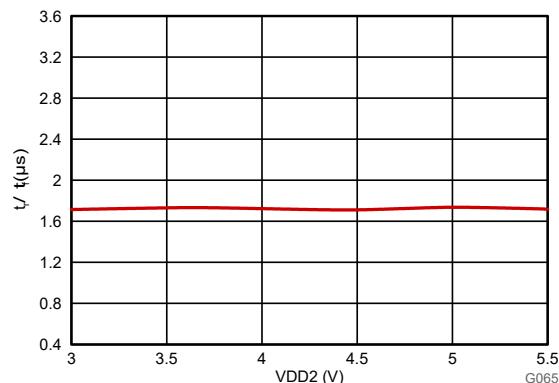


Figure 6-37. Output Rise and Fall Time vs Low-Side Supply

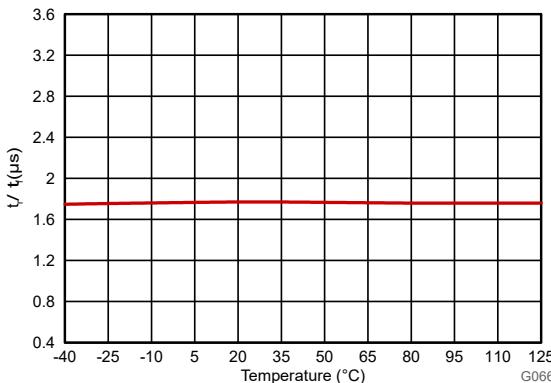


Figure 6-38. Output Rise and Fall Time vs Temperature

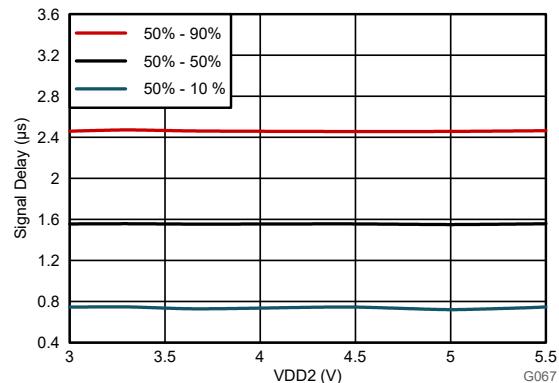


Figure 6-39. V<sub>IN</sub> to V<sub>OUT</sub> Signal Delay vs Low-Side Supply Voltage

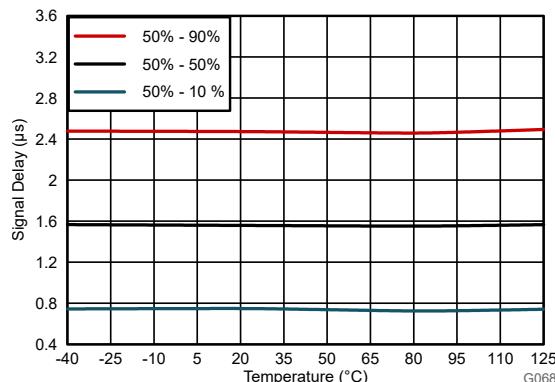


Figure 6-40. V<sub>IN</sub> to V<sub>OUT</sub> Signal Delay vs Temperature

## 7 Detailed Description

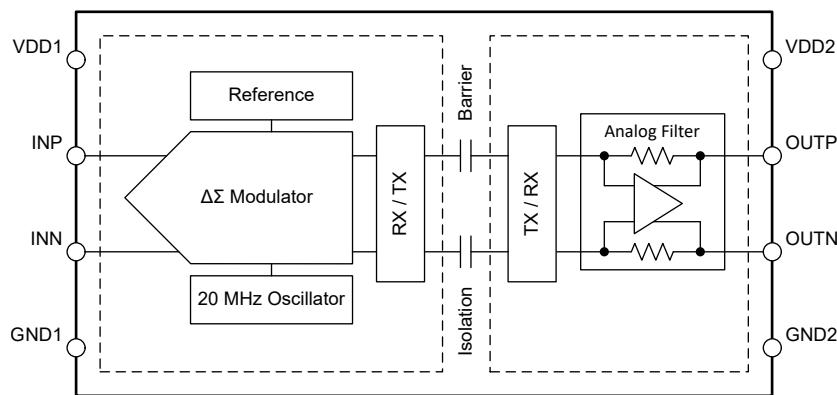
### 7.1 Overview

The AMC0x02D-Q1 is a precision, galvanically isolated amplifier with a  $\pm 50\text{mV}$ , differential input and differential output. The input stage of the device drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side.

On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins. This differential output signal is proportional to the input signal.

The  $\text{SiO}_2$ -based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#). The digital modulation used in the AMC0x02D-Q1 transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Analog Input

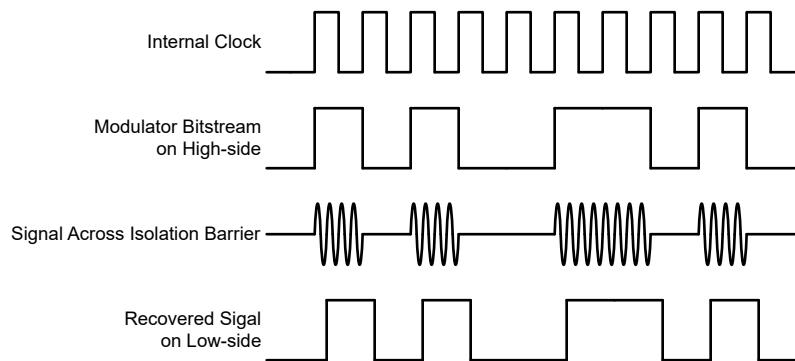
The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range ( $V_{FSR}$ ).  $V_{FSR}$  is specified in the *Recommended Operating Conditions* table.

### 7.3.2 Isolation Channel Signal Transmission

As shown in [Figure 7-1](#), the AMC0x02D-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the  $\text{SiO}_2$ -based isolation barrier. The transmit driver (TX) is illustrated in the *Functional Block Diagram*. TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital one. However, TX does not send a signal to represent a digital zero. The nominal frequency of the carrier used inside the AMC0x02D-Q1 is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC0x02D-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.



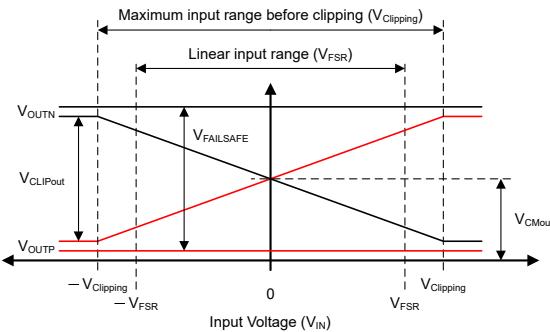
**Figure 7-1. OOK-Based Modulation Scheme**

### 7.3.3 Analog Output

The AMC0x02D-Q1 provides a differential analog output voltage on the OUTP and OUTN pins proportional to the input voltage. For input voltages in the range from  $V_{FSR, MIN}$  to  $V_{FSR, MAX}$ , the device has a linear response with an output voltage equal to:

$$V_{OUT} = V_{OUTP} - V_{OUTN} = 41 \times V_{IN} = 41 \times (V_{INP} - V_{INN}) \quad (1)$$

At zero input, both pins output the same common-mode output voltage  $V_{CMout}$ , as specified in the [Electrical Characteristics](#) table. For absolute input voltages greater than  $|V_{FSR}|$  but less than  $|V_{Clipping}|$ , the differential output voltage continues to increase in magnitude, but with reduced linearity performance. The outputs saturate at a differential output voltage of  $V_{CLIPout}$ , as shown in [Figure 7-2](#), if the input voltage exceeds the  $V_{Clipping}$  value.



**Figure 7-2. Input to Output Transfer Curve of the AMC0x02D-Q1**

The AMC0x02D-Q1 output offers a fail-safe feature that simplifies diagnostics on a system level. [Figure 7-2](#) shows the behavior in fail-safe mode, in which the AMC0x02D-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active:

- When the high-side supply VDD1 of the AMC0x02D-Q1 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold  $VDD1_{UV}$

Use the maximum  $V_{FAILSAFE}$  voltage specified in the [Electrical Characteristics](#) table as a reference value for fail-safe detection on a system level.

## 7.4 Device Functional Modes

The AMC0x02D-Q1 operates in one of the following states:

- Off-state: The low-side supply (VDD2) is below the  $VDD2_{UV}$  threshold. The device is not responsive. OUTP and OUTN are in Hi-Z state. Internally, OUTP and OUTN are clamped to VDD2 and GND2 by ESD protection diodes.
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within recommended operating conditions. The high-side supply (VDD1) is below the  $VDD1_{UV}$  threshold. The device outputs the  $V_{FAILSAFE}$  voltage.
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage  $V_{IN}$  is above the maximum clipping voltage  $V_{Clipping, MAX}$ . The device outputs positive  $V_{CLIPout}$ .
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage  $V_{IN}$  is below the minimum clipping voltage  $V_{Clipping, MIN}$ . The device outputs negative  $V_{CLIPout}$ .
- Normal operation: VDD1, VDD2, and  $V_{IN}$  are within the recommended operating conditions. The device outputs a differential voltage that is proportional to the input voltage.

Table 7-1 lists the operating modes.

**Table 7-1. Device Operational Modes**

| OPERATING CONDITION      | VDD1                 | VDD2                 | $V_{IN}$                     | DEVICE RESPONSE   |
|--------------------------|----------------------|----------------------|------------------------------|---|
| Off                      | Don't care           | $VDD2 < VDD2_{UV}$   | Don't care                   | OUTP and OUTN are in Hi-Z state. Internally, OUTP and OUTN are clamped to VDD2 and GND2 by ESD protection diodes. |
| Missing high-side supply | $VDD1 < VDD1_{UV}$   | Valid <sup>(1)</sup> | Don't care                   | The device outputs the $V_{FAILSAFE}$ voltage.  |
| Input overrange          | Valid <sup>(1)</sup> | Valid <sup>(1)</sup> | $V_{IN} > V_{Clipping, MAX}$ | The device outputs positive $V_{CLIPout}$ .   |
| Input underrange         | Valid <sup>(1)</sup> | Valid <sup>(1)</sup> | $V_{IN} < V_{Clipping, MIN}$ | The device outputs negative $V_{CLIPout}$ .   |
| Normal operation         | Valid <sup>(1)</sup> | Valid <sup>(1)</sup> | Valid <sup>(1)</sup>         | The device outputs a differential voltage that is proportional to the input voltage.                              |

(1) *Valid* denotes operation within the recommended operating conditions.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The AMC0x02D-Q1 has low analog input voltage range, high accuracy, low temperature drift, and high common-mode transient immunity. The AMC0x02D-Q1 is primarily designed for shunt-based current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC0x02D-Q1 is preferred for isolated current sensing in HEV/EV charging piles, HEV/EV onboard chargers (OBC), HEV/EV DC/DC converters, and HEV/EV traction inverters applications.

### 8.2 Typical Application

The following image shows the AMC0x02D-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop. The AMC0x02D-Q1 high-side circuitry senses the voltage drop across the shunt resistor, then digitizes and transfers data across the isolation barrier to the low side. Low-side circuitry reconstructs the digitized data into an analog signal and provides the signal as a differential voltage on the output pins.

The differential input, differential output, and high common-mode transient immunity (CMTI) of the AMC0x02D-Q1 provide reliable and accurate operation even in high-noise environments.

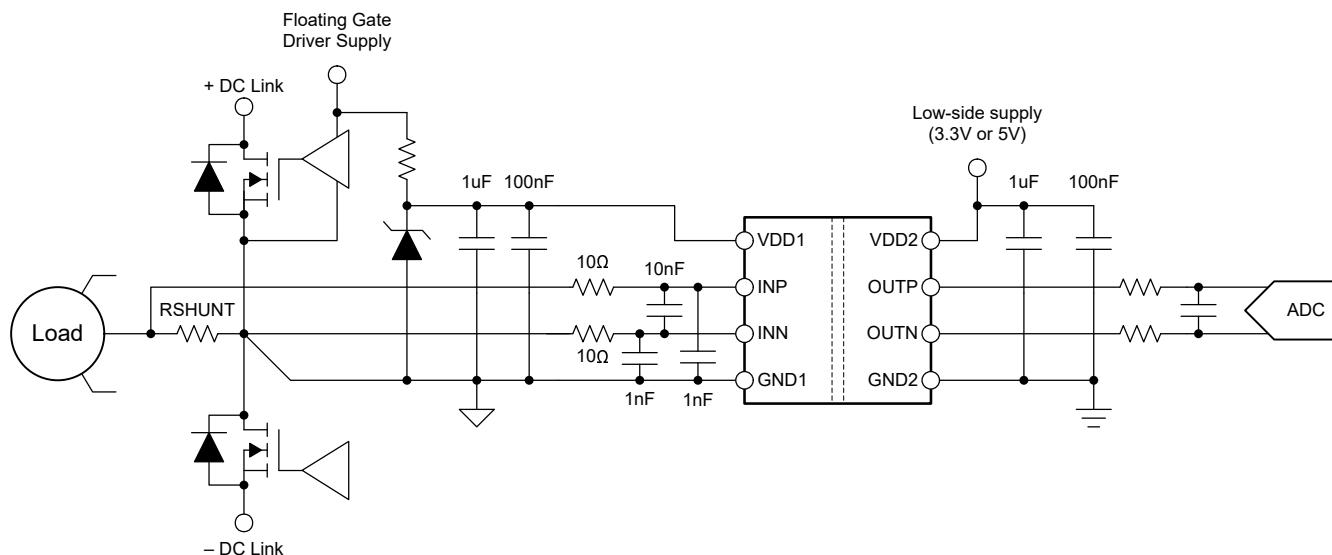


Figure 8-1. Using the AMC0x02D-Q1 for Current Sensing in a Typical Application

### 8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

**Table 8-1. Design Requirements**

| PARAMETER  | VALUE                       |
|--|-----------------------------|
| High-side supply voltage                         | 3.3V or 5V                  |
| Low-side supply voltage                          | 3.3V or 5V                  |
| Voltage drop across RSHUNT for a linear response | $\pm 50\text{mV}$ (maximum) |

### 8.2.2 Detailed Design Procedure

In the [Typical Application](#) figure, the high-side power supply (VDD1) for the AMC0x02D-Q1 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC0x02D-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC0x02D-Q1 are connected to the inner leads. GND1 is then connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. Do not short GND1 to INN directly at the device input; see the [Layout Example](#) section for more details.

Use Ohm's Law to calculate the voltage drop across the shunt resistor ( $V_{\text{SHUNT}}$ ) for the desired measured current:

$$V_{\text{SHUNT}} = I \times R_{\text{SHUNT}} \quad (2)$$

Select a RSHUNT value to satisfy the following two conditions:

- First, the voltage drop caused by the nominal current range does not exceed the recommended differential input voltage range of  $V_{\text{SHUNT}} \leq \pm 50\text{mV}$ .
- Secondly, the voltage drop caused by the maximum allowed overcurrent does not exceed the input voltage that causes a clipping output. Keep  $V_{\text{SHUNT}} \leq V_{\text{Clipping}}$ .

#### 8.2.2.1 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20MHz) of the  $\Delta\Sigma$  modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Place capacitors C6 and C7 to improve common-mode rejection at high frequencies (>1MHz) and to improve offset voltage performance. For best performance, verify C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering.

For most applications, the structure shown in [Figure 8-2](#) achieves excellent performance.

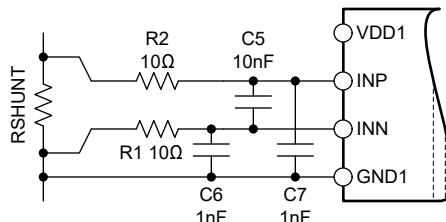


Figure 8-2. Input Filter

### 8.2.2.2 Differential-to-Single-Ended Output Conversion

Many systems use ADCs with single-ended inputs that cannot connect directly to the differential output of the AMC0x02D-Q1. Figure 8-3 shows a circuit for converting the differential output signal into a single-ended signal in front of the ADC. For  $R1 = R3$  and  $R2 = R4$ , the output voltage equals  $(R2 / R1) \times (V_{OUTP} - V_{OUTN}) + V_{REF}$ . For  $C1 = C2$  the bandwidth of the filter becomes  $1 / (2 \times \pi \times C1 \times R1)$ . Configure the bandwidth of the filter to match the bandwidth requirement of the system. For best linearity, use capacitors with low voltage coefficients (such as NP0-type capacitors). For most applications,  $R1 = R2 = R3 = R4 = 3.3\text{k}\Omega$  and  $C1 = C2 = 330\text{pF}$  yield good performance.

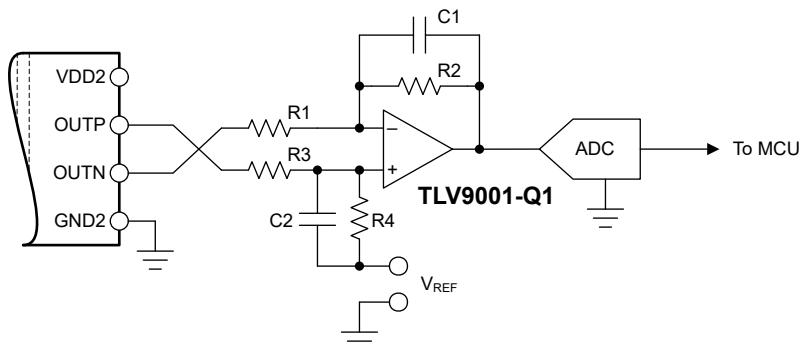


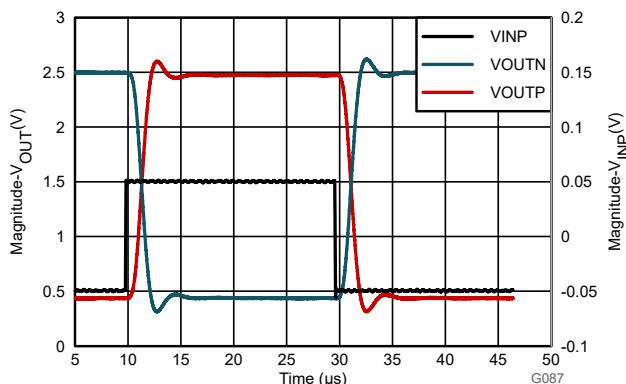
Figure 8-3. Connecting the AMC0x02D-Q1 Output to a Single-Ended Input ADC

The following reference guides provide further information on the general procedure to design the filtering and driving stages of SAR ADCs. These reference guides are available for download at [www.ti.com](http://www.ti.com).

- [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) reference guide
- [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guide

### 8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, the isolated amplifier is required to have low signal delay. [Figure 8-4](#) shows the typical full-scale step response of the AMC0x02D-Q1.



**Figure 8-4. Step Response of the AMC0x02D-Q1**

## 8.3 Best Design Practices

Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not short GND1 to INN directly at the device input. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. See the [Layout Example](#) section for more details.

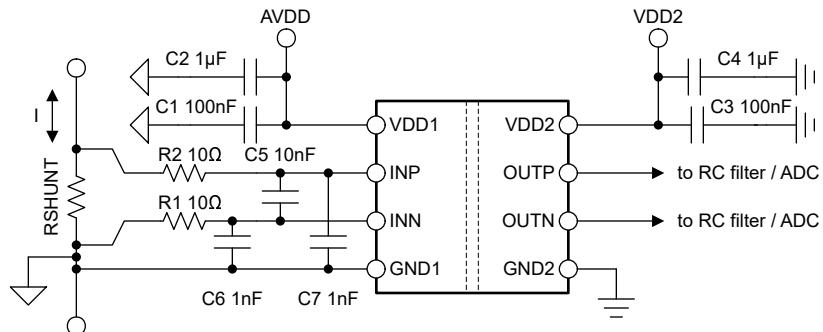
Do not leave the inputs of the AMC0x02D-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current potentially drives the inputs to a positive value that exceeds the operating common-mode input voltage. This condition causes the device to output the fail-safe voltage described in the [Analog Output](#) section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the [Recommended Operating Conditions](#) table.

## 8.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0x02D-Q1 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver [SN6501-Q1](#) and a transformer that supports the desired isolation voltage ratings.

The AMC0x02D-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1μF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. [Figure 8-5](#) shows a decoupling diagram for the AMC0x02D-Q1.



**Figure 8-5. Decoupling of the AMC0x02D-Q1**

Verify capacitors provide adequate **effective** capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

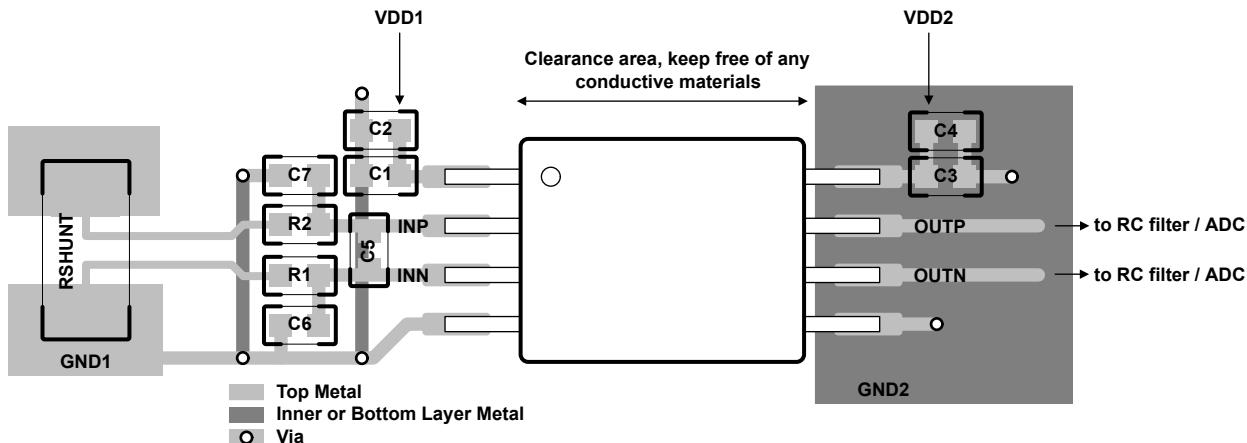
## 8.5 Layout

### 8.5.1 Layout Guidelines

The [Layout Example](#) section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0x02D-Q1 supply pins). This example also depicts the placement of other components required by the device.

### 8.5.2 Layout Example

**Figure 8-6. Recommended Layout of the AMC0x02D-Q1**



## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *TLV900x-Q1 Low-Power, RRIO, 1MHz Automotive Operational Amplifier* data sheet
- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool
- Texas Instruments, *Isolated Amplifier Current Sensing Excel Calculator* design tool

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE          | REVISION | NOTES           |
|---------------|----------|-----------------|
| December 2025 | *        | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 11.1 Mechanical Data

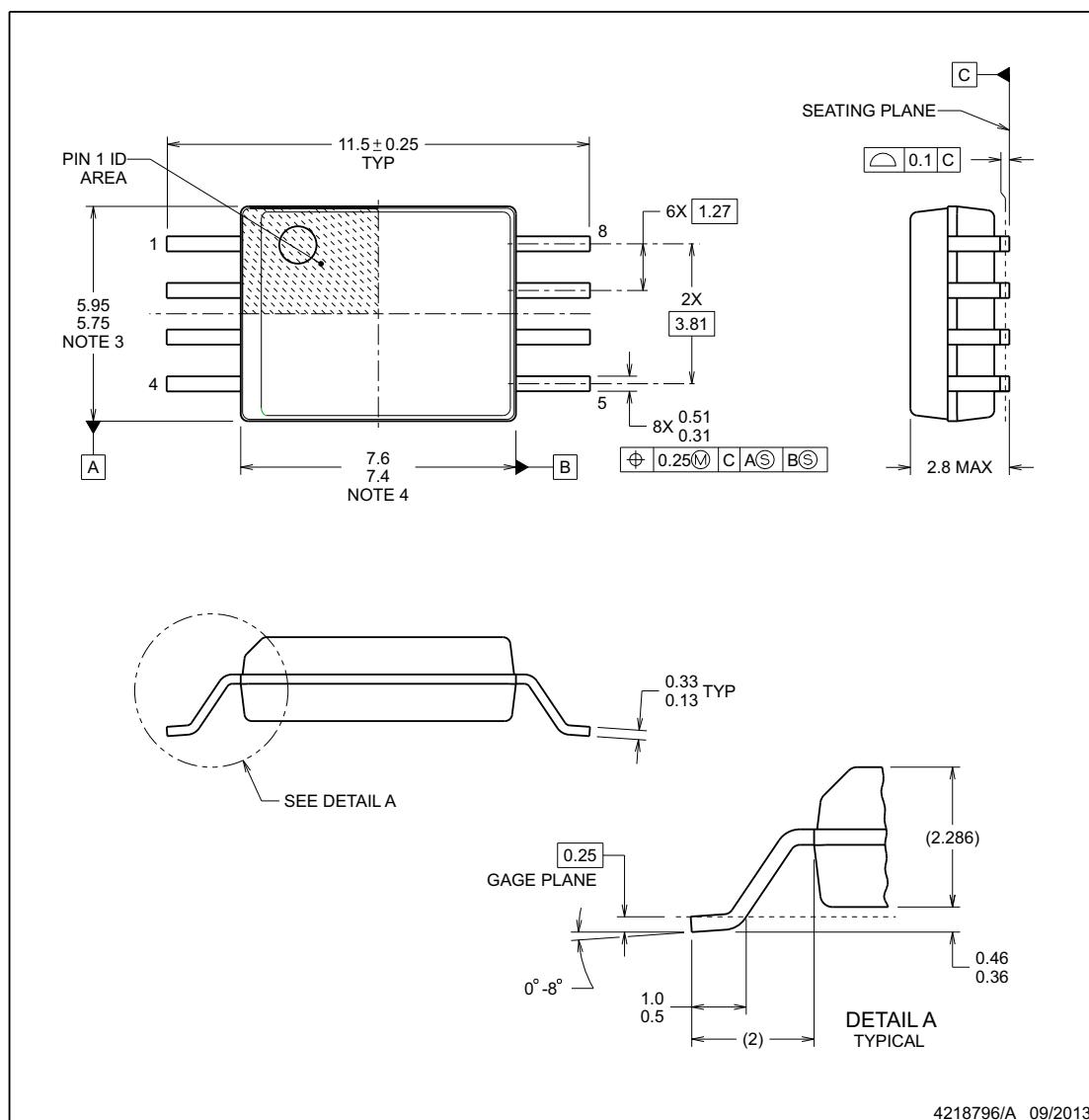
### PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

SOIC



#### NOTES:

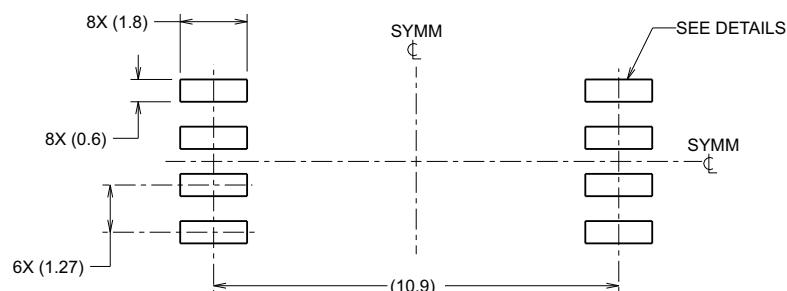
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

## EXAMPLE BOARD LAYOUT

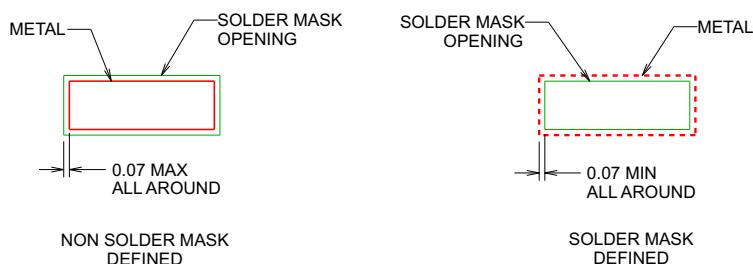
DWV0008A

SOIC - 2.8 mm max height

SOIC



LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

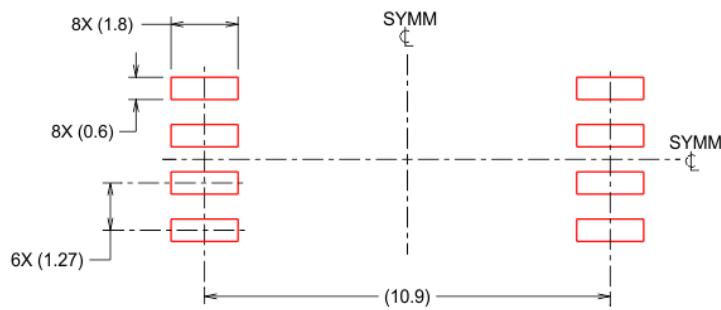
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DWV0008A

SOIC - 2.8 mm max height

SOIC



4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

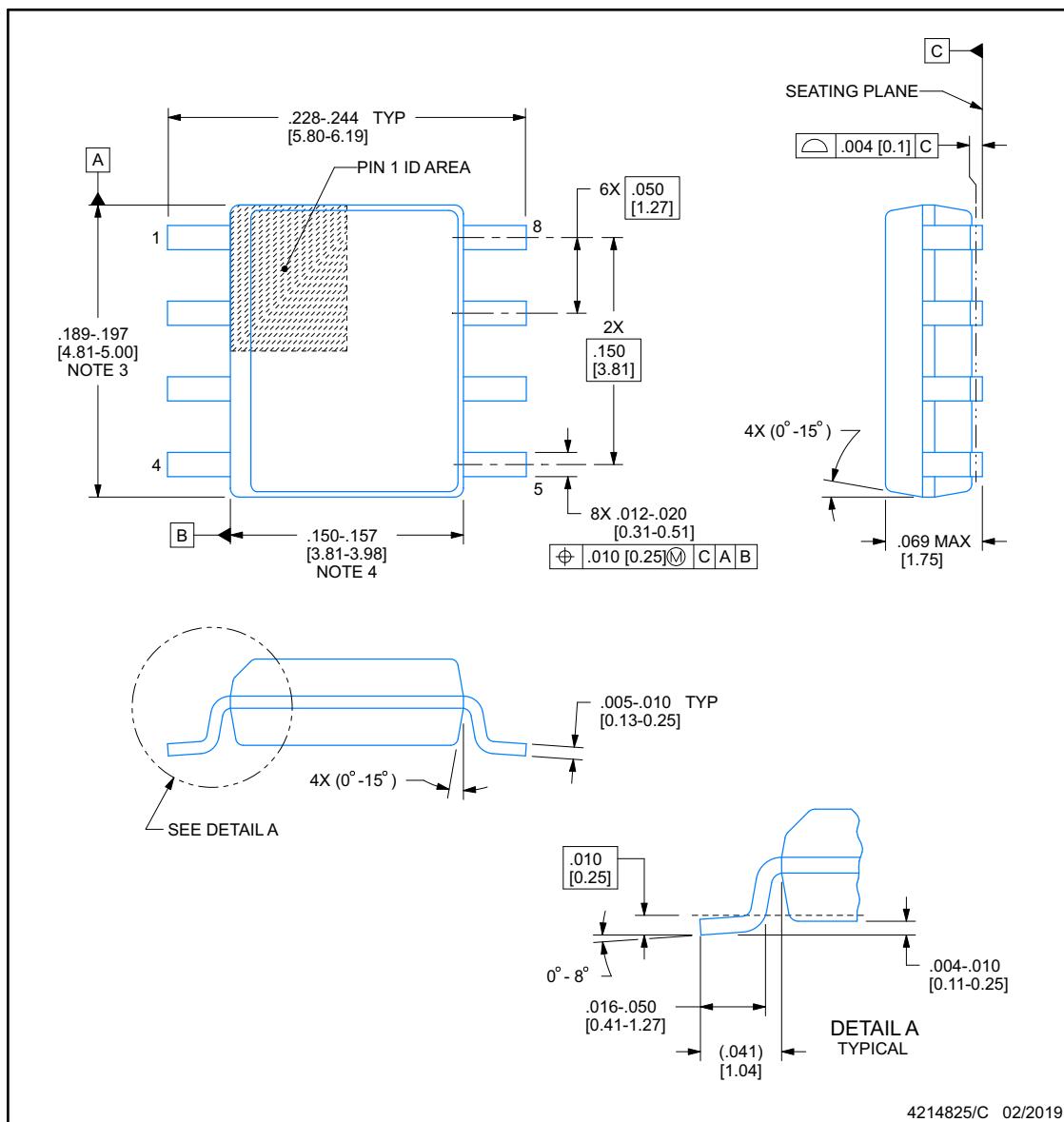


## PACKAGE OUTLINE

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

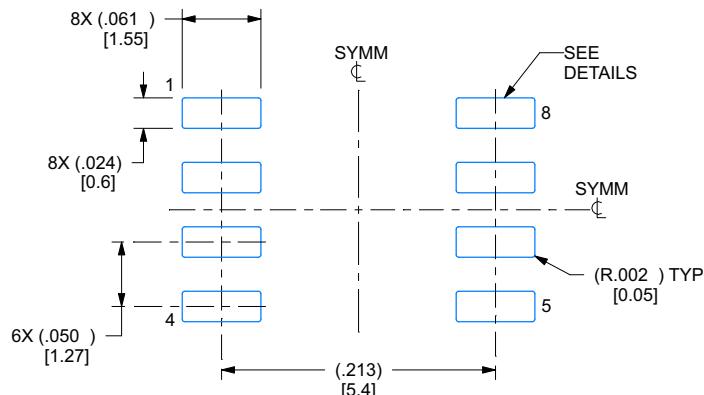
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

## EXAMPLE BOARD LAYOUT

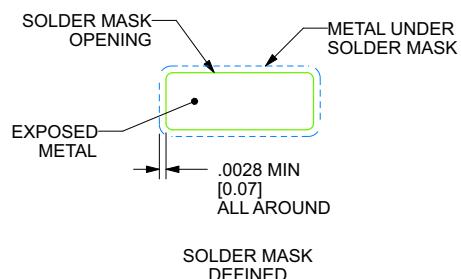
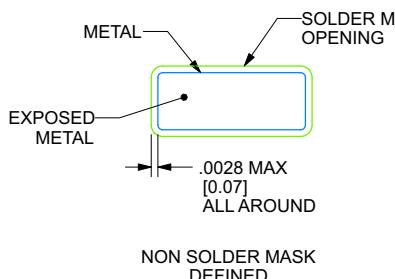
D0008A

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

#### NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

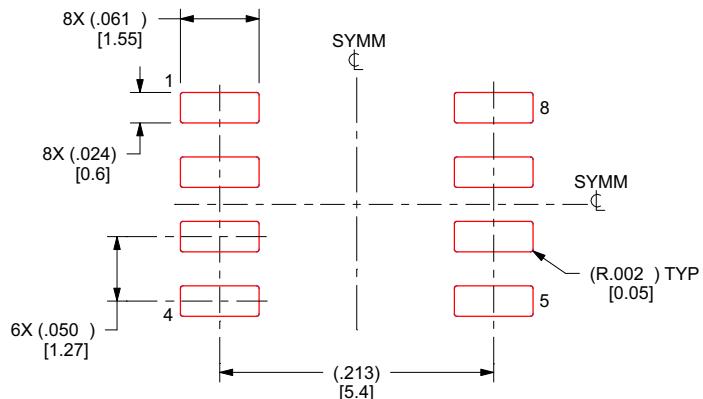


## EXAMPLE STENCIL DESIGN

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| AMC0302DQDWVRQ1       | Active        | Production           | SOIC (DWV)   8 | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | C0302D-Q            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

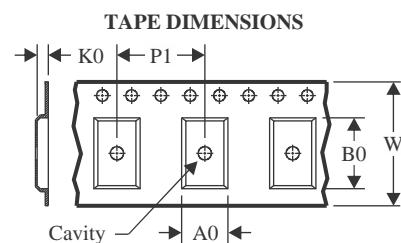
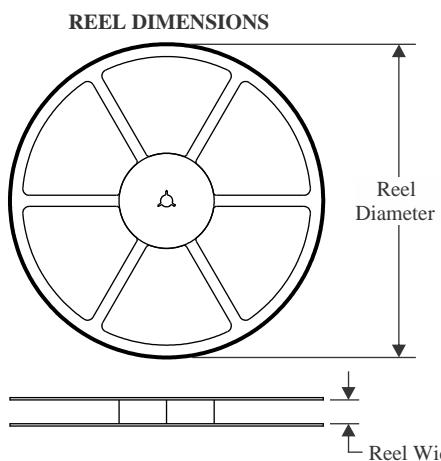
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

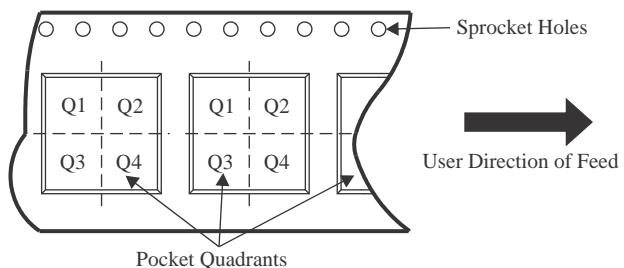
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

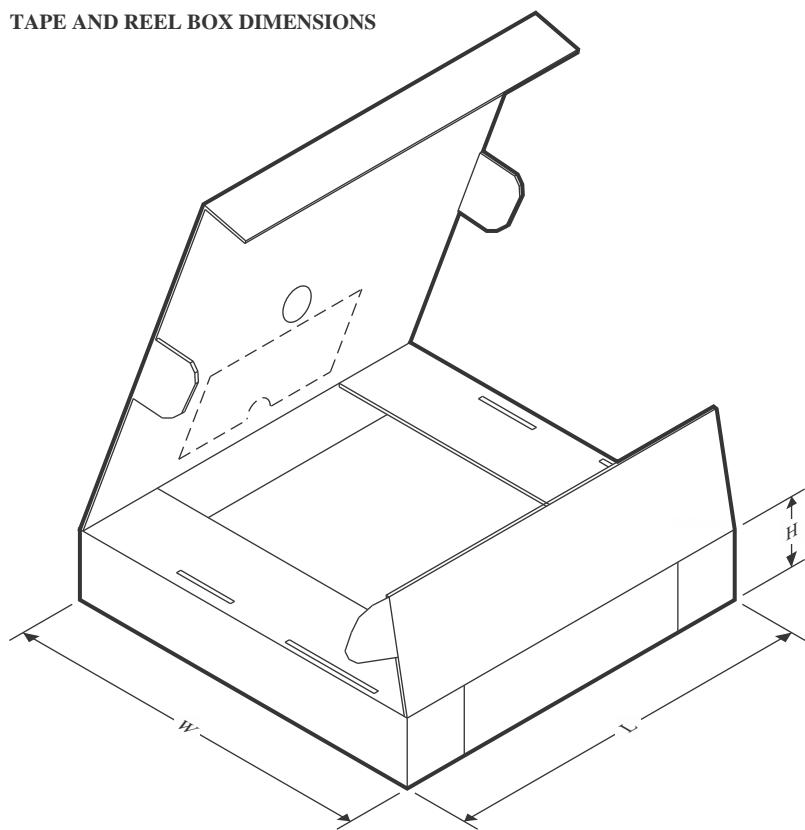
**TAPE AND REEL INFORMATION**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AMC0302DQDWVRQ1 | SOIC         | DWV             | 8    | 1000 | 330.0              | 16.4               | 12.15   | 6.2     | 3.05    | 16.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AMC0302DQDWVRQ1 | SOIC         | DWV             | 8    | 1000 | 353.0       | 353.0      | 32.0        |

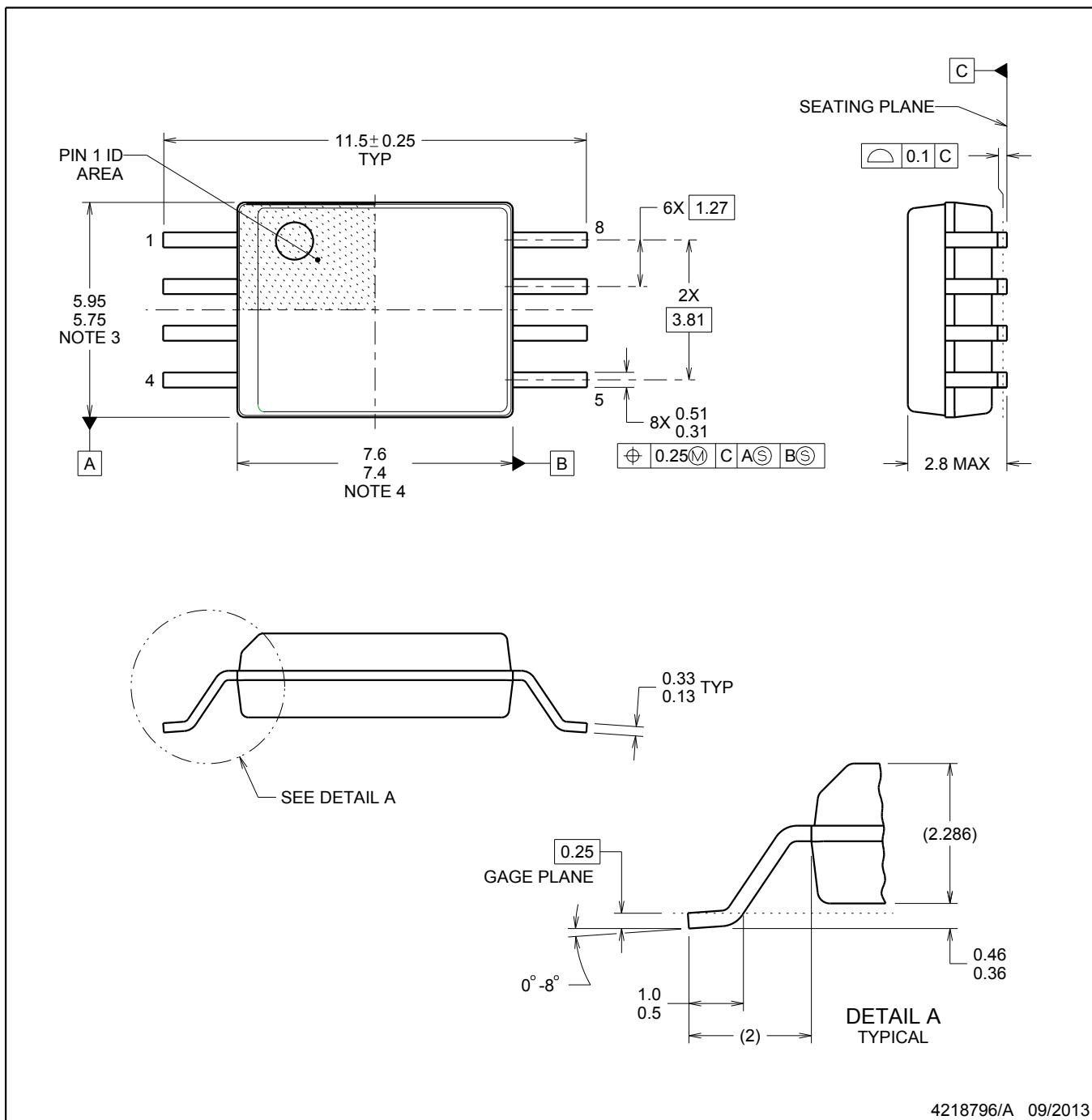
# PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

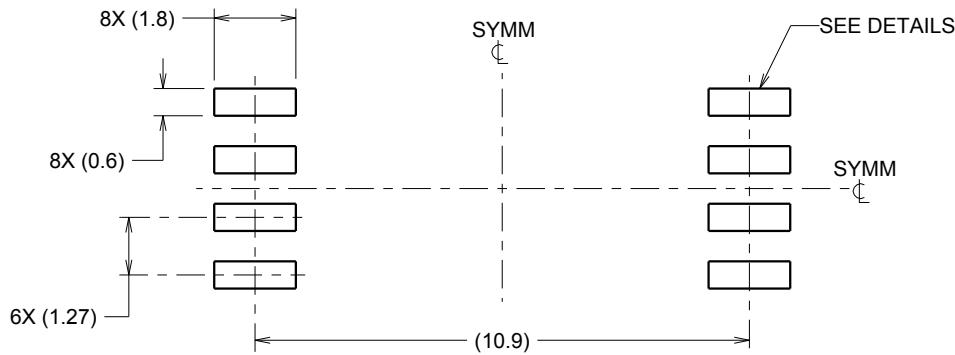
SOIC



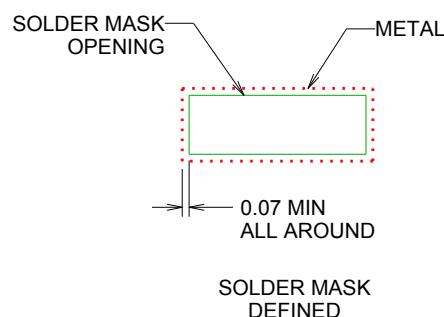
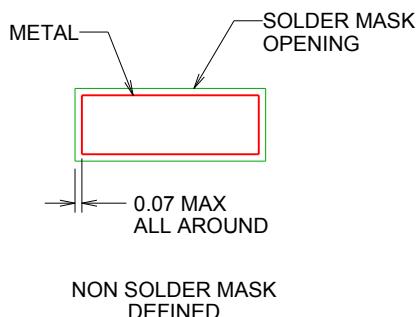
4218796/A 09/2013

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

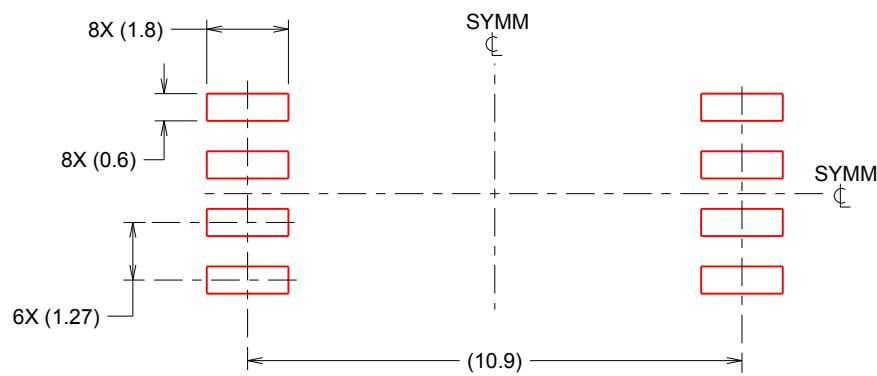
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025