ALM2402F-Q1 Automotive, Dual Operational Amplifier With High Current Output for Resolver Excitation

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional-Safety Capable
  - Documentation available to aid functional safety system design
- Low offset voltage: 1 mV (typical)
- High output current drive: 400 mA, continuous (per channel)
  - Replaces discrete op amps and transistors
- Wide supply range for both supplies (up to 16 V)
- Overtemperature shutdown
- Current limit
- Shutdown pin for low I_Q applications
- Stable with large capacitive loads
- 2-MHz gain bandwidth with 3.4-V/µs slew rate
- Internal RF/EMI filter
- Package: 14-pin HTSSOP (PWP)

2 Applications

- Resolver-based automotive applications
- Inverter and motor control
- Brake system
- Electric power steering (EPS)
- Rearview mirror module
- Automotive eMirrors
- Servo drive power stage module

3 Description

The ALM2402F-Q1 is a dual-power op amp with features and performance that make this device preferable for resolver-based automotive applications. The high gain bandwidth and slew rate of the device, along with a continuous high-output current-drive capability, make this device an excellent choice to provide a low distortion and differential high amplitude excitation required for modern resolvers. Current limiting and overtemperature detection enhance overall system robustness when driving analog signals over wires that are susceptible to faults.

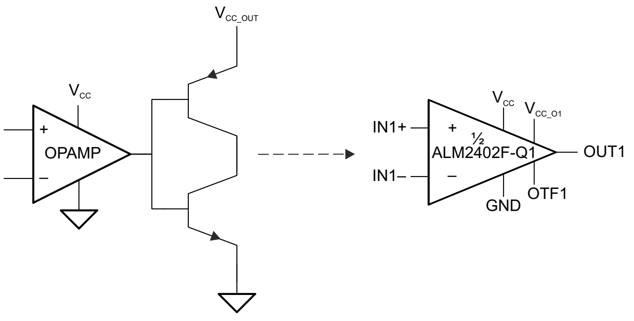
The ALM2402F-Q1 rail-to-rail output, enabled by the low $R_{ds(on)}$ PMOS and NMOS transistors, keeps the power dissipation low. The small HTSSOP package with thermal pad and low $R_{\theta JA}$ allows users to deliver high currents to loads while minimizing board space. This minimized board space is one of the key advantages offered by the ALM2402F-Q1 when used in modern hybrid and electric vehicles.

The ALM2402F-Q1 maximum output voltage is determined using the *Maximum Output Voltage vs Frequency* plot at the bottom of this page.

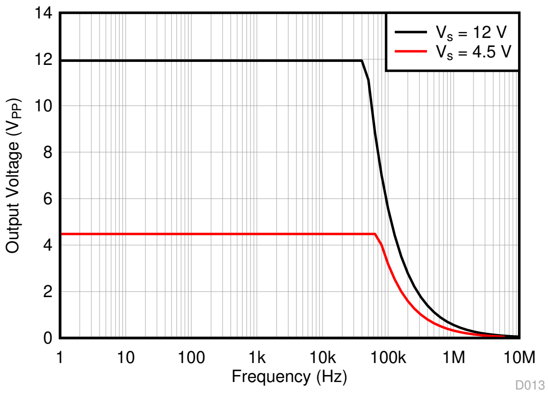
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ALM2402F-Q1	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic



Maximum Output Voltage vs Frequency

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (October 2021)	**Page**
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Added functional safety bullets to *Features* section.	1

Changes from Revision * (May 2019) to Revision A (September 2019)	**Page**
• Changed device from advanced information (preview) to production data (active).	1

5 Pin Configuration and Functions

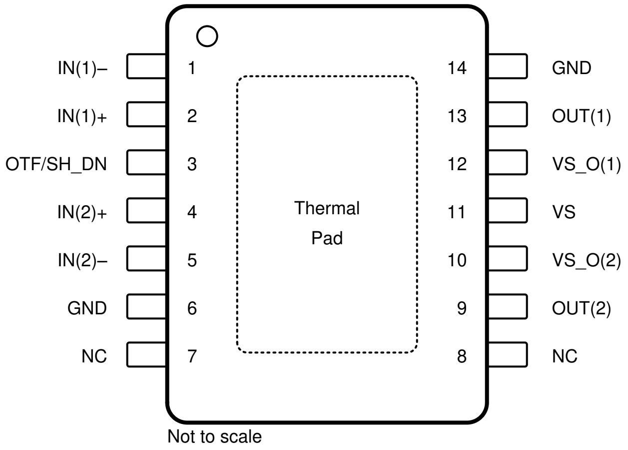


Figure 5-1. PWP (14-Pin HTSSOP) Package, Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	6, 14	Input	Ground pin (both ground pins must be used and connected together on board)
IN(1)+	2	Input	Noninverting op amp input terminal 1
IN(2)+	4	Input	Noninverting op amp input terminal 2
IN(1)–	1	Input	Inverting op amp input terminal 1
IN(2)–	5	Input	Inverting op amp input terminal 2
NC	7, 8	—	No internal connection (do no connect)
OTF/SH_DN	3	Input/output	Overtemperature flag and shutdown (see Table 7-1 for truth table)
OUT(1)	13	Output	Op amp output 1
OUT(2)	9	Output	Op amp output 2
VS	11	Input	Gain stage supply pin
VS_O(1)	12	Input	Output stage supply pin
VS_O(2)	10	Input	Output stage supply pin
Thermal pad	—	—	Connect the exposed thermal pad to ground for best thermal performance. Do not connect the thermal pad to any pin other than GND. The thermal pad can also be left floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Input supply voltage, V_S = (V+) – (V–)	–0.3	18	V
Output supply voltage, V_{S_O}	–0.3	18	V
Positive and negative input to GND voltage	–0.3	18	V
Overtemperature flag pin current		20	mA
Overtemperature flag pin voltage	0	7	V
Output short-circuit[2]	Continuous	Continuous	
Operating temperature	–40	125	°C
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground; one amplifier per package. Long-term, short-circuit operation leads to an elevated die temperature and a shorter lifetime, and places the amplifier into open-loop operation. Prolonged open-loop operation (especially at high temperatures and supplies) can lead to a shift in the dc electrical characteristics, such as offset voltage (see the *Open-Loop and Closed-Loop Operation* section).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±2000	V
		Charge Device Model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input supply voltage, V_S = (V+) – V(–)	4.5		16	V
Output supply voltage, V_{S_O}	3		16	V
Continous output current (sourcing) (1)			400	mA
Continous output current (sinking) (1)			400	mA
OTF input high voltage (op amp on or full operational state)	1			V
OTF input low voltage (op amp off or shutdown state)			0.35	V
Postitive and negative input to GND voltage	0		7	V
Overtemperature flag pin voltage	2		5	V
Specified temperature	–40		125	°C

(1) Current Limit must be taken into consideration when choosing maximum output current.

6.4 Thermal Information

THERMAL METRIC(1)		ALM2402FQ1 PWP (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_S = 12 V

at T_A = 25°C, $V_S = V_{S\_O1} = V_{S\_O2}$ = 12 V, R_L = 10 kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, V_{OTF} = 5 V, and $V_O = V_S$ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±1	±7	mV
		T_A = –40°C to +125°C			±15	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		65		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 10 V to 16 V	70	76		dB
		V_S = 10 V to 16 V, T_A = –40°C to +125°C	65			
INPUT BIAS CURRENT						
I_B	Input bias current			±3.5	±15	nA
		T_A = –40°C to +125°C			±140	
I_{OS}	Input offset current			±2	±12	nA
		T_A = –40°C to +125°C			±35	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		35		μV_{PP}
				5.5		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz		115		$nV/\sqrt{Hz}$
i_N	Input current noise	f = 1 kHz		20		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	V_S > 8.2 V	0.2		7	V
CMRR	Common-mode rejection ratio	0.2 V < V_{CM} < 7 V	81	97		dB
		T_A = –40°C to +125°C, 0.2 V < V_{CM} < 7 V	52			
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	0.3 V < V_O < (V_S) – 1.5 V, R_L = 10 kΩ	85	93		dB
		T_A = –40°C to +125°C	60			
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 15 pF		2.1		MHz
SR	Slew rate	5-V step, G = +1 V/V, C_L = 50 pF		3.4		V/µs
t_S	Settling time	To 0.1%, 5-V step , G = +1 V/V		2.4		µs
	Overload recovery time	V_{IN} × (–1) × gain > V_S		10		µs
THD+N	Total harmonic distortion + noise	(V+) = 11 V, (V–) = –5 V, V_O = 6 V_{PP}, G = +2 V/V, f = 1 kHz, R_L = 100 Ω		–73		dB

6.5 Electrical Characteristics: V_S = 12 V (continued)

at T_A = 25°C, $V_S = V_{S\_O1} = V_{S\_O2}$ = 12 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OTF} = 5 V, and V_O = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_o	Voltage output swing from rail	Positive rail, V_{ID} = 100 mV	T_A = 25°C		0.3	0.5	mV
			T_A = –40°C to +125°C, I_{SOURCE} = 200 mA		130	300	
			T_A = –40°C to +125°C, I_{SOURCE} = 100 mA		60	150	
		Negative rail, V_{ID} = 100 mV	T_A = 25°C		0.4	0.6	mV
			TA = –40°C to +125°C, I_{SINK} = 200 mA		200	550	
			T_A = –40°C to +125°C, I_{SINK} = 100 mA		100	200	
I_{SC}	Short-circuit current	Sinking (short to supply)			540		mA
		Sourcing (short to ground)			750		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = 25°C			4	5	mA
		I_O = 0 A, T_A = –40°C to +125°C				6	
		V_{OTF/SH_DN} = 0 V			0.5		
TEMPERATURE							
	Thermal shutdown				165		°C
	Thermal shutdown recovery				159		°C
V_{OL_OTF}	Overtemperature fault low voltage	R_{PULLUP} = 2.5 kΩ, V_{PULLUP} = 5.0 V				400	mV
V_{IH_OTF}	Amplifier enable voltage			1			V
V_{IL_OTF}	Amplifier disable voltage					0.35	V

6.6 Electrical Characteristics: V_S = 5 V

at T_A = 25°C, $V_S = V_{S\_O1} = V_{S\_O2}$ = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OTF} = 5 V, and V_O = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		±1	±7	mV
		T_A = –40°C to +125°C			±15	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		65		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 4.5 V to 10 V	82	94		dB
		V_S = 4.5 V to 10 V, T_A = –40°C to +125°C	75			
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		0.5	±2	nA
		T_A = –40°C to +125°C			±30	
I_{OS}	Input offset current	T_A = 25°C		±2	±2	nA
		T_A = –40°C to +125°C			±9	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		35		μV_{PP}
				5.5		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz		115		nV/√Hz
i_N	Input current noise	f = 1 kHz		20		fA/√Hz

6.6 Electrical Characteristics: V_S = 5 V (continued)

at T_A = 25°C, $V_S = V_{S\_O1} = V_{S\_O2}$ = 5 V, R_L = 10 kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, V_{OTF} = 5 V, and $V_O = V_S$ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			0.2		(V+) – 1.2	V
CMRR	Common-mode rejection ratio	0.2 V < V_{CM} < (V+) – 1.2 V		80	95		dB
		T_A = –40°C to +125°C, 0.2 V < V_{CM} < (V+) – 1.2 V		52			
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.3 V < V_O < (V_S) – 1.5 V, R_L = 10 kΩ	T_A = 25°C	85	93		dB
			T_A = –40°C to +125°C	60			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 15 pF			1.3		MHz
SR	Slew rate	2-V step, G = +1 V/V, C_L = 50 pF			1.7		V/µs
t_S	Settling time	To 0.1%, 2-V step , G = +1 V/V			2		µs
	Overload recovery time	V_{IN} × (–1) × gain > V_S			5		µs
THD+N	Total harmonic distortion + noise	V_S = 5 V, V_O = 2.82 V_{PP}, G = +2 V/V, f = 1 kHz, R_L = 100 Ω			–73		dB
OUTPUT							
V_o	Voltage output swing from rail	Positive rail, V_{ID} = 100 mV	T_A = 25°C		0.3	0.5	mV
			T_A = –40°C to +125°C, I_{SINK} = 200 mA		130	300	
			T_A = –40°C to +125°C, I_{SINK} = 100 mA		60	150	
		Negative rail, V_{ID} = 100 mV	T_A = 25°C		0.4	0.6	mV
			TA = –40°C to +125°C, I_{SINK} = 200 mA		200	575	
			T_A = –40°C to +125°C, I_{SINK} = 100 mA		100	200	
I_{SC}	Short-circuit current	Sinking (short to supply)			500		mA
		Sourcing (short to ground)			550		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = 25°C			4	4.5	mA
		I_O = 0 A, T_A = –40°C to +125°C				5	
		V_{OTF/SH_DN} = 0 V			0.5		
TEMPERATURE							
	Thermal shutdown				165		°C
	Thermal shutdown recovery				159		°C
V_{OL_OTF}	Overtemperature fault low voltage	R_{PULLUP} = 2.5 kΩ, V_{PULLUP} = 5.0 V				400	mV
V_{IH_OTF}	Amplifier enable voltage			1			V
V_{IL_OTF}	Amplifier disable voltage					0.35	V

6.7 Typical Characteristics

at T_A= 25°C, V_S = 12 V, V_{CM}= V_{S_O1}= V_{S_O2}= V_S/2, and R_L= 10 kΩ (unless otherwise noted)

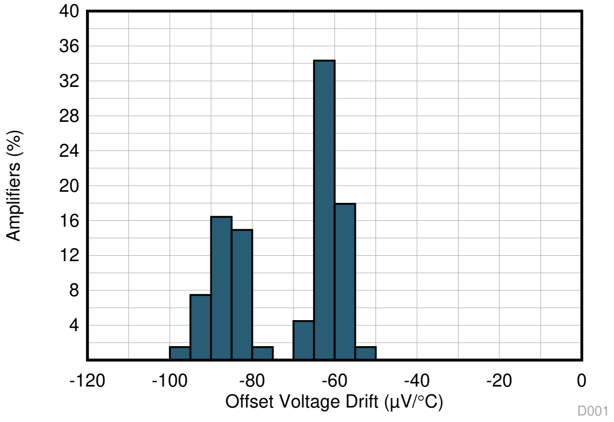
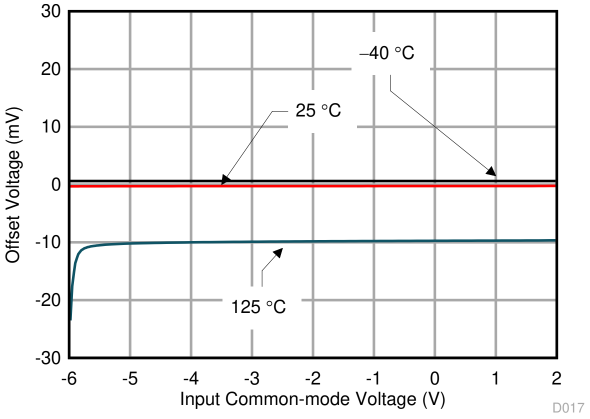
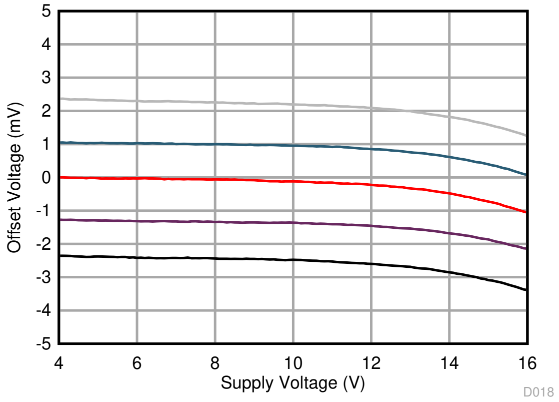


Figure 6-1. Offset Voltage Drift Production Distribution



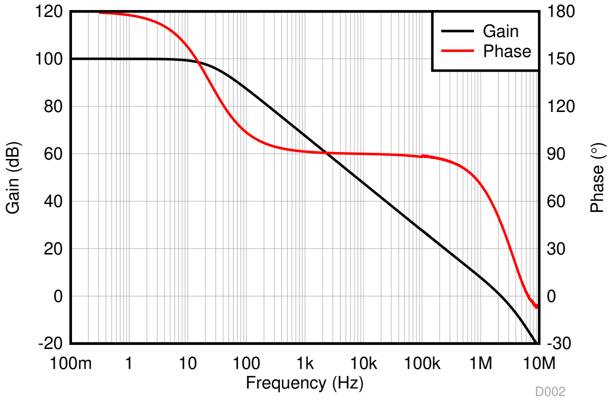
5 typical units

Figure 6-2. Offset Voltage vs Input Common-Mode Voltage



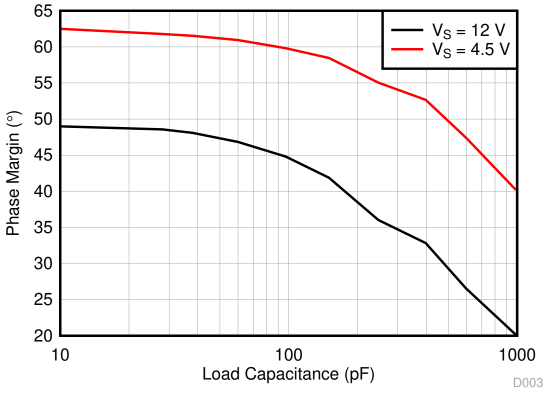
5 typical units

Figure 6-3. Offset Voltage vs Power Supply



C_{LOAD} = 200 nF R_L = 50 Ω

Figure 6-4. Open-Loop Gain and Phase vs Frequency



Gain = 1 V/V

Figure 6-5. Phase Margin vs Capacitive Load

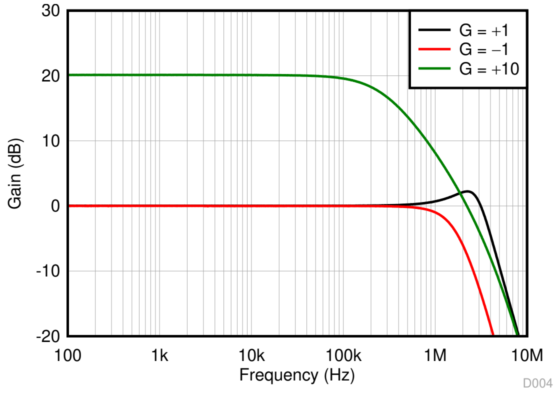


Figure 6-6. Closed-Loop Gain vs Frequency

6.7 Typical Characteristics (continued)

at T_A= 25°C, V_S = 12 V, V_{CM}= V_{S_O1}= V_{S_O2}= $V_S/2$, and R_L= 10 kΩ (unless otherwise noted)

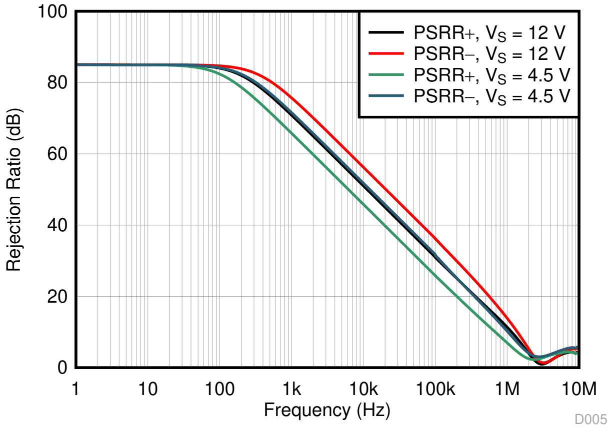


Figure 6-7. PSRR vs Frequency

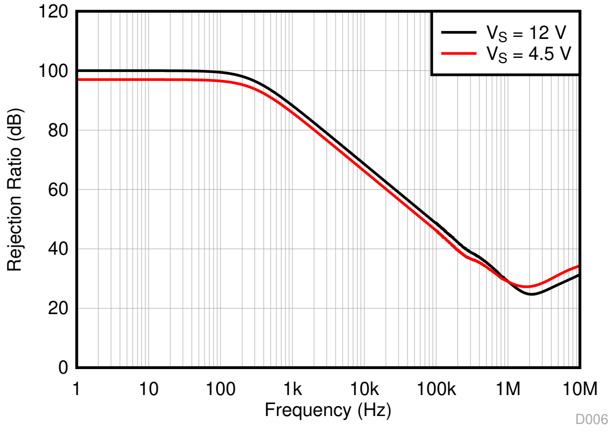
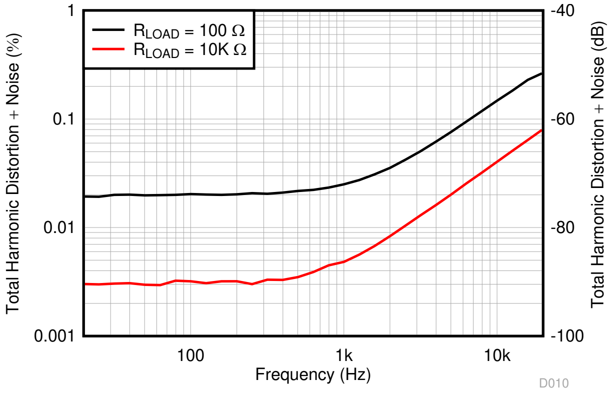
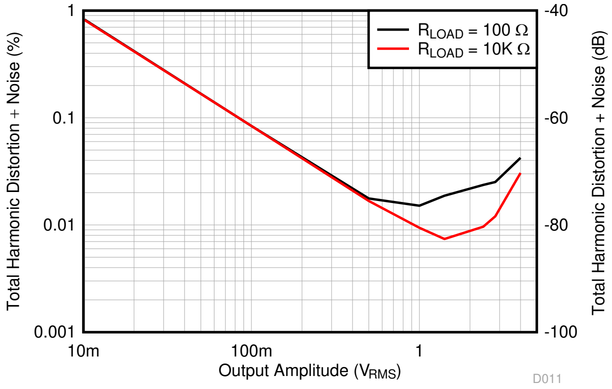


Figure 6-8. CMRR vs Frequency



V_O = 8 V_{PP} Gain = 2 V/V Measurement bandwidth = 80 kHz

Figure 6-9. THD+N Ratio vs Frequency



Input signal frequency =1 kHz Measurement bandwidth = 80 kHz

Figure 6-10. THD+N vs Output Amplitude

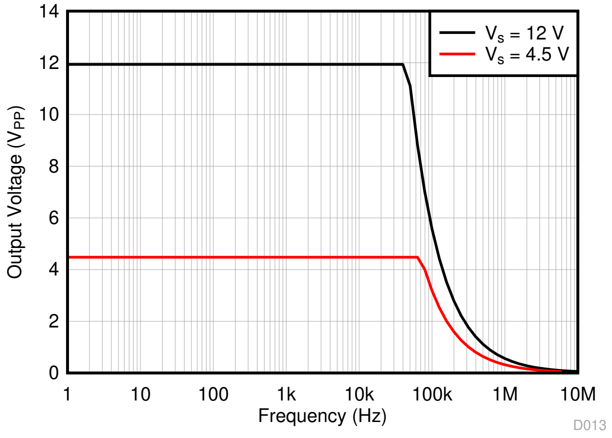


Figure 6-11. Maximum Output Voltage vs Frequency

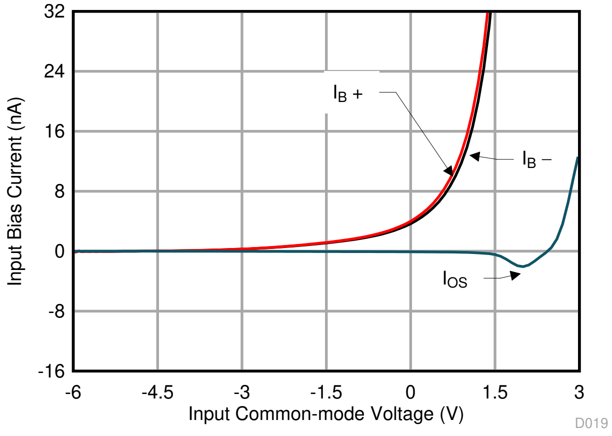


Figure 6-12. Input Bias Current vs Common-Mode Voltage

6.7 Typical Characteristics (continued)

at T_A= 25°C, V_S = 12 V, V_{CM}= V_{S_O1}= V_{S_O2}= $V_S/2$, and R_L= 10 kΩ (unless otherwise noted)

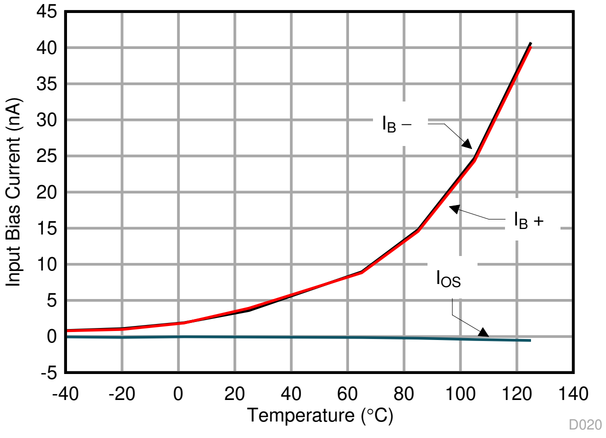


Figure 6-13. Input Bias Current vs Temperature

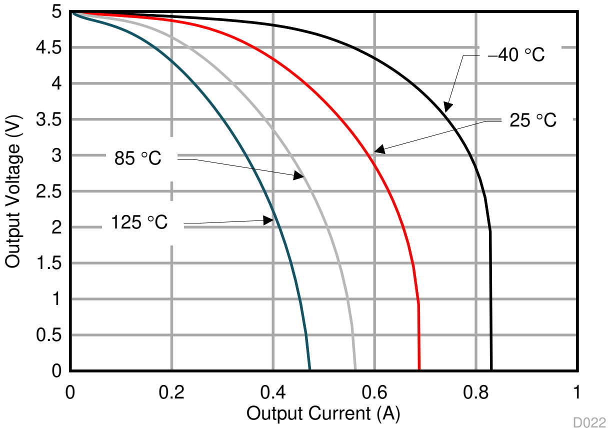


Figure 6-14. Output Voltage Swing vs Output Source Current

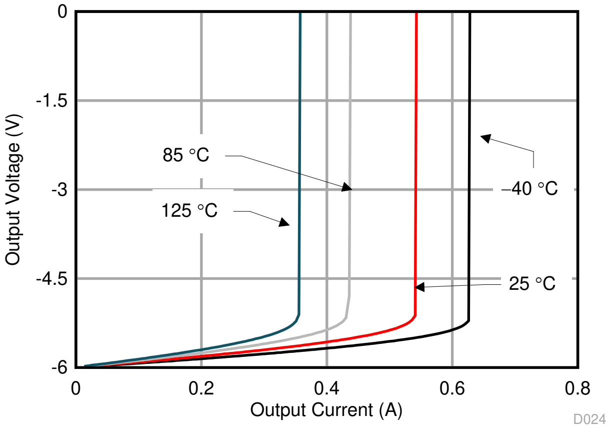


Figure 6-15. Output Voltage Swing vs Output Sink Current

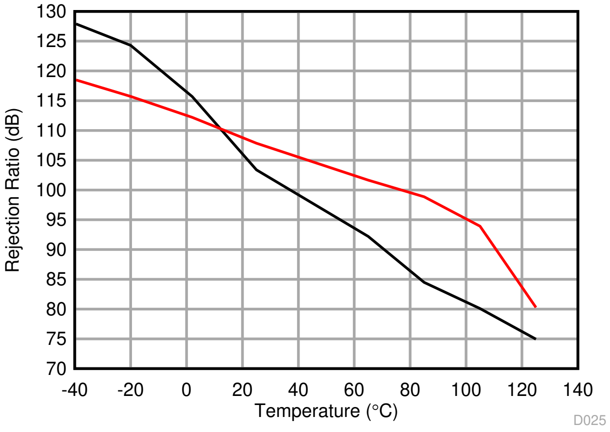


Figure 6-16. CMRR vs Temperature

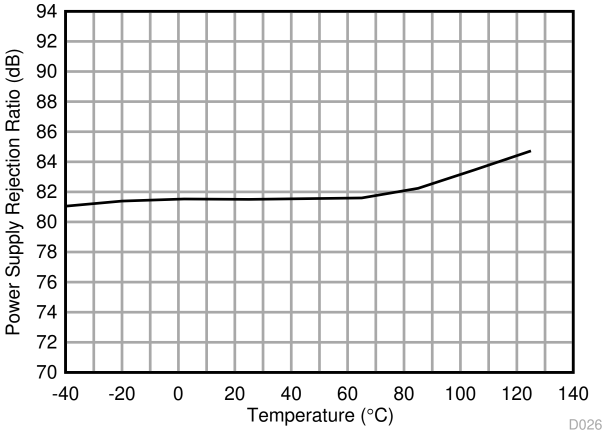


Figure 6-17. PSRR vs Temperature

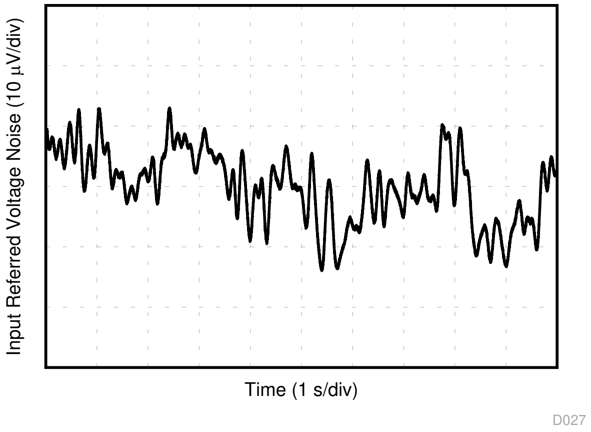


Figure 6-18. 0.1-Hz to 10-Hz Noise

6.7 Typical Characteristics (continued)

at T_A= 25°C, V_S = 12 V, V_{CM}= V_{S_O1}= V_{S_O2}= V_S/2, and R_L= 10 kΩ (unless otherwise noted)

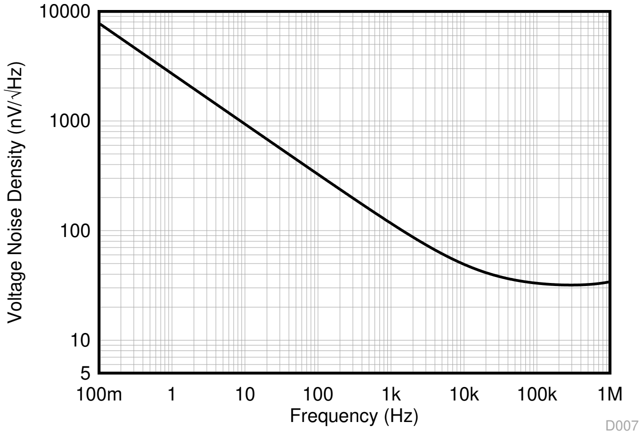
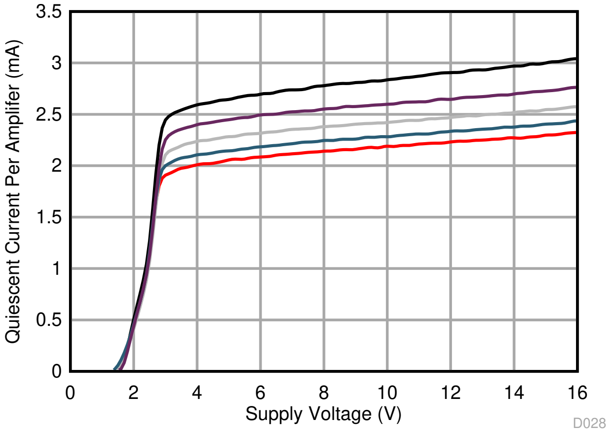
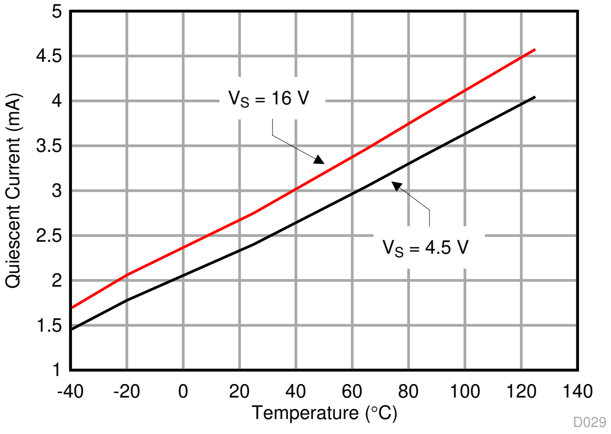


Figure 6-19. Input Voltage Spectral Noise Density vs Frequency



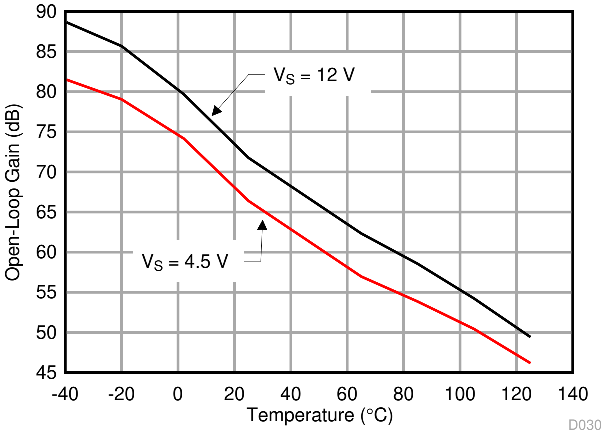
5 typical units V_O = 8 V_{PP}

Figure 6-20. Quiescent Current vs Power Supply



5 typical units

Figure 6-21. Quiescent Current vs Temperature



R_L = 100 Ω

Figure 6-22. Open-Loop Gain vs Temperature

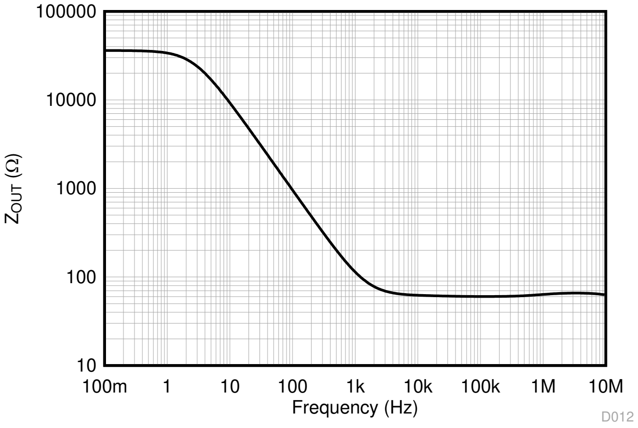
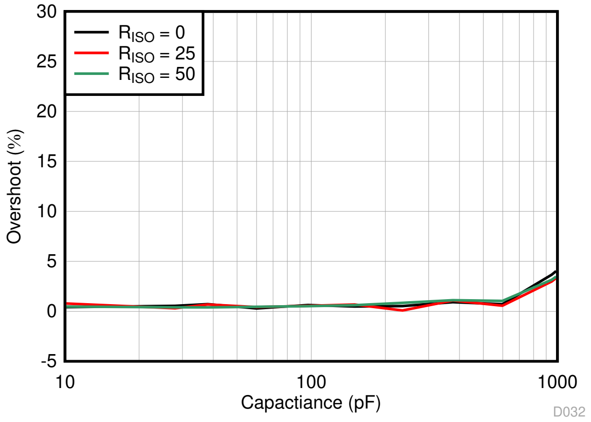


Figure 6-23. Open-Loop Output Impedance vs Frequency

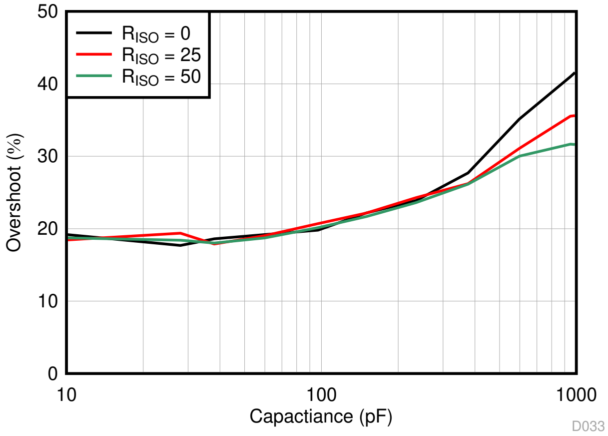


10-mV output step Gain = –1 V/V

Figure 6-24. Small-Signal Overshoot vs Capacitive Load

6.7 Typical Characteristics (continued)

at T_A= 25°C, V_S = 12 V, V_{CM}= V_{S_O1}= V_{S_O2}= V_S/2, and R_L= 10 kΩ (unless otherwise noted)



10-mV output step Gain = 1 V/V

Figure 6-25. Small-Signal Overshoot vs Capacitive Load

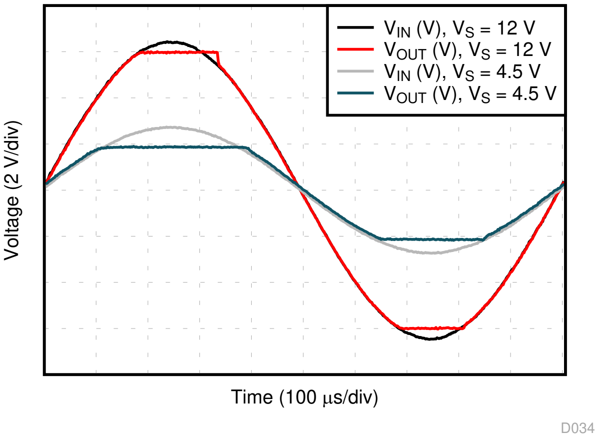
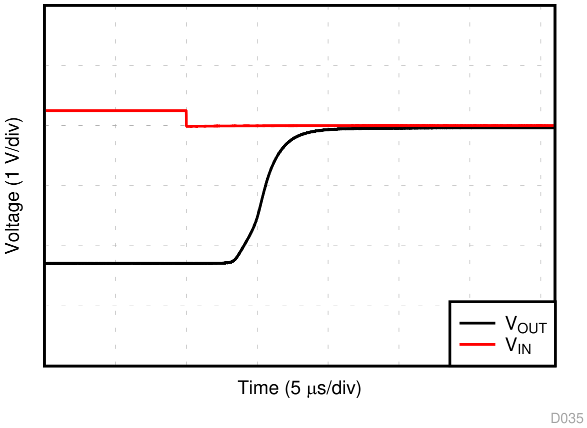
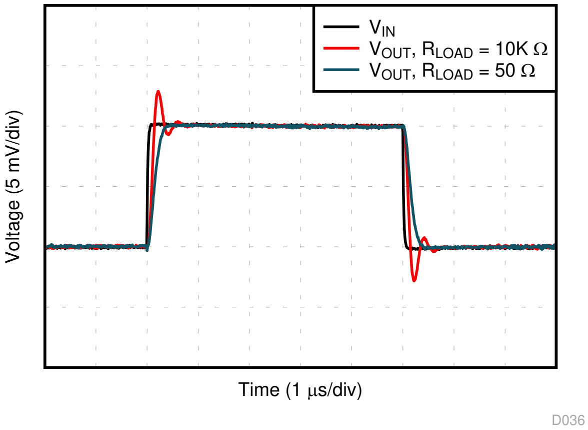


Figure 6-26. No Phase Reversal



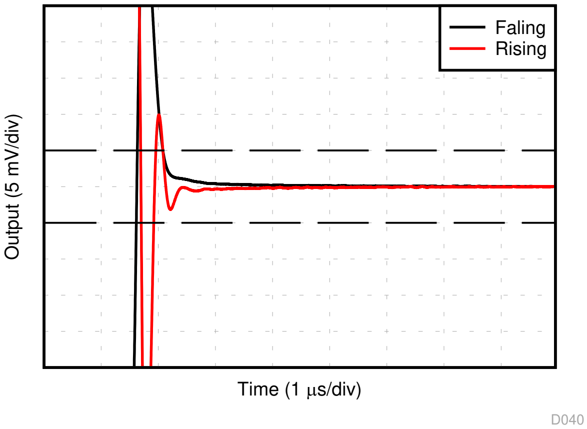
V_S = 4.5 V

Figure 6-27. Negative Overload Recovery



V_{IN} = 10 mV_{PP}

Figure 6-28. Small-Signal Step Response



V_{IN} = 5 V

Figure 6-29. Settling Time

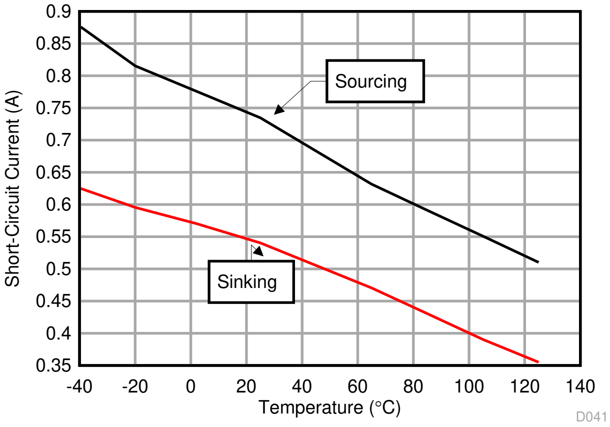
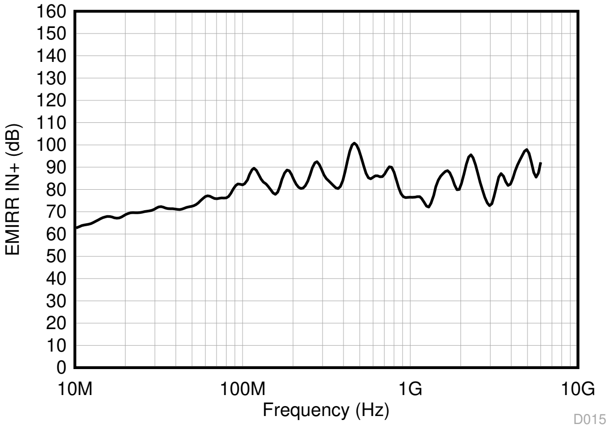


Figure 6-30. Short-Circuit Current vs Temperature

6.7 Typical Characteristics (continued)

at T_A= 25°C, V_S = 12 V, V_{CM}= V_{S_O1}= V_{S_O2}= V_S/2, and R_L= 10 kΩ (unless otherwise noted)



PRF = –10 dBm

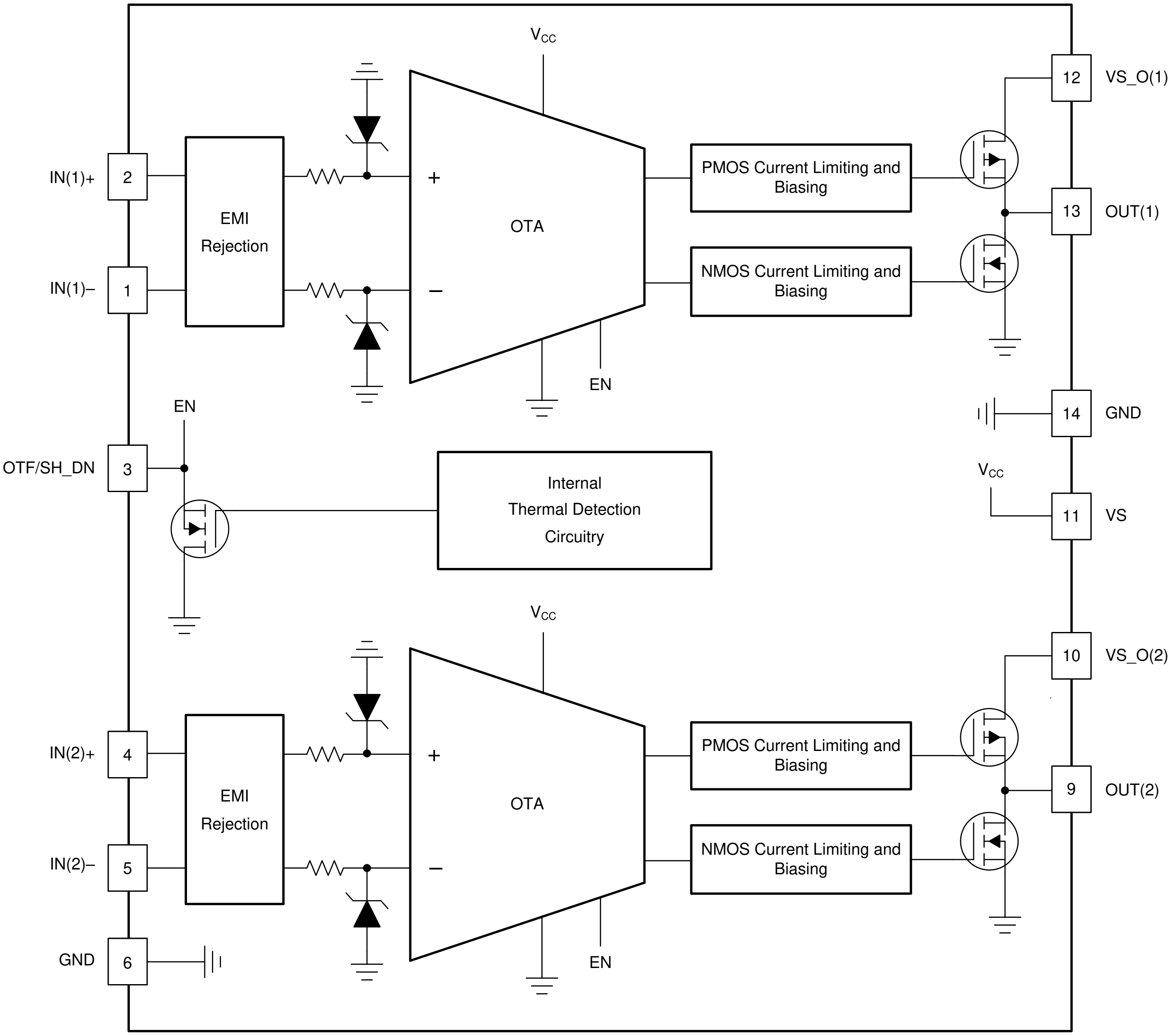
Figure 6-31. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The ALM2402F-Q1 is a dual-power op amp qualified for use in automotive applications. Key features for this device are low offset voltage, high output current drive capability, and high FPBW capability. The device also offers protection features such as thermal shutdown and current limit. The 14-pin HTSSOP package minimizes board space and power dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 OTF/SH_DN

The overtemperature and shutdown (OTF/SH_DN) pin is a bidirectional pin that allows both op amps to be put into a low I_Q state (~500 µA) when forced low or less than V_{IL_OTF}. As a result of this pin being bidirectional, and the respective enable and disable functionality, this pin must be pulled high or greater than V_{IH_OTF} through a pullup resistor; see the *Electrical Characteristics* table.

When the junction temperature of ALM2402F-Q1 exceeds the limits specified in the *Recommended Operating Conditions* table, the OTF/SH_DN pin goes low to alert the application that both the outputs have turned off because of an overtemperature event. Also, the OTF pin goes low if VS_O1 and VS_O2 are 0 V. In case of an overtemperature event, the op amps are shut down even if OTF/SH_DN is forced high.

When OTF/SH_DN is pulled low and the op amps are shut down, the op amps are in an open loop, even when there is negative feedback applied. This occurrence is due to the loss of the open-loop gain in the op amps when the biasing is disabled. See *Section 7.4.1* for more details on open- and closed-loop considerations.

7.3.2 Output Stage Supply Voltage

The ALM2402F-Q1 uses three power rails. VS powers the op-amp signal path (OTA) and protection circuitry. VS_O1 and VS_O2 power the output high side driver. Each supply can operate at separate voltage levels (higher or lower). The minimum and maximum values listed in the *Recommended Operating Conditions* table are voltages that enable the ALM2402F-Q1 to properly function at or near the specification listed in *Electrical Characteristics* table.

7.3.3 Current-Limit and Short-Circuit Protection

Each op amp in the ALM2402F-Q1 has separate internal current limiting for the PMOS (high-side) and NMOS (low-side) output transistors. If the output is shorted to ground then the PMOS (high-side) current limit is activated, and limits the current to 750 mA nominally. If the output is shorted to supply then the NMOS (low-side) current limit is activated and limits the current to 550 mA nominally at 25°C. The current limit value decreases with increasing temperature as a result of the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures.

In the case of short-to-ground scenarios, a programmable current limit for the PMOS (high-side) is achieved by adding resistance between VS_O(*x*), where x = 1 or 2, and the supply VS. The added current limit resistor reduces the drain-source voltage across the PMOS output transistor, thus reducing the output current drive capability. For a desired current limit (I_{LIMIT}), an appropriate current limiting resistor (R_{limit}) is selected using Equation 1.

$$R_{LIMIT} = (VS - 1.5) / I_{LIMIT} \quad (1)$$

When current is limited, the safe limits for the die temperature must be taken in to account; see the *Recommended Operating Conditions* and *Absolute Maximum Ratings* tables. With too much power dissipation, the die temperature can surpass thermal shutdown limits; the op amp shuts down and reactivates after the die has fallen below thermal limits. However, do not continuously operate the device in thermal hysteresis for long periods of time (see the *Absolute Maximum Ratings* table).

7.3.4 Input Common-Mode Overvoltage Clamps

The input common mode range of the ALM2402F-Q1 is between (V–) + 0.2 V and (V+) – 1.2 V (see the *Electrical Characteristics* table). Staying within this range allows the op amps to perform and operate within the specification listed in the *Electrical Characteristics*. Operating beyond these limits can cause distortion and nonlinearities.

In order for the inputs to tolerate high voltages in the event of a short to supply, Zener diodes have been added (see Figure 7-1). The current into this Zener diode is limited through internal resistors (10 kΩ each). When operating near or above the Zener voltage (7 V), the additional voltage error caused by the mismatch in internal resistors must be taken in to account. In unity gain configurations, the op amp forces both gate voltages to be equal to the Zener voltage on the positive input pin, and ideally both Zeners sink the same amount of current and force the output voltage to be equal to V_{IN}. However, in reality, R_N and R_P and V_Z between both Zener diodes do not perfectly match, and have some percentage difference between their values. This occurrence leads to the output being $V_O = V_{IN} \times (\Delta R + \Delta V_Z)$.

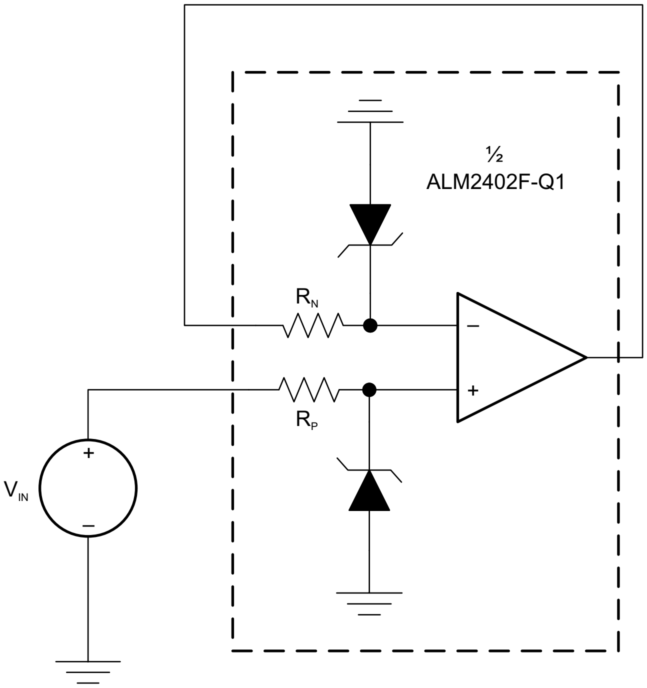


Figure 7-1. Schematic Including Input Clamps

7.3.5 Thermal Shutdown

If the die temperature exceeds safe limits, all outputs are disabled, and the OTF/SH_DN pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The OTF/SH_DN pin is released after operation has resumed.

When operating the die at a high temperature, the op amp toggles on and off between the thermal shutdown hysteresis. In this event, the safe limits for the die temperature must be taken in to account; see the *Recommended Operating Conditions* and *Thermal Conditions* tables. Do not continuously operate the device in thermal hysteresis for long periods of time; see the *Recommended Operating Conditions* table.

7.3.6 Output Stage

Designed as a high-voltage, high current operational amplifier, the ALM2402F-Q1 device delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails.

Each output transistor has internal reverse diodes between drain and source that conduct if the output is forced greater than the supply or less than ground (reverse current flow). These diodes can be used as flyback protection in inductive-load driving applications. Limit the use of these diodes to pulsed operation to minimize junction temperature overheating due to ($V_F \times I_F$). Internal current limiting circuitry does not operate when current is flown in the reverse direction and the reverse diodes are active.

7.3.7 EMI Susceptibility and Input Filtering

Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op-amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The ALM2402F-Q1 incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 990 MHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

7.4 Device Functional Modes

7.4.1 Open-Loop and Closed-Loop Operation

As a result of the very high open-loop dc gain of the ALM2402F-Q1, the device functions as a comparator in open-loop for most applications. As noted in the *Electrical Characteristics* table, the majority of electrical characteristics are verified in negative feedback, closed-loop configurations. Certain dc electrical characteristics, like offset, may have a higher drift across temperature and lifetime when continuously operated in open loop over the lifetime of the device.

7.4.2 Shutdown

When the OTF/SH_DN pin is left floating or is grounded, the op amp shuts down to a low I_Q state and does not operate; the op amp outputs go to a high-impedance state. See the *OTF/SH_DN* section for more detailed information on the OTF/SH_DN pin.

Table 7-1. Shutdown Truth Table

NAME	LOGIC STATE	OP AMP STATE
OTF/SH_DN	High (> VIH_OTF see *Recommended Operating Conditions*)	Operating
	Low (< VIL_OTF see *Recommended Operating Conditions*)	Shutdown (low I_Q state)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ALM2402F-Q1 is a dual-power op amp with performance and protection features that are optimal for many applications. For op amps, there are many general design consideration that must taken into account. The following sections describe what to consider for most closed-loop applications, and gives a specific example of the ALM2402F-Q1 being used in a motor-drive application.

8.1.1 Capacitive Load and Stability

The ALM2402F-Q1 is designed to be used in applications where driving a capacitive load is required. As with all op amps, specific instances can occur where the ALM2402F-Q1 device can become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher-noise gain. The capacitive load, in conjunction with the op-amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the ALM2402F-Q1 remains stable with a pure capacitive load up to approximately 1 nF. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 100 mΩ to 10 Ω, in series with the output (R_S), as shown in Figure 8-1. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads.

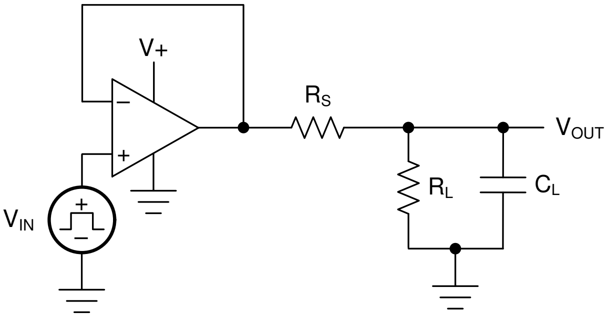


Figure 8-1. Capacitive Load Drive

8.2 Typical Application

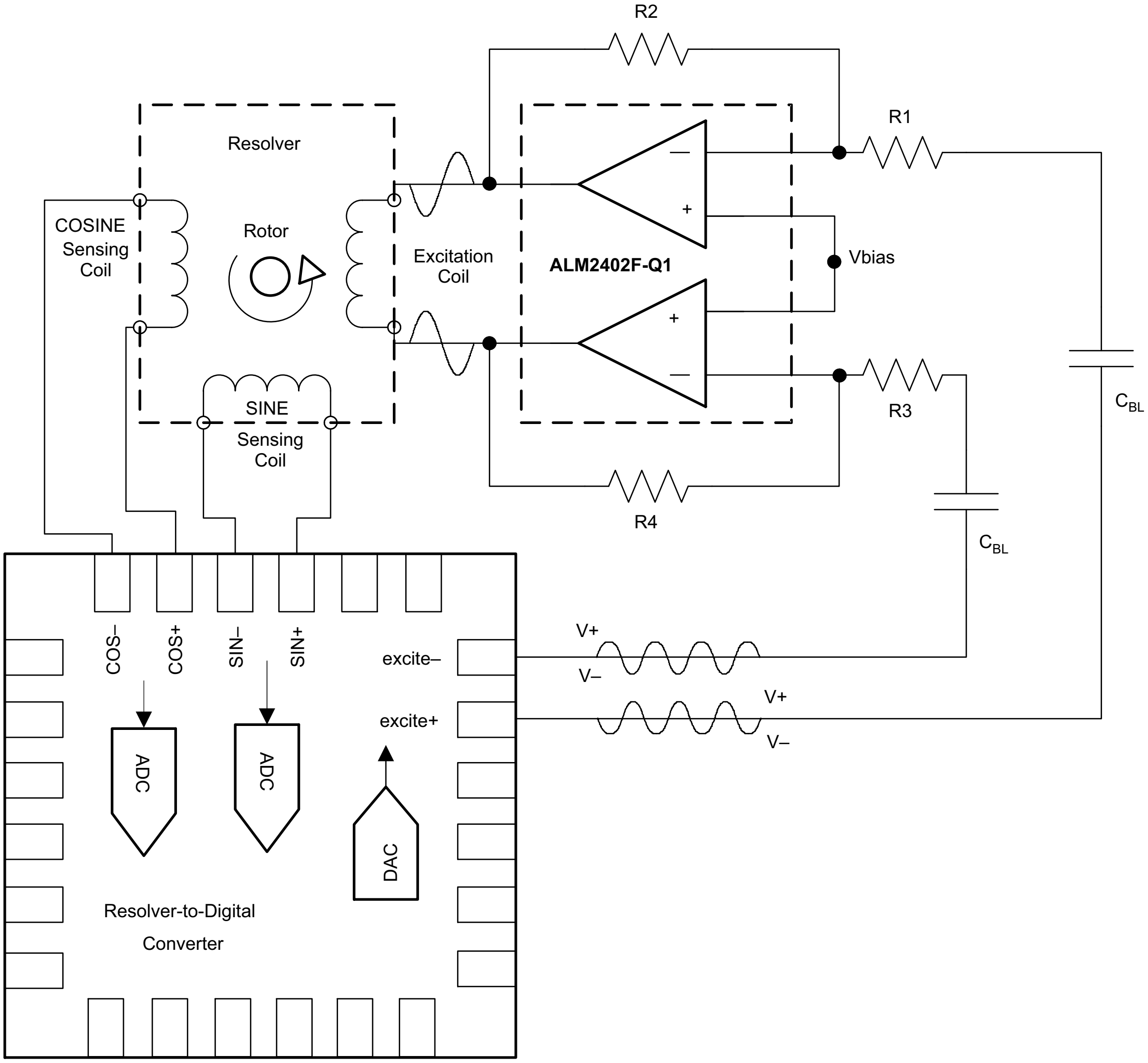


Figure 8-2. Resolver-Based Application

High-power ac and brushless DC (BLDC) motor-drive applications need angular and position feedback in order to efficiently and accurately drive the motor. Position feedback can be achieved by using optical encoders, hall sensors, or resolvers. Resolvers are the goto choice when environmental or longevity requirements are challenging and extensive.

A resolver acts like a transformer with one primary coil and two secondary coils. The primary coil, or excitation coil, is located on the rotor of the resolver. As the rotor of the resolver spins, the excitation coil induces a current into the sine and cosine sensing coils. These coils are oriented 90 degrees from one another, and produce a vector position read by the resolver to digital converter chip.

Resolver excitation coils can have a very low dc resistance (< 100 Ω), requiring a sink and a source of up to 200 mA from the excitation driver. The ALM2402F-Q1 can source and sink this current while providing current limiting and thermal shutdown protection. Incorporating these protections in a resolver design can increase the life of the end product.

The fundamental design steps and ALM2402F-Q1 benefits shown in this application example can be applied to other inductive load applications, such as dc and servo motors.

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Ambient temperature range	–40°C to +125°C
Available supply voltages	12 V
EMC capacitance (CL)	50 nF
Excitation input voltage range	2 V_{RMS} to 7 V_{RMS}
Excitation frequency	10 kHz

8.2.2 Detailed Design Procedure

When using the ALM2402F-Q1 in a resolver application, determine:

- Resolver excitation input impedance or resistance and inductance: Z_O= 100 + j188; (R = 100 Ω and L = 3 mH)
- Resolver transformation ration (V_{EXC} / V_{SINCOS}): 0.5 V/V at 10 kHz
- Package and $R_{\theta JA}$: HTSSOP, 46.5°C/W
- Op amp maximum junction temperature: 150°C
- Op amp bandwidth: 1.3 MHz
- Op amp Slew Rate: 1.2 V/µs

8.2.2.1 Resolver Excitation Input (Op Amp Output)

Like a transformer, a resolver needs an alternating current input to function properly. The resolver receives alternating current from the primary coil (excitation input) and creates a multiple of this input current on the secondary sides (SIN, COS ports). When determining how to generate this alternating current, make sure to understand the op amp abilities and limitations. For the excitation input, the resolver input impedance, stability RMS voltage, and desired frequency must be taken in to account.

8.2.2.1.1 Excitation Voltage

The resolver primary winding or excitation coil can be driven by a single-ended op amp output with the other side of the coil grounded, or differentially as shown in Figure 8-2. A differential drive offers higher voltage (double) on to the excitation coil, while not using as much output voltage headroom from the op amp. This larger output voltage due to the differential drive leads to lower distortion on the output signal.

For this example, the resolver impedance is specified from 2 V_{RMS} and 7 V_{RMS} up to 20-kHz maximum frequency. To highlight use with a 7 V_{RMS} resolver, an excitation voltage of 10 V_{PP} is applied from each channel of the ALM2402F-Q1. The op amp is set in an inverting gain = –2 V/V, while applying an adequate common-mode bias. These conditions give the required 7 V_{RMS} differential output (3.5 V_{RMS} per each op amp channel) to the resolver primary winding without running into any op-amp headroom issues.

Another consideration for excitation is op-amp power dissipation. As described in the *Power Dissipation and Thermal Reliability* section, power dissipation from the op amp can be lowered by driving the output peak voltages close to the supply and ground voltages. With the very low V_{OH}/V_{OL} of the ALM2402F-Q1, lower power dissipation is easily accomplished. See the *Output Stage* section for a further description of the rail-rail output stage.

8.2.2.1.2 Excitation Frequency

The excitation frequency is chosen based on the desired secondary-side output signal resolution. The excitation signal is similar to a sampling pulse in ADCs, with the real information being in the envelope created by the rotor. With a GBW of 1.3 MHz, the ALM2402F-Q1 has more than enough open-loop gain at 10 kHz to create negligible closed-loop gain error.

Along with GBW, the ALM2402F-Q1 has optimal THD and SR performance to achieve 10-V_{PP} output per channel.

8.2.2.1.3 Excitation Impedance

Knowledge of the primary-side impedance is very important when choosing an op amp for this application. As shown in Figure 8-3, the excitation coil looks like an inductance in series with a resistance. Often, these values are not given, or are given as a function of frequency or phase angle, and must by calculated from the Cartesian or polar form. This calculation is a trivial task.

After the coil resistance is determined, the maximum or peak-peak current needed from ALM2402F-Q1 is determined using Equation 2:

$$I_{OUT} = \frac{V_{PP}}{R_L} \tag{2}$$

In this example, the peak-to-peak output current equates to approximately 100 mA. Each op amp handles the peak current, with one op amp sinking current while the other op amp is sourcing current. Knowledge of the op amp current is very important when determining the device power dissipation, a topic that is discussed in *Power Dissipation and Thermal Reliability*.

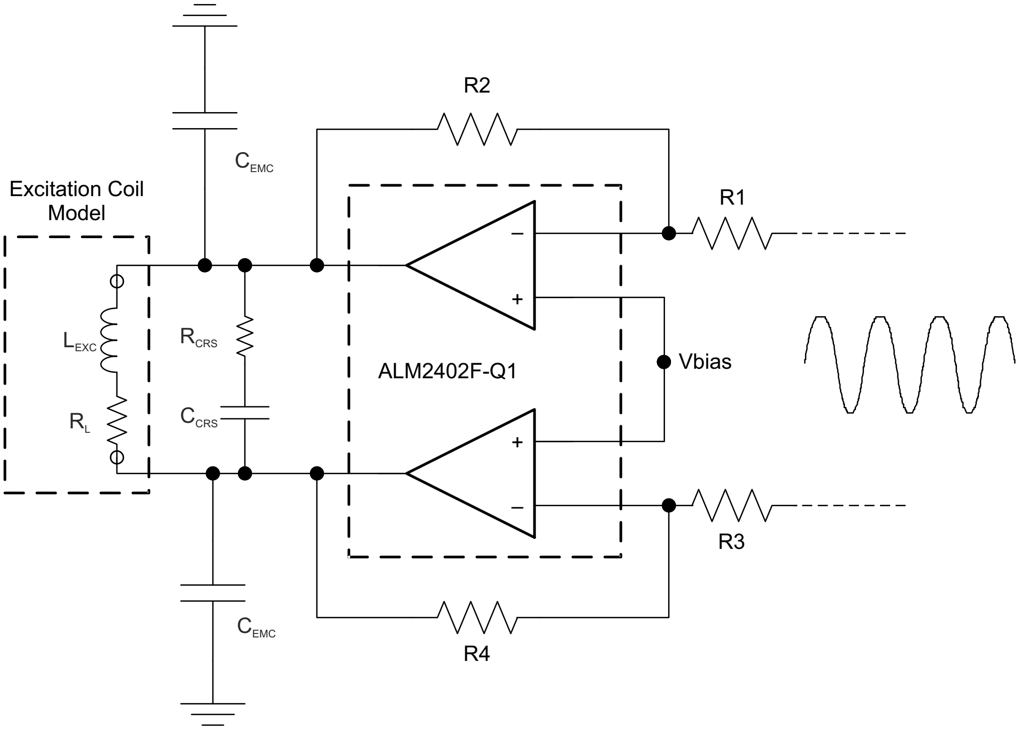


Figure 8-3. Excitation Coil Implementation

As shown in Figure 8-3, designers often add a resistor (R_{CRS}) in series with a capacitor (C_{CRS}) to eliminate crossover distortion. This distortion occurs as a result of the biasing of BJTs in a discrete implementation. With the ALM2402F-Q1 rail-rail output and high-output current drive capability, this configuration is rarely needed.

Common practice is to also add EMC capacitors to the op-amp outputs to help shield other devices on the PCB from the radiation created by the motor and resolver. When choosing C_{EMC}, make sure to take the stability of the op amp into account.

8.2.2.2 Resolver Output

As mentioned in *Section 8.2.2.1.2*, the excitation signal is similar to a sampling pulse in ADCs, with the real information being in the envelope created by the rotor. Equation 3, Equation 4, and Equation 5 show the behavior of the sin and cos outputs. The excitation signal is attenuated and enveloped by the voltage created from the electromagnetic response of the rotating rotor. The resolver analog-output-to-digital converter filters out the excitation signal, and processes the sine and cosine angles produced by the rotor. Hence, signal integrity or the sine and cosine envelope is most important in resolver design; although, some trade-offs in signal integrity of the excitation signal can be made for cost or convenience. Often, a square wave or sawtooth signal is used to accomplish excitation, as opposed to a sine wave.

$$V_{EXC} = V_{PP} \times \sin(2\pi ft) \tag{3}$$

$$V_{SIN} = T_R \times V_{PP} \times \sin(2\pi ft) \times \sin(\theta) \tag{4}$$

$$V_{COS} = T_R \times V_{PP} \times \sin(2\pi ft) \times \cos(\theta) \tag{5}$$

8.2.2.3 Power Dissipation and Thermal Reliability

Power dissipation is critical to many industrial and automotive applications. Resolvers are typically chosen over other position feedback techniques because of reliability and accuracy in harsh conditions and high temperatures.

The ALM2402F-Q1 is capable of high output current with power-supply voltages up to 16 V. Internal power dissipation increases when operating at high supply voltages. The power dissipated in the op amp (P_{OPA}) is calculated using Equation 6:

$$P_{OPA} = (V^+ - VO(X)) \times I_{OUT} = (V^+ - VO(X)) \times \frac{VO(X)}{R_L} \tag{6}$$

To calculate the worst-case power dissipation in the op amp, the ac and dc cases must be considered separately.

In the case of constant output current (dc) to a resistive load, the maximum power dissipation in the op amp occurs when the output voltage is half the positive supply voltage. This calculation assumes that the op amp is sourcing current from the positive supply to a grounded load. If the op amp sinks current from a grounded load, modify Equation 7 to include the negative supply voltage instead of the positive.

$$P_{OPA(MAX\_DC)} = P_{OPA}\left(\frac{VO(X)}{2}\right) = \frac{(VO(X))^2}{4R_L} \tag{7}$$

The maximum power dissipation in the op amp for a sinusoidal output current (ac) to a resistive load occurs when the peak output voltage is 2/π times the supply voltage, given symmetrical supply voltages, as shown in Equation 8:

$$P_{OPA(MAX\_AC)} = P_{OPA}\left(\frac{2VO(X)}{\pi}\right) = \frac{2 \cdot (VO(X))^2}{\pi^2 \cdot R_L} \tag{8}$$

After the total power dissipation is determined, the junction temperature at the worst expected ambient temperature case must be determined by using Equation 9:

$$T_{J(MAX)} = P_{OPA} \times R_{\theta JA} + T_{A(MAX)} \tag{9}$$

8.2.2.3.1 Improving Package Thermal Performance

The value of $R_{\theta JA}$ depends on the PCB layout. An external heat sink, a cooling mechanism such as a cold air fan, or both, can help reduce $R_{\theta JA}$ and thus improve device thermal capabilities. See TI's design support web page at www.ti.com/thermal for general guidance on improving device thermal performance.

8.2.3 Application Curves

The THD+N performance for the circuit described in the *Excitation Voltage* section is measured for a 10-kHz, 10-V_{PP} output signal from each op-amp channel. These measurement results are displayed in Table 8-2.

Table 8-2. Maximum Output Power and THD+N

LOAD IMPEDANCE (Ω)	MAXIMUM OUTPUT POWER (mW)	THD+N AT MAXIMUM OUTPUT POWER (dB)
100	292	–50

Figure 8-4 shows the THD+N performance for different input signal frequencies with a measurement bandwidth of 80 kHz. Figure 8-5 shows the circuit response with load capacitances of up to 100 nF. Using a larger resistor in series with the output, as shown in Section 8.1.1 further improves phase margin.

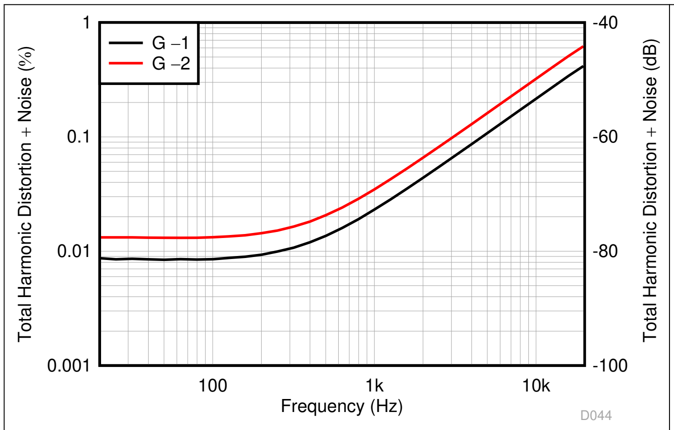


Figure 8-4. THD+N vs Frequency

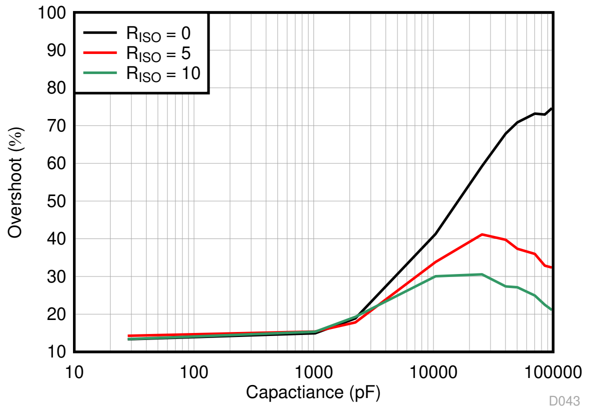


Figure 8-5. Small-Signal Overshoot vs Capacitive Load

9 Power Supply Recommendations

The ALM2402F-Q1 is specified for continuous operation from 4.5 V to 16 V (±2.25 V to ±8 V) for V_S, and 3 V to 16V (±1.5 V to ±8 V) for $V_{S\_O(X)}$; many specifications apply from –40°C to +125°C.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

CAUTION

Supply voltages larger than 18 V can permanently damage the device (see the *Absolute Maximum Ratings*).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If keeping the traces separate is not possible, then cross the sensitive trace perpendicular, as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

10.2 Layout Example

This layout does not verify optimum thermal impedance performance. See TI's design support web page at www.ti.com/thermal for general guidance on improving device thermal performance.

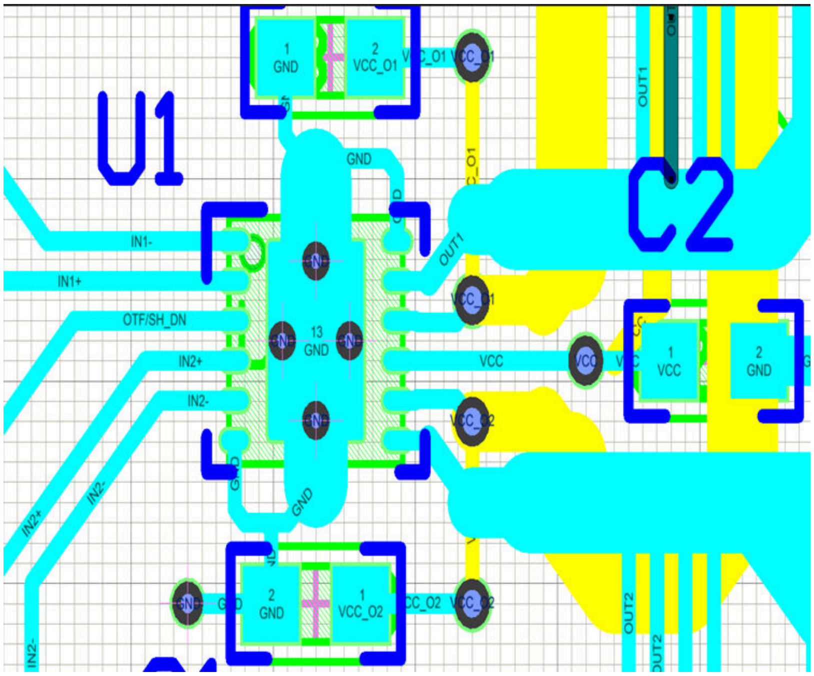


Figure 10-1. ALM2402F-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *ALM2402F-Q1 Evaluation Module* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ALM2402FQPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	A2402FQ
ALM2402FQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	A2402FQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

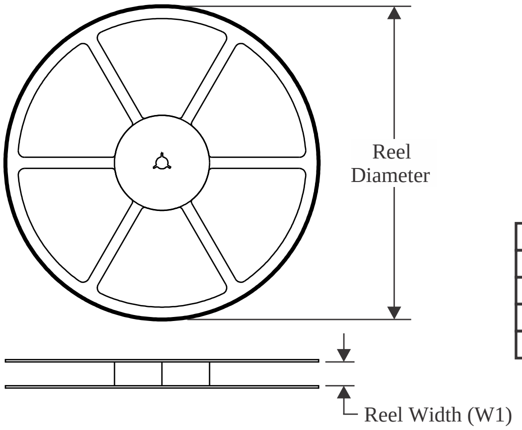
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

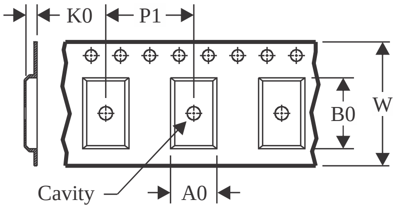
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

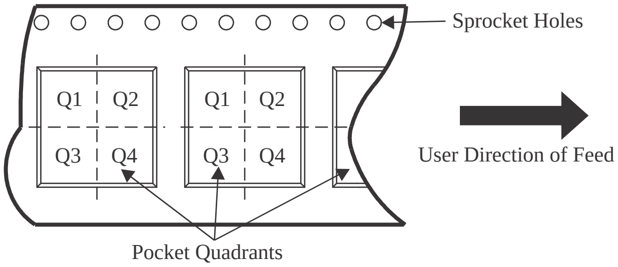


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

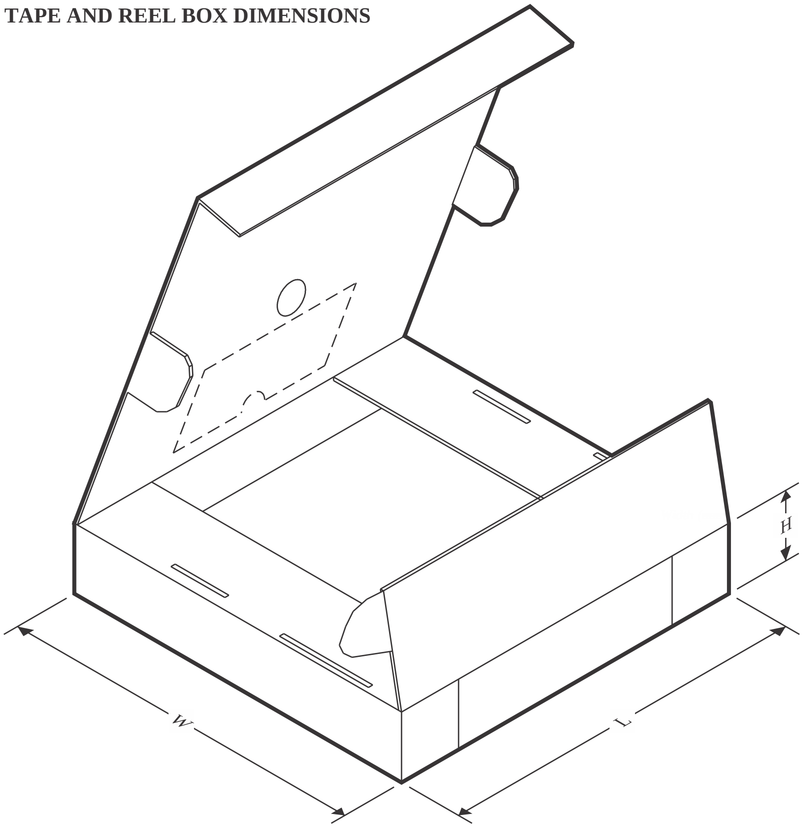
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ALM2402FQPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ALM2402FQPWPRQ1	HTSSOP	PWP	14	2000	353.0	353.0	32.0

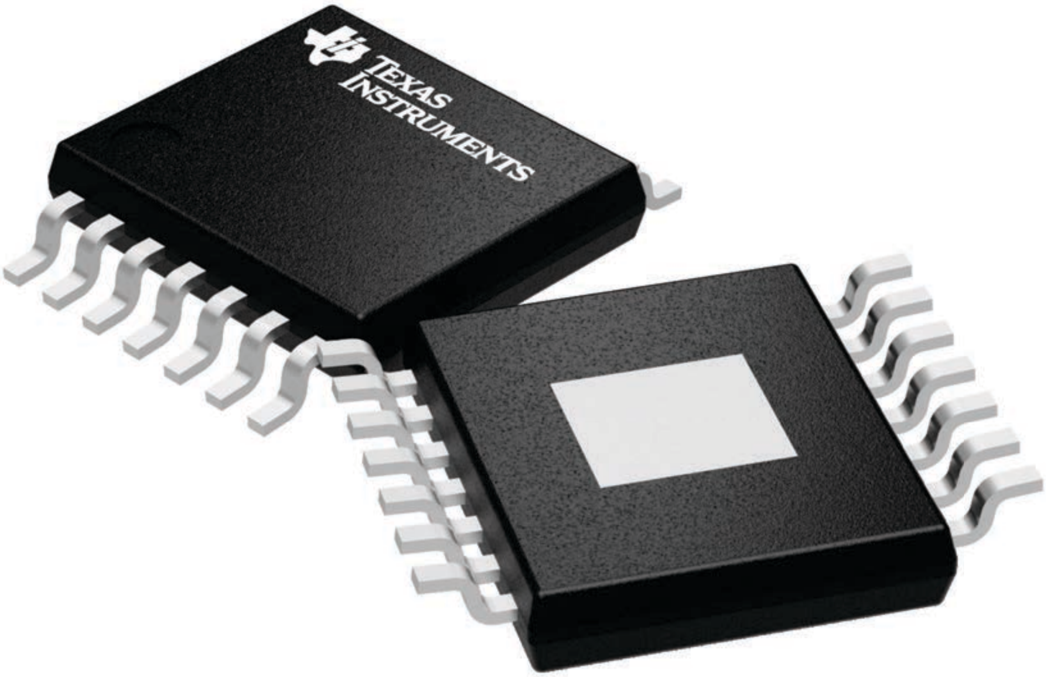
PWP 14

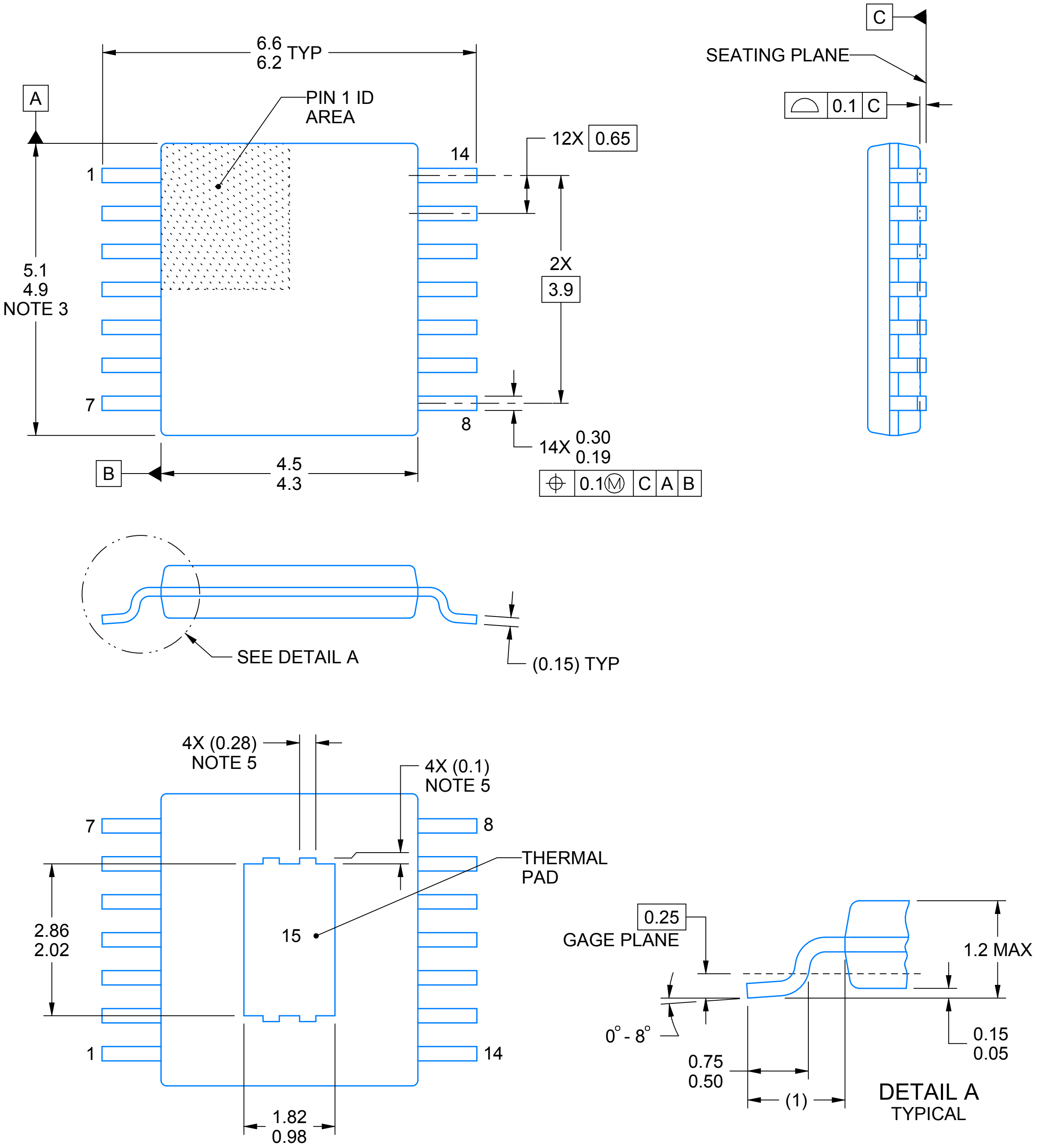
PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



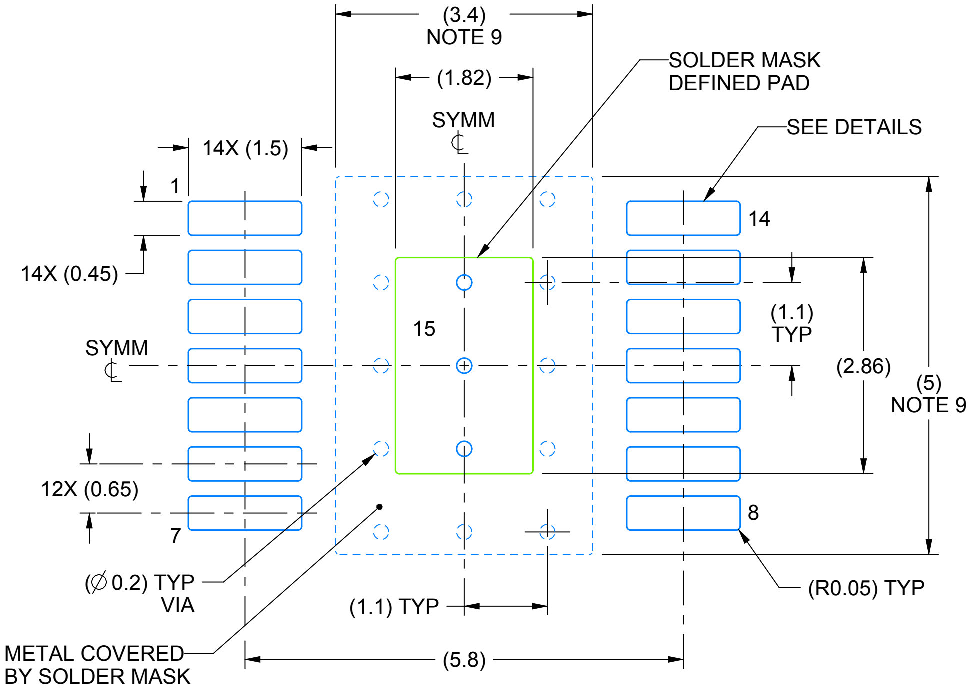


4224353/A 07/2018

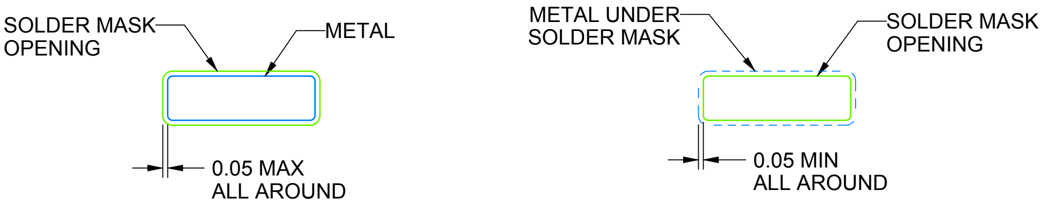
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

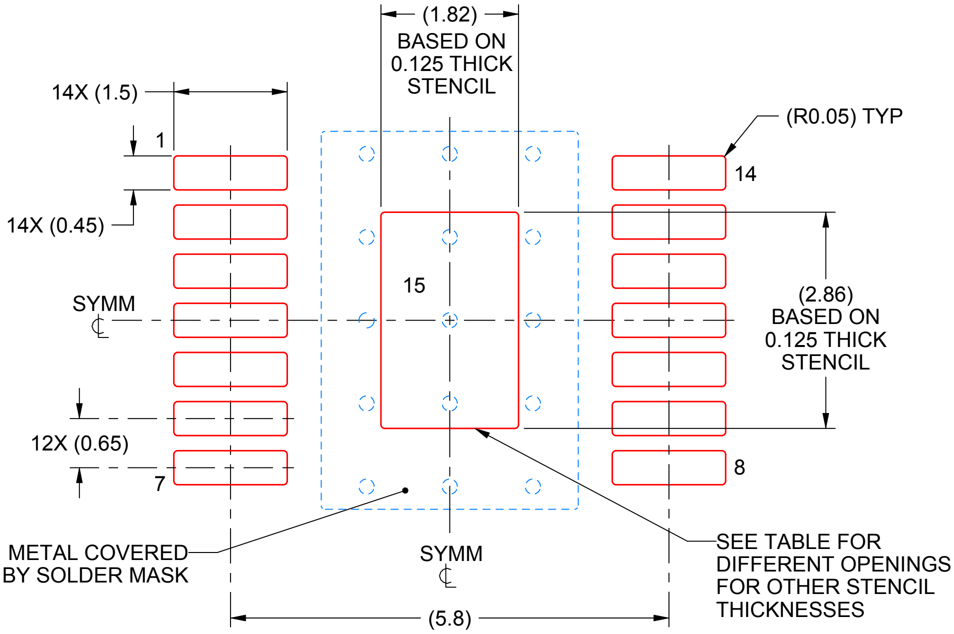
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
PADS 1-14

/A 07/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.03 X 3.20
0.125	1.86 X 2.86 (SHOWN)
0.15	1.66 X 2.61
0.175	1.54 X 2.42

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025