

# ADS52J6x, 8/4-Channel, 16/14-Bit, 125MSPS, 70mW/Ch for 8-CH ADC With JESD204B Interface

## 1 Features

- 16/14-Bit Resolution, 8/4-Channel ADC
- Idle Signal-to-Noise Ratio (SNR):
  - 80dBFS for 16bit ADC
  - 79dBFS for 14bit ADC
- Power dissipation at 125MSPS, 4CH per Lane:
  - 70mW/Ch for ADS52J65/66 (8CH ADC)
  - 82mW/Ch for ADS52J67/68 (4CH ADC)
- Power dissipation at 62.5MSPS, 8CH per Lane:
  - 45mW/Ch for ADS52J65/66 (8CH ADC)
  - 65mW/Ch for ADS52J67/66 (4CH ADC)
- Full-Scale Input: 2V<sub>PP</sub>
- Full-Scale SNR at f<sub>IN</sub> = 10MHz:
  - 78dBFS for 16bit ADC
  - 77dBFS for 14bit ADC
- Full-Scale SFDR: –85dBc at f<sub>IN</sub> = 10MHz
- Analog Input –3dB Bandwidth = 250MHz
- Maximum Input Signal Frequency for 2V<sub>PP</sub> Input = 130MHz
- Fast and Consistent Overload Recovery
- Advanced Digital Features
  - Automatic DC Offset Correction
  - Digital Average
- Digital I/Q Demodulator
  - Fractional Decimation Filter M = 1 to 63 With Increments of 0.25
  - Data Output Rate Reduction After Decimation
  - Power dissipation at 80MSPS and Decimation = 2
    - 64mW/Ch for ADS52J65/66 (8-CH ADC)
    - 91mW/Ch for ADS52J67/68 (4-CH ADC)
  - On-Chip RAM With 32 Preset Profiles
- JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
  - 10Gbps JESD Interface
  - Supports lane rate up to 12.8Gbps for short trace length (< 5 Inch)
  - 64-Pin Non-Magnetic 9 × 9mm Package

## 2 Applications

- Medical Imaging: Ultrasound, MRI
- High Frequency Ultrasound
- Non-Destructive Tests (NDT)
- Radar, Lidar, and [Spectroscopy](#)
- Digital Oscilloscopes and Data Acquisition
- Flow cytometry, flow cytometer, Hematology analyze

## 3 Description

The 8/4-channel, 16/14-bit ADS52J6x analog-to-digital converter (ADC) uses CMOS process and remarkable circuit techniques. The device is designed to operate at low power and give very high signal-to-noise ratio (SNR) performance with a 2-V<sub>PP</sub> full-scale input. The ADS52J65 device gives 80dBFS idle SNR and 78dBFS full scale SNR at 5MHz. The large input bandwidth of 250MHz makes the device well suited for a wide range of applications, such as high frequency medical ultrasound, magnetic resonance imaging, multi-channel data acquisition, flow cytometry, and hematology analyzer. The ADC integrates an internal reference trimmed to match across devices.

### Device Comparison

Part Number	Resolution	Number of Channels
ADS52J65	16-bit	8
ADS52J66	14-bit	8
ADS52J67	16-bit	4
ADS52J68	14-bit	4

ADS52J6x has advanced digital features, including a digital I/Q demodulator with fractional decimation filter. The ADC data from each channel is encoded using an 8B to 10B format and is sent as a SerDes data stream using current-mode logic (CML) output buffers, as per the JESD204B standard. The ADC data from all eight channels can be output over a single CML buffer (1-lane SerDes) with the data rate limited to a maximum of 12.8Gbps. Using SerDes outputs reduces the number of interface lines. This, together with the low-power design, enables eight channels to be packaged in a 9mm × 9mm VQFN allowing high system integration densities. ADS52J6x also supports modes where all ADC data is sent over four CML buffers (4-Lane SerDes), reducing the SerDes data rate per lane for low-cost FPGAs. The ADS52J6x is available in a non-magnetic VQFN package that does not create any magnetic artifact. The device is specified over –40°C to +85°C.

### Device Information

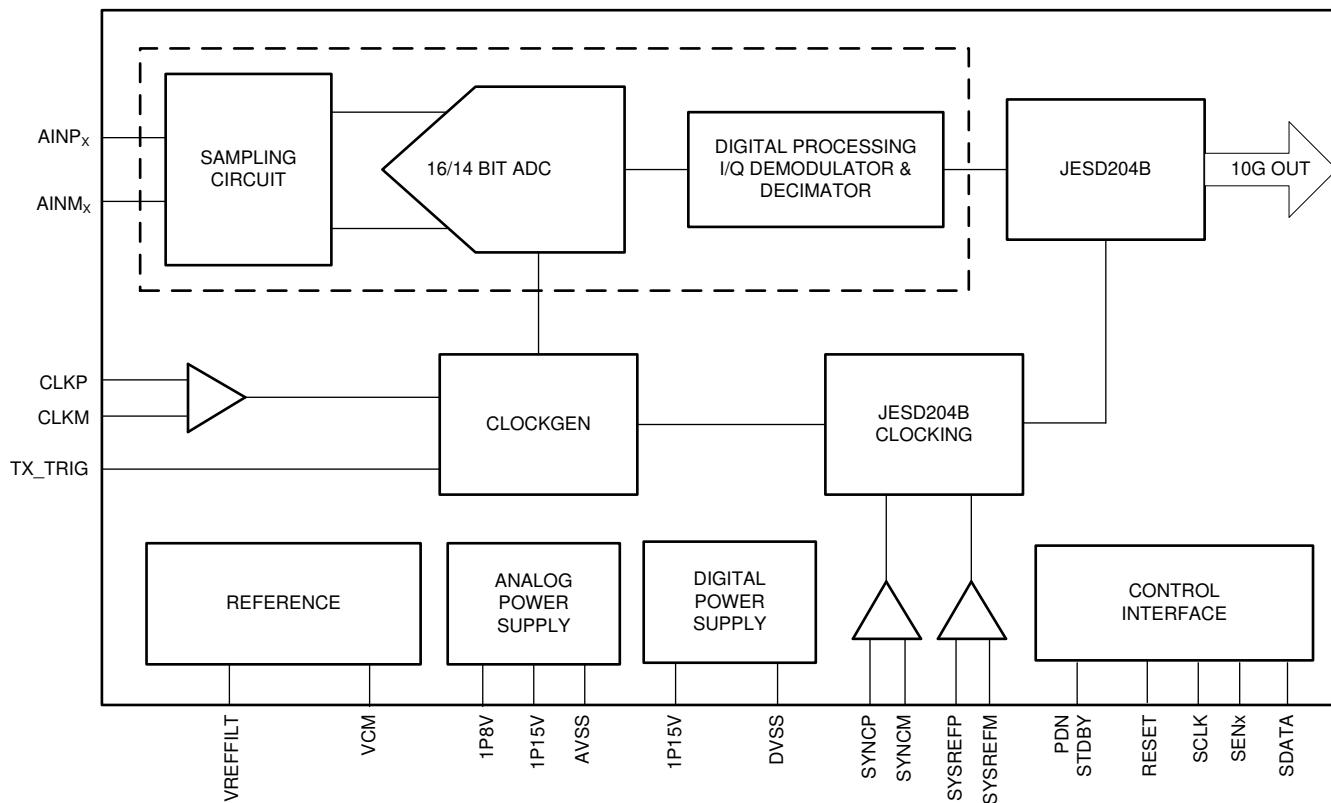
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE (NOM) <sup>(2)</sup>
ADS52J6x	VQFN (64)	9.00mm × 9.00mm

(1) See the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Block Diagram**

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## 4 Device and Documentation Support

### 4.1 Related Documentation

For related documentation see the following:

- [JESD204B Overview](#)
- [Clocking High-Speed Data Converters](#)
- [ADS52J90 10-Bit, 12-Bit, 14-Bit, Multichannel, Low-Power, High-Speed ADC with LVDS, JESD Outputs](#)
- [ADS5263 Quad Channel 16-Bit, 100-MSPS High-SNR ADC](#)
- [AFE5818 16-Channel, Ultrasound, Analog Front-End with 140-mW/Channel Power, 0.75-nV/ \$\sqrt{\text{Hz}}\$  Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer](#)
- [ISO724x High-Speed, Quad-Channel Digital Isolators](#)
- [LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs](#)
- [SN74AUP1T04 LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE INVERTER GATE](#)
- [THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers](#)

### 4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 4.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 4.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 4.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2020) to Revision B (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	<a href="#">1</a>
• Added description of 14-bit and 4-channel device parts.....	<a href="#">1</a>

Changes from Revision * (December 2018) to Revision A (June 2020)	Page
• Added <i>Application</i> : Flow cytometry, flow cytometer, Hematology analyze.....	<a href="#">1</a>

- Added text to the first paragraph of the *Description*: flow cytometry, flow cytometer, hematology analyzation..1

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## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ADS52J65IRGCR</a>	Active	Production	VQFN (RGC)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
ADS52J65IRGCR.A	Active	Production	VQFN (RGC)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
<a href="#">ADS52J65IRGCT</a>	Active	Production	VQFN (RGC)   64	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
ADS52J65IRGCT.A	Active	Production	VQFN (RGC)   64	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J65
<a href="#">ADS52J66IRGCR</a>	Active	Production	VQFN (RGC)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J66
<a href="#">ADS52J67IRGCR</a>	Active	Production	VQFN (RGC)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J67
<a href="#">ADS52J68IRGCR</a>	Active	Production	VQFN (RGC)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS52J68

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

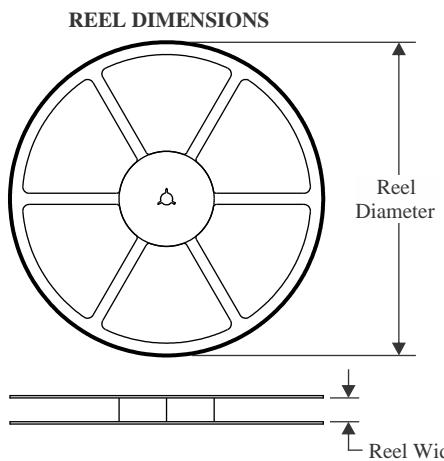
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

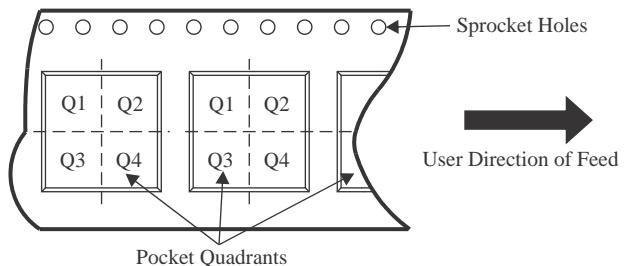
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**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS52J65IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS52J66IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS52J67IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS52J68IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS52J65IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS52J66IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS52J67IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS52J68IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

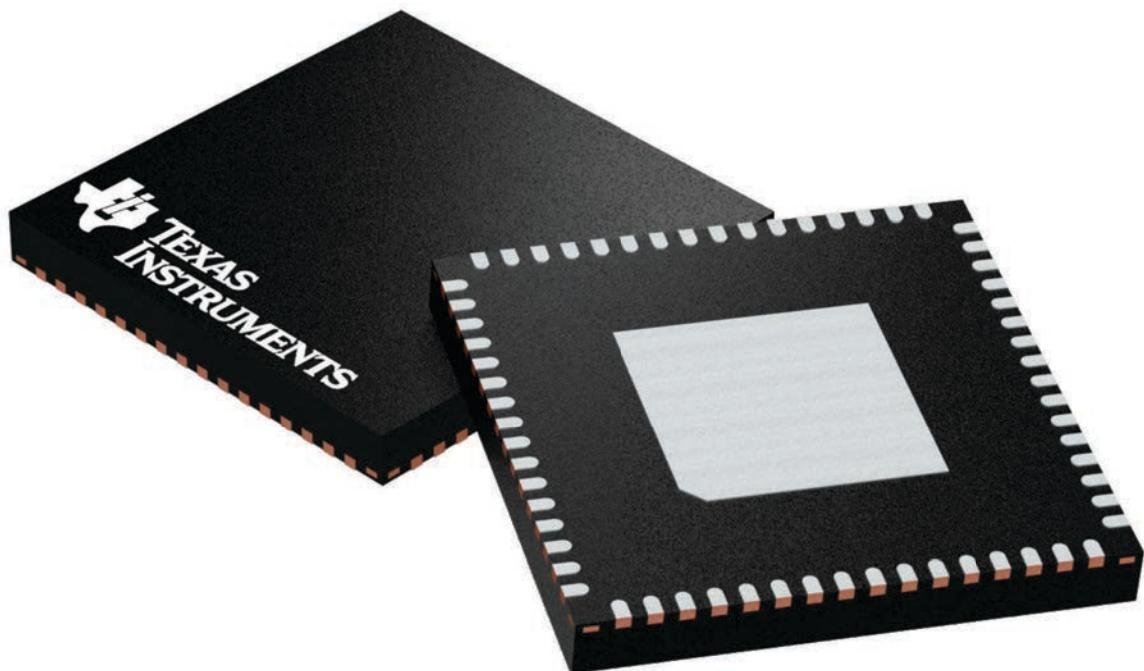
## GENERIC PACKAGE VIEW

**RGC 64**

**VQFN - 1 mm max height**

**9 x 9, 0.5 mm pitch**

**PLASTIC QUAD FLATPACK - NO LEAD**

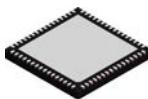


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224597/A

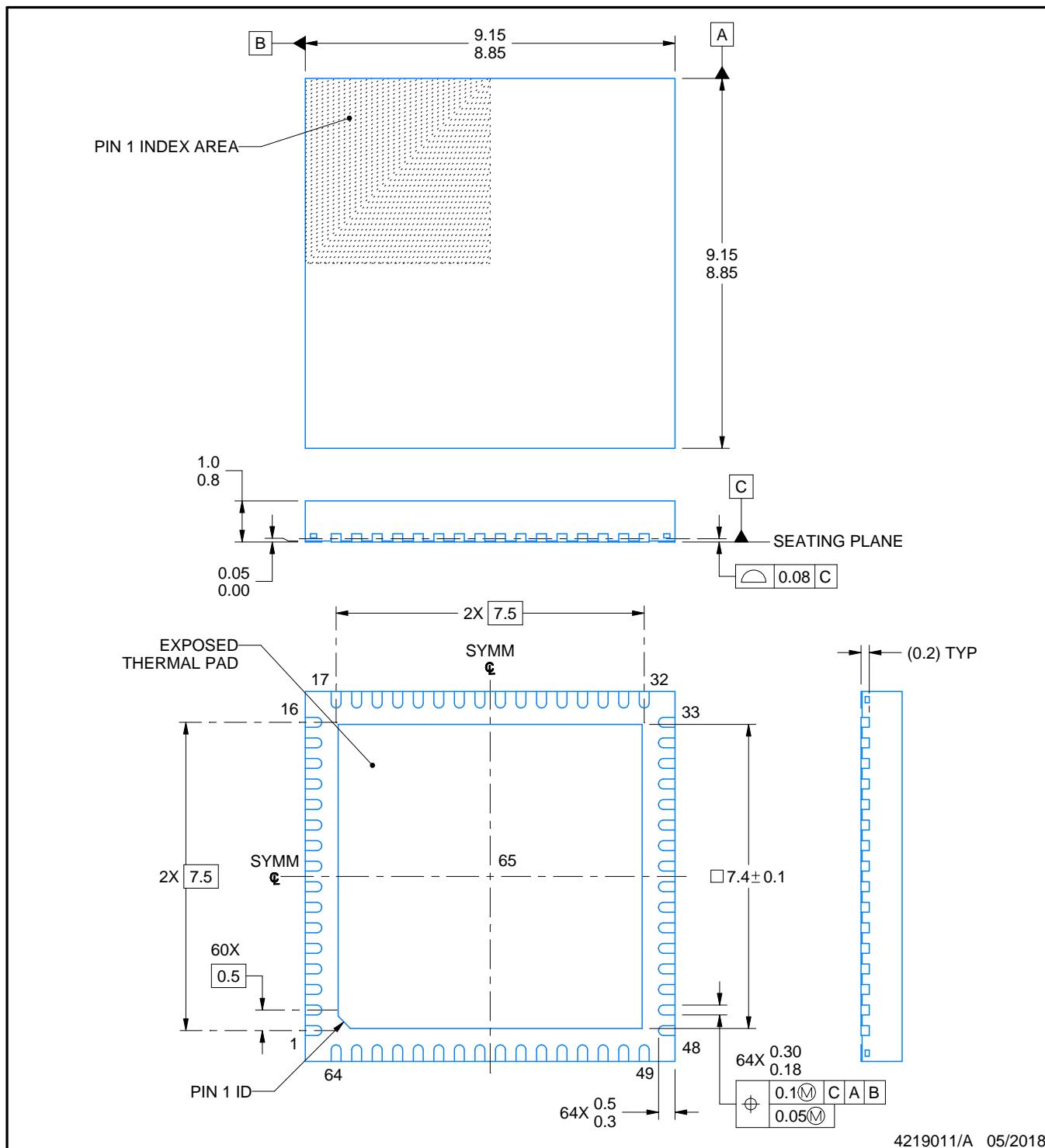
## PACKAGE OUTLINE

**RGC0064H**



## **VQFN - 1 mm max height**

#### PLASTIC QUAD FLATPACK - NO LEAD



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## NOTES:

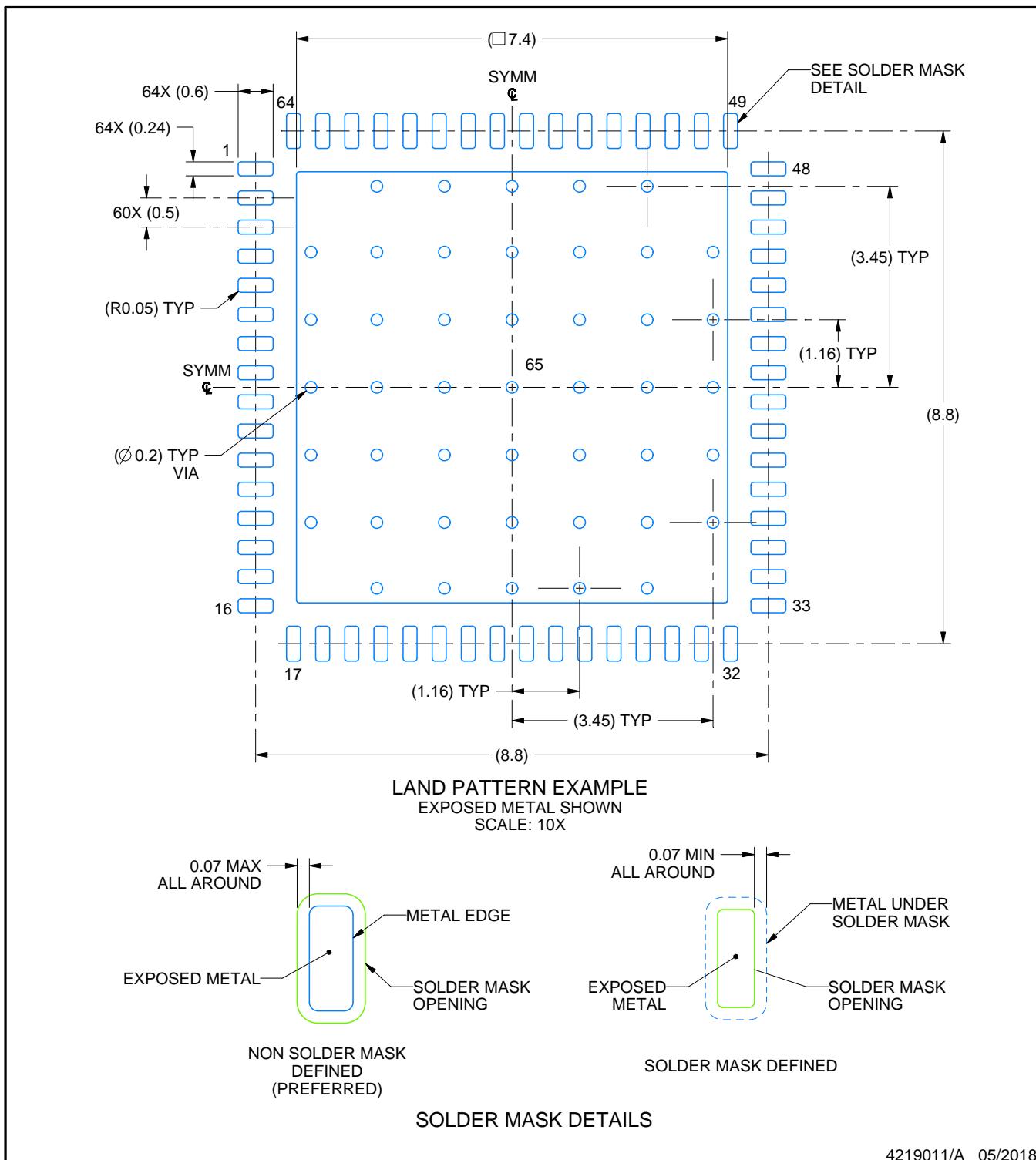
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGC0064H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

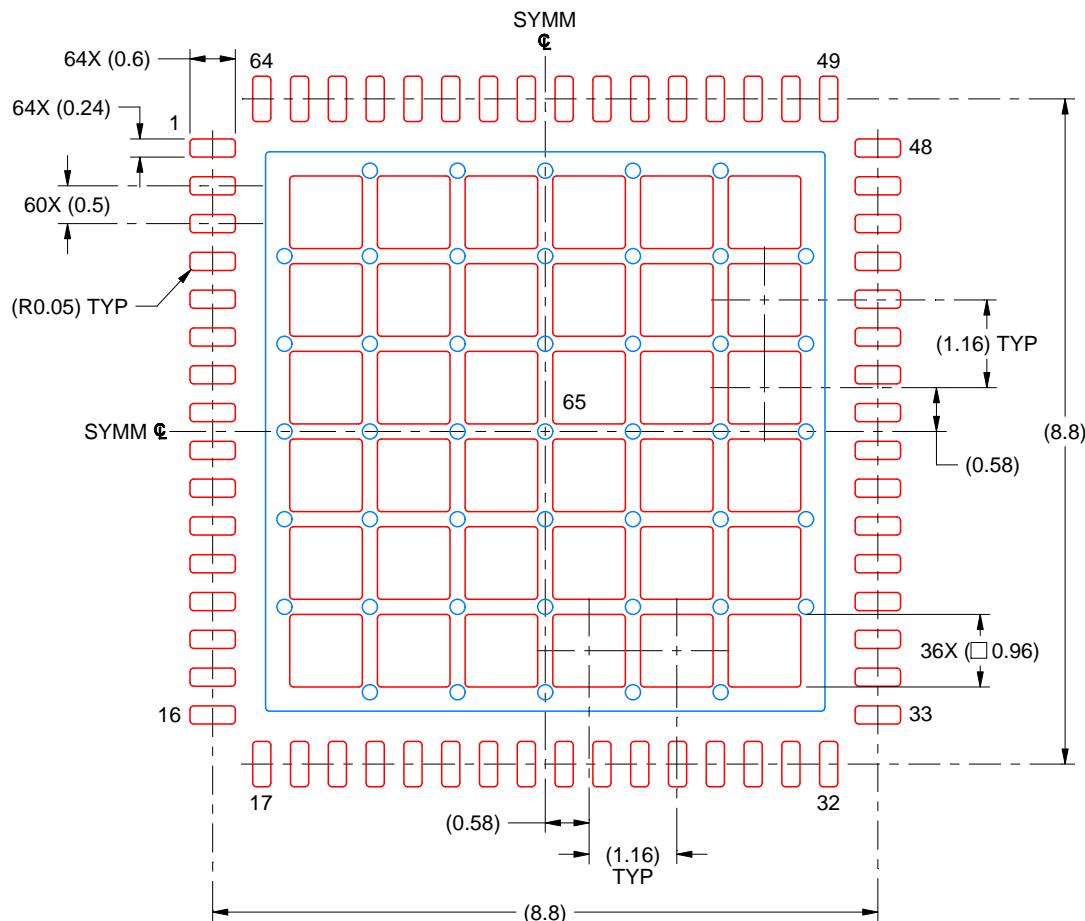
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGC0064H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 10X

EXPOSED PAD 65  
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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