ADS1278QML-SP Radiation Hardened 8-Ch Simultaneous-Sampling 24-Bit Analog-to-Digital Converter

1 Features

- Radiation Hardened
  - TID Radiation Lot Acceptance Test (RLAT): 50krad
  - Single Event Latchup (SEL) Immune to LET: 51MeV-cm^2/mg at 125°C
- Simultaneously Samples Eight Channels
- Up to 128kSPS Data Rate
- AC Performance:
  - 63kHz Bandwidth
  - 111dB SNR (High-Resolution Mode)
  - –108dB THD
- DC Accuracy:
  - 0.8µV/°C Offset Drift
  - 1.3ppm/°C Gain Drift
- Selectable Operating Modes:
  - High-Speed: 128kSPS, 106dB SNR
  - High-Resolution: 52kSPS, 111dB SNR
  - Low-Power: 52kSPS, 31 mW/ch
  - Low-Speed: 10kSPS, 7 mW/ch
- Linear Phase Digital Filter
- SPI™ or Frame-Sync Serial Interface
- Low Sampling Aperture Error
- Modulator Output Option (Digital Filter Bypass)
- Analog Supply: 5V
- Digital Core: 1.8V
- I/O Supply: 1.8V to 3.3V

2 Applications

- Space Systems (Satellites, Shuttles, Stations)
  - Satellite Temperature and Position Sensing
  - Orbital Observation Systems
  - Precision and Scientific Applications
  - High-Accuracy Instrumentation

3 Description

The ADS1278QML-SP is an 8-channel, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with data rates up to 128k samples per second (SPS), allowing simultaneous sampling of eight channels.

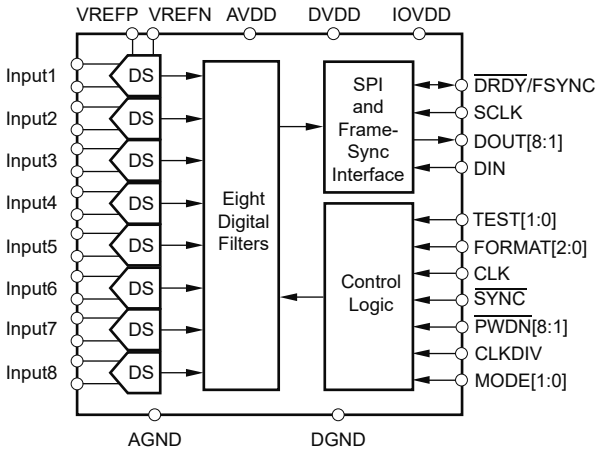
Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large passband droop. As a result, these ADCs have limited signal bandwidth and are mostly designed for dc measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than respective industrial counterparts. The ADS1278QML-SP combines these types of converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. These ADCs provide a usable signal bandwidth up to 90% of the Nyquist frequency with less than 0.005dB of ripple.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(2)
5962L2521001VXC	Flight Grade 50krad (Si) (–55°C to 125°C)	84-Pin HFQ Weight: 4.46g (within ±10%)
5962L2521002VXC	Flight Grade 50krad (Si) (–55°C to 115°C)	

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

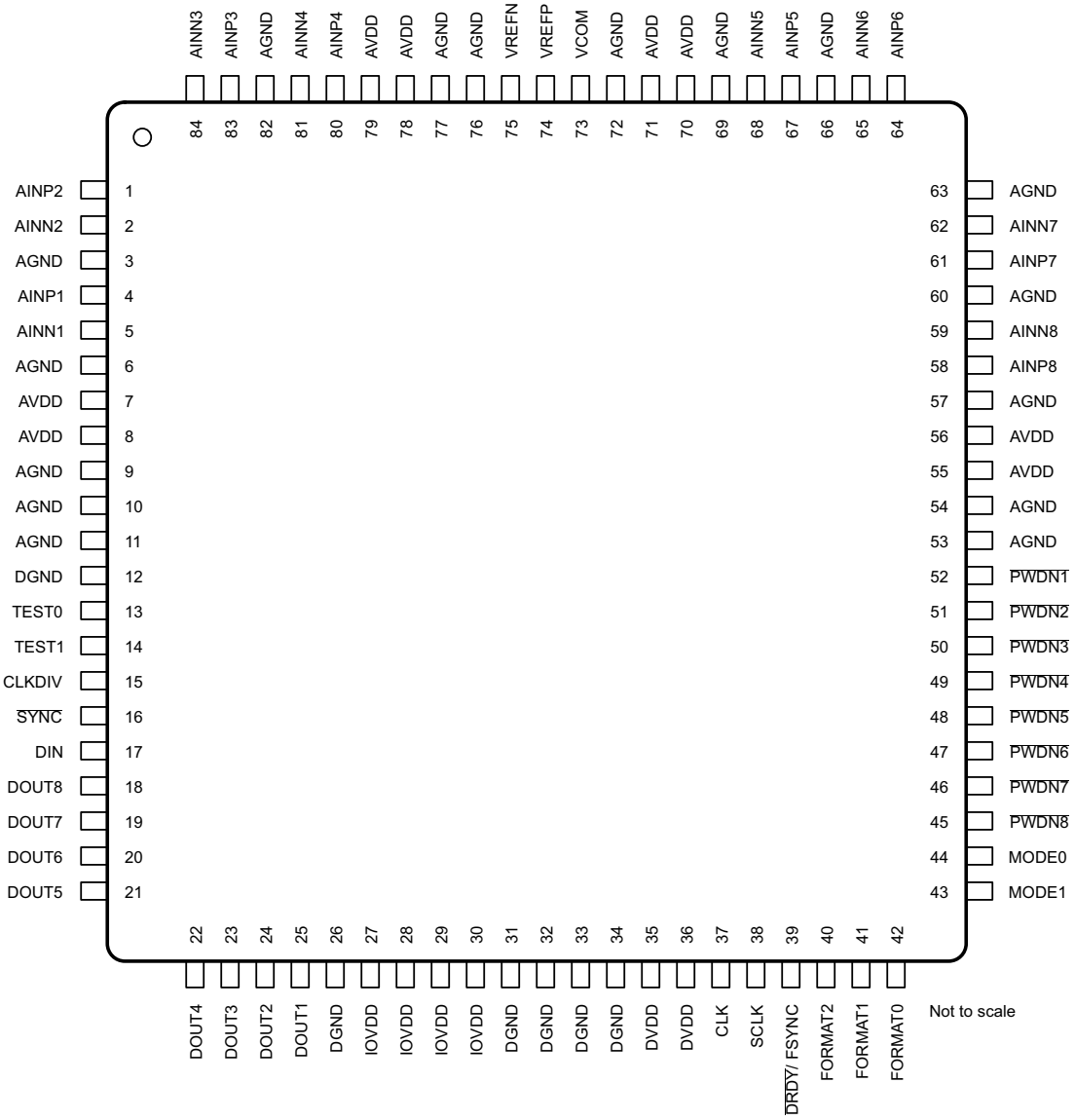


Figure 4-1. HFQ Package 84-Pin CFP Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	3, 6, 9, 10, 11, 53, 54, 57, 60, 63, 66, 69, 72, 76, 77, 82	Analog ground	Analog ground; connect to DGND using a single plane.
AINP1	4	Analog input	AINP[8:1] Positive analog input, channels 8 through 1.
AINP2	1	Analog input	
AINP3	83	Analog input	
AINP4	80	Analog input	
AINP5	67	Analog input	
AINP6	64	Analog input	
AINP7	61	Analog input	
AINP8	58	Analog input	
AINN1	5	Analog input	AINN[8:1] Negative analog input, channels 8 through 1.
AINN2	2	Analog input	
AINN3	84	Analog input	
AINN4	81	Analog input	
AINN5	68	Analog input	
AINN6	65	Analog input	
AINN7	62	Analog input	
AINN8	59	Analog input	
AVDD	7, 8, 55, 56, 70, 71, 78, 79	Analog power supply	Analog power supply (4.75V to 5V).
VCOM	73	Analog output	AVDD / 2 Unbuffered voltage output.
VREFN	75	Analog input	Negative reference input.
VREFP	74	Analog input	Positive reference input.
CLK	37	Digital input	Clock input.
CLKDIV	15	Digital input	CLK input divider control: 1 = 32.768MHz (High-Speed mode only) / 27MHz 0 = 13.5MHz (low-power) / 5.4MHz (low-speed)
DGND	12, 26, 31, 32, 33, 34	Digital ground	Digital ground power supply.
DIN	17	Digital input	Daisy-chain data input.
DOUT1	25	Digital output	DOUT1 is TDM data output (TDM mode).
DOUT2	24	Digital output	DOUT[8:1] Data output for channels 8 through 1.
DOUT3	23	Digital output	
DOUT4	22	Digital output	
DOUT5	21	Digital output	
DOUT6	20	Digital output	
DOUT7	19	Digital output	
DOUT8	18	Digital output	
$\overline{\text{DRDY}}$/ FSYNC	39	Digital input/output	Frame-Sync protocol: frame clock input; SPI protocol: data ready output.
DVDD	35, 36	Digital power supply	Digital core power supply (+1.65V to +1.95V).
FORMAT0	42	Digital input	FORMAT[2:0] Selects Frame-Sync/SPI protocol, TDM/discrete data outputs, fixed/dynamic position TDM data, and modulator mode/normal operating mode.
FORMAT1	41	Digital input	
FORMAT2	40	Digital input	
IOVDD	27, 28, 29, 30	Digital power supply	I/O power supply (+1.65V to +3.6V).

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
MODE0	44	Digital input	MODE[1:0] Selects High-Speed, High-Resolution, Low-Power, or Low-Speed mode operation.
MODE1	43	Digital input	
$\overline{\text{PWDN1}}$	52	Digital input	$\overline{\text{PWDN}}$[8:1] Power-down control for channels 8 through 1.
$\overline{\text{PWDN2}}$	51	Digital input	
$\overline{\text{PWDN3}}$	50	Digital input	
$\overline{\text{PWDN4}}$	49	Digital input	
$\overline{\text{PWDN5}}$	48	Digital input	
$\overline{\text{PWDN6}}$	47	Digital input	
$\overline{\text{PWDN7}}$	46	Digital input	
$\overline{\text{PWDN8}}$	45	Digital input	
SCLK	38	Digital input/output	Serial clock input, modulator clock output.
$\overline{\text{SYNC}}$	16	Digital input	Synchronize input (all channels).
TEST0	13	Digital input	TEST[1:0] Test mode select: 00 = Normal operation 01 = Do not use 11 = Test mode 10 = Do not use
TEST1	14	Digital input	

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AVDD to AGND		–0.3	5.25	V
AGND to DGND		–0.3	0.3	V
DVDD, IOVDD to DGND		–0.3	3.6	V
Input current	Momentary	100		mA
	Continuous	10		
Analog input to AGND		–0.3	AVDD + 0.3	V
Digital input or output to DGND		–0.3	DVDD + 0.3	V
Junction temperature		–55	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	5962L2521001VXC	–55		125	°C
		5962L2521002VXC	–55		115	

5.4 Thermal Information

THERMAL METRIC(1)		ADS1278QML-SP HFQ (CFP) 84 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

All specifications at T_A = –55°C to 125°C, AVDD = 5V, DVDD = 1.8V, IOVDD = 3.3V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	SUBGROUP (1) (2)	–55°C to +125° (5962L2521001VXC)			–55°C to +115° (5962L2521002VXC)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS										
Full-scale input voltage (FSR(3))		V_{IN} = (AINP – AINN)			±V_{REF}			±V_{REF}		V
Absolute input voltage		AINP or AINN to AGND	1, 2, 3	AGND – 0.1		AVDD + 0.1	AGND – 0.1		AVDD + 0.1	V
Common-mode input voltage (V_{CM})		V_{CM} = (AINP + AINN) / 2			2.5			2.5		V
Differential input impedance	High-Speed mode				14			14		kΩ
	High-Resolution mode				14			14		
	Low-Power mode				28			28		
	Low-Speed mode				140			140		
DC PERFORMANCE										
Resolution		No missing codes	1, 2, 3	24			24			Bits
Maximum data rate (f_{DATA})	High-Speed mode	f_{CLK} = 32.768MHz(5)			128,000			128,000		SPS(4)
		f_{CLK} = 27MHz			105,469			105,469		
	High-Resolution mode				52,734			52,734		
	Low-Power mode				52,734			52,734		
	Low-Speed mode				10,547			10,547		
Integral nonlinearity (INL)(6)		Differential input, V_{CM} = 2.5V	1, 2, 3		±0.0003	±0.0012		±0.0003	±0.0012	% FSR
Offset error			1, 2, 3		0.25	2		0.25	2	mV
Offset drift					0.8			0.8		µV/°C
Gain error			1, 2, 3		0.1	0.5		0.1	0.5	% FSR
Gain drift					1.3			1.3		ppm/°C
Noise	High-Speed mode	Shorted input	1, 2, 3		8.5	23		8.5	21	µV rms
	High-Resolution mode	Shorted input	1, 2, 3		5.5	14		5.5	13	
	Low-Power mode	Shorted input	1, 2, 3		8.5	23		8.5	21	
	Low-Speed mode	Shorted input	1, 2, 3		8.0	23		8.0	21	
Common-mode rejection		f_{CM} = 60Hz	1, 2, 3	90	108		90	108		dB
Power-supply rejection	AVDD	f_{PS} = 60Hz			80			80		dB
	DVDD				85			85		
	IOVDD				105			105		
V_{COM} output voltage		No load			AVDD / 2			AVDD / 2		V
AC PERFORMANCE										
Crosstalk		f = 1kHz, –0.5dBFS(9)			–107			–107		dB
Signal-to-noise ratio (SNR(7)) (unweighted)	High-Speed mode		4, 5, 6	98	106		98	106		dB
	High-Resolution mode	V_{REF} = 2.5V	4, 5, 6	101	110		101	110		
		V_{REF} = 3V			111			111		
	Low-Power mode		4, 5, 6	98	106		98	106		
	Low-Speed mode		4, 5, 6	98	107		98	107		
Total harmonic distortion (THD)(8)		V_{IN} = 1kHz, –0.5dBFS	4, 5, 6		–108	–96		–108	–96	dB
Spurious-free dynamic range					109			109		dB
Passband ripple					±0.005			±0.005		dB
Passband					0.453f_{DATA}			0.453f_{DATA}		Hz
–3dB bandwidth					0.49f_{DATA}			0.49f_{DATA}		Hz
Stop band attenuation	High-Resolution mode		4, 5, 6	95			95			dB
	All other modes		4, 5, 6	100			100			

All specifications at T_A = –55°C to 125°C, AVDD = 5V, DVDD = 1.8V, IOVDD = 3.3V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	SUBGROUP (1) (2)	–55°C to +125° (5962L2521001VXC)			–55°C to +115° (5962L2521002VXC)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Stop band	High-Resolution mode		4, 5, 6	0.547 f_{DATA}		127.453 f_{DATA}	0.547 f_{DATA}		127.453 f_{DATA}	Hz
	All other modes		4, 5, 6	0.547 f_{DATA}		63.453 f_{DATA}	0.547 f_{DATA}		63.453 f_{DATA}	
Group delay	High-Resolution mode				39/f_{DATA}			39/f_{DATA}		s
	All other modes				38/f_{DATA}			38/f_{DATA}		
Settling time (latency)	High-Resolution mode	Complete settling			78/f_{DATA}			78/f_{DATA}		s
	All other modes	Complete settling			76/f_{DATA}			76/f_{DATA}		
VOLTAGE REFERENCE INPUTS										
Reference input voltage (V_{REF}) (V_{REF} = VREFP – VREFN)		f_{CLK} = 27MHz	1, 2, 3	0.5	2.5	3.1	0.5	2.5	3.1	V
		f_{CLK} = 32.768MHz(5)	1, 2, 3	0.5	2.5	2.6	0.5	2.5	2.6	
Negative reference input (VREFN)			1, 2, 3	AGND – 0.1		AGND + 0.1	AGND – 0.1		AGND + 0.1	V
Positive reference input (VREFP)			1, 2, 3	VREFN + 0.5		AVDD + 0.1	VREFN + 0.5		AVDD + 0.1	V
Reference Input impedance	High-Speed mode				0.65			0.65		kΩ
	High-Resolution mode				0.65			0.65		
	Low-Power mode				1.3			1.3		
	Low-Speed mode				6.5			6.5		
DIGITAL INPUT/OUTPUT (IOVDD = 1.8V to 3.6V)										
V_{IH}			4, 5, 6	0.7 IOVDD		IOVDD	0.7 IOVDD		IOVDD	V
V_{IL}			4, 5, 6	DGND		0.3 IOVDD	DGND		0.3 IOVDD	V
V_{OH}		I_{OH} = 4mA	4, 5, 6	0.8 IOVDD		IOVDD	0.8 IOVDD		IOVDD	V
V_{OL}		I_{OL} = 4mA	4, 5, 6	DGND		0.2 IOVDD	DGND		0.2 IOVDD	V
Input leakage		0 < $V_{IN\ DIGITAL}$ < IOVDD	4, 5, 6			±11			±10	µA
Clock input (f_{CLK})		High-Speed mode(5)	4, 5, 6	0.1		32.768	0.1		32.768	MHz
		Other modes	1, 2, 3	0.1		27	0.1		27	
POWER SUPPLY										
AVDD			1, 2, 3	4.75		5	4.75		5	V
DVDD			1, 2, 3	1.65	1.8	1.95	1.65	1.8	1.95	V
IOVDD			1, 2, 3	1.65		3.6	1.65		3.6	V
Power-down current	AVDD		1, 2, 3		1	11		1	10	µA
	DVDD		1, 2, 3		1	52		1	50	
	IOVDD		1, 2, 3		1	12		1	11	
AVDD current	High-Speed mode		1, 2, 3		97	148		97	145	mA
	High-Resolution mode		1, 2, 3		97	148		97	145	
	Low-Power mode		1, 2, 3		44	66		44	64	
	Low-Speed mode		1, 2, 3		9	20		9	20	
DVDD current	High-Speed mode		1, 2, 3		23	31		23	30	mA
	High-Resolution mode		1, 2, 3		16	21		16	20	
	Low-Power mode		1, 2, 3		12	18		12	17	
	Low-Speed mode		1, 2, 3		2.5	7		2.5	7	
IOVDD current	High-Speed mode		1, 2, 3		0.25	1.5		0.25	1	mA
	High-Resolution mode		1, 2, 3		0.125	0.8		0.125	0.6	
	Low-Power mode		1, 2, 3		0.125	0.8		0.125	0.6	
	Low-Speed mode		1, 2, 3		0.035	0.5		0.035	0.3	

All specifications at T_A = –55°C to 125°C, AVDD = 5V, DVDD = 1.8V, IOVDD = 3.3V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	SUBGROUP (1) (2)	–55°C to +125° (5962L2521001VXC)			–55°C to +115° (5962L2521002VXC)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Power dissipation	High-Speed mode		1, 2, 3		530	805		530	785	mW
	High-Resolution mode		1, 2, 3		515	785		515	765	
	Low-Power mode		1, 2, 3		245	370		245	355	
	Low-Speed mode		1, 2, 3		50	110		50	110	

(1) For subgroup definitions, please see Quality Conformance Inspection table.
(2) Subgroups apply to –55°C to +125°C column only.
(3) FSR = full-scale range = $2V_{REF}$.
(4) SPS = samples per second.
(5) f_{CLK} = 32.768MHz max for High-Speed mode and 27MHz max for all other modes. When f_{CLK} > 27MHz, operation is limited to Frame-Sync mode and $V_{REF} \leq 2.6V$.
(6) Best fit method.
(7) Minimum SNR is verified by the limit of the *DC noise* specification.
(8) THD includes the first nine harmonics of the input signal; Low-Speed mode includes the first five harmonics.
(9) Worst-case channel crosstalk between one or more channels.

5.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55
12	Setting time at	25
13	Setting time at	125
14	Setting time at	–55

5.7 Timing Requirements: SPI Format

For T_A = –55°C to 125°C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 1.95V. (6)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period (1 / f_{CLK}) (1)	37		10,000	ns
t_{CPW}	CLK positive or negative pulse width	15			ns
t_{CONV}	Conversion period (1 / f_{DATA}) (2)	256		2560	t_{CLK}
t_{CD} (3)	Falling edge of CLK to falling edge of $\overline{DRDY}$		22		ns
t_{DS} (3)	Falling edge of $\overline{DRDY}$ to rising edge of first SCLK to retrieve data	1			t_{CLK}
t_{MSBPD}	$\overline{DRDY}$ falling edge to DOUT MSB valid (propagation delay)			16	ns
t_{SD} (3)	Falling edge of SCLK to rising edge of $\overline{DRDY}$		18		ns
t_{SCLK} (4)	SCLK period	1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width	0.4			t_{CLK}
t_{DOHD} (3) (5)	SCLK falling edge to new DOUT invalid (hold time)	10			ns
t_{DOPD} (3)	SCLK falling edge to new DOUT valid (propagation delay)			32	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)	6			ns
t_{DIHD} (5)	Old DIN valid to falling edge of SCLK (hold time)	6			ns

(1) f_{CLK} = 27MHz maximum.
(2) Depends on MODE[1:0] and CLKDIV selection. See Table 6-5 (f_{CLK} / f_{DATA}).
(3) Load on $\overline{DRDY}$ and DOUT = 20pF.
(4) For best performance, limit f_{SCLK} / f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, and so on.
(5) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is > 4ns.
(6) Timing parameters are characterized or verified by design for specified temperature but not production tested.

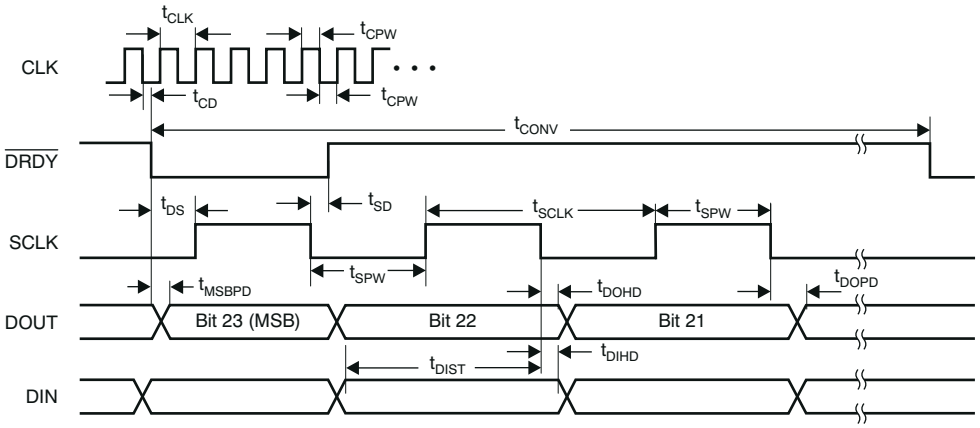


Figure 5-1. SPI Format Timing Characteristics

5.8 Timing Requirements: Frame-Sync Format

over operating free-air temperature range (unless otherwise noted) (4)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period (1 / f_{CLK})	All modes	37		10,000	ns
		High-Speed mode only	30.5			ns
t_{CPW}	CLK positive or negative pulse width		12			ns
t_{CS}	Falling edge of CLK to falling edge of SCLK		–0.25		0.25	t_{CLK}
t_{FRAME}	Frame period (1 / f_{DATA})(1)		256		2560	t_{CLK}
t_{FPW}	FSYNC positive or negative pulse width		1			t_{SCLK}
t_{FS}	Rising edge of FSYNC to rising edge of SCLK		5			ns
t_{SF}	Rising edge of SCLK to rising edge of FSYNC		5			ns
t_{SCLK}	SCLK period(2)		1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width		0.4			t_{CLK}
t_{DOHD} (5) (3)	SCLK falling edge to old DOUT invalid (hold time)		10			ns
t_{DOPD} (3)	SCLK falling edge to new DOUT valid (propagation delay)				31	ns
t_{MSBPD}	FSYNC rising edge to DOUT MSB valid (propagation delay)				31	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)		6			ns
t_{DIHD} (5)	Old DIN valid to falling edge of SCLK (hold time)		6			ns

(1) Depends on MODE[1:0] and CLKDIV selection. See Table 6-5 (f_{CLK} / f_{DATA}).
(2) SCLK must be continuously running and limited to ratios of 1, 1/2, 1/4, and 1/8 of f_{CLK}.
(3) Load on DOUT = 20pF.
(4) Timing parameters are characterized or verified by design for specified temperature but not production tested.
(5) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is > 4ns.

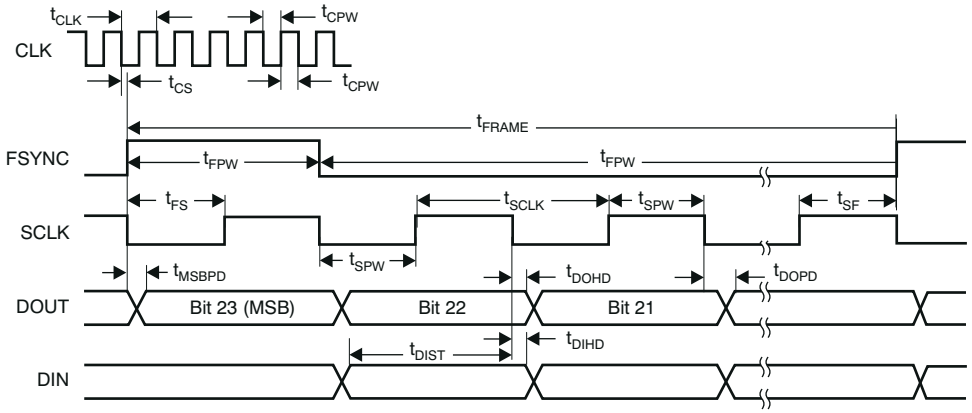


Figure 5-2. Frame-Sync Format Timing Characteristics

5.9 Typical Characteristics

At T_A = 25°C, High-Speed mode, AVDD = 5V, DVDD = 1.8V, IOVDD = 3.3V, f_{CLK} = 27MHz, VREFP = 2.5V, and VREFN = 0V, unless otherwise noted.

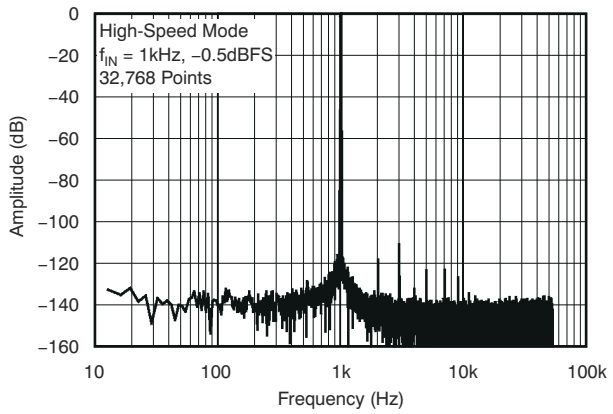


Figure 5-3. Output Spectrum

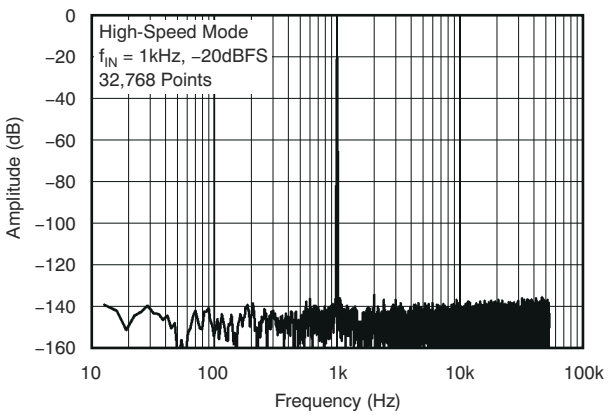


Figure 5-4. Output Spectrum

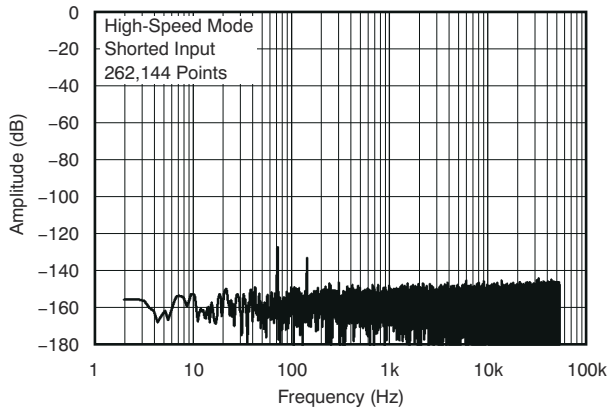


Figure 5-5. Output Spectrum

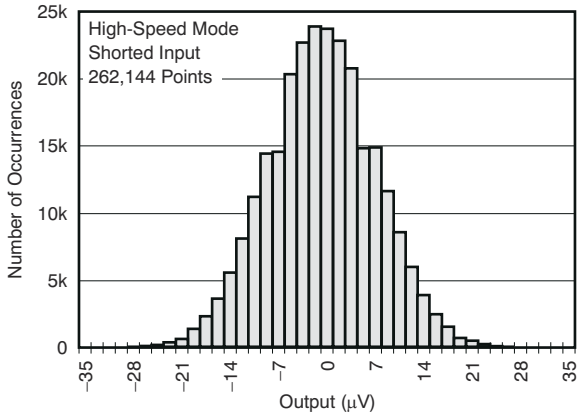


Figure 5-6. Noise Histogram

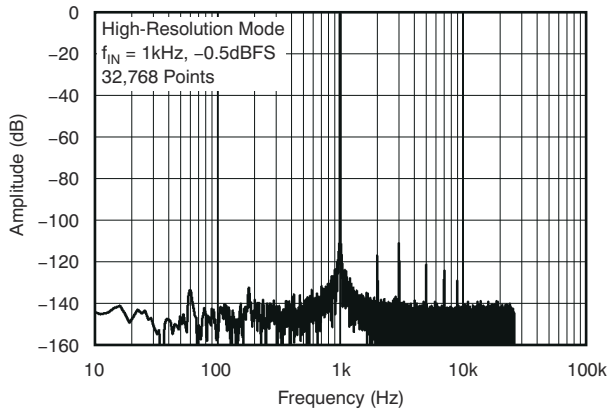


Figure 5-7. Output Spectrum

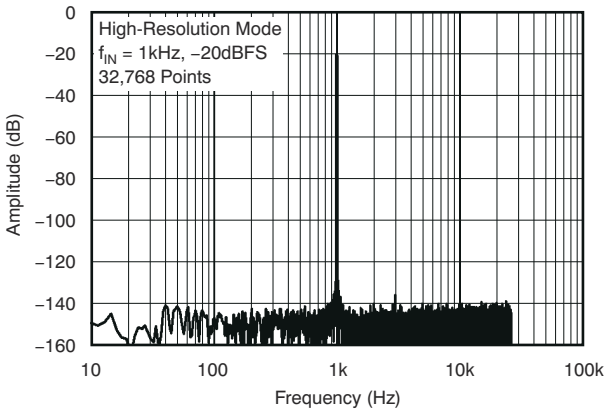


Figure 5-8. Output Spectrum

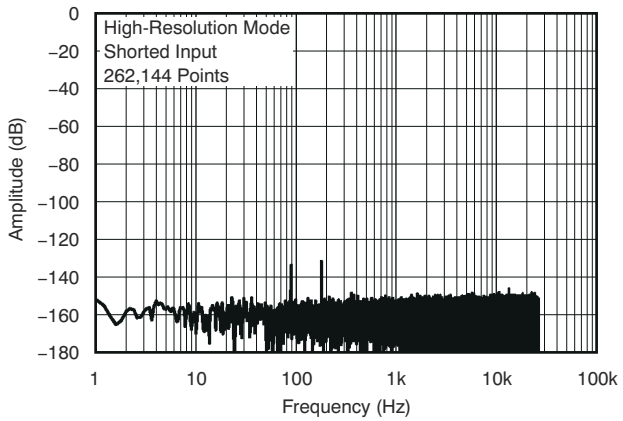


Figure 5-9. Output Spectrum

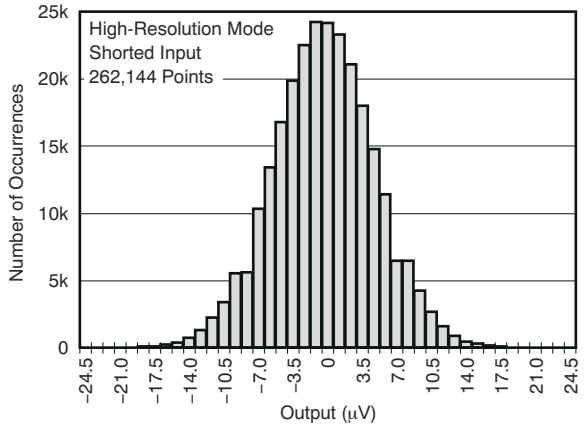


Figure 5-10. Noise Histogram

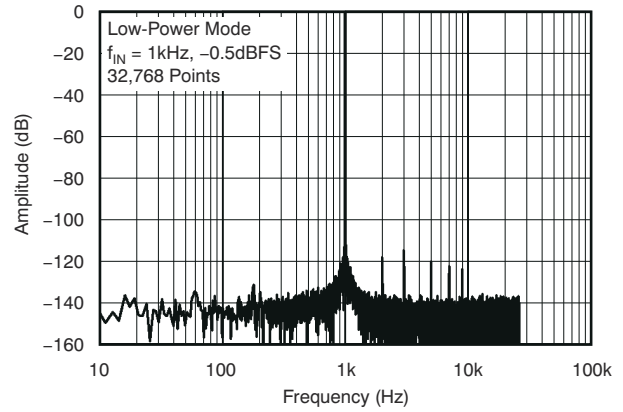


Figure 5-11. Output Spectrum

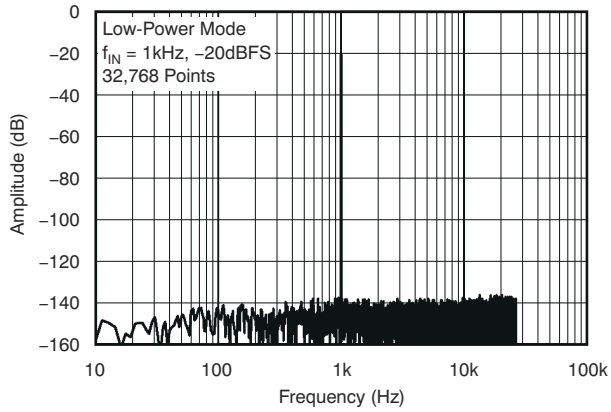


Figure 5-12. Output Spectrum

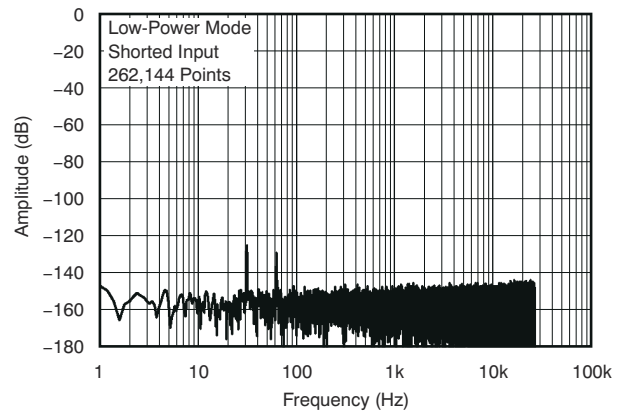


Figure 5-13. Output Spectrum

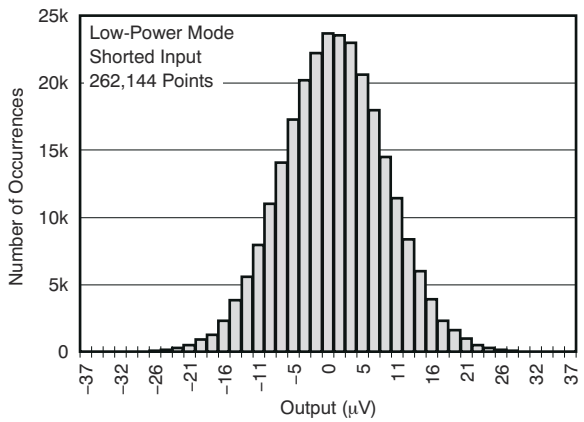


Figure 5-14. Noise Histogram

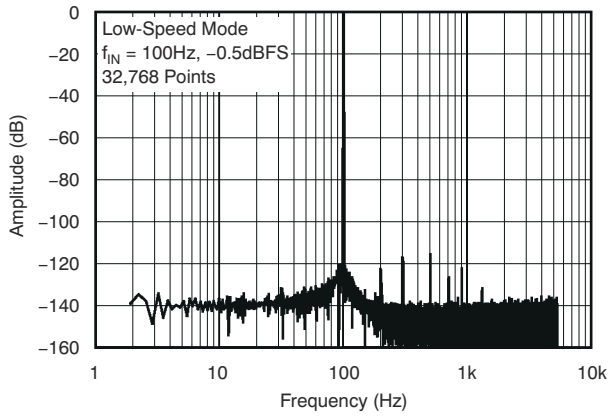


Figure 5-15. Output Spectrum

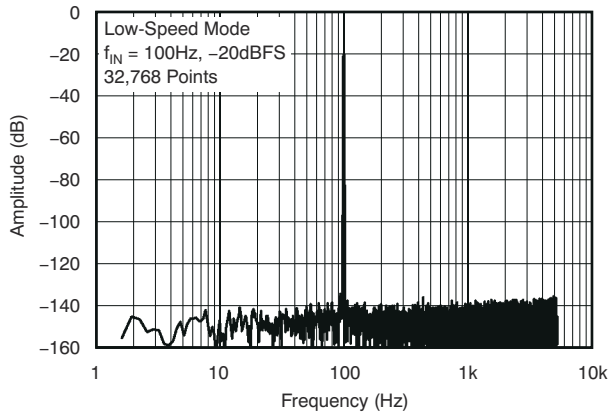


Figure 5-16. Output Spectrum

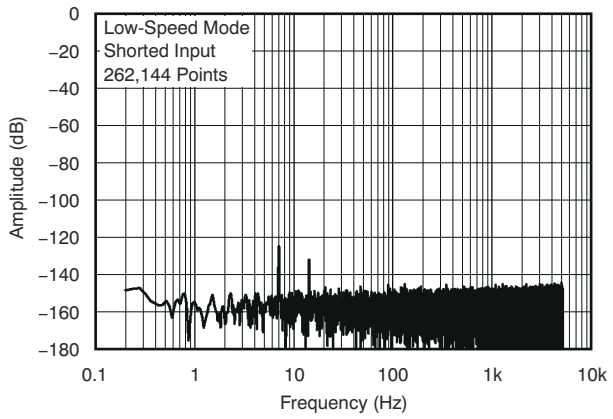


Figure 5-17. Output Spectrum

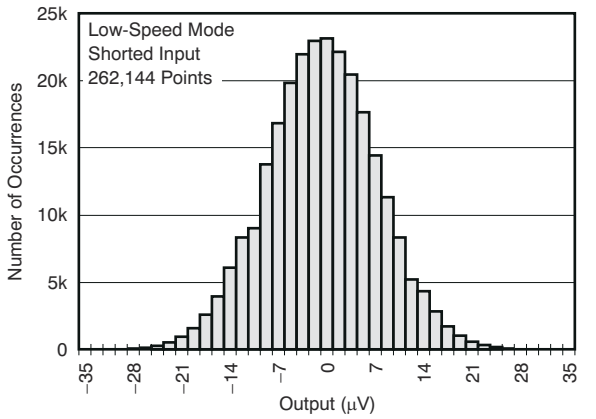


Figure 5-18. Noise Histogram

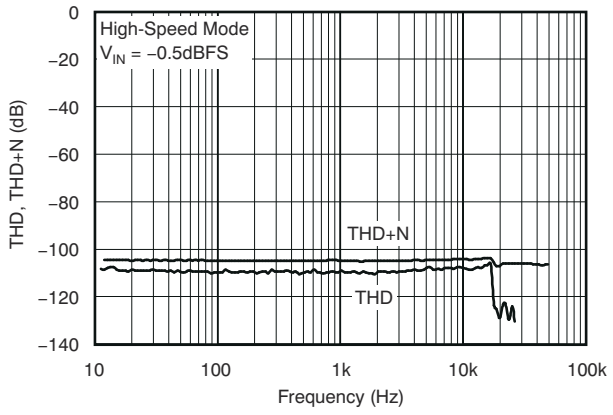


Figure 5-19. Total Harmonic Distortion vs Frequency

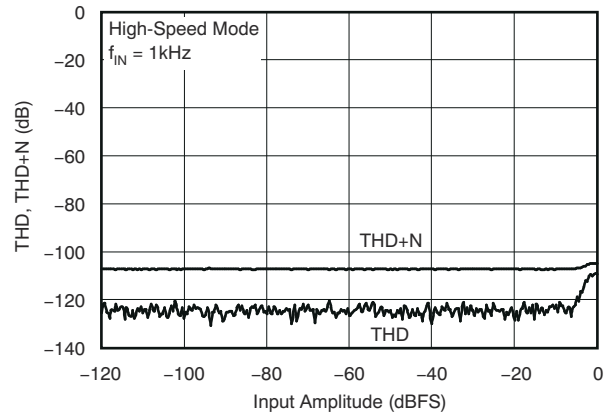


Figure 5-20. Total Harmonic Distortion vs Input Amplitude

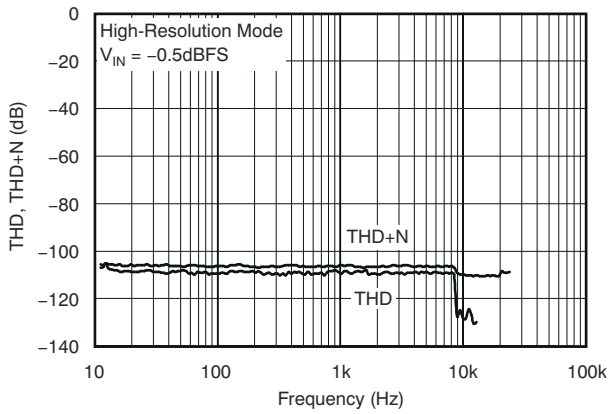


Figure 5-21. Total Harmonic Distortion vs Frequency

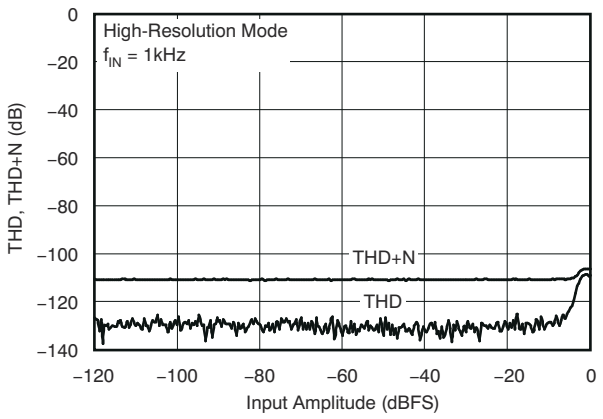


Figure 5-22. Total Harmonic Distortion vs Input Amplitude

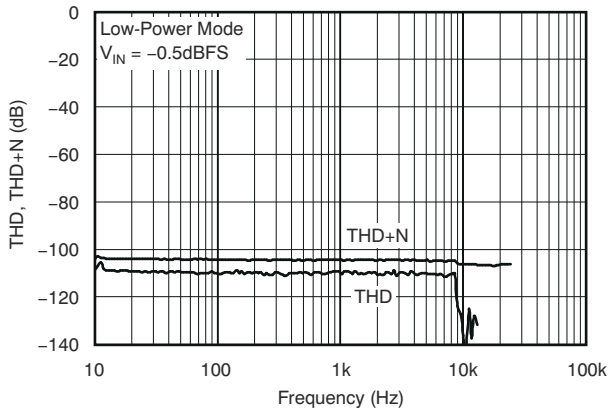


Figure 5-23. Total Harmonic Distortion vs Frequency

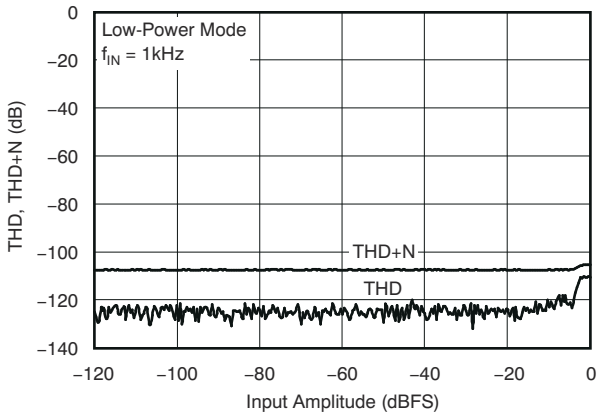


Figure 5-24. Total Harmonic Distortion vs Input Amplitude

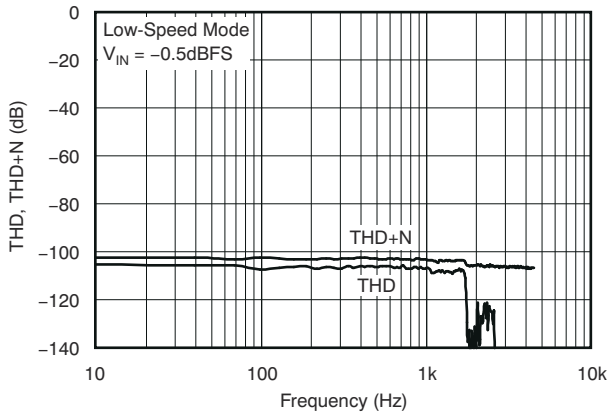


Figure 5-25. Total Harmonic Distortion vs Frequency

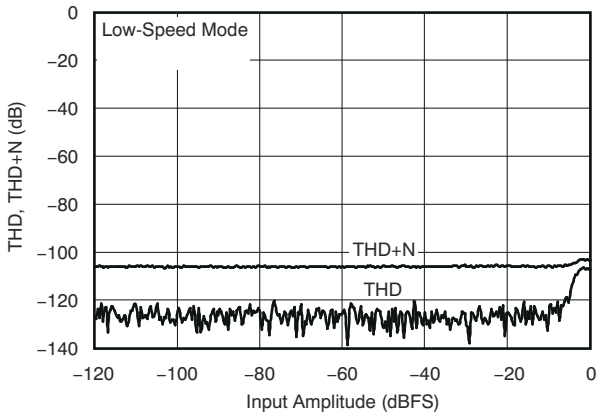


Figure 5-26. Total Harmonic Distortion vs Input Amplitude

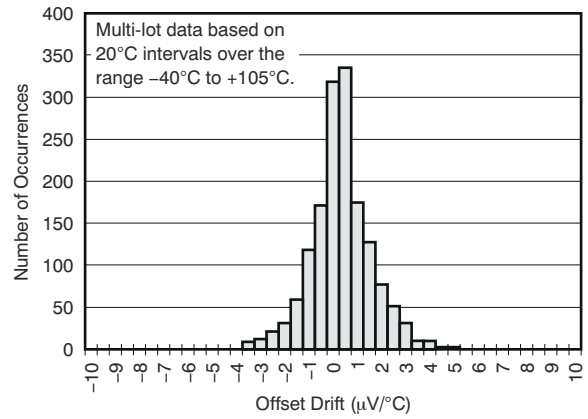


Figure 5-27. Offset Drift Histogram

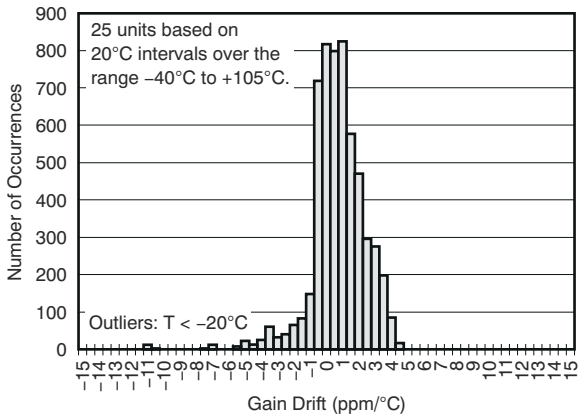


Figure 5-28. Gain Drift Histogram

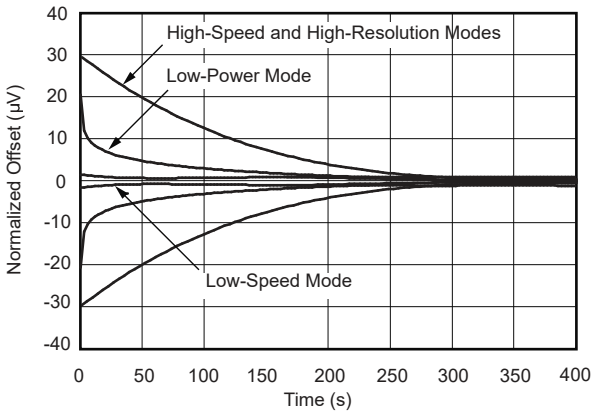


Figure 5-29. Offset Warmup Drift Response Band

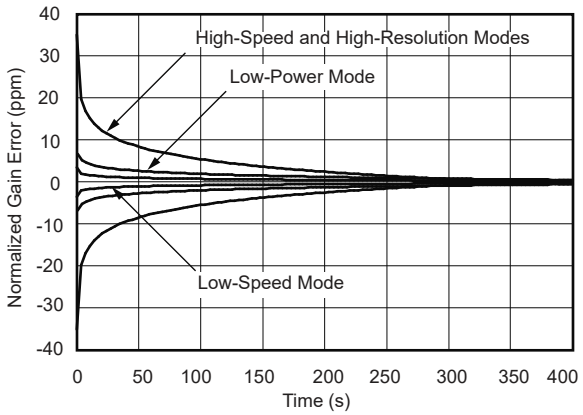


Figure 5-30. Gain Warmup Drift Response Band

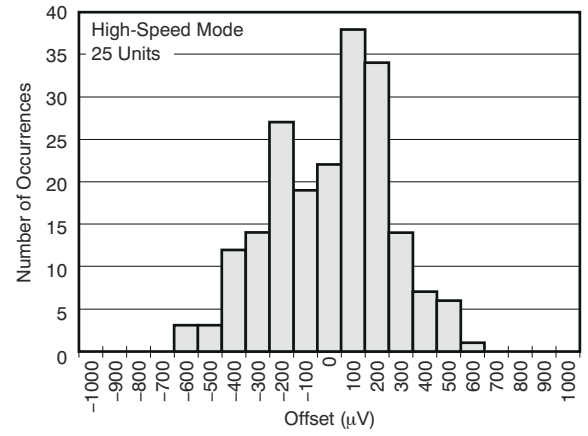


Figure 5-31. Offset Error Histogram

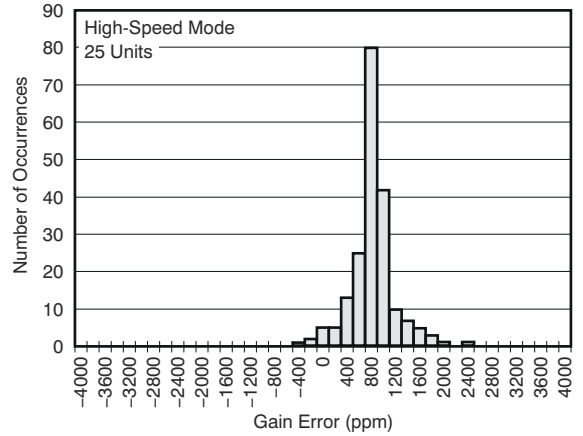


Figure 5-32. Gain Error Histogram

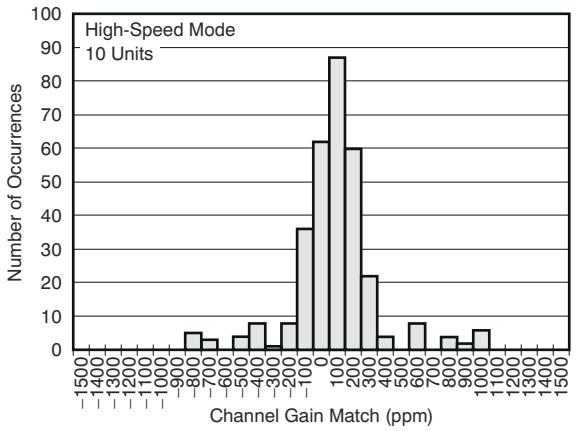


Figure 5-33. Channel Gain Match Histogram

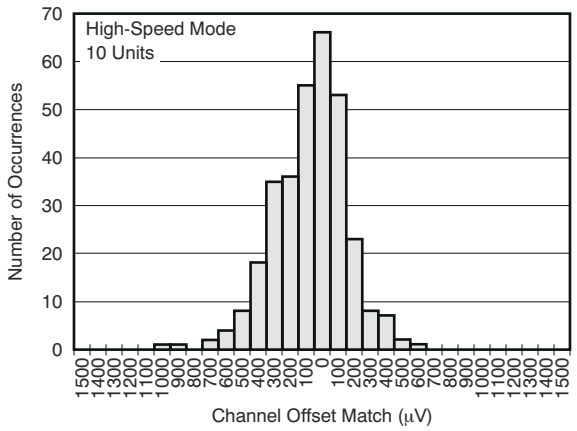


Figure 5-34. Channel Offset Match Histogram

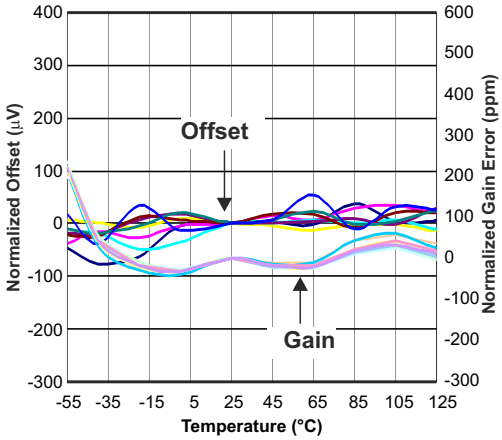


Figure 5-35. Offset and Gain vs Temperature

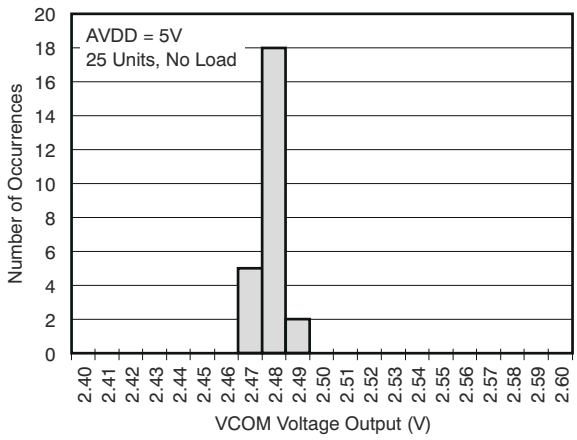


Figure 5-36. VCOM Voltage Output Histogram

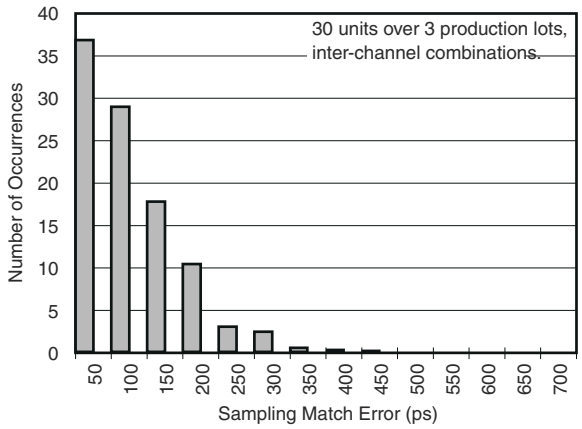


Figure 5-37. Sampling Match Error Histogram

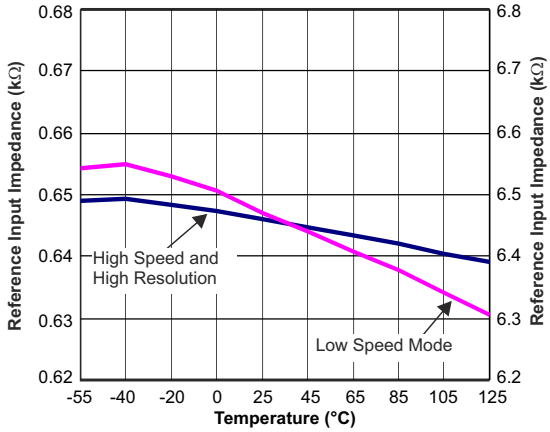


Figure 5-38. Reference Input Differential Impedance vs Temperature

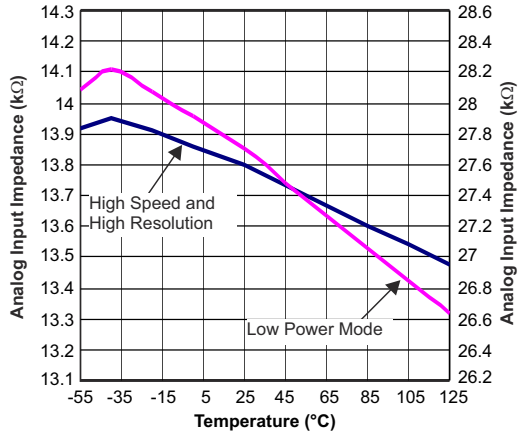


Figure 5-39. Analog Input Differential Impedance vs Temperature

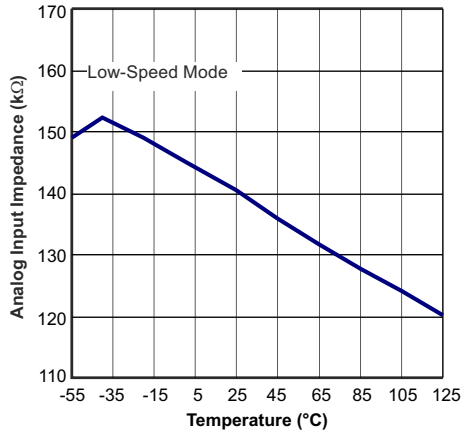


Figure 5-40. Analog Input Differential Impedance vs Temperature

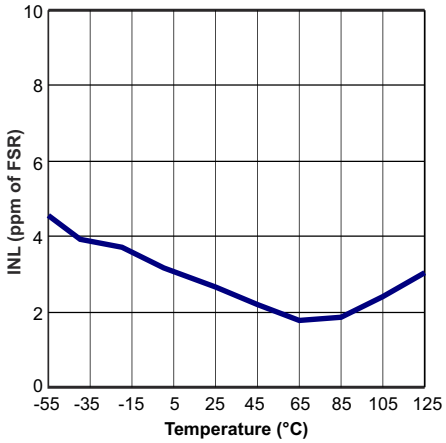


Figure 5-41. Integral Nonlinearity vs Temperature

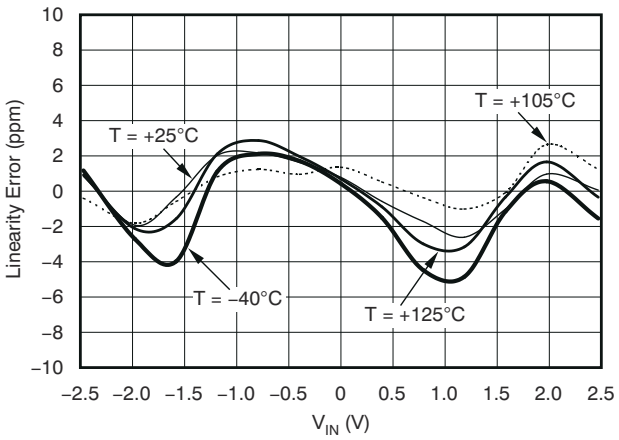


Figure 5-42. Linearity Error vs Input Level

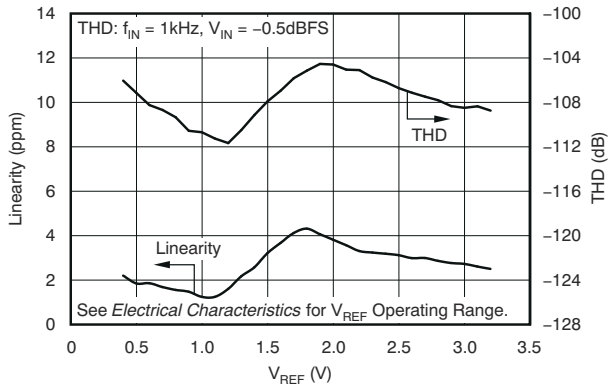


Figure 5-43. Linearity and Total Harmonic Distortion vs Reference Voltage

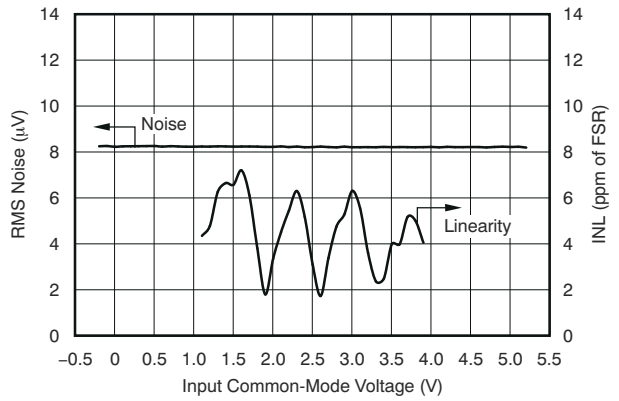


Figure 5-44. Noise and Linearity vs Input Common-Mode Voltage

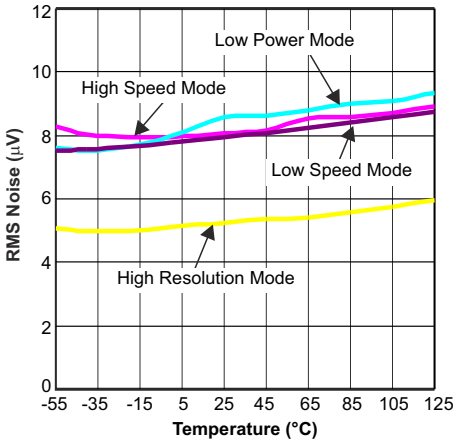


Figure 5-45. Noise vs Temperature

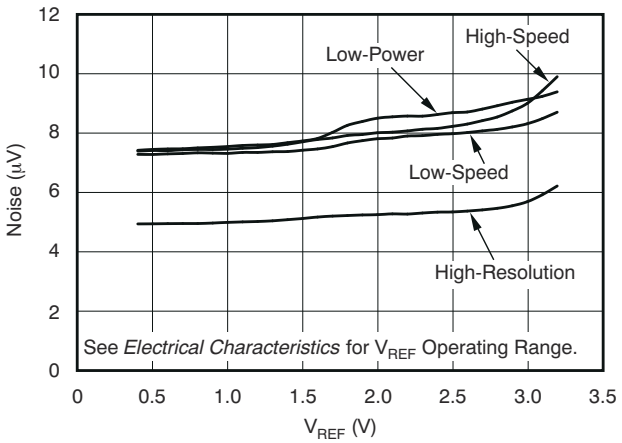


Figure 5-46. Noise vs Reference Voltage

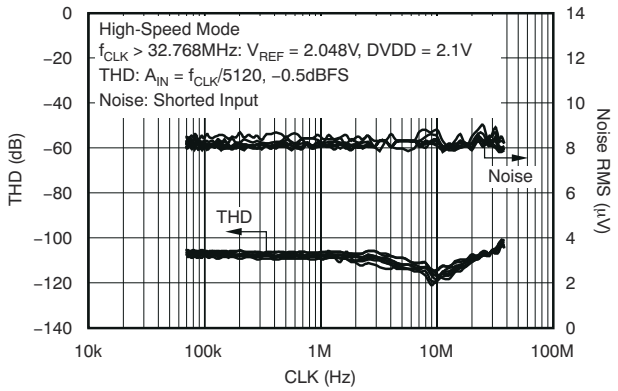


Figure 5-47. Total Harmonic Distortion and Noise vs CLK

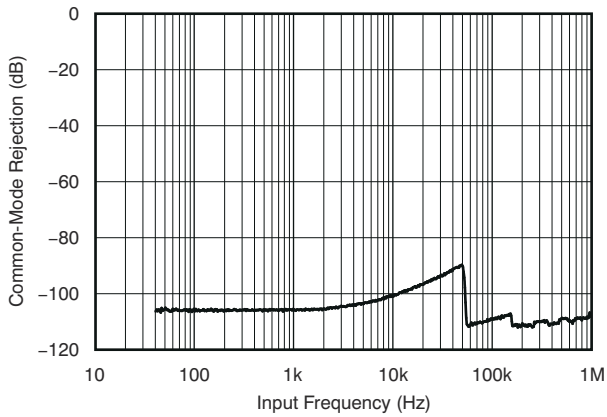


Figure 5-48. Common-Mode Rejection vs Input Frequency

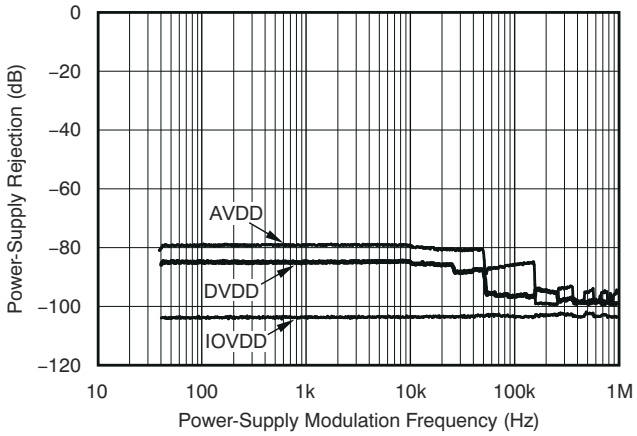


Figure 5-49. Power-Supply Rejection vs Power-Supply Frequency

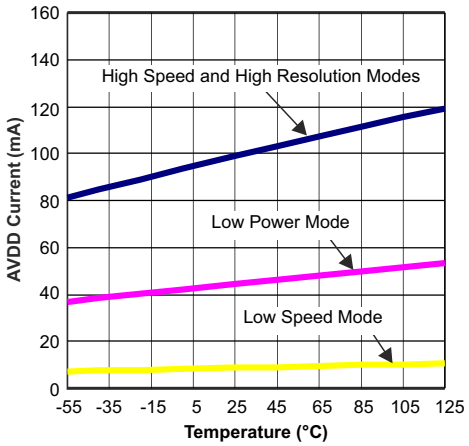


Figure 5-50. AVDD Current vs Temperature

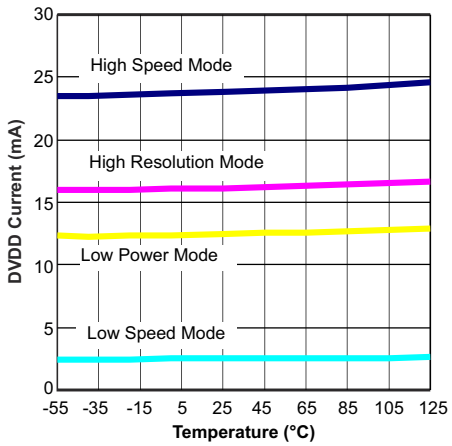


Figure 5-51. DVDD Current vs Temperature

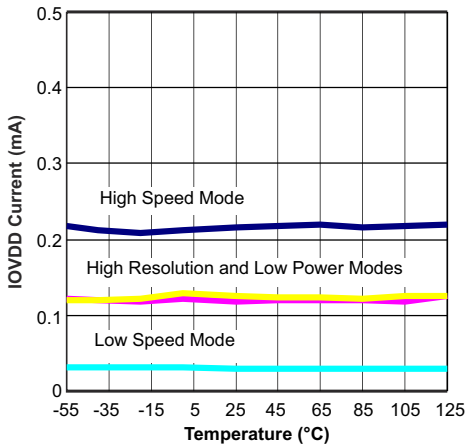


Figure 5-52. IOVDD Current vs Temperature

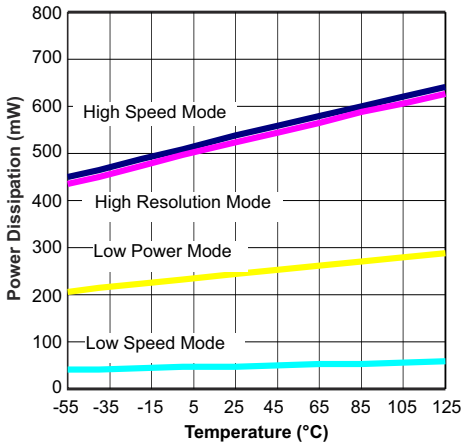


Figure 5-53. Power Dissipation vs Temperature

6 Detailed Description

6.1 Overview

The ADS1278QML-SP is a delta-sigma ADC consisting of eight independent converters that digitize eight input signals in parallel.

The converter is composed of two main functional blocks to perform the ADC conversions: the modulator and the digital filter. The modulator samples the input signal together with sampling the reference voltage to produce a 1s density output stream. The density of the output stream is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by the internal digital filter where the output conversion result is produced.

In operation, the input signal is sampled by the modulator at a high rate (typically 64x higher than the final output data rate). The quantization noise of the modulator is moved to a higher frequency range where the internal digital filter removes the noise. Oversampling results in very low levels of noise within the signal passband.

Since the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency is at the modulator sampling rate. This architecture greatly relaxes the requirement of external antialiasing filters because of the high modulator sampling rate.

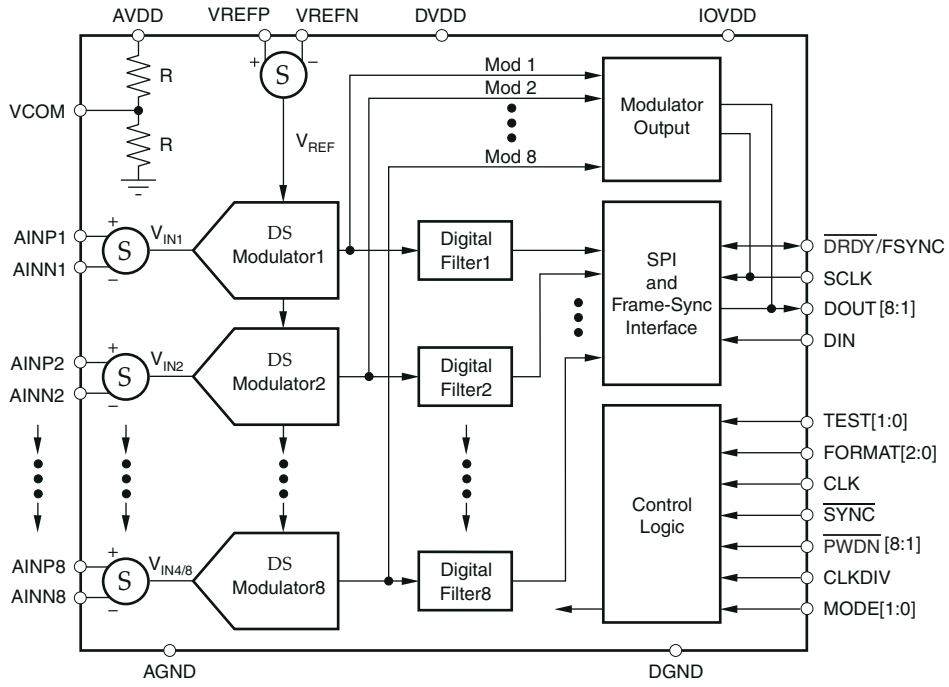
The ADS1278QML-SP is an octal 24-bit, delta-sigma ADC. The device offers the combination of outstanding dc accuracy and superior ac performance. The Functional Block Diagram shows the major blocks of the device. The converter is comprised of eight advanced, 6th-order, chopper-stabilized, delta-sigma modulators followed by low-ripple, linear phase FIR filters. The modulators measure the differential input signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The digital filters receive the modulator signal and provide a low-noise digital output. To allow tradeoffs among speed, resolution, and power, four operating modes are supported:

High-Speed, High-Resolution, Low-Power, and Low-Speed. Table 6-15 summarizes the performance of each mode.

In High-Speed mode, the maximum data rate is 128kSPS (when operating at 128kSPS, Frame-Sync format must be used). In High-Resolution mode, the SNR = 111dB (V_{REF} = 3.0V); in Low-Power mode, the power dissipation is 31mW/channel; and in Low-Speed mode, the power dissipation is only 7mW/channel at 10.5kSPS. The digital filters can be bypassed, enabling direct access to the modulator output.

The ADS1278QML-SP is configured by simply setting the appropriate I/O pins—there are no registers to program. Data are retrieved over a serial interface that supports both SPI and Frame-Sync formats. The ADS1278QML-SP has a daisy-chainable output and the ability to synchronize externally, so the device can be used conveniently in systems requiring more than eight channels.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Sampling Aperture Matching

The ADS1278QML-SP converter operates from the same CLK input. The CLK input controls the timing of the modulator sampling instant. The converter is designed such that the sampling skew, or modulator sampling aperture match between channels, is controlled. Furthermore, the digital filters are synchronized to start the convolution phase at the same modulator clock cycle. This design results in excellent phase match among the ADS1278QML-SP channels.

Figure 5-37 shows the inter-device channel sample matching for the ADS1278QML-SP.

6.3.2 Frequency Response

The digital filter sets the overall frequency response. The filter uses a multi-stage FIR topology to provide linear phase with minimal passband ripple and high stop band attenuation. The filter coefficients are identical to the coefficients used in the ADS1271. The oversampling ratio of the digital filter (that is, the ratio of the modulator sampling to the output data rate, or f_{MOD}/f_{DATA}) is a function of the selected mode, as shown in Table 6-1.

Table 6-1. Oversampling Ratio vs Mode

MODE SELECTION	OVERSAMPLING RATIO (f_{MOD}/f_{DATA})
High-Speed	64
High-Resolution	128
Low-Power	64
Low-Speed	64

6.3.2.1 High-Speed, Low-Power, And Low-Speed Modes

The digital filter configuration is the same in High-Speed, Low-Power, and Low-Speed modes with the oversampling ratio set to 64. Figure 6-1 shows the frequency response in High-Speed, Low-Power, and Low-Speed modes normalized to f_{DATA}. Figure 6-2 shows the passband ripple. The transition from passband to stop band is shown in Figure 6-3. The overall frequency response repeats at 64x multiples of the modulator frequency f_{MOD}, as shown in Figure 6-4.

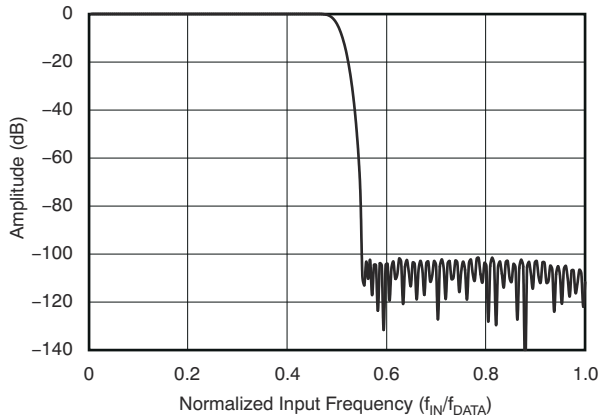


Figure 6-1. Frequency Response For High-Speed, Low-Power, And Low-Speed Modes

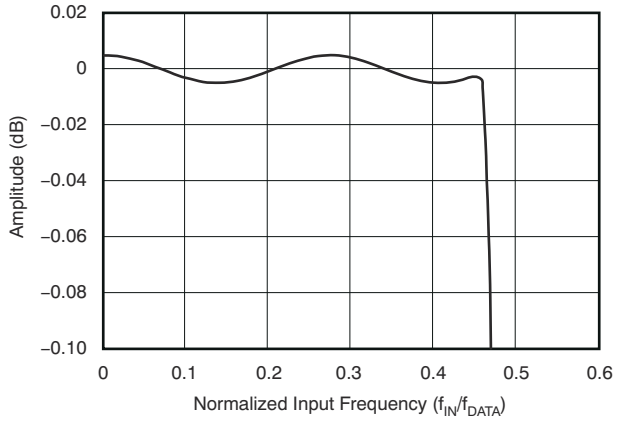


Figure 6-2. Passband Response For High-Speed, Low-Power, And Low-Speed Modes

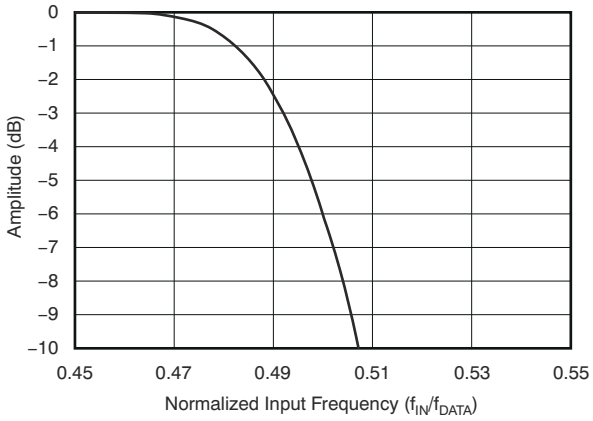


Figure 6-3. Transition Band Response For High-Speed, Low-Power, and Low-Speed Modes

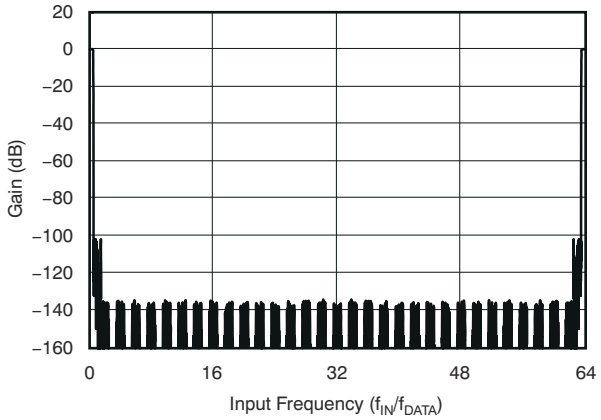


Figure 6-4. Frequency Response Out To F_{MOD} For High-Speed, Low-Power, And Low-Speed Modes

These image frequencies, if present in the signal and not externally filtered, folds back (or alias) into the passband, causing errors. The stop band of the ADS1278QML-SP provides 100dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an anti-aliasing, low-pass filter in front of the ADS1278QML-SP inputs is recommended to limit possible high-amplitude, out-of-band signals and noise. Often, a simple RC filter is sufficient. Table 6-2 lists the image rejection versus external filter order.

Table 6-2. Antialiasing Filter Order Image Rejection

ANTIALIASING FILTER ORDER	IMAGE REJECTION (dB) (f_{-3dB} at f_{DATA})	
	HS, LP, LS	HR
1	39	45
2	75	87
3	111	129

6.3.2.2 High-Resolution Mode

The oversampling ratio is 128 in High-Resolution mode. Figure 6-5 shows the frequency response in High-Resolution mode normalized to f_{DATA}. Figure 6-6 shows the passband ripple, and the transition from passband to stop band is shown in Figure 6-7. The overall frequency response repeats at multiples of the modulator frequency f_{MOD} (128 × f_{DATA}), as shown in Figure 6-8. The stop band of the ADS1278QML-SP provides 100dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1278QML-SP inputs is recommended to limit possible high-amplitude out-of-band signals and noise. Often, a simple RC filter is sufficient. Table 6-2 lists the image rejection versus external filter order.

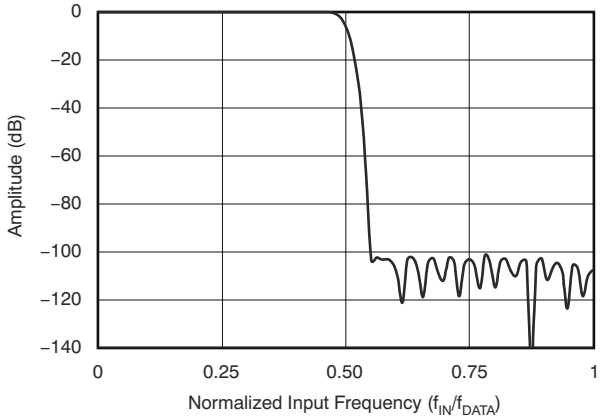


Figure 6-5. Frequency Response For High-Resolution Mode

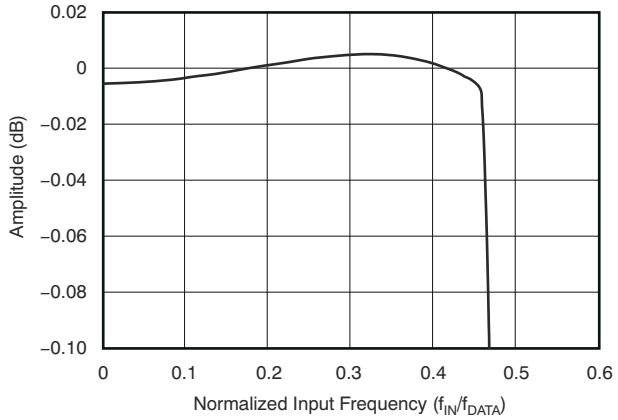


Figure 6-6. Passband Response For High-Resolution Mode

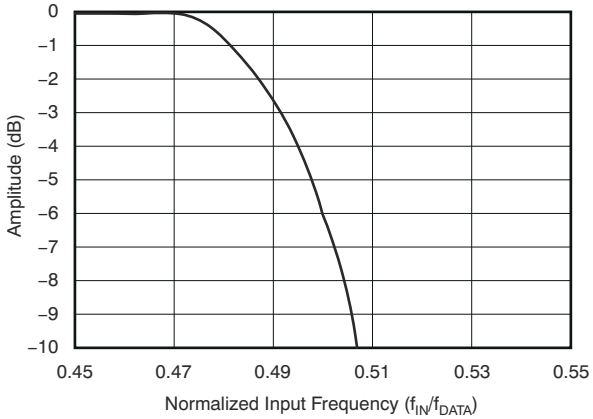


Figure 6-7. Transition Band Response For High-Resolution Mode

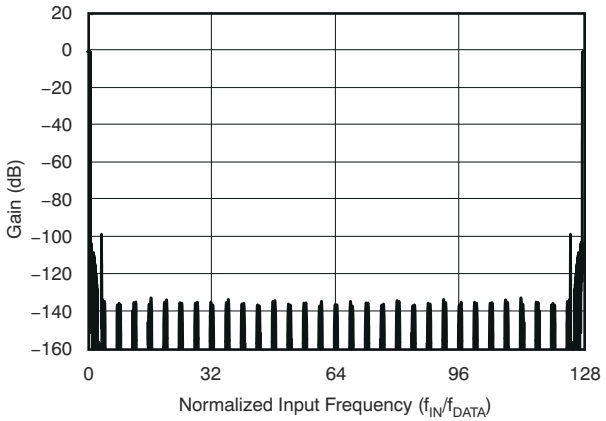


Figure 6-8. Frequency Response Out To F_{MOD} For High-Resolution Mode

6.3.3 Phase Response

The ADS1278QML-SP incorporates a multiple stage, linear phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (constant group delay). This characteristic means the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of input signal frequency. This behavior results in essentially zero phase errors when analyzing multi-tone signals.

6.3.4 Settling Time

As with frequency and phase response, the digital filter also determines settling time. Figure 6-9 shows the output settling behavior after a step change on the analog inputs normalized to conversion periods. The X-axis is given in units of conversion. Note that after the step change on the input occurs, the output data change very little prior to 30 conversion periods. The output data are fully settled after 76 conversion periods for High-Speed and Low-Power modes, and 78 conversion periods for High-Resolution mode.

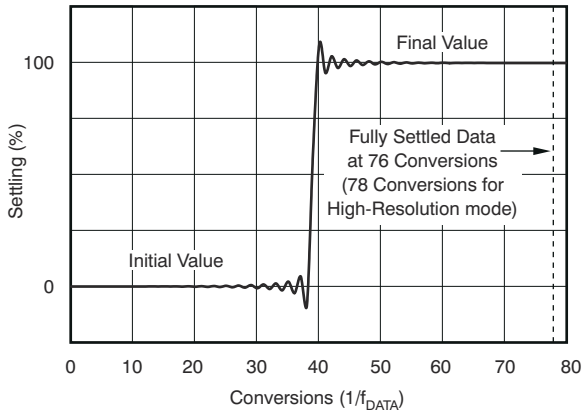


Figure 6-9. Step Response

6.3.5 Data Format

The ADS1278QML-SP outputs 24 bits of data in twos complement format.

A positive full-scale input produces an ideal output code of 7FFFFFh, and the negative full-scale input produces an ideal output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 6-3 summarizes the ideal output codes for different input signals.

Table 6-3. Ideal Output Code Versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ $+V_{REF}$	7FFFFFh
$\frac{+ V_{REF}}{2^{23} - 1}$	000001h
0	000000h
$\frac{- V_{REF}}{2^{23} - 1}$	FFFFFFh
$\leq -V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

6.3.6 Analog Inputs (AINP, AINN)

The ADS1278QML-SP measures each differential input signal V_{IN} = (AINP – AINN) against the common differential reference V_{REF} = (VREFP – VREFN). The most positive measurable differential input is $+V_{REF}$, which produces the most positive digital output code of 7FFFFFh. Likewise, the most negative measurable differential input is $–V_{REF}$, which produces the most negative digital output code of 800000h.

For optimum performance, the inputs of the ADS1278QML-SP are intended to be driven differentially. For single-ended applications, one of the inputs (AINP or AINN) can be driven while the other input is fixed (typically to AGND or 2.5V). Fixing the input to 2.5V permits bipolar operation, thereby allowing full use of the entire converter range.

While the ADS1278QML-SP measures the differential input signal, the absolute input voltage is also important. This value is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

–0.1V < (AINN or AINP) < AVDD + 0.1V

If either input is taken below –0.4V or above (AVDD + 0.4V), ESD protection diodes on the inputs can turn on. If these conditions are possible, external Schottky clamp diodes or series resistors can be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

The ADS1278QML-SP is a very high-performance ADC. For optimum performance, the appropriate circuitry must be used to drive the ADS1278QML-SP inputs. See the *Application Information* section for several recommended circuits.

The ADS1278QML-SP uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged. Figure 6-10 shows a conceptual diagram of these circuits. Switch S_2 represents the net effect of the modulator circuitry in discharging the sampling capacitor; the actual implementation is different. The timing for switches S_1 and S_2 is shown in Figure 6-11. The sampling time (t_{SAMPLE}) is the inverse of modulator sampling frequency (f_{MOD}) and is a function of the mode, the CLKDIV input, and CLK frequency, as shown in Table 6-4.

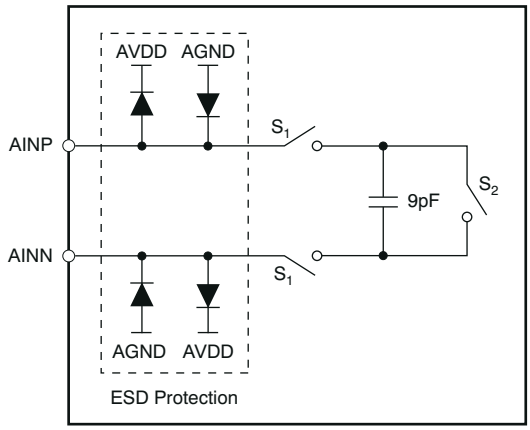


Figure 6-10. Equivalent Analog Input Circuitry

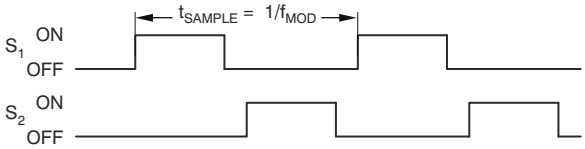


Figure 6-11. S_1 and S_2 Switch Timing for Figure 6-10

Table 6-4. Modulator Frequency (F_{MOD}) Mode Selection

MODE SELECTION	CLKDIV	f_{MOD}
High-Speed	1	f_{CLK} / 4
High-Resolution	1	f_{CLK} / 4
Low-Power	1	f_{CLK} / 8
	0	f_{CLK} / 4
Low-Speed	1	f_{CLK} / 40
	0	f_{CLK} / 8

The average load presented by the switched capacitor input can be modeled with an effective differential impedance, as shown in Figure 6-12. Note that the effective impedance is a function of f_{MOD}.

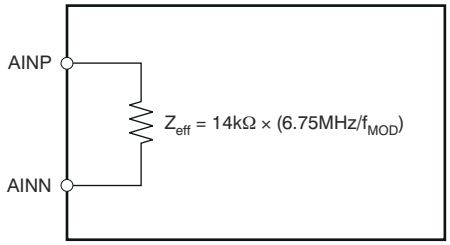


Figure 6-12. Effective Input Impedances

6.3.7 Voltage Reference Inputs (VREFP, VREFN)

The voltage reference for the ADS1278QML-SP ADC is the differential voltage between VREFP and VREFN: V_{REF} = (VREFP – VREFN). The voltage reference is common to all channels. The reference inputs use a structure similar to that of the analog inputs with the equivalent circuitry on the reference inputs shown in Figure 6-13. As with the analog inputs, the load presented by the switched capacitor can be modeled with an effective impedance, as shown in Figure 6-14. However, the reference input impedance depends on the number of active (enabled) channels in addition to f_{MOD}. As a result of the change of reference input impedance caused by enabling and disabling channels, the regulation and setting time of the external reference must be noted, so as not to affect the readings.

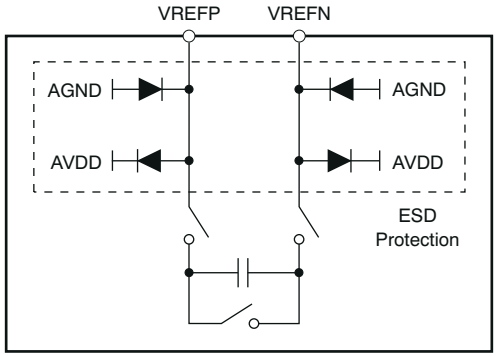
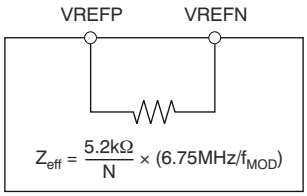


Figure 6-13. Equivalent Reference Input Circuitry



N = number of active channels.

Figure 6-14. Effective Reference Impedance

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 0.4V, and likewise do not exceed AVDD by 0.4V. If these conditions are possible, external Schottky clamp diodes or series resistors can be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Note that the valid operating range of the reference inputs is limited to the following parameters:

–0.1V ≤ VREFN ≤ +0.1V

VREFN + 0.5V ≤ VREFP ≤ AVDD + 0.1V

6.3.8 Clock Input (CLK)

The ADS1278QML-SP requires a clock input for operation. The individual converters of the ADS1278QML-SP operate from the same clock input. At the maximum data rate, the clock input can be either 27MHz or 13.5MHz for Low-Power mode, or 27MHz or 5.4MHz for Low-Speed mode, determined by the setting of the CLKDIV input. For High-Speed mode, the maximum CLK input frequency is 32.768MHz. For High-Resolution mode, the maximum CLK input frequency is 27MHz. The selection of the external clock frequency (f_{CLK}) does not affect the resolution of the ADS1278QML-SP. Use of a slower f_{CLK} can reduce the power consumption of an external clock buffer. The output data rate scales with clock frequency, down to a minimum clock frequency of f_{CLK} = 100kHz. Table 6-5 summarizes the ratio of the clock input frequency (f_{CLK}) to data rate (f_{DATA}), maximum data rate and corresponding maximum clock input for the four operating modes.

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keeping the clock trace as short as possible, and using a 50Ω series resistor placed close to the source end, often helps.

Table 6-5. Clock Input Options

MODE SELECTION	MAX f_{CLK} (MHz)	CLKDIV	f_{CLK}/f_{DATA}	DATA RATE (SPS)
High-Speed	32.768	1	256	128,000
High-Resolution	27	1	512	52,734
Low-Power	27	1	512	52,734
	13.5	0	256	
Low-Speed	27	1	2,560	10,547
	5.4	0	512	

6.3.9 Mode Selection (MODE)

The ADS1278QML-SP supports four modes of operation: High-Speed, High-Resolution, Low-Power, and Low-Speed. The modes offer optimization of speed, resolution, and power. Mode selection is determined by the status of the digital input MODE[1:0] pins, as shown in Table 6-6. The ADS1278QML-SP continually monitors the status of the MODE pin during operation.

Table 6-6. Mode Selection

MODE[1:0]	MODE SELECTION	MAX f_{DATA} (1)
00	High-Speed	128,000
01	High-Resolution	52,734
10	Low-Power	52,734
11	Low-Speed	10,547

(1) f_{CLK} = 27MHz max (32.768MHz max in High-Speed mode).

When using the SPI protocol, $\overline{DRDY}$ is held high after a mode change occurs until settled (or valid) data are ready; see Figure 6-15 and Table 6-7.

In Frame-Sync protocol, the DOUT pins are held low after a mode change occurs until settled data are ready; see Figure 6-15 and Table 6-7. Data can be read from the device to detect when DOUT changes to logic 1, indicating that the data are valid.

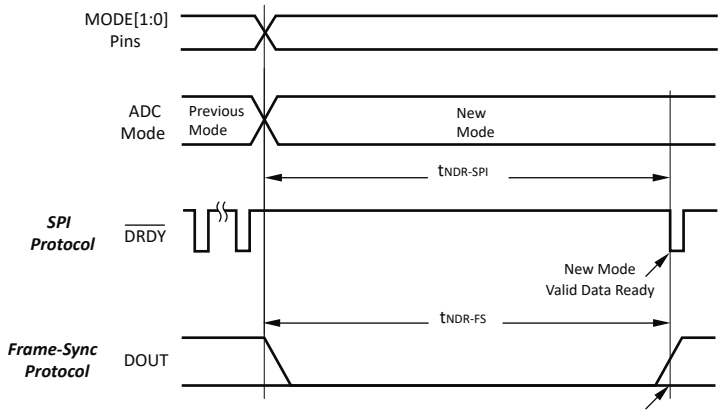


Figure 6-15. Mode Change Timing

Table 6-7. New Data After Mode Change

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{NDR-SPI}$	Time for new data to be ready (SPI)			129	Conversions ($1/f_{DATA}$)
t_{NDR-FS}	Time for new data to be ready (Frame-Sync)	127		128	Conversions ($1/f_{DATA}$)

6.3.10 Synchronization ($\overline{SYNC}$)

The ADS1278QML-SP can be synchronized by pulsing the $\overline{SYNC}$ pin low and then returning the pin high. When the pin goes low, the conversion process stops, and the internal counters used by the digital filter are reset. When the $\overline{SYNC}$ pin returns high, the conversion process restarts. Synchronization allows the conversion to be aligned with an external event, such as the changing of an external multiplexer on the analog inputs, or by a reference timing pulse.

Because the ADS1278QML-SP converters operate in parallel from the same clock input and use the same $\overline{SYNC}$ input control, the converters are always in synchronization with each other. The aperture match among internal channels is typically less than 500ps. However, the synchronization of multiple devices is somewhat different. At device power-on, variations in internal reset thresholds from device to device can result in uncertainty in conversion timing.

The $\overline{SYNC}$ pin can be used to synchronize multiple devices to within the same CLK cycle. Figure 6-16 illustrates the timing requirement of $\overline{SYNC}$ and CLK in SPI format.

See Figure 6-17 for the Frame-Sync format timing requirement.

After synchronization, indication of valid data depends on whether SPI or Frame-Sync format is used.

In the SPI format, $\overline{DRDY}$ goes high as soon as $\overline{SYNC}$ is taken low; see Figure 6-16. After $\overline{SYNC}$ is returned high, $\overline{DRDY}$ stays high while the digital filter is settling. Once valid data are ready for retrieval, $\overline{DRDY}$ goes low.

In the Frame-Sync format, DOUT goes low as soon as $\overline{SYNC}$ is taken low; see Figure 6-17. After $\overline{SYNC}$ is returned high, DOUT stays low while the digital filter is settling. Once valid data are ready for retrieval, DOUT begins to output valid data. For proper synchronization, FSYNC, SCLK, and CLK must be established before taking $\overline{SYNC}$ high, and must then remain running. If the clock inputs (CLK, FSYNC or SCLK) are subsequently interrupted or reset, re-assert the $\overline{SYNC}$ pin.

For consistent performance, re-assert $\overline{SYNC}$ after device power-on when data first appear.

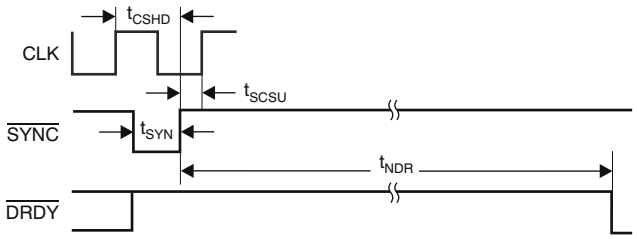


Figure 6-16. Synchronization Timing (SPI Protocol)

Table 6-8. SPI Protocol

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CSHD}	CLK to $\overline{SYNC}$ hold time	10			ns
t_{SCSU}	$\overline{SYNC}$ to CLK setup time	5			ns
t_{SYN}	Synchronize pulse width	1			CLK periods
t_{NDR}	Time for new data to be ready			129	Conversions ($1/f_{DATA}$)

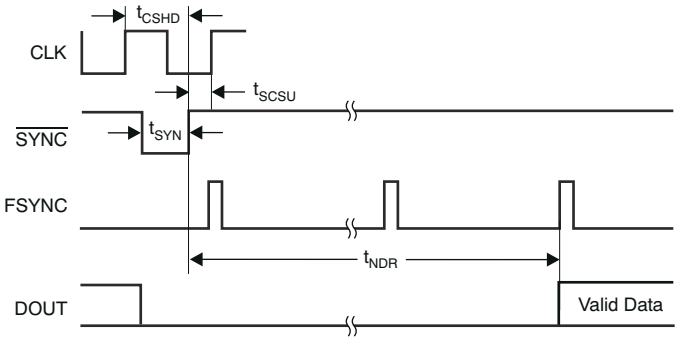


Figure 6-17. Synchronization Timing (Frame-Sync Protocol)

Table 6-9. Frame-Sync Protocol

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CSHD}	CLK to $\overline{SYNC}$ hold time	10			ns
t_{SCSU}	$\overline{SYNC}$ to CLK setup time	5			ns
t_{SYN}	Synchronize pulse width	1			CLK periods
t_{NDR}	Time for new data to be ready	127		128	Conversions ($1/f_{DATA}$)

6.3.11 Power-Down ($\overline{PWDN}$)

The channels of the ADS1278QML-SP can be independently powered down by use of the $\overline{PWDN}$ inputs. To enter the power-down mode, hold the respective $\overline{PWDN}$ pin low for at least two CLK cycles. To exit power-down, return the corresponding $\overline{PWDN}$ pin high. Note that when all channels are powered down, the ADS1278QML-SP enters a microwatt (μW) power state where all internal biasing is disabled. In this state, the TEST[1:0] input pins must be driven; all other input pins can float. The ADS1278QML-SP outputs remain driven.

As shown in Figure 6-18 and Table 6-10, a maximum of 130 conversion cycles must elapse for SPI, and 129 conversion cycles must elapse for Frame-Sync, before reading data after exiting power-down. Data from channels already running are not affected. The user software can perform the required delay time in any of the following ways:

1. Count the number of data conversions after taking the $\overline{PWDN}$ pin high.
2. Delay $129/f_{DATA}$ or $130/f_{DATA}$ after taking the $\overline{PWDN}$ pins high, then read data.
3. Detect for non-zero data in the powered-up channel.

After powering up one or more channels, the channels are synchronized to each other. The $\overline{SYNC}$ pin does not necessarily need to be used to synchronize the channels.

When a channel is powered down in TDM data format, the data for that channel are either forced to zero (fixed-position TDM data mode) or replaced by shifting the data from the next channel into the vacated data position (dynamic-position TDM data mode).

In Discrete data format, the data are always forced to zero. When powering-up a channel in dynamic-position TDM data format mode, the channel data remain packed until the data are ready, at which time the data frame is expanded to include the just-powered channel data. See the *Data Format* section for details.

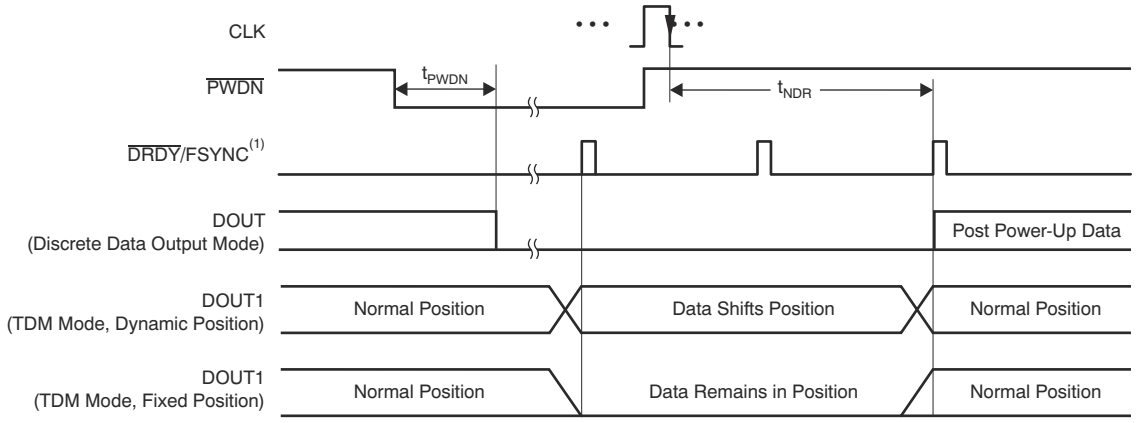


Figure 6-18. Power-Down Timing

Table 6-10. Power-Down Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PWDN}	$\overline{PWDN}$ pulse width to enter Power-Down mode	2			CLK periods
t_{NDR}	Time for new data ready (SPI)	129		130	Conversions ($1/f_{DATA}$)
t_{NDR}	Time for new data ready (Frame-Sync)	128		129	Conversions ($1/f_{DATA}$)

6.3.12 Format[2:0]

Data can be read from the ADS1278QML-SP with two interface protocols (SPI or Frame-Sync) and several options of data formats (TDM/Discrete and Fixed/Dynamic data positions). The FORMAT[2:0] inputs are used to select among the options. Table 6-11 lists the available options. See the *DOUT Modes* section for details of the DOUT Mode and Data Position.

Table 6-11. Data Output Format

FORMAT[2:0]	INTERFACE PROTOCOL	DOUT MODE	DATA POSITION
000	SPI	TDM	Dynamic
001	SPI	TDM	Fixed
010	SPI	Discrete	—
011	Frame-Sync	TDM	Dynamic
100	Frame-Sync	TDM	Fixed
101	Frame-Sync	Discrete	—
110	Modulator Mode	—	—

6.3.13 Serial Interface Protocols

Data are retrieved from the ADS1278QML-SP using the serial interface. Two protocols are available: SPI and Frame-Sync. The same pins are used for both interfaces: SCLK, $\overline{DRDY}$/FSYNC, DOUT[8:1], and DIN. The FORMAT[2:0] pins select the desired interface protocol.

6.3.14 SPI Serial Interface

The SPI-compatible format is a read-only interface. Data ready for retrieval are indicated by the falling $\overline{\text{DRDY}}$ output and are shifted out on the falling edge of SCLK, MSB first. The interface can be daisy-chained using the DIN input when using multiple devices. See the *Daisy-Chaining* section for more information.

Note

NOTE: The SPI format is limited to a CLK input frequency of 27MHz, maximum. For CLK input operation above 27MHz (High-Speed mode only), use Frame-Sync format.

6.3.14.1 SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. SCLK also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. The device shifts data out on the falling edge and the user typically shifts this data in on the rising edge.

Even though the SCLK input has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data.

SCLK can be run as fast as the CLK frequency. SCLK can be either in free-running or stop-clock operation between conversions. Note that one f_{CLK} is required after the falling edge of $\overline{\text{DRDY}}$ until the first rising edge of SCLK. For best performance, limit f_{SCLK} / f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, and more. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

6.3.14.2 $\overline{\text{DRDY}}$/FSYNC (SPI Format)

In the SPI format, this pin functions as the $\overline{\text{DRDY}}$ output. The pin goes low when data are ready for retrieval and then returns high on the falling edge of the first subsequent SCLK. If data are not retrieved (that is, SCLK is held low), $\overline{\text{DRDY}}$ pulses high just before the next conversion data are ready, as shown in Figure 6-19. The new data are loaded within one CLK cycle before $\overline{\text{DRDY}}$ goes low. All data must be shifted out before this time to avoid being overwritten.

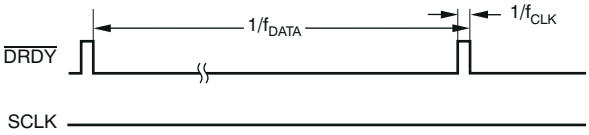


Figure 6-19. $\overline{\text{DRDY}}$ Timing With No Readback

6.3.14.3 DOUT

The conversion data are output on DOUT[8:1]. The MSB data are valid on DOUT[8:1] after $\overline{\text{DRDY}}$ goes low. Subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT after all channel data have been shifted out. When the device is configured for modulator output, DOUT[8:1] becomes the modulator data output for each channel (see the *Modulator Output* section).

6.3.14.4 DIN

This input is used when multiple ADS1278QML-SPs are to be daisy-chained together. The DOUT1 pin of the first device connects to the DIN pin of the next, and more. DIN can be used with either the SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1278QML-SP, tie DIN low. See the *Daisy-Chaining* section for more information.

6.3.15 Frame-Sync Serial Interface

Frame-Sync format is similar to the interface often used on audio ADCs. The Frame-Sync operates in target fashion—the user must supply framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data are output MSB first or *left-justified* on the rising edge of FSYNC. When using Frame-Sync format, the FSYNC and SCLK inputs must be continuously running with the relationships shown in the *Timing Requirements: Frame-Sync Format* table.

6.3.15.1 SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. SCLK also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. Even though SCLK has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When using Frame-Sync format, SCLK must run continuously. If SCLK is shut down, the data readback can be corrupted. The number of SCLKs within a frame period (FSYNC clock) can be any power-of-2 ratio of CLK cycles (1, 1/2, 1/4, and more), as long as the number of cycles is sufficient to shift the data output from all channels within one frame. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

6.3.15.2 $\overline{\text{DRDY}}$/FSYNC (Frame-Sync Format)

In Frame-Sync format, this pin is used as the FSYNC input. The frame-sync input (FSYNC) sets the frame period, which must be the same as the data rate. The required number of f_{CLK} cycles to each FSYNC period depends on the mode selection and the CLKDIV input. Table 6-5 indicates the number of CLK cycles to each frame (f_{CLK}/f_{DATA}). If the FSYNC period is not the proper value, data readback can be corrupted.

6.3.15.3 DOUT

The conversion data are shifted out on DOUT[8:1]. The MSB data become valid on DOUT[8:1] after FSYNC goes high. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT[8:1] after all channel data have been shifted out. When the device is configured for modulator output, DOUT becomes the modulator data output (see the *Modulator Output* section).

6.3.15.4 DIN

This input is used when multiple ADS1278QML-SPs are to be daisy-chained together. DIN can be used with either SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1278QML-SP, tie DIN low. See the *Daisy-Chaining* section for more information.

6.3.16 DOUT Modes

For both SPI and Frame-Sync interface protocols, the data are shifted out either through individual channel DOUT pins, in a parallel data format (Discrete mode), or the data for all channels are shifted out, in a serial format, through a common pin, DOUT1 (TDM mode).

6.3.16.1 TDM Mode

In TDM (time-division multiplexed) data output mode, the data for all channels are shifted out, in sequence, on a single pin (DOUT1). As shown in Figure 6-20, the data from channel 1 are shifted out first, followed by channel 2 data, and more. After the data from the last channel are shifted out, the data from the DIN input follow. The DIN is used to daisy-chain the data output from an additional ADS1278QML-SP or other compatible device. Note that when all channels of the ADS1278QML-SP are disabled, the interface is disabled, rendering the DIN input disabled as well. When one or more channels of the device are powered down, the data format of the TDM mode can be fixed or dynamic.

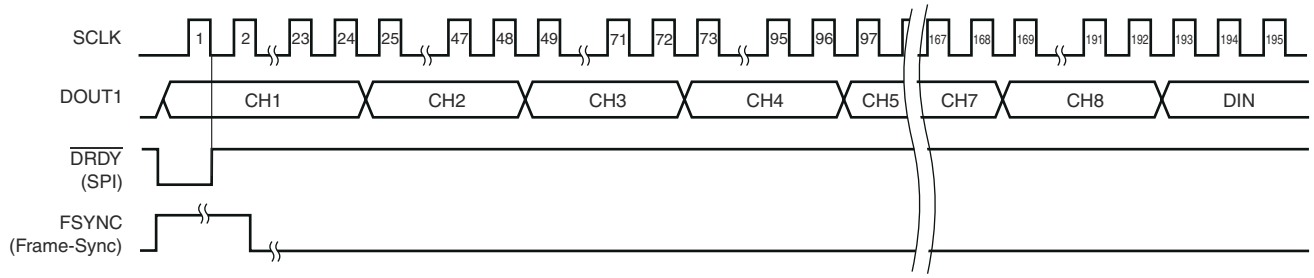


Figure 6-20. TDM Mode (All Channels Enabled)

6.3.16.2 TDM Mode, Fixed-Position Data

In this TDM data output mode, the data position of the channels remain fixed, regardless of whether the channels are powered down. If a channel is powered down, the data are forced to zero but occupy the same position within the data stream. Figure 6-21 shows the data stream with channel 1 and channel 3 powered down.

6.3.16.3 TDM Mode, Dynamic Position Data

In this TDM data output mode, when a channel is powered down, the data from higher channels shift one position in the data stream to fill the vacated data slot. Figure 6-22 shows the data stream with channel 1 and channel 3 powered down.

6.3.16.4 Discrete Data Output Mode

In Discrete data output mode, the channel data are shifted out in parallel using individual channel data output pins DOUT[8:1]. After the 24th SCLK, the channel data are forced to zero. The data are also forced to zero for powered down channels. Figure 6-23 shows the discrete data output format.

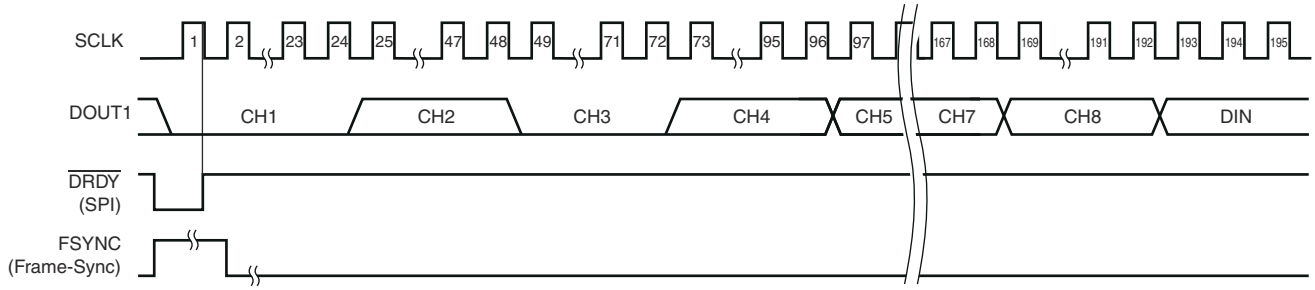


Figure 6-21. TDM Mode, Fixed-Position Data (Channels 1 And 3 Shown Powered Down)

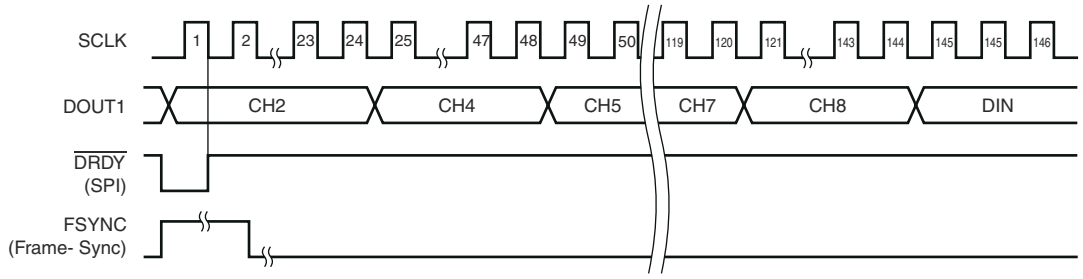


Figure 6-22. TDM Mode, Dynamic Position Data (Channels 1 And 3 Shown Powered Down)

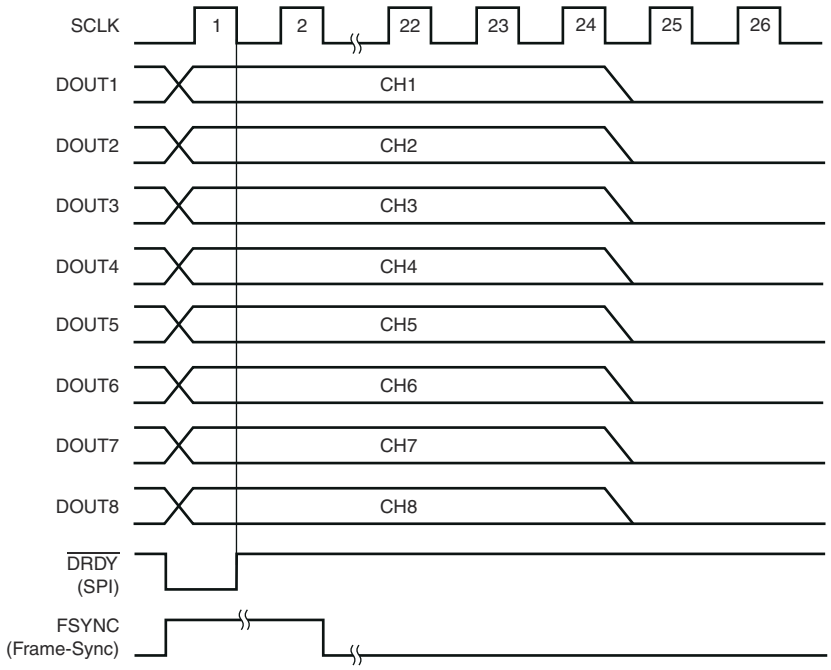


Figure 6-23. Discrete Data Output Mode

6.3.17 Daisy-Chaining

Multiple ADS1278QML-SPs can be daisy-chained together to output data on a single pin. The DOUT1 data output pin of one device is connected to the DIN of the next device. As shown in Figure 6-24, the DOUT1 pin of device 1 provides the output data to a controller, and the DIN of device 2 is grounded. Figure 6-25 shows the data format when reading back data.

The maximum number of channels that can be daisy-chained in this way is limited by the frequency of f_{SCLK}, the mode selection, and the CLKDIV input. The frequency of f_{SCLK} must be high enough to completely shift the data out from all channels within one f_{DATA} period. Table 6-12 lists the maximum number of daisy-chained channels when $f_{SCLK} = f_{CLK}$.

To increase the number of data channels possible in a chain, a segmented DOUT scheme can be used, producing two data streams. Figure 6-26 illustrates four ADS1278QML-SPs, with pairs of ADS1278QML-SPs daisy-chained together. The channel data of each daisy-chained pair are shifted out in parallel and received by the processor through independent data channels.

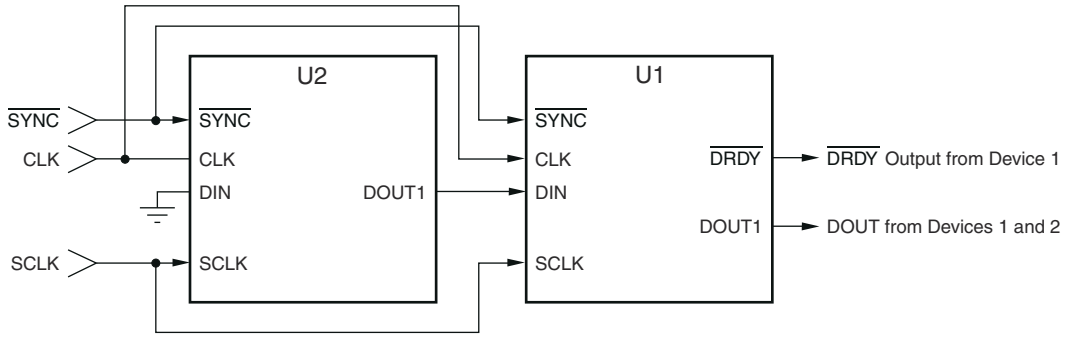
Table 6-12. Maximum Channels In A Daisy-Chain ($F_{SCLK} = F_{CLK}$)

MODE SELECTION	CLKDIV	MAXIMUM NUMBER OF CHANNELS
High-Speed	1	10
High-Resolution	1	21
Low-Power	1	21
	0	10
Low-Speed	1	106
	0	21

Whether the interface protocol is SPI or Frame-Sync, synchronize all devices by tying the $\overline{SYNC}$ inputs together. When synchronized in SPI protocol, monitor only the $\overline{DRDY}$ output of one ADS1278QML-SP.

In Frame-Sync interface protocol, the data from all devices are ready after the rising edge of FSYNC.

Since DOUT1 and DIN are both shifted on the falling edge of SCLK, the propagation delay on DOUT1 creates a setup time on DIN. Minimize the skew in SCLK to avoid timing violations.



The number of chained devices is limited by the SCLK rate and device mode.

Figure 6-24. Daisy-Chaining of Two Devices, SPI Protocol (Format[2:0] = 000 or 001)

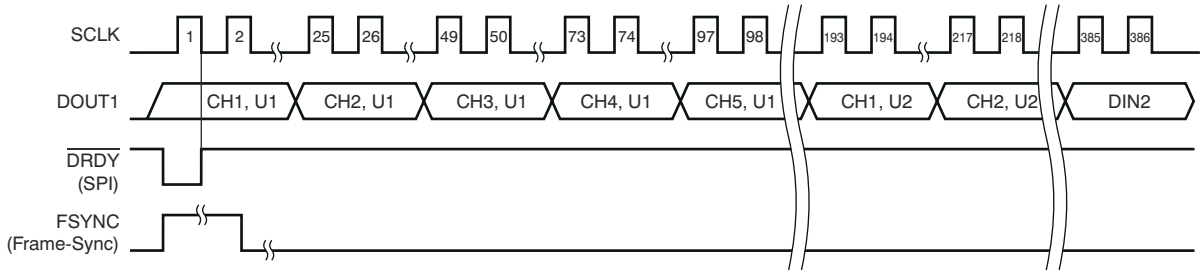
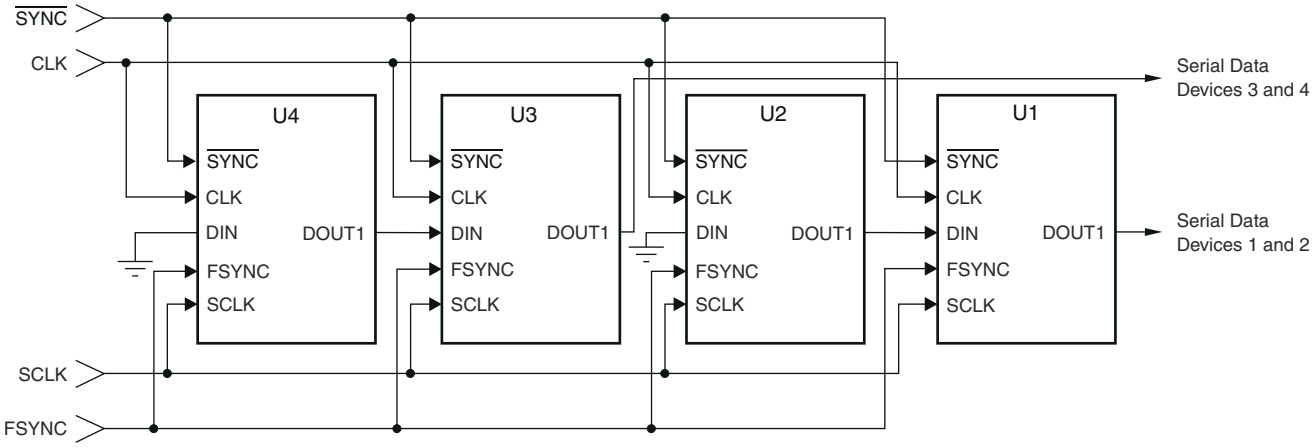


Figure 6-25. Daisy-Chain Data Format of Figure 6-24



The number of chained devices is limited by the SCLK rate and device mode.

Figure 6-26. Segmented DOUT Daisy-Chain, Frame-Sync Protocol (Format[2:0] = 011 or 100)

6.3.18 Modulator Output

The ADS1278QML-SP incorporates a 6th-order, single-bit, chopper-stabilized modulator followed by a multi-stage digital filter that yields the conversion results. The data stream output of the modulator is available directly, bypassing the internal digital filter. The digital filter is disabled, reducing the DVDD current, as shown in Table 6-13. In this mode, an external digital filter implemented in an ASIC, FPGA, or similar device is required. To invoke the modulator output, tie FORMAT[2:0], as shown in Figure 6-27. DOUT[8:1] then becomes the modulator data stream outputs for each channel and SCLK becomes the modulator clock output. The $\overline{\text{DRDY}}$/FSYNC pin becomes an unused output and can be ignored. The normal operation of the Frame-Sync and SPI is disabled, and the functionality of SCLK changes from an input to an output, as shown in Figure 6-27.

Table 6-13. Modulator Output Clock Frequencies

MODE [1:0]	CLKDIV	MODULATOR CLOCK OUTPUT (SCLK)	DVDD (mA)
00	1	f_{CLK} / 4	8
01	1	f_{CLK} / 4	7
10	1	f_{CLK} / 8	4
	0	f_{CLK} / 4	4
11	1	f_{CLK} / 40	1
	0	f_{CLK} / 8	1

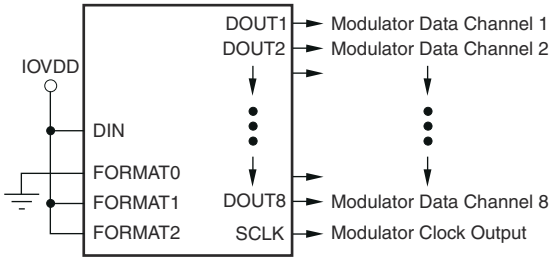


Figure 6-27. Modulator Output

In modulator output mode, the frequency of the modulator clock output (SCLK) depends on the mode selection of the ADS1278QML-SP. Table 6-13 lists the modulator clock output frequency and DVDD current versus device mode.

Figure 6-28 shows the timing relationship of the modulator clock and data outputs.

The data output is a modulated 1s density data stream. When V_{IN} = +V_{REF}, the 1s density is approximately 80% and when V_{IN} = –V_{REF}, the 1s density is approximately 20%.

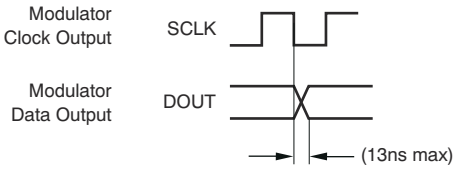


Figure 6-28. Modulator Output Timing

6.3.19 Pin Test Using Test[1:0] Inputs

The test mode feature of the ADS1278QML-SP allows continuity testing of the digital I/O pins. In this mode, the normal functions of the digital pins are disabled and routed to each other as pairs through internal logic, as shown in Table 6-14. The pins in the left column drive the output pins in the right column. **Note:** some of the digital input pins become outputs; these outputs must be accommodated in the design. The analog input, power supply, and ground pins all remain connected as normal. The test mode is engaged by setting the pins TEST [1:0] = 11. For normal converter operation, set TEST[1:0] = 00. Do not use '01' or '10'.

Table 6-14. Test Mode Pin Map (Test[1:0] = 11)

TEST MODE PIN MAP	
INPUT PINS	OUTPUT PINS
$\overline{\text{PWDN}}$1	DOUT1
$\overline{\text{PWDN}}$2	DOUT2
$\overline{\text{PWDN}}$3	DOUT3
$\overline{\text{PWDN}}$4	DOUT4
$\overline{\text{PWDN}}$5	DOUT5
$\overline{\text{PWDN}}$6	DOUT6

Table 6-14. Test Mode Pin Map (Test[1:0] = 11) (continued)

TEST MODE PIN MAP	
INPUT PINS	**OUTPUT PINS**
$\overline{\text{PWDN}}$7	DOUT7
$\overline{\text{PWDN}}$8	DOUT8
MODE0	DIN
MODE1	$\overline{\text{SYNC}}$
FORMAT0	CLKDIV
FORMAT1	FSYNC/ $\overline{\text{DRDY}}$
FORMAT2	SCLK

6.3.20 VCOM Output

The VCOM pin provides a voltage output equal to AVDD / 2. The intended use of this output is to set the output common-mode level of the analog input drivers. The drive capability of the output is limited; therefore, the output must only be used to drive high-impedance nodes (> 1MΩ). In some cases, an external buffer can be necessary. A 0.1µF bypass capacitor is recommended to reduce noise pickup.

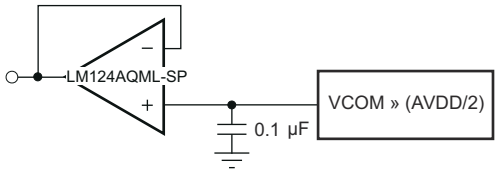


Figure 6-29. VCOM Output

6.4 Device Functional Modes

Table 6-15. Operating Mode Performance Summary

MODE	MAX DATA RATE (SPS)	PASSBAND (kHz)	SNR (dB)	NOISE (μV_{RMS})	POWER/CHANNEL (mW)
High-Speed	128,000	57,984	106	8.5	70
High-Resolution	52,734	23,889	110	5.5	64
Low-Power	52,734	23,889	106	8.5	31
Low-Speed	10,547	4,798	107	8.0	7

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ADS1278QML-SP is a radiation-hardened high resolution delta-sigma ADC that is ideal for precision sensing and high accuracy instrumentation applications. With eight simultaneous sampling 24-bit ADCs integrated, the device reduces the board area needed to digitize eight analog signals.

7.2 Typical Application

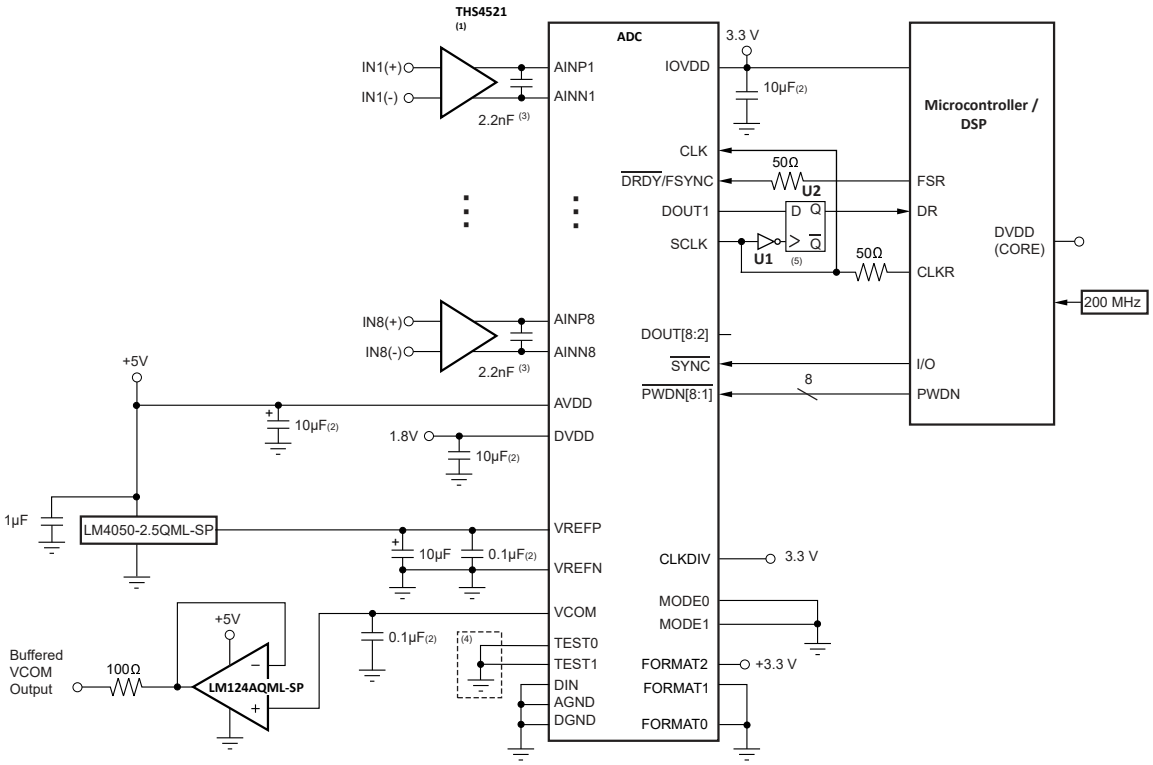


Figure 7-1. Typical Application Schematic

1. External Schottky clamp diodes or series resistors can be needed to prevent overvoltage on the inputs. Place the THS4521 drivers close to the ADC inputs.
2. Indicates ceramic capacitors.
3. Indicates COG ceramic capacitors.
4. Optional. For pin test mode.
5. U1: SN74LVC1G04; U2: SN74LVC2G74. These optional components re-clock the ADC data output to interface to the TMS320VC5509.

7.2.1 Design Requirements

Depending on the accuracy and speed requirements of the sensing application to be digitized by the ADS1278QML-SP, users must first determine the optimal device configuration. Table 7-1 shows the possible configurations for device for the maximum fCLKIN for each configuration. The first four columns indicate user

defined inputs (through I/O pins) to the device, while the italic row indicates the default configuration of the ADS1278EVM-CVAL EVM that is available as a reference design. As shown, a maximum data rate of 52734 SPS is possible while using the High Resolution mode, which yields a typical SNR of 111dB or an ENOB of 18 bits.

Table 7-1. ADS1278QML-SP Configuration Modes

Mode	CLKDIV	f_{CLK}/f_{MOD}	f_{CLKIN_max} (MHz)	Oversampling (f_{MOD}/f_{DATA})	f_{MOD} (MHz)	f_{DATA_max} (SPS)	f_{CLKIN}/f_{MOD}
High-Speed	1	4	32.768	64	8.192	128000	4
High-Speed	1	4	32.768	64	8.192	128000	4
High-Speed	*1*	*4*	*27*	*64*	*6.75*	*105469*	*4*
High-Resolution	1	4	27	128	6.75	52734	4
Low-Power	1	8	27	64	3.375	52734	8
Low-Power	0	4	13.5	64	3.375	52734	4
Low-Speed	1	40	27	64	0.675	10547	40
Low-Speed	0	8	5.4	64	0.675	10547	8

7.2.2 Detailed Design Procedure

To obtain the specified performance from the ADS1278QML-SP, the following layout and component guidelines must be considered.

1. **Power Supplies:** The device requires three power supplies for operation: DVDD, IOVDD, and AVDD. The allowed range for DVDD is 1.65V to 1.95V; the range of IOVDD is 1.65V to 3.6V; AVDD is restricted to 4.75V to 5V. For all supplies, use a 10µF tantalum capacitor, bypassed with a 0.1µF ceramic capacitor, placed close to the device pins. Alternatively, a single 10µF ceramic capacitor can be used. The supplies must be relatively free of noise and must not be shared with devices that produce voltage spikes (such as relays, LED display drivers, and more). If a switching power-supply source is used, the voltage ripple must be low (less than 2mV) and the switching frequency outside the passband of the converter.
2. **Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.
3. **Digital Inputs:** Source-terminate the digital inputs to the device with 50Ω series resistors. The resistors must be placed close to the driving end of digital source (oscillator, logic gates, DSP, and more) This placement helps to reduce ringing on the digital lines (ringing can lead to degraded ADC performance).
4. **Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.
5. **Reference Inputs:** Use a minimum 10µF tantalum with a 0.1µF ceramic capacitor directly across the reference inputs, VREFP and VREFN. The reference input must be driven by a low-impedance source. For best performance, the reference must have less than $3\mu V_{RMS}$ in-band noise. For references with noise higher than this level, external reference filtering can be necessary.
6. **Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks. A 1nF to 10nF capacitor must be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) must be used to maintain low THD. Capacitors from each analog input to ground can be used. The capacitors must be no larger than 1/10 the size of the difference capacitor (typically 100pF) to preserve the ac common-mode performance.
7. **Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This layout is particularly important for small-value ceramic capacitors. Larger (bulk) decoupling capacitors can be located farther from the device than the smaller ceramic capacitors.

7.2.3 Application Curve

Figure 7-2 illustrates how the noise of the device, and thus, the SNR, is determined by the mode that is utilized.

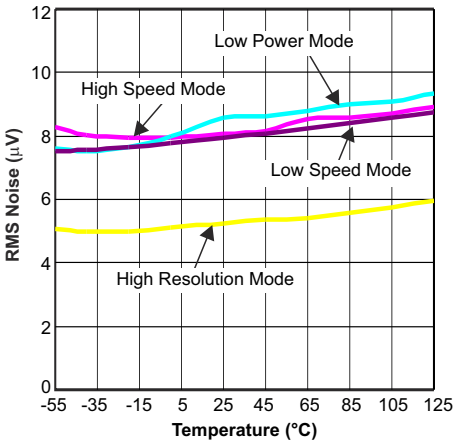


Figure 7-2. Noise vs Temperature

7.3 Power Supply Recommendations

The ADS1278QML-SP has three power supplies: AVDD, DVDD, and IOVDD. AVDD is the analog supply that powers the modulator, DVDD is the digital supply that powers the digital core, and IOVDD is the digital I/O power supply. The IOVDD and DVDD power supplies can be tied together if desired (1.8V). To achieve rated performance, the power supplies must be bypassed with 0.1µF and 10µF capacitors placed as close as possible to the supply pins. A single 10µF ceramic capacitor can be substituted in place of the two capacitors.

Figure 7-3 shows the start-up sequence of the ADS1278QML-SP. At power-on, bring up the DVDD supply first, followed by IOVDD and then AVDD. Check the power-supply sequence for proper order, including the ramp rate of each supply. DVDD and IOVDD can be sequenced at the same time if the supplies are tied together. Each supply has an internal reset circuit whose outputs are summed together to generate a global power-on reset. After the supplies have exceeded the reset thresholds, 2^{18} f_{CLK} cycles are counted before the converter initiates the conversion process. Following the CLK cycles, the data for 129 conversions are suppressed by the ADS1278QML-SP to allow output of fully-settled data. In SPI protocol, $\overline{DRDY}$ is held high during this interval. In frame-sync protocol, DOUT is forced to zero. The power supplies must be applied before any analog or digital pin is driven. For consistent performance, assert $\overline{SYNC}$ after device power-on when data first appear.

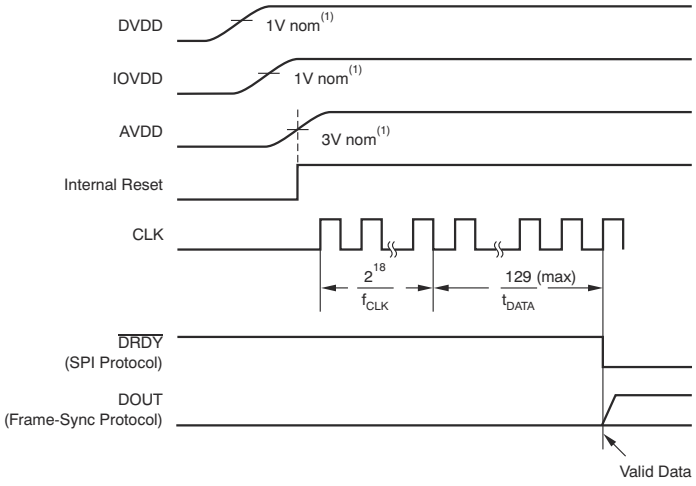


Figure 7-3. Start-Up Sequence

7.4 Layout

7.4.1 Layout Guidelines

In any mixed-signal system design, the power-supply and grounding design plays a significant role. The device distinguishes between two different grounds: AVSS (analog ground) and DGND (digital ground). In low frequency applications such as temperature sensing with thermocouples, laying out the printed circuit board (PCB) to use a single ground plane is adequate but care must be taken so that ground loops are avoided. Ground loops act as loop antennas picking up interference currents which transform into voltage fluctuations. These fluctuations are effectively noise which can degrade system performance in high resolution applications. When placing components and routing over the ground plane, pay close attention to the path that ground currents take. Avoid having return currents for digital functions pass close to analog sensitive devices or traces.

Additionally, the proximity of digital devices to an analog signal chain has the potential to induce unwanted noise into the system. One primary source of noise is the switching noise from any digital circuitry such as the data output serializer or the microprocessor receiving the data. For the device, care must be taken to verify that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductances of the supply and ground pins results in better noise suppression. For this reason, multiple pins are used to connect to the digital ground. Low inductance properties must be maintained throughout the design of the PCB layout by use of proper planes and layer thickness.

To avoid noise coupling through supply pins, TI recommends to keep sensitive input pins away from the DVDD and DGND planes. Do not route the traces or vias connected to these pins across these planes; that is, avoid the digital power planes under the analog input pins. Care must be taken to minimize inductance and route digital signals away from analog section.

The analog inputs represent the most sensitive node of the ADC as the total system accuracy depends on the how well the integrity of this signal is maintained. The analog differential inputs to the ADC must be routed tightly coupled and symmetrical for common mode rejection. These inputs must be as short in length as possible to minimize exposure to potential sources of noise.

7.4.2 Layout Example

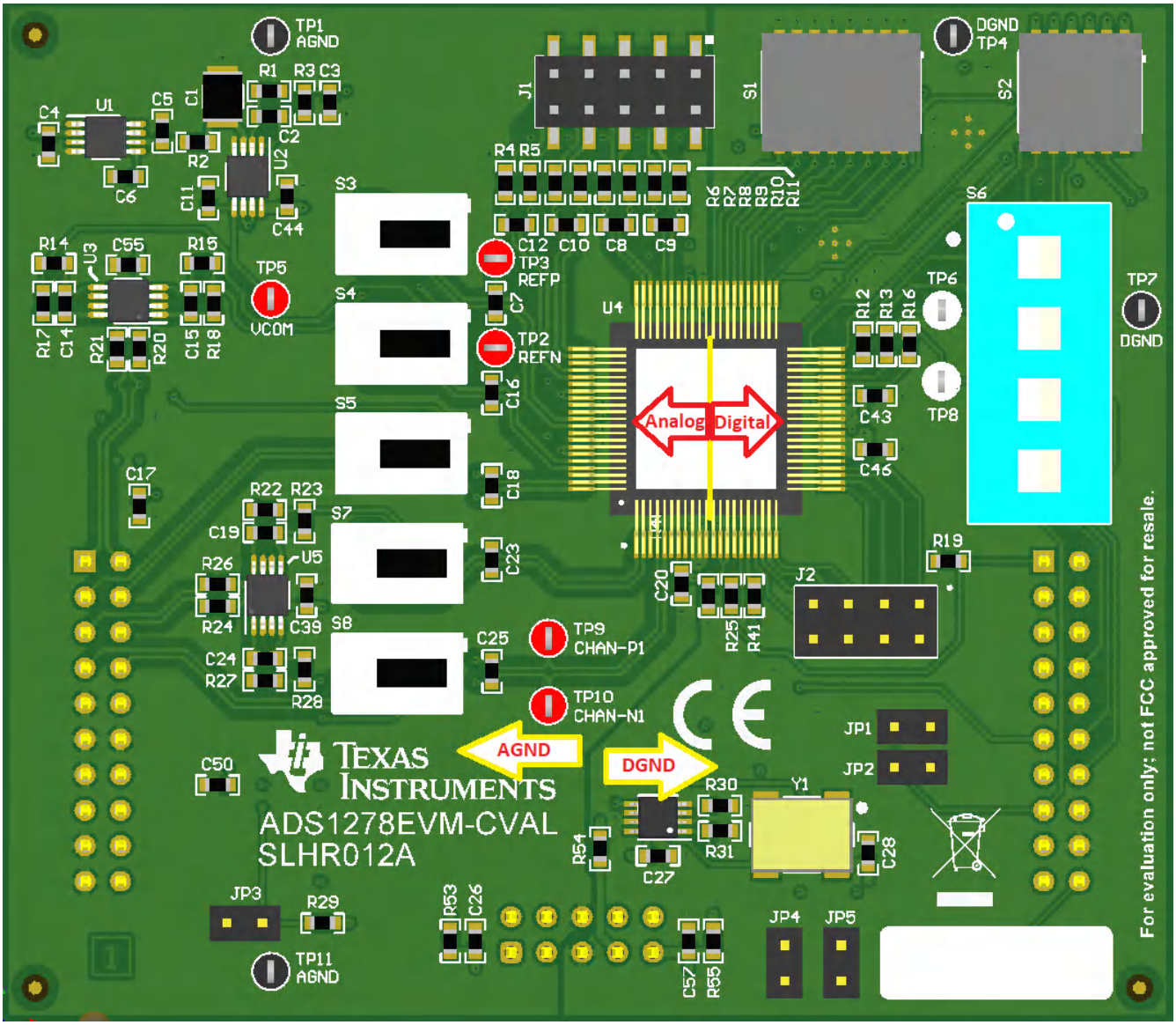


Figure 7-4. ADS1278QML-SP Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

8.3 Trademarks

SPI™ is a trademark of Motorola, Inc.
All trademarks are the property of their respective owners.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

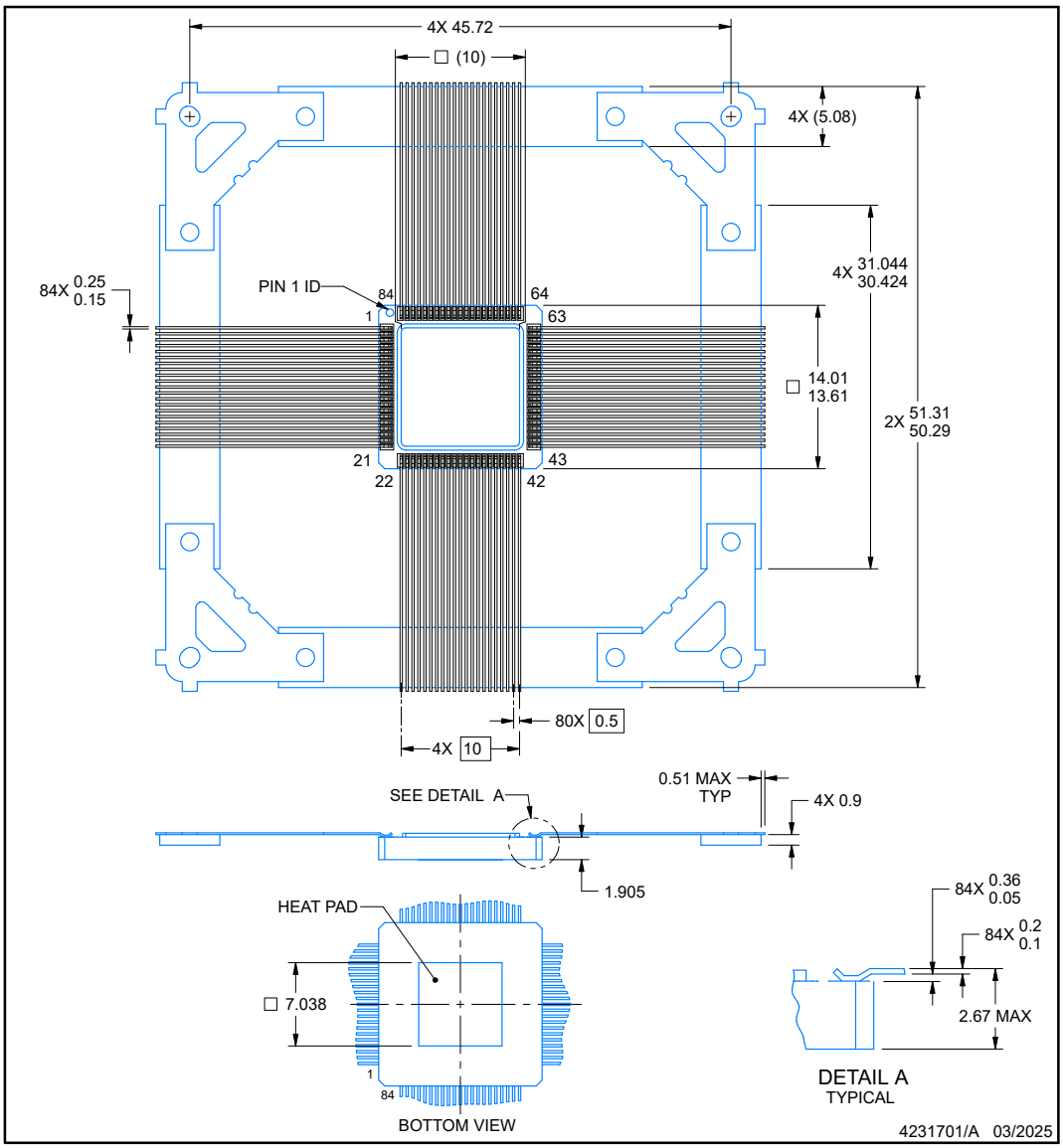
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

HFQ0084A

CFP - 2.67 mm max height

CFP



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
4. This package is hermetically sealed with a metal lid.
5. The leads are gold plated and can be solder dipped.
6. The lid and the heat sink are connected to ground leads.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962L2521001VXC	Active	Production	null (null) |	72 | SMALL T&R	ROHS Exempt	Call TI	Call TI	-55 to 125	5962L2521001VXC ADS1278-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Last updated 10/2025