

# ADC3910Dx and ADC3910Sx 10-bit, 25 to 125MSPS Low Latency, Low Power, Small, Single and Dual Channel ADC with Integrated Input Buffers

## 1 Features

- Sampling rate up to 125MSPS
- Latency: 1 clock cycle
- Low power (2 channel):
  - 92mW at 125MSPS
  - 59mW at 25MSPS
  - 4mW in PD mode
- Small footprint: 32-VQFN (4mm x 4mm)
- Single or dual channel ADC
- Dual digital comparators
- Reference: internal or external
- No missing codes,  $\pm 1$  LSB INL
- Buffered, differential or single ended inputs
- Input bandwidth: 150MHz (3-dB)
- Single 1.8V supply
  - Optional 3.3V<sub>IO</sub> capability
- Industrial temperature range: -40 to 105°C
- On-chip digital filter (optional)
  - Decimation by 2, 4, 8, 16
- Parallel (SDR, DDR) and serial CMOS interface
- Spectral performance ( $f_{IN} = 5\text{MHz}$ ):
  - SNR: 61dBFS
  - SFDR: 65dBc

## 2 Applications

- [Radio receiver](#)
- LiDAR
- Low latency control loops
- Laser scanners
- [Global positioning systems](#)
- [Source measure unit](#)
- Detection equipment

## 3 Description

The ADC3910Dx and ADC3910Sx are a family ultra-low power 10-bit 125MSPS high-speed single and dual channel analog-to-digital converters. High-speed control loops benefit from the short latency of only 1 clock cycle. The ADC consumes only 92mW at 125MSPS with a power consumption that scales with lower sampling rates.

The device uses DDR, HDDR, SDR or serial CMOS interface to output the data from +1.8V to +3.3V to accommodate various receiver requirements. The device implements analog monitoring function by event triggered interrupts per channel using a digital comparator with programmable high and low thresholds, hysteresis, and event counter. The device is a pin-to-pin compatible family of ADCs with 8 and 10-bit resolution and different speed grades. The device is available in a 32-pin VQFN package, and supports industrial temperature range from -40 to +105°C.

### Package Information

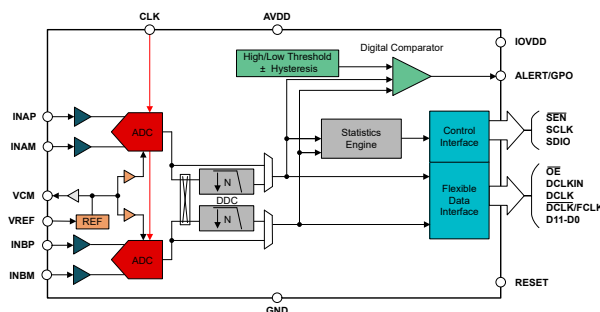
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
ADC3910D025, 'D065, 'D125 ADC3910S025, 'S065, 'S125	VQFN (32)	4mm × 4mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

### Device Information

PART NUMBER (c= #CH; sss= MSPS)	RESOLUTION	SAMPLING RATE MSPS
ADC3910csss	10-Bit	25, 65, 125
ADC3908csss	08-Bit	25, 65, 125



Block Diagram



## Table of Contents

<b>1 Features</b> .....	1	<b>6 Detailed Description</b> .....	30
<b>2 Applications</b> .....	1	6.1 Overview.....	30
<b>3 Description</b> .....	1	6.2 Functional Block Diagram.....	30
<b>4 Pin Configuration and Functions</b> .....	3	6.3 Feature Description.....	31
<b>5 Specifications</b> .....	5	6.4 Device Functional Modes.....	49
5.1 Absolute Maximum Ratings.....	5	6.5 Programming.....	50
5.2 ESD Ratings.....	5	6.6 Register Maps.....	52
5.3 Recommended Operating Conditions.....	5	<b>7 Application Information Disclaimer</b> .....	115
5.4 Thermal Information.....	5	7.1 Application Information.....	115
5.5 Electrical Characteristics - Power Consumption.....	6	7.2 Typical Application.....	115
5.6 Electrical Characteristics - DC Specifications.....	6	7.3 Initialization Set Up.....	117
5.7 Electrical Characteristics - AC Specifications (25 MSPS).....	9	7.4 Power Supply Recommendations.....	118
5.8 Electrical Characteristics - AC Specifications (65 MSPS).....	9	7.5 Layout.....	119
5.9 Electrical Characteristics - AC Specifications (125 MSPS).....	10	<b>8 Device and Documentation Support</b> .....	121
5.10 Timing Requirements.....	12	8.1 Receiving Notification of Documentation Updates..	121
5.11 Output Interface Timing Diagram.....	14	8.2 Support Resources.....	121
5.12 Typical Characteristics - 25MSPS.....	18	8.3 Trademarks.....	121
5.13 Typical Characteristics - 65MSPS.....	22	8.4 Electrostatic Discharge Caution.....	121
5.14 Typical Characteristics - 125MSPS.....	26	8.5 Glossary.....	121
		<b>9 Revision History</b> .....	121
		<b>10 Mechanical, Packaging, and Orderable Information</b> .....	122

## 4 Pin Configuration and Functions

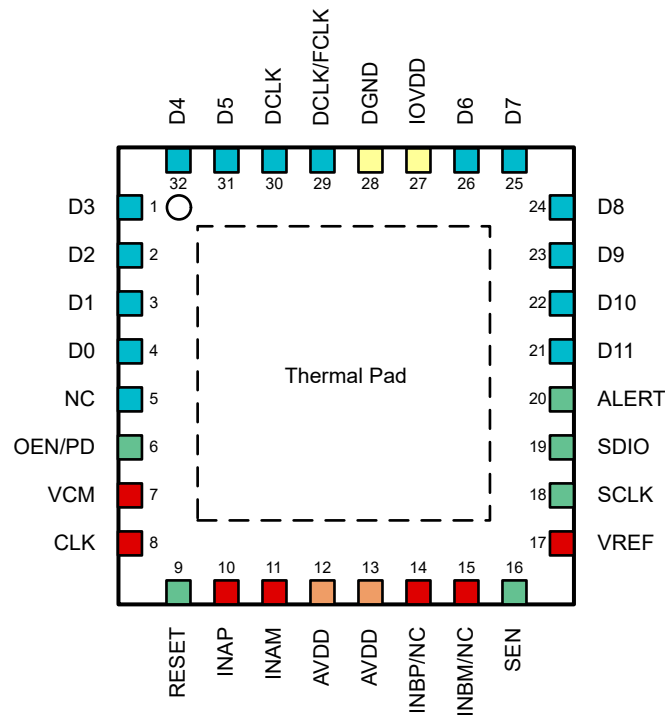


Figure 4-1. RSM (VQFN) Package, 32-Pin (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
<b>INPUT or REFERENCE</b>			
INAP	10	I	Positive analog input, channel A
INAM	11	I	Negative analog input, channel A
INBP/NC	14	I	Positive analog input, channel B (NC on single channel device)
INBM/NC	15	I	Negative analog input, channel B (NC on single channel device)
VREF	17	I	1.2V external voltage reference input. A 10 $\mu$ F and a 0.1 $\mu$ F ceramic bypass capacitor connected between VREF and GND pins and placed as close to the pins as possible is recommended when using external reference. Otherwise, connect to GND when using internal reference.
VCM	7	O	Common-mode voltage output to provide DC bias for the analog inputs, 1.25V
<b>CLOCK</b>			
CLK	8	I	Sampling clock input for the ADC
<b>CONFIGURATION</b>			
RESET	9	I	Hardware reset. Active high. This pin has an internal 60k $\Omega$ pull-down resistor.
SEN	16	I	Serial interface enable, Active low, internal 40k $\Omega$ pull-down resistor.
SCLK	18	I	Serial interface clock input, internal 40k $\Omega$ pull-down resistor.
SDIO	19	I/O	Serial interface data input and output, internal 40k $\Omega$ pull-down resistor.
ALERT	20	O	Digital window comparator status pin or over range alert.
<b>DIGITAL INTERFACE</b>			

**Table 4-1. Pin Functions (continued)**

PIN		TYPE	DESCRIPTION
NAME	NO.		
D0	4	O	CMOS digital lane output data.
D1	3	O	
D2	2	O	
D3	1	O	
D4	32	O	
D5	31	O	
D6	26	O	
D7	25	O	
D8	24	O	
D9	23	O	
D10	22	O	
D11	21	O	
DCLK	30	O	CMOS output for data bit clock.
$\overline{\text{DCLK}}/\text{FCLK}$	29	O	Default is Inverse data bit clock for CMOS output data. Frame clock can be selected via SPI write
$\overline{\text{OEN}}/\text{PD}$	6	I	Output data enable. This pin is active low with default 60k $\Omega$ pull-down. Can be configured as power down pin through SPI.
<b>POWER SUPPLY</b>			
AVDD	12, 13	I	Analog 1.8V power supply
GND	PowerPAD™	I	Analog Ground, 0V
IOVDD	27	I	1.8V to 3.3V power supply for digital interface
DGND	28	I	Ground, 0V for digital interface
<b>OTHER</b>			
NC	17	N/A	No connection. Connect to ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range 1.8 V, AVDD		-0.3	2.1	V
Supply voltage range 1.8 V to 3.3 V, IOVDD		-0.3	3.6	
Supply voltage range, GND, DGND		-0.3	0.3	
Voltage applied to input pins	INAP/M, INBP/M, CLK, DCLKIN	-0.3	2.1	
	VREF	-0.3	2.1	
	RESET, SCLK, $\overline{SEN}$ , SDIO, $\overline{OEN}$	-0.3	2.1	
Junction temperature, $T_J$			110	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT	
Supply voltage range	Supply voltage range 1.8v	AVDD <sup>(1)</sup>	1.7	1.8	1.9	V	
Supply voltage range		IOVDD <sup>(1)</sup>	1.7	1.8	1.9	V	
Supply voltage range	Supply voltage range 3.3v	IOVDD <sup>(1)</sup>	3.2	3.3	3.4	V	
$T_A$	Operating free-air temperature		-40			105	°C
$T_J$	Operating junction temperature					105 <sup>(2)</sup>	°C

- (1) Measured to GND.  
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADC39xx	UNIT
		RSM (QFN)	
		32 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	17.9	°C/W

## 5.4 Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		ADC39xx	UNIT
		RSM (QFN)	
		32 Pins	
R <sub>ΘJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T<sub>A</sub> = 25°C, AVDD = IOVDD = 1.8 V, F<sub>IN</sub> = 5MHz, A<sub>IN</sub> = -1dBFS, Interface = DDR, Internal 1.2 V reference, 5 pF output load, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC3910D025</b>						
I <sub>AVDD</sub>	Analog supply current	F <sub>S</sub> = 25 MSPS, dual channel		29	31	mA
I <sub>IOVDD</sub>	Digital supply current			4	9	mA
P <sub>DIS</sub>	Power dissipation			59		mW
<b>ADC3910S025</b>						
I <sub>AVDD</sub>	Analog supply current	F <sub>S</sub> = 25 MSPS, single channel		19	22	mA
I <sub>IOVDD</sub>	Digital supply current			4	8	mA
P <sub>DIS</sub>	Power dissipation			41		mW
<b>ADC3910D065</b>						
I <sub>AVDD</sub>	Analog supply current	F <sub>S</sub> = 65 MSPS, dual channel		33	36	mA
I <sub>IOVDD</sub>	Digital supply current			9	18	mA
P <sub>DIS</sub>	Power dissipation			76		mW
<b>ADC3910S065</b>						
I <sub>AVDD</sub>	Analog supply current	F <sub>S</sub> = 65 MSPS, single channel		22	24	mA
I <sub>IOVDD</sub>	Digital supply current			10	19	mA
P <sub>DIS</sub>	Power dissipation			58		mW
<b>ADC3910D125</b>						
I <sub>AVDD</sub>	Analog supply current	F <sub>S</sub> = 125 MSPS, dual channel		39	44	mA
I <sub>IOVDD</sub>	Digital supply current			15	18.5	mA
P <sub>DIS</sub>	Power dissipation			97		mW
<b>ADC3910S125</b>						
I <sub>AVDD</sub>	Analog supply current	F <sub>S</sub> = 125 MSPS, single channel		25	28	mA
I <sub>IOVDD</sub>	Digital supply current			19	32	mA
P <sub>DIS</sub>	Power dissipation			80		mW
<b>Power down</b>						
P <sub>DIS</sub>	Power consumption in global power down mode			4		mW

## 5.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T<sub>A</sub> = 25°C, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, Internal 1.2 V reference, and -1-dBFS differential input, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC ACCURACY (25 MSPS)</b>					

## 5.6 Electrical Characteristics - DC Specifications (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , 50% clock duty cycle,  $AVDD = IOVDD = 1.8\text{ V}$ , Internal 1.2 V reference, and -1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
No missing codes	No missing codes		10			bits
DNL	Differential nonlinearity		-0.95	$\pm 0.4$	2.1	LSB
INL	Integral nonlinearity		-2	$\pm 0.5$	2.1	LSB
$V_{OS\_ERR}$	Offset error		-2.75	$\pm 1$	2.75	LSB
$V_{OS\_DRIFT}$	Offset drift over temperature			0.001		LSB/ $^\circ\text{C}$
$GAIN_{ERR}$	Gain error	External Reference	-2.25	$\pm 0.2$	2.25	%FSR
		Internal Reference		$\pm 0.8$		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	External Reference		-35		ppm/ $^\circ\text{C}$
		Internal Reference		-102		ppm/ $^\circ\text{C}$
<b>DC ACCURACY (65 MSPS)</b>						
No missing codes	No missing codes		10			bits
DNL	Differential nonlinearity		-0.95	$\pm 0.4$	2.1	LSB
INL	Integral nonlinearity		-2	$\pm 0.5$	2.1	LSB
$V_{OS\_ERR}$	Offset error		-2.75	$\pm 1$	2.75	LSB
$V_{OS\_DRIFT}$	Offset drift over temperature			0.001		LSB/ $^\circ\text{C}$
$GAIN_{ERR}$	Gain error	External Reference	-2.25	$\pm 0.2$	2.25	%FSR
		Internal Reference		$\pm 0.8$		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	External Reference		-35		ppm/ $^\circ\text{C}$
		Internal Reference		-102		ppm/ $^\circ\text{C}$
<b>DC ACCURACY (125 MSPS)</b>						
No missing codes	No missing codes		10			bits
DNL	Differential nonlinearity		-0.95	$\pm 0.4$	2.1	LSB
INL	Integral nonlinearity		-2	$\pm 0.5$	2.1	LSB
$V_{OS\_ERR}$	Offset error		-2.75	$\pm 1$	2.75	LSB
$V_{OS\_DRIFT}$	Offset drift over temperature			0.001		LSB/ $^\circ\text{C}$
$GAIN_{ERR}$	Gain error	External Reference	-2.25	$\pm 0.3$	2.25	%FSR
		Internal Reference		$\pm 0.8$		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	External Reference		-35		ppm/ $^\circ\text{C}$
		Internal Reference		-102		ppm/ $^\circ\text{C}$
<b>ADC ANALOG INPUT (INAP/M, INBP/M)</b>						
FS	Input full scale	Differential		1.9		V <sub>pp</sub>
		Single-ended		0.95		V <sub>pp</sub>
$C_{IN}$	Differential input Capacitance	$F_{IN} = 100\text{ kHz}$		7		pF
$V_{CM}$	Input common mode voltage		$V_{OCM} - 50\text{mV}$	1.275	$V_{OCM} + 50\text{mV}$	V
$V_{OCM}$	Output common mode voltage			1.25		V
BW	Analog Input Bandwidth (-3dB)			150		MHz
<b>EXTERNAL VOLTAGE REFERENCE (VREF)</b>						
$V_{REF}$	External voltage reference			1.2		V
Input Current				0.1		mA
Input impedance				12		k $\Omega$
<b>CLOCK INPUT</b>						
Input clock frequency			5		125	MHz

## 5.6 Electrical Characteristics - DC Specifications (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , 50% clock duty cycle,  $AVDD = IOVDD = 1.8\text{ V}$ , Internal 1.2 V reference, and  $-1\text{-dBFS}$  differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IH}$	High level input voltage		$AVDD - 0.3$	1.8		V	
$V_{IL}$	Low level input voltage			0	$AVSS + 0.3$	V	
$C_{IN}$	Input capacitance			0.5		pF	
Clock duty cycle			45	50	55	%	
<b>DIGITAL INPUTS (DCLKIN, RESET, <math>\overline{OEN}</math>, SCLK, SEN, SDIO)</b>							
$V_{IH}$	High level input voltage	DCLKIN	$AVDD - 0.1$	$AVDD$		V	
$V_{IL}$	Low level input voltage				0.1	V	
$V_{IH}$	High level input voltage	RESET, $\overline{OEN}$ , SCLK, SEN, SDIO	1.4			V	
$V_{IL}$	Low level input voltage				0.4	V	
$I_{IH}$	High level input current				90	150	$\mu\text{A}$
$I_{IL}$	Low level input current			-150	-90		$\mu\text{A}$
$C_i$	Input capacitance				1.5		pF
<b>DIGITAL OUTPUT (SDOUT)</b>							
$V_{OH}$	High level output voltage	$I_{LOAD} = -400\ \mu\text{A}$	$AVDD - 0.1$	$AVDD$		V	
$V_{OL}$	Low level output voltage	$I_{LOAD} = 400\ \mu\text{A}$			0.1	V	
<b>DIGITAL CMOS OUTPUTS (D0:D11)</b>							
Output data rate		per CMOS output pin			250	MHz	
$V_{OH}$	High level output voltage	$I_{LOAD} = -400\ \mu\text{A}$	$IOVDD - 0.1$	$IOVDD$		V	
$V_{OL}$	Low level output voltage	$I_{LOAD} = 400\ \mu\text{A}$			0.1	V	
$V_{OH}$	High level output voltage	$I_{LOAD} = -400\ \mu\text{A}$ , ALERT/GPO	$IOVDD - 0.1$	$IOVDD$		V	
$V_{OL}$	Low level output voltage				0.1	V	



## 5.7 Electrical Characteristics - AC Specifications (25 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $F_S = 25\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$  differential input, Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	$f_{IN} = 10\text{ MHz}$ , $A_{IN} = -20\text{ dBFS}$		-132		dBFS/Hz
SNR	Signal to noise ratio, excluding DC, HD2 to HD5	$f_{IN} = 1.1\text{ MHz}$		61.1		dBFS
		$f_{IN} = 5\text{ MHz}$	57	60.7		
		$f_{IN} = 10\text{ MHz}$		61.1		
		$f_{IN} = 20\text{ MHz}$		61.0		
SINAD	Signal to noise and distortion ratio, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		59.1		dBFS
		$f_{IN} = 5\text{ MHz}$		59.9		
		$f_{IN} = 10\text{ MHz}$		59.7		
		$f_{IN} = 20\text{ MHz}$		59.8		
ENOB	Effective number of bits, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		9.9		Bit
		$f_{IN} = 5\text{ MHz}$		9.9		
		$f_{IN} = 10\text{ MHz}$		9.8		
		$f_{IN} = 20\text{ MHz}$		9.8		
THD	Total Harmonic Distortion (First five harmonics)	$f_{IN} = 1.1\text{ MHz}$		-62		dBc
		$f_{IN} = 5\text{ MHz}$		-65		
		$f_{IN} = 10\text{ MHz}$		-65		
		$f_{IN} = 20\text{ MHz}$		-65		
SFDR	Spur free dynamic range including second and third harmonic	$f_{IN} = 1.1\text{ MHz}$		63		dBFS
		$f_{IN} = 5\text{ MHz}$	57	66		
		$f_{IN} = 10\text{ MHz}$		65		
		$f_{IN} = 20\text{ MHz}$		65		
SPUR	Spur free dynamic range (excluding DC, HD2, HD3)	$f_{IN} = 1.1\text{ MHz}$		83		dBFS
		$f_{IN} = 5\text{ MHz}$	58	85		
		$f_{IN} = 10\text{ MHz}$		85		
		$f_{IN} = 20\text{ MHz}$		82		
IMD3	Two tone inter-modulation distortion	$f_{IN} = 10/12\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/ tone}$		-98		dBc
XTALK	Channel-to-channel crosstalk	Aggressor = 1.1 MHz		107		dBFS
		Aggressor = 10 MHz		97		
		Aggressor = 20 MHz		93		

## 5.8 Electrical Characteristics - AC Specifications (65 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $F_S = 65\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$  differential input, Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	$f_{IN} = 10\text{ MHz}$ , $A_{IN} = -20\text{ dBFS}$		-135.9		dBFS/Hz
SNR	Signal to noise ratio, excluding DC, HD2 to HD5	$f_{IN} = 1.1\text{ MHz}$		61.0		dBFS
		$f_{IN} = 5\text{ MHz}$	57	61.1		
		$f_{IN} = 10\text{ MHz}$		61.1		
		$f_{IN} = 20\text{ MHz}$		61.1		
		$f_{IN} = 40\text{ MHz}$		61.0		
		$f_{IN} = 70\text{ MHz}$		60.7		

## 5.8 Electrical Characteristics - AC Specifications (65 MSPS) (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $F_S = 65\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$  differential input, Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal to noise and distortion ratio, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		59.2		dBFS
		$f_{IN} = 5\text{ MHz}$		59.7		
		$f_{IN} = 10\text{ MHz}$		59.8		
		$f_{IN} = 20\text{ MHz}$		60.0		
		$f_{IN} = 40\text{ MHz}$		59.5		
		$f_{IN} = 70\text{ MHz}$		58.5		
ENOB	Effective number of bits, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		9.8		Bit
		$f_{IN} = 5\text{ MHz}$		9.9		
		$f_{IN} = 10\text{ MHz}$		9.9		
		$f_{IN} = 20\text{ MHz}$		9.8		
		$f_{IN} = 40\text{ MHz}$		9.8		
		$f_{IN} = 70\text{ MHz}$		9.8		
THD	Total Harmonic Distortion (First five harmonics)	$f_{IN} = 1.1\text{ MHz}$		-62		dBc
		$f_{IN} = 5\text{ MHz}$		-64		
		$f_{IN} = 10\text{ MHz}$		-65		
		$f_{IN} = 20\text{ MHz}$		-66		
		$f_{IN} = 40\text{ MHz}$		-64		
		$f_{IN} = 70\text{ MHz}$		-62		
SFDR	Spur free dynamic range including second and third harmonic	$f_{IN} = 1.1\text{ MHz}$		63		dBFS
		$f_{IN} = 5\text{ MHz}$	57	65		
		$f_{IN} = 10\text{ MHz}$		65		
		$f_{IN} = 20\text{ MHz}$		66		
		$f_{IN} = 40\text{ MHz}$		64		
		$f_{IN} = 70\text{ MHz}$		62		
SPUR	Spur free dynamic range (excluding DC, HD2, HD3)	$f_{IN} = 1.1\text{ MHz}$		85		dBFS
		$f_{IN} = 5\text{ MHz}$	58	85		
		$f_{IN} = 10\text{ MHz}$		85		
		$f_{IN} = 20\text{ MHz}$		82		
		$f_{IN} = 40\text{ MHz}$		77		
		$f_{IN} = 70\text{ MHz}$		71		
IMD3	Two tone inter-modulation distortion	$f_{IN} = 10/12\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/tone}$		-94		dBc
XTALK	Channel-to-channel crosstalk	Aggressor = 1.1 MHz		105		dBFS
		Aggressor = 10 MHz		102		
		Aggressor = 20 MHz		97		

## 5.9 Electrical Characteristics - AC Specifications (125 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $F_S = 125\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$  differential input, Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	$f_{IN} = 10\text{ MHz}$ , $A_{IN} = -20\text{ dBFS}$		-138.8		dBFS/Hz

## 5.9 Electrical Characteristics - AC Specifications (125 MSPS) (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $AVDD = IOVDD = 1.8\text{ V}$ ,  $F_S = 125\text{ MSPS}$ ,  $F_{IN} = 5\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$  differential input, Internal 1.2 V reference, and 50% clock duty cycle, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal to noise ratio, excluding DC, HD2 to HD5	$f_{IN} = 1.1\text{ MHz}$		60.8		dBFS
		$f_{IN} = 5\text{ MHz}$	57	60.6		
		$f_{IN} = 10\text{ MHz}$		60.6		
		$f_{IN} = 20\text{ MHz}$		60.6		
		$f_{IN} = 40\text{ MHz}$		60.6		
		$f_{IN} = 70\text{ MHz}$		60.4		
SINAD	Signal to noise and distortion ratio, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		58.5		dBFS
		$f_{IN} = 5\text{ MHz}$		58.9		
		$f_{IN} = 10\text{ MHz}$		59.1		
		$f_{IN} = 20\text{ MHz}$		59.1		
		$f_{IN} = 40\text{ MHz}$		59.6		
		$f_{IN} = 70\text{ MHz}$		57.7		
ENOB	Effective number of bits, excluding DC offset	$f_{IN} = 1.1\text{ MHz}$		9.8		Bit
		$f_{IN} = 5\text{ MHz}$		9.8		
		$f_{IN} = 10\text{ MHz}$		9.8		
		$f_{IN} = 20\text{ MHz}$		9.8		
		$f_{IN} = 40\text{ MHz}$		9.8		
		$f_{IN} = 70\text{ MHz}$		9.7		
THD	Total Harmonic Distortion (First five harmonics)	$f_{IN} = 1.1\text{ MHz}$		-61		dBc
		$f_{IN} = 5\text{ MHz}$		-63		
		$f_{IN} = 10\text{ MHz}$		-63		
		$f_{IN} = 20\text{ MHz}$		-64		
		$f_{IN} = 40\text{ MHz}$		-65		
		$f_{IN} = 70\text{ MHz}$		-60		
SFDR	Spur free dynamic range including second and third harmonic	$f_{IN} = 1.1\text{ MHz}$		62		dBFS
		$f_{IN} = 5\text{ MHz}$	57	64		
		$f_{IN} = 10\text{ MHz}$		64		
		$f_{IN} = 20\text{ MHz}$		65		
		$f_{IN} = 40\text{ MHz}$		67		
		$f_{IN} = 70\text{ MHz}$		61		
SPUR	Spur free dynamic range (excluding DC, HD2, HD3)	$f_{IN} = 1.1\text{ MHz}$		84		dBFS
		$f_{IN} = 5\text{ MHz}$	58	82		
		$f_{IN} = 10\text{ MHz}$		84		
		$f_{IN} = 20\text{ MHz}$		82		
		$f_{IN} = 40\text{ MHz}$		78		
		$f_{IN} = 70\text{ MHz}$		75		
IMD3	Two tone inter-modulation distortion	$f_{IN} = 10/12\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/ tone}$		-84		dBc
		$f_{IN} = 90/92\text{ MHz}$ , $A_{IN} = -7\text{ dBFS/ tone}$		-97		
XTALK	Channel-to-channel crosstalk	Aggressor = 1.1 MHz		102		dBFS
		Aggressor = 10 MHz		90		
		Aggressor = 20 MHz		98		

## 5.10 Timing Requirements

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AVDD = IOVDD = 1.8\text{ V}$ , Internal 1.2 V reference, 5 pF output load, and  $-1\text{-dBFS}$  differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>ADC TIMING SPECIFICATIONS</b>						
$t_{AD}$	Aperture Delay			0.5		ns
$t_A$	Aperture Jitter	square wave clock with fast edges		500		fs
$t_{ACQ}$	Signal acquisition period, referenced to sampling clock falling edge			$-T_S/5$		Sampling Clock Period
$t_{CONV}$	Signal conversion period, referenced to sampling clock falling edge	$F_S = 25\text{ MSPS}$		5.5		ns
		$F_S = 65\text{ MSPS}$		5.5		ns
		$F_S = 125\text{ MSPS}$		5.5		ns
Wake up time	Time to valid data after coming out of power down. Internal reference.			30		us
	Time to valid data after coming out of power down. External 1.2V reference.			19		us
ADC Latency	Signal input to data output	Low Latency Mode <sup>(1)</sup>		1		ADC clock cycles
		Digital features enabled (includes Serial CMOS interface modes)		5		
Add. Latency	Real Decimation	2		25		
		4		60		
		8		130		
		16		270		
<b>INTERFACE TIMING - DDR CMOS</b>						
$t_{PD}$	Propagation delay: sampling clock falling edge to DCLK rising edge			$T_S/4 + 3$		ns
$t_{DE}$	DCLK edge to previous data transition	$F_S = 25\text{ MSPS}$		-10	-9	
		$F_S = 65\text{ MSPS}$		-3.8	-3.4	
		$F_S = 125\text{ MSPS}$		-2	-1.8	
$t_{DL}$	DCLK edge to next data transition	$F_S = 25\text{ MSPS}$		9	10	
		$F_S = 65\text{ MSPS}$		3.4	3.8	
		$F_S = 125\text{ MSPS}$		1.8	2	
<b>INTERFACE TIMING - SDR CMOS</b>						
$t_{PD}$	Propagation delay: sampling clock falling edge to DCLK rising edge			$T_S/4 + 3$		ns
$t_{DE}$	DCLK edge to previous data transition	$F_S = 25\text{ MSPS}$		-20	-18	
		$F_S = 65\text{ MSPS}$		-7.6	-6.9	
		$F_S = 125\text{ MSPS}$		-4	-3.6	
$t_{DV}$	DCLK edge to next data transition	$F_S = 25\text{ MSPS}$		18	20	
		$F_S = 65\text{ MSPS}$		6.9	7.7	
		$F_S = 125\text{ MSPS}$		3.6	4	

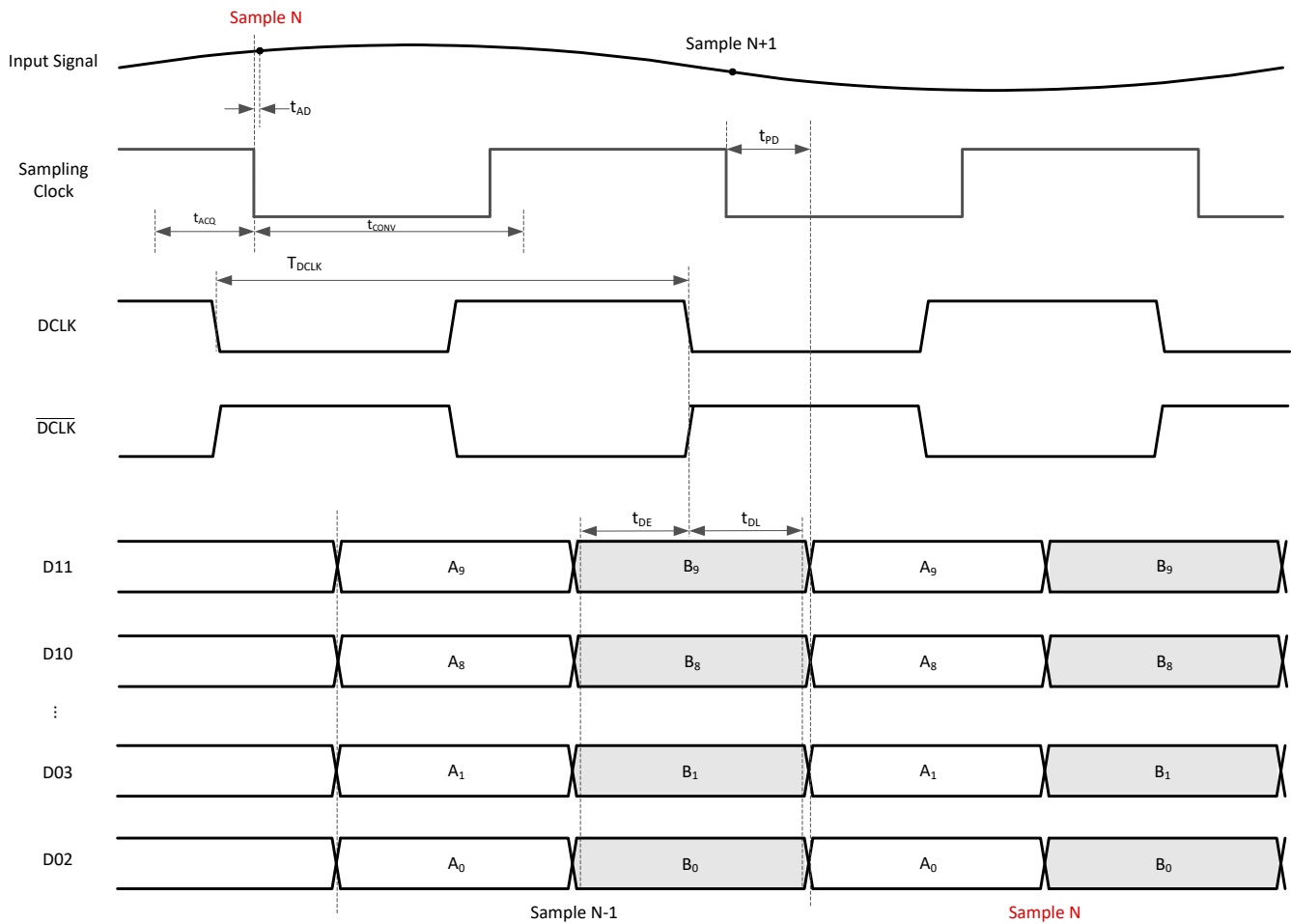
## 5.10 Timing Requirements (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = IO_{VDD} = 1.8\text{ V}$ , Internal 1.2 V reference, 5 pF output load, and  $-1\text{-dBFS}$  differential input, unless otherwise noted

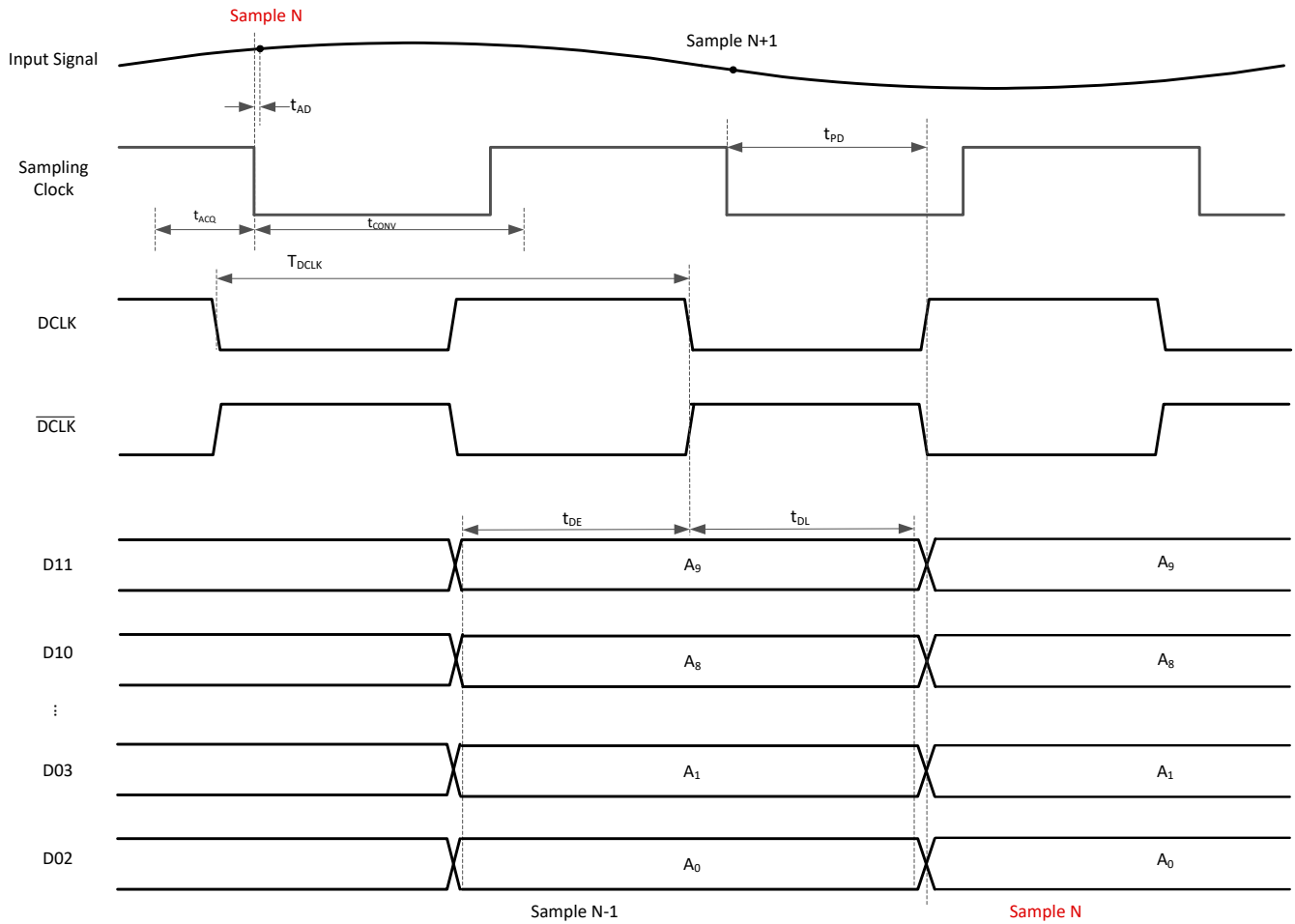
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{PD}$	Propagation delay: sampling clock falling edge to output data delay	Delay between sampling clock falling edge to DCLKIN falling edge < 2.5ns. $T_{DCLK} = \text{DCLK period}$ $t_{CDCLK} = \text{Sampling clock falling edge to DCLKIN falling edge}$		$T_S/4 + 3$		ns
		Delay between sampling clock falling edge to DCLKIN falling edge $\geq 2.5\text{ns}$ . $T_{DCLK} = \text{DCLK period}$ $t_{CDCLK} = \text{Sampling clock falling edge to DCLKIN falling edge}$		$T_S/4 + 3$		
$t_{CD}$	DCLK rising edge to output data delay 4 Lane serial CMOS	$F_{out} = 10\text{ MSPS}$	-7.25	-6.25	-5.25	ns
		$F_{out} = 20\text{ MSPS}$	-4.125	-3.125	-2.125	
		$F_{out} = 30\text{ MSPS}$	-3.08	-2.08	-1.08	
	DCLK rising edge to output data delay 2 Lane serial CMOS	$F_{out} = 5\text{ MSPS}$	-7.25	-6.25	-5.25	
		$F_{out} = 10\text{ MSPS}$	-4.125	-3.125	-2.125	
		$F_{out} = 15\text{ MSPS}$	-3.08	-2.08	-1.08	
$t_{DV}$	Data valid, 4 Lane serial CMOS	$F_{out} = 10\text{ MSPS}$	-7.25	-6.25	-5.25	ns
		$F_{out} = 20\text{ MSPS}$	-4.125	-3.125	-2.125	
		$F_{out} = 30\text{ MSPS}$	-3.08	-2.08	-1.08	
	Data valid, 2 Lane serial CMOS	$F_{out} = 5\text{ MSPS}$	-7.25	-6.25	-5.25	
		$F_{out} = 10\text{ MSPS}$	-4.125	-3.125	-2.125	
		$F_{out} = 15\text{ MSPS}$	-3.08	-2.08	-1.08	
<b>SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input</b>						
$f_{CLK,SCLK}$	Serial clock frequency				20	MHz
$t_{S,SEN}$	SEN falling edge to SCLK rising edge		10			ns
$t_{H,SEN}$	SCLK rising edge to SEN rising edge		10			
$t_{S,SDIO}$	SDIO setup time from rising edge of SCLK		17			
$t_{H,SDIO}$	SDIO hold time from rising edge of SCLK		9			
<b>SERIAL PROGRAMMING INTERFACE (SDIO) - Output</b>						
$t_{OZD}$	Delay from falling edge of 8th SCLK cycle during read operation for SDIO transition from tri-state to valid data		3.9		10.8	ns
$t_{ODZ}$	Delay from SEN rising edge for SDIO transition from valid data to tri-state		3.4		14	
$t_{OD}$	Delay from falling edge of 8th SCLK cycle during read operation to SDIO valid		3.9		10.8	

- (1) In low latency mode the default interface is DDR for dual channel devices and SDR for single channel devices. Other interface configurations such as serial CMOS will add additional latency.

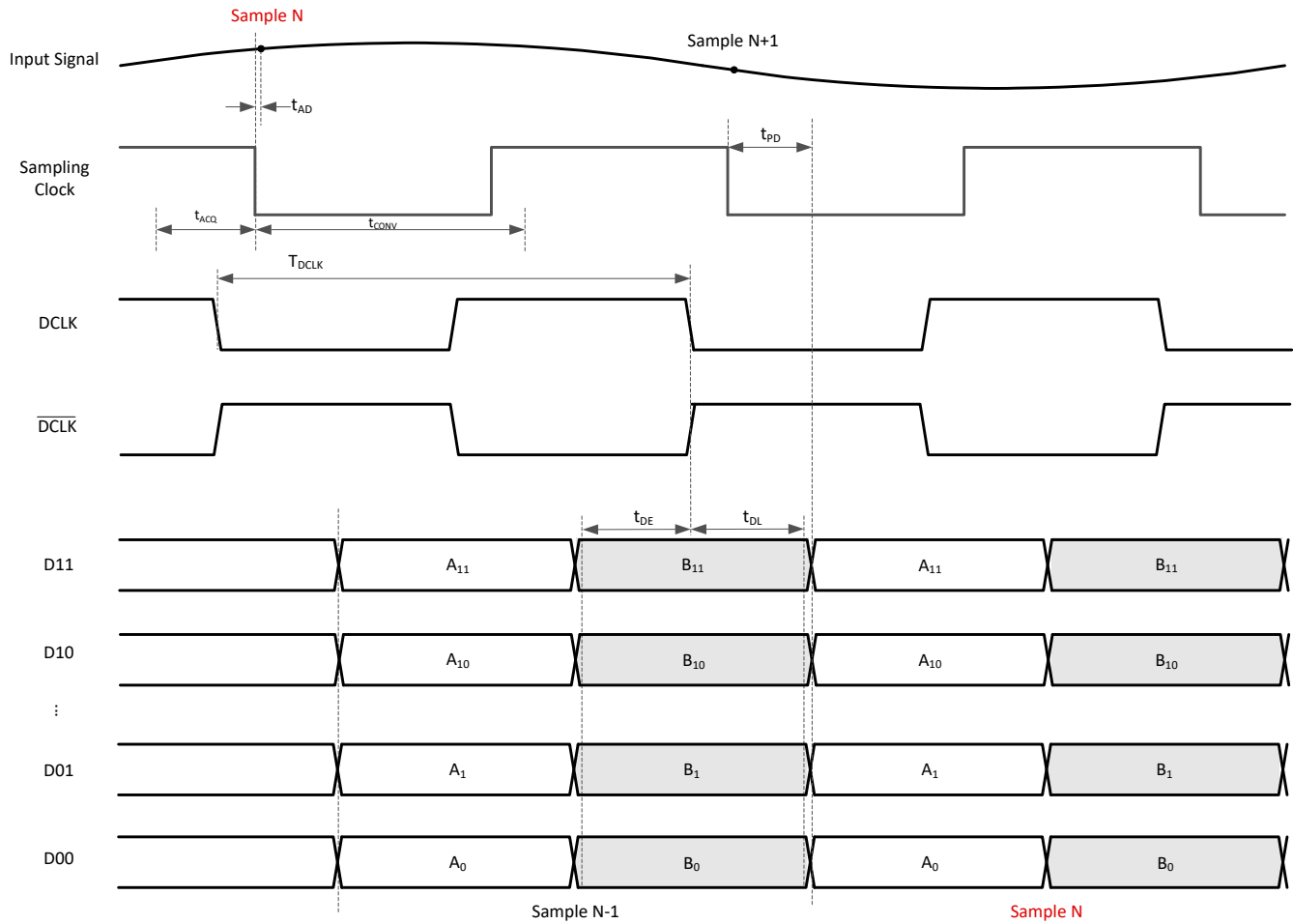
## 5.11 Output Interface Timing Diagram



**Figure 5-1. Timing Diagram: 10-Bit DDR (Default: 10 Lanes)**

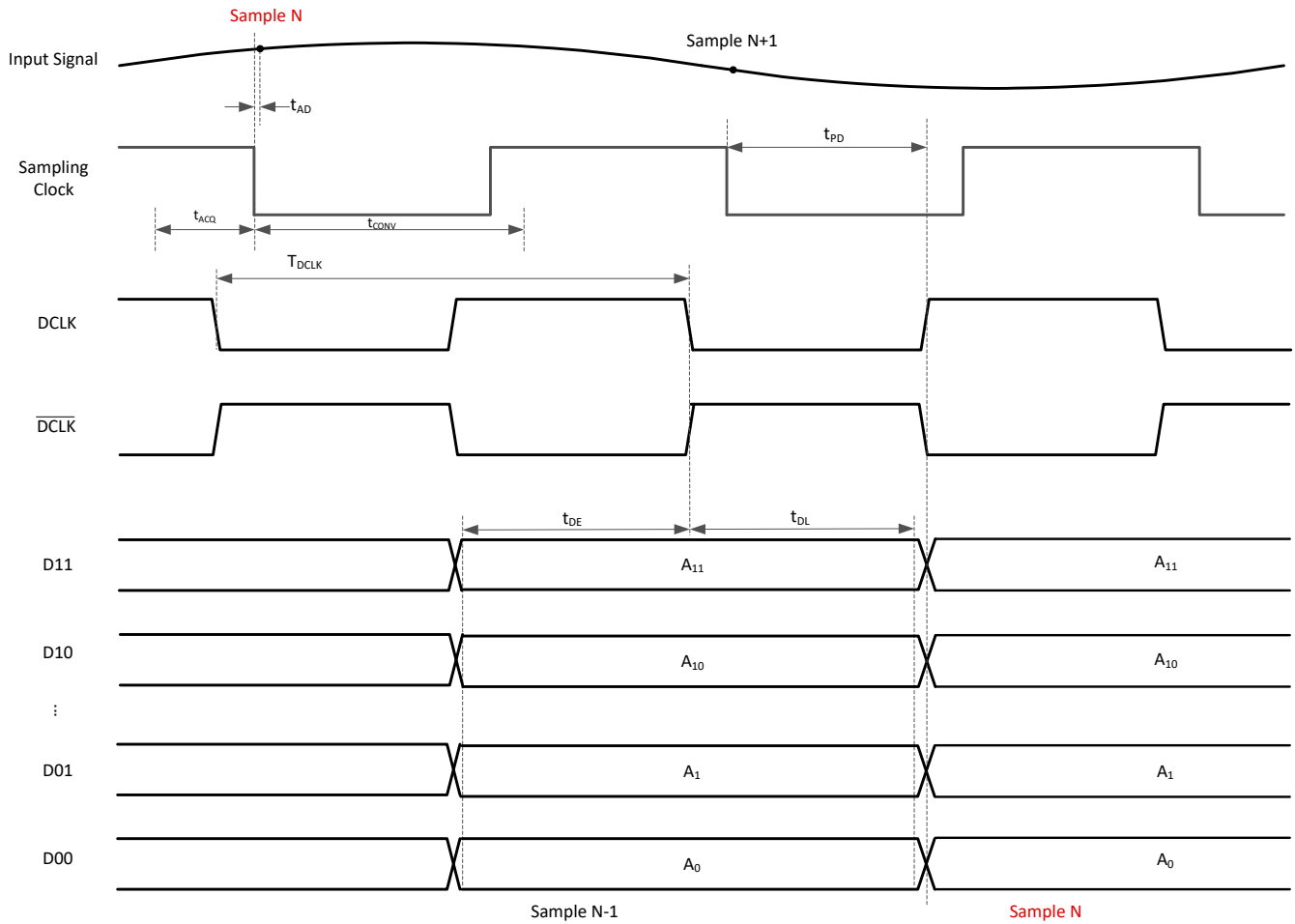


**Figure 5-2. Timing Diagram: 10-Bit SDR (Default: 10 Lanes)**



**Figure 5-3. Timing Diagram: 12-Bit DDR (Default: 10 Lanes)**

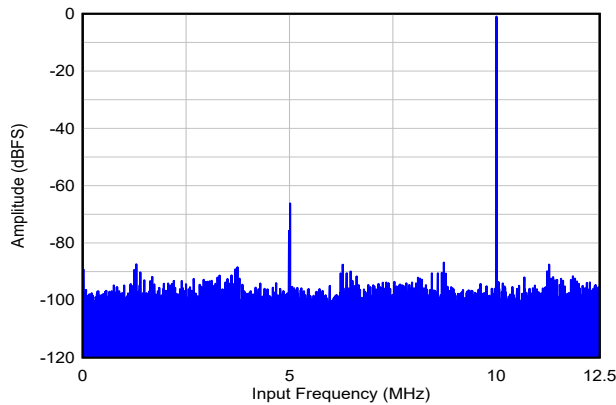




**Figure 5-4. Timing Diagram: 12-Bit SDR (Default: 10 Lanes)**

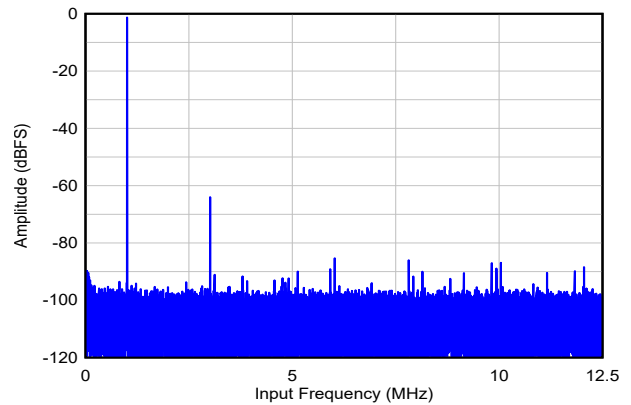
## 5.12 Typical Characteristics - 25MSPS

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



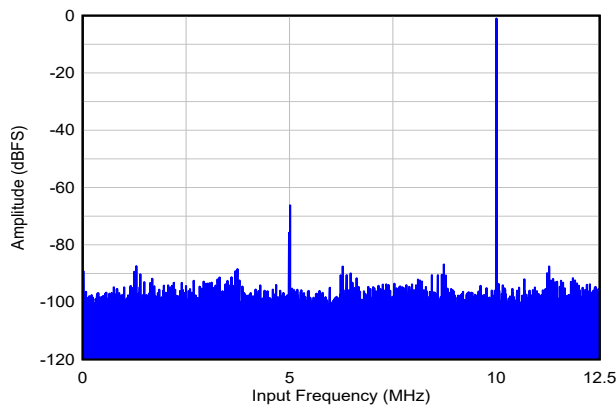
SNR = 61.2dBFS, SFDR = 64dBc, Non HD23 = 84dBFS

Figure 5-5. Single Tone FFT at  $F_{IN} = 1\text{MHz}$



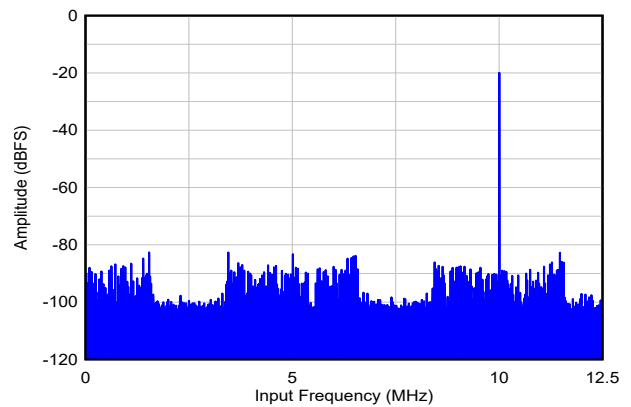
SNR = 59dBFS, SFDR = 63dBc, Non HD23 = 85dBFS

Figure 5-6. Single Tone FFT at  $F_{IN} = 1\text{MHz}$ , Single-ended Input



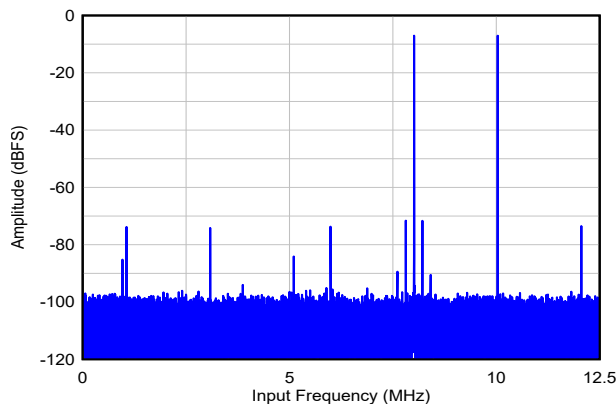
SNR = 61dBFS, SFDR = 65dBc, Non HD23 = 87dBFS

Figure 5-7. Single Tone FFT at  $F_{IN} = 10\text{MHz}$



SNR = 61.2dBFS, SFDR = 63dBc, Non HD23 = 83dBFS

Figure 5-8. Single Tone FFT at  $F_{IN} = 10\text{MHz}$ ,  $A_{IN} = -20\text{dBFS}$



$A_{IN} = -7\text{dBFS}/\text{tone}$ , IMD3 = -98dBc

Figure 5-9. Two Tone FFT at  $F_{IN} = 10/12\text{MHz}$

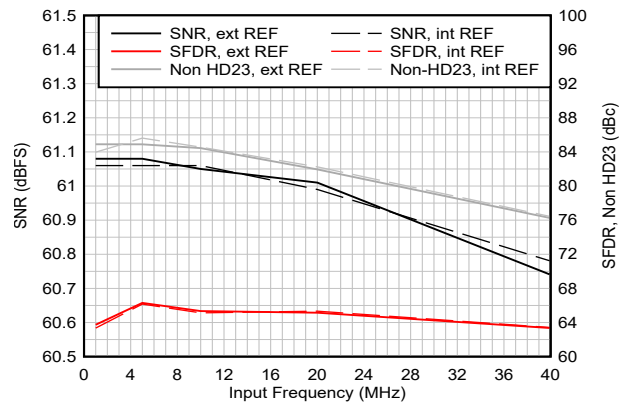
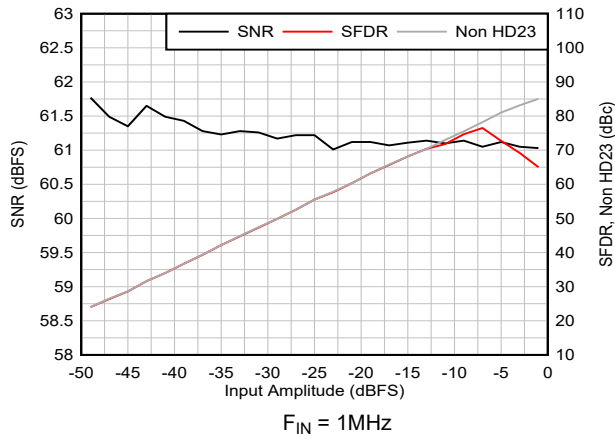


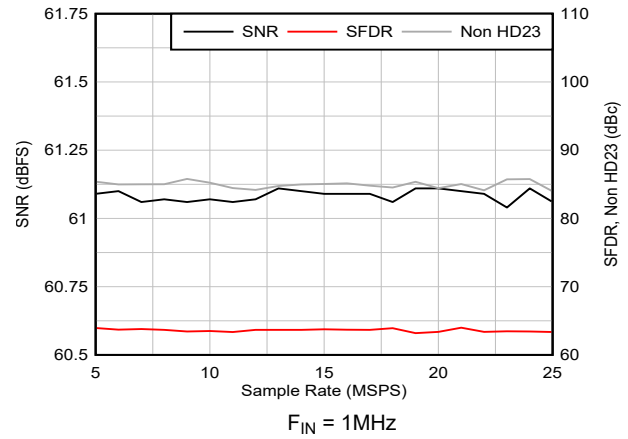
Figure 5-10. AC Performance vs Input Frequency

### 5.12 Typical Characteristics - 25MSPS (continued)

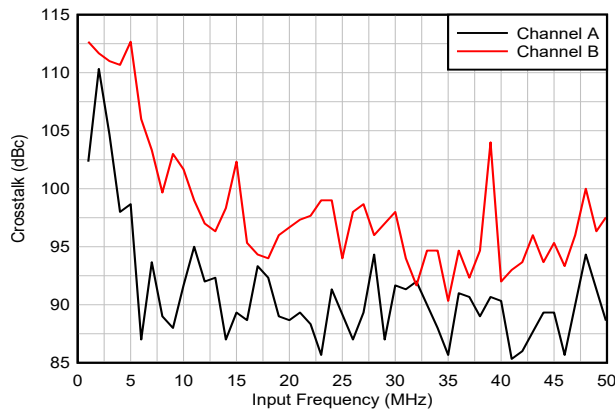
Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



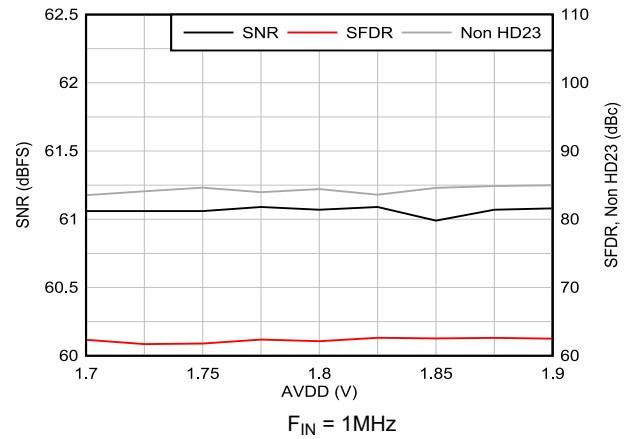
**Figure 5-11. AC Performance vs Input Amplitude**



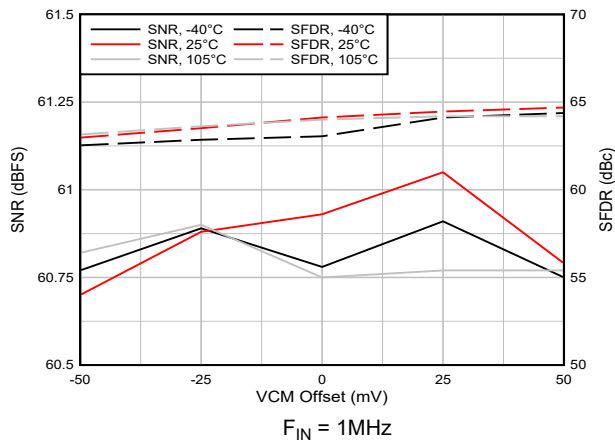
**Figure 5-12. AC Performance vs Sampling Rate**



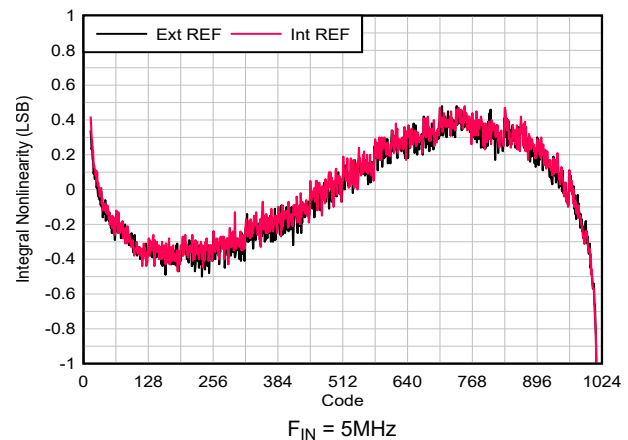
**Figure 5-13. Crosstalk vs Input Frequency**



**Figure 5-14. AC Performance vs AVDD**



**Figure 5-15. AC Performance vs VCM vs Temperature**



**Figure 5-16. INL vs ADC Code**

## 5.12 Typical Characteristics - 25MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.

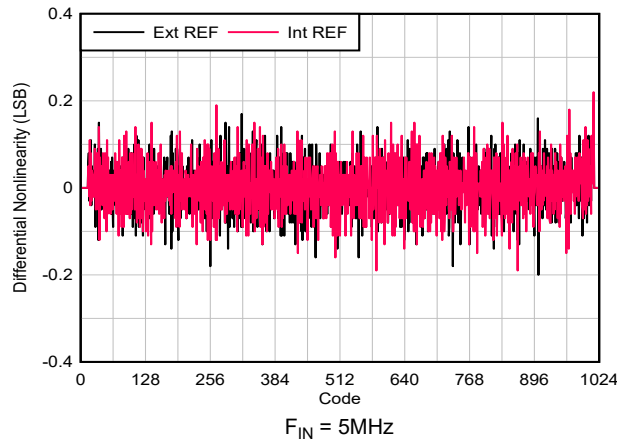


Figure 5-17. DNL vs ADC Code

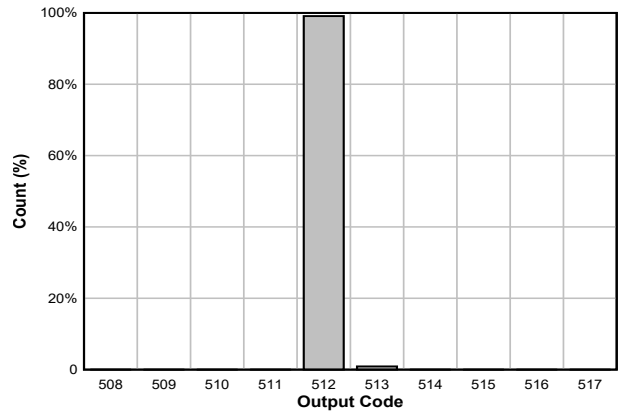


Figure 5-18. DC Offset Histogram

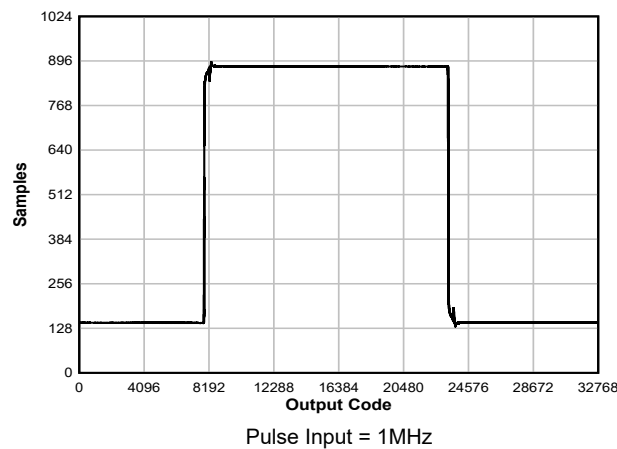


Figure 5-19. Pulse Response

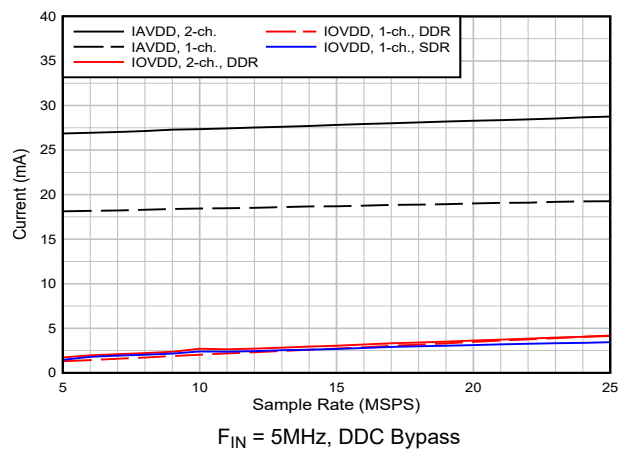


Figure 5-20. Current vs Sampling Rate

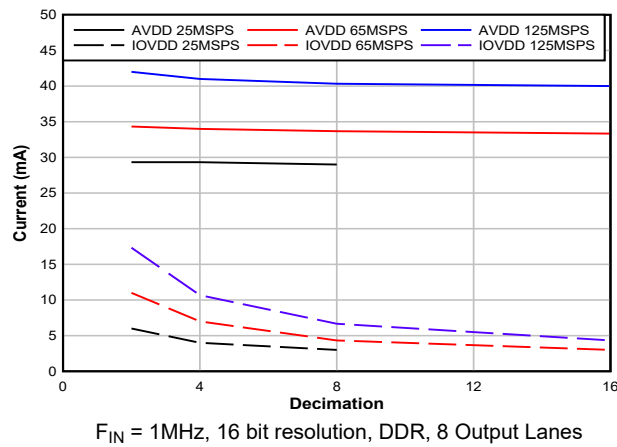


Figure 5-21. Current vs Decimation

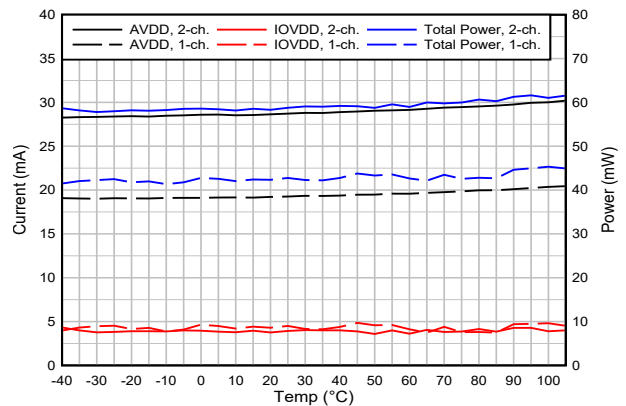
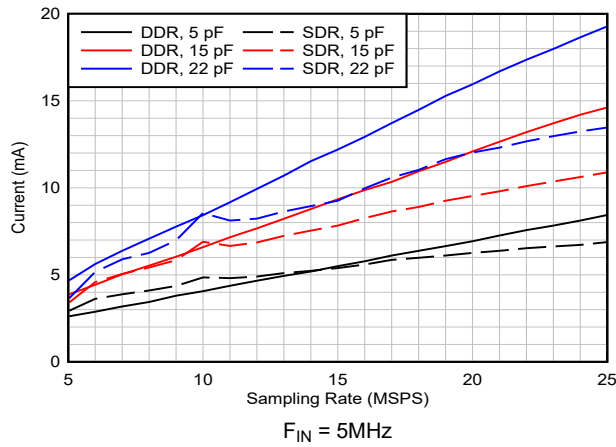


Figure 5-22. Current vs Temperature

### 5.12 Typical Characteristics - 25MSPS (continued)

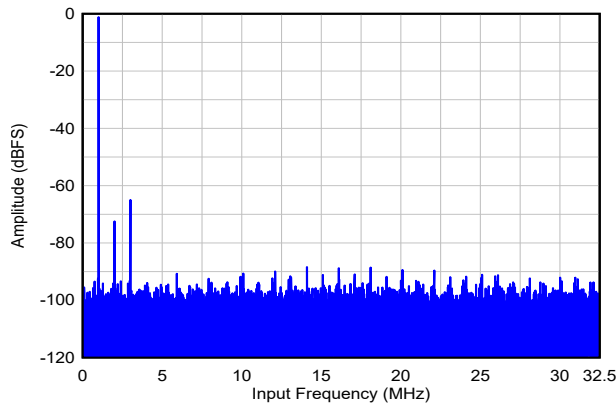
Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



**Figure 5-23.  $I_{IOVDD}$  Current vs Load Capacitance**

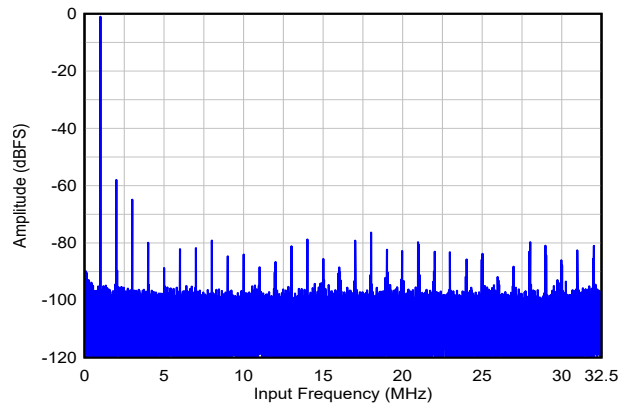
### 5.13 Typical Characteristics - 65MSPS

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AV_{DD} = IO_{VDD} = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



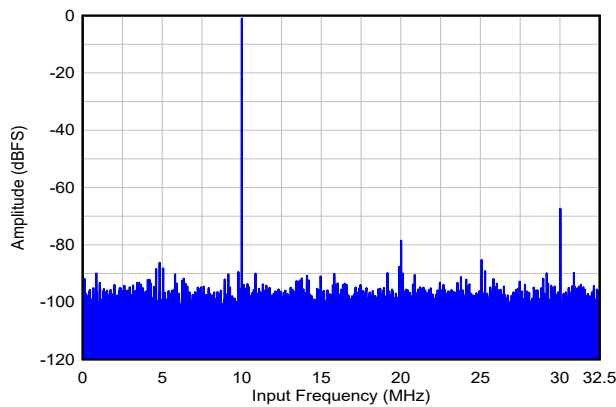
SNR = 61dBFS, SFDR = 64dBc, Non-HD23 = 88dBFS

**Figure 5-24. Single Tone FFT at  $F_{IN} = 1\text{MHz}$**



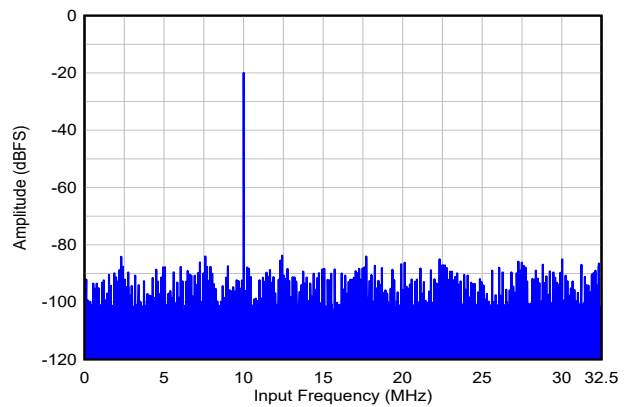
SNR = 58.3dBFS, SFDR = 57dBc, Non-HD23 = 76dBFS

**Figure 5-25. Single Tone FFT at  $F_{IN} = 1\text{MHz}$ , Single-ended input**



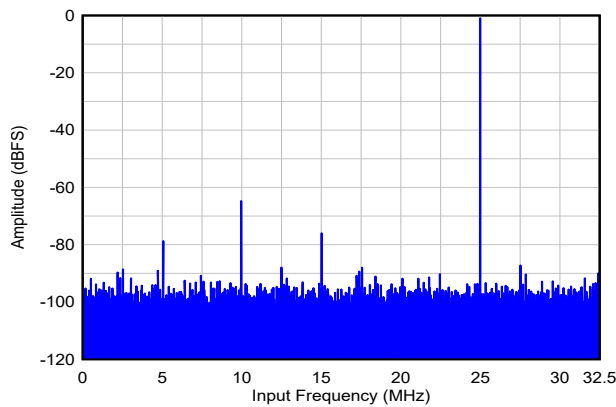
SNR = 61dBFS, SFDR = 66dBc, Non-HD23 = 85dBFS

**Figure 5-26. Single Tone FFT at  $F_{IN} = 10\text{MHz}$**



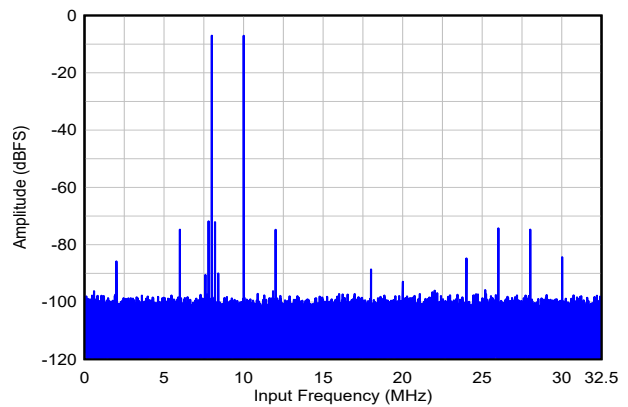
SNR = 61.3dBFS, SFDR = 64dBc, Non-HD23 = 84dBFS

**Figure 5-27. Single Tone FFT at  $F_{IN} = 10\text{MHz}$ ,  $A_{IN} = -20\text{dBFS}$**



SNR = 60.9dBFS, SFDR = 64dBc, Non-HD23 = 79dBFS

**Figure 5-28. Single Tone FFT at  $F_{IN} = 40\text{MHz}$**

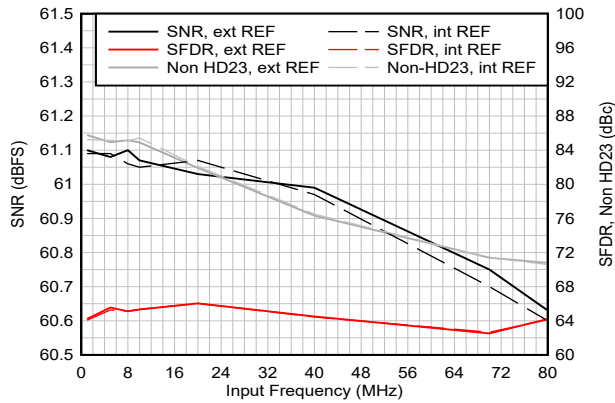


$A_{IN} = -7\text{dBFS}/\text{tone}$ , IMD3 = -94dBc

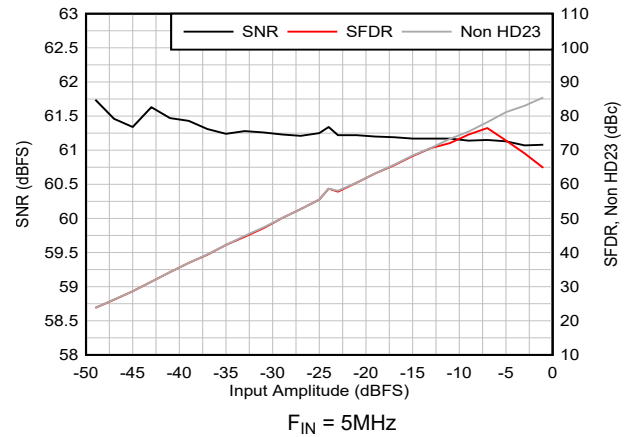
**Figure 5-29. Two Tone FFT at  $F_{IN} = 10/12\text{MHz}$**

### 5.13 Typical Characteristics - 65MSPS (continued)

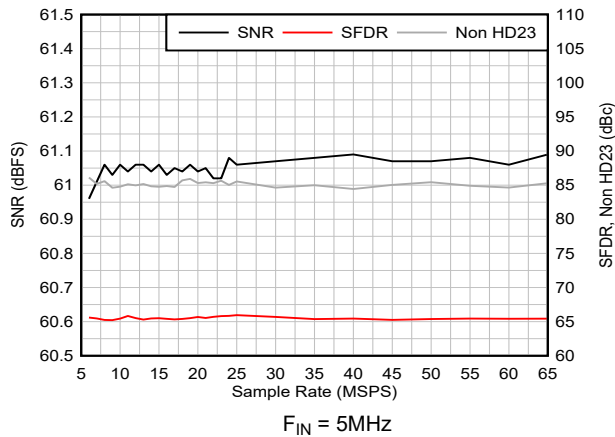
Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



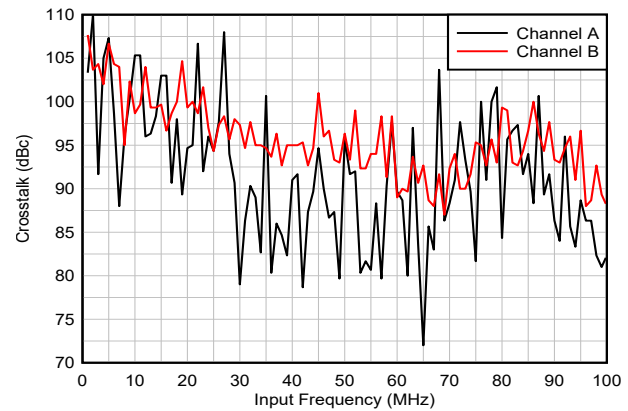
**Figure 5-30. AC Performance vs Input Frequency**



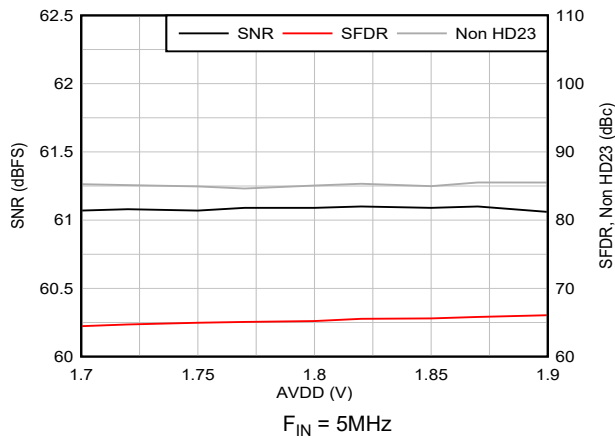
**Figure 5-31. AC Performance vs Input Amplitude**



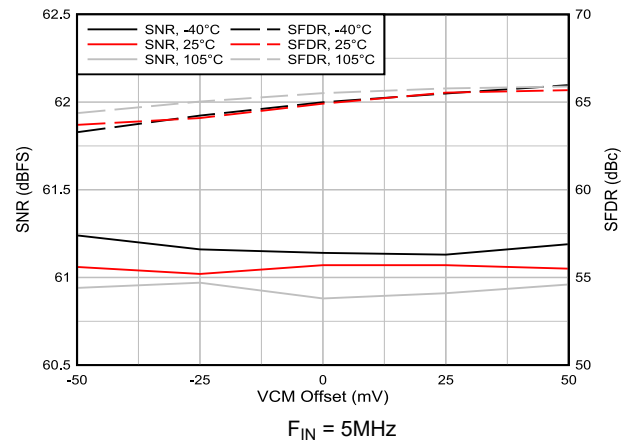
**Figure 5-32. AC Performance vs Sampling Rate**



**Figure 5-33. Crosstalk vs Input Frequency**



**Figure 5-34. AC Performance vs AVDD**



**Figure 5-35. AC Performance vs VCM vs Temperature**

### 5.13 Typical Characteristics - 65MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AV_{DD} = IO_{VDD} = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.

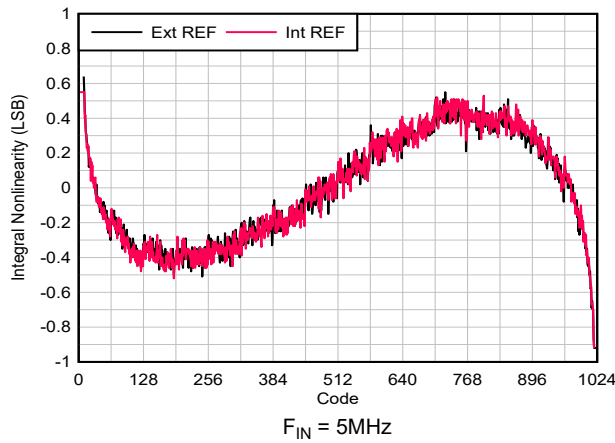


Figure 5-36. INL vs ADC Code

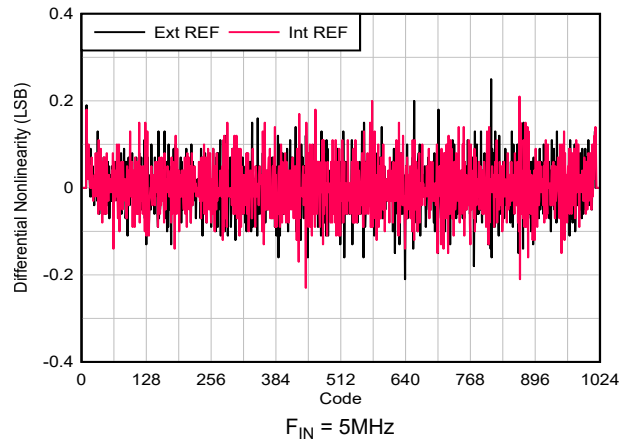


Figure 5-37. DNL vs ADC Code

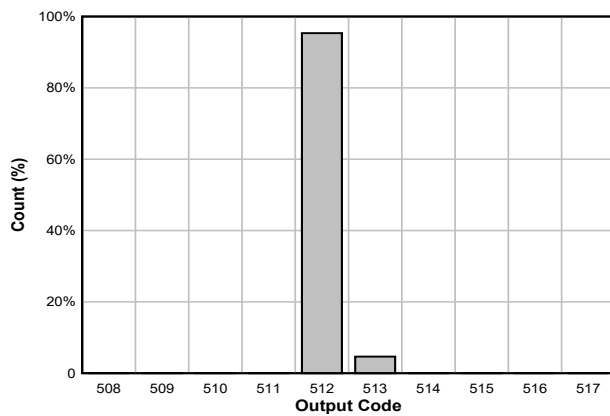


Figure 5-38. DC Offset Histogram

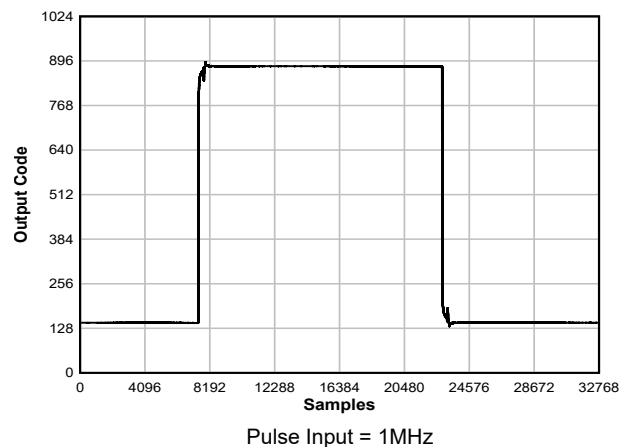


Figure 5-39. Pulse Response

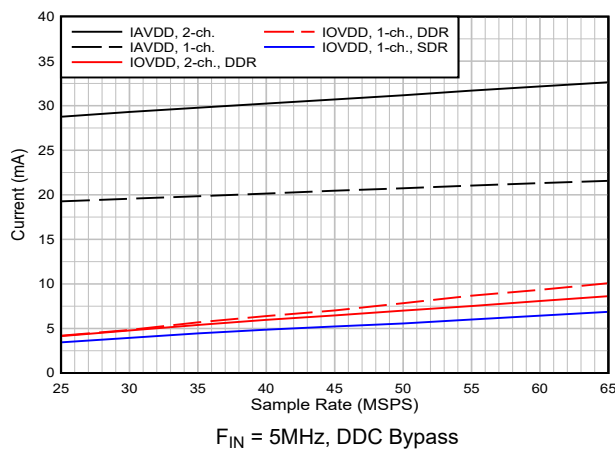


Figure 5-40. Current vs Sampling Rate

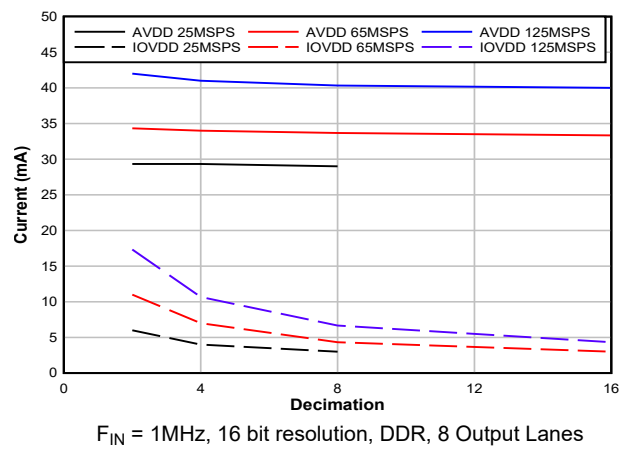


Figure 5-41. Current vs Decimation



### 5.13 Typical Characteristics - 65MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 65 MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.

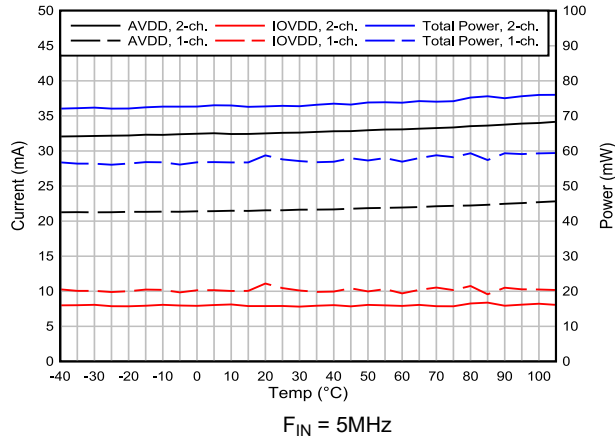


Figure 5-42. Current vs Temperature

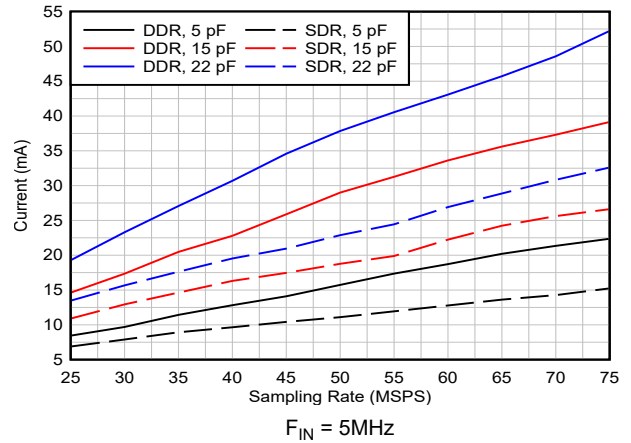
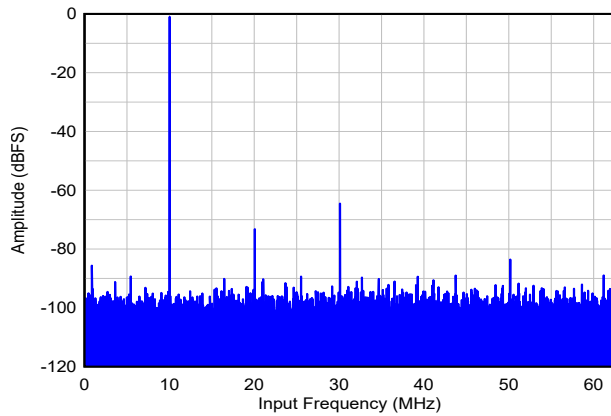


Figure 5-43.  $I_{OVDD}$  Current vs Load Capacitance

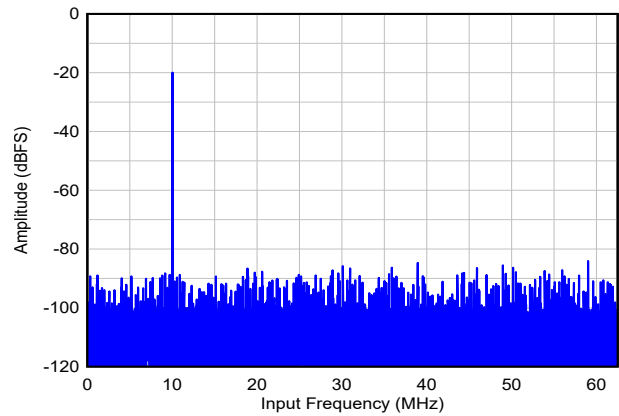
## 5.14 Typical Characteristics - 125MSPS

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



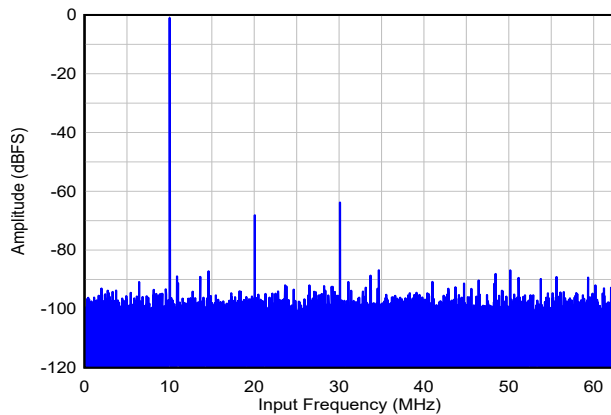
SNR = 60.6dBFS, SFDR = 63.5dBc, Non-HD23 = 83.5dBFS

**Figure 5-44. Single Tone FFT at  $F_{IN} = 10\text{MHz}$**



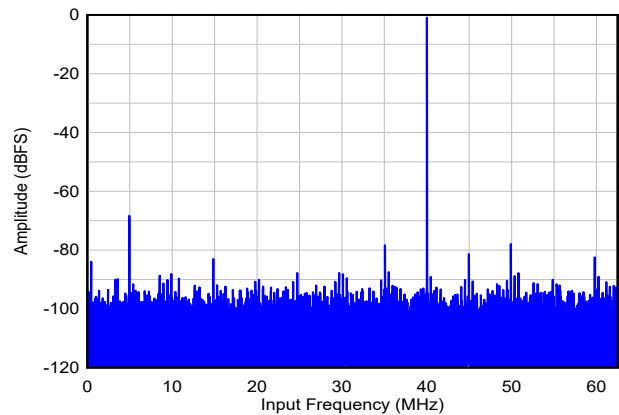
SNR = 60.9dBFS, SFDR = 64dBc, Non-HD23 = 84dBFS

**Figure 5-45. Single Tone FFT at  $F_{IN} = 10\text{MHz}$ ,  $A_{IN} = -20\text{dBFS}$**



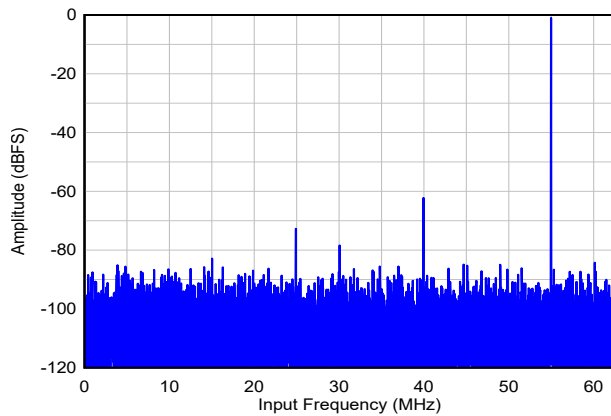
SNR = 60.5dBFS, SFDR = 63dBc, Non-HD23 = 86dBFS

**Figure 5-46. Single Tone FFT at  $F_{IN} = 10\text{Hz}$ , Single-ended input**



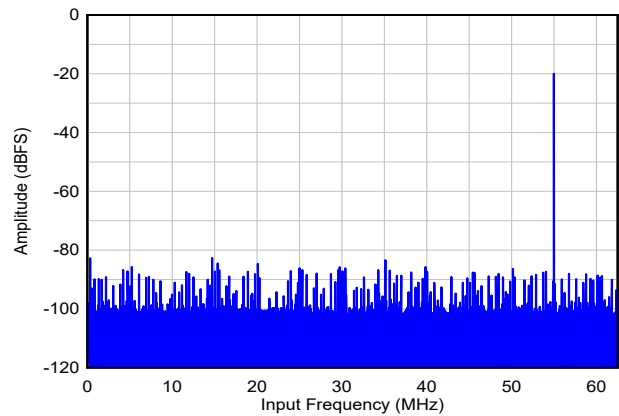
SNR = 60.2dBFS, SFDR = 67dBc, Non-HD23 = 78dBFS

**Figure 5-47. Single Tone FFT at  $F_{IN} = 40\text{MHz}$**



SNR = 58.9dBFS, SFDR = 61.2dBc, Non-HD23 = 72dBFS

**Figure 5-48. Single Tone FFT at  $F_{IN} = 70\text{MHz}$**

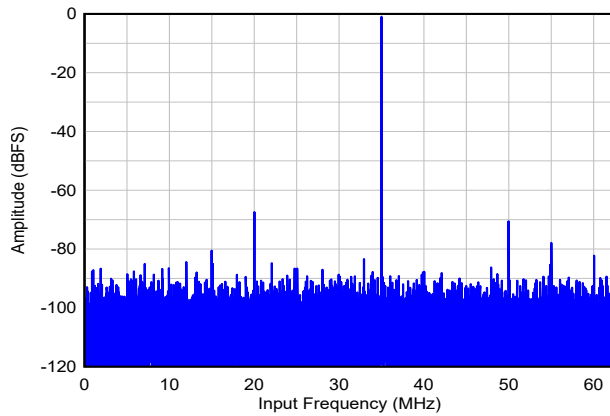


SNR = 60.9dBFS, SFDR = 63dBc, Non-HD23 = 83dBFS

**Figure 5-49. Single Tone FFT at  $F_{IN} = 70\text{MHz}$ ,  $A_{IN} = -20\text{dBFS}$**

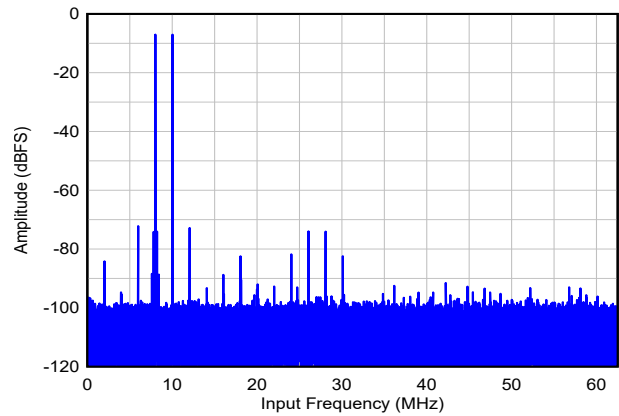
### 5.14 Typical Characteristics - 125MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



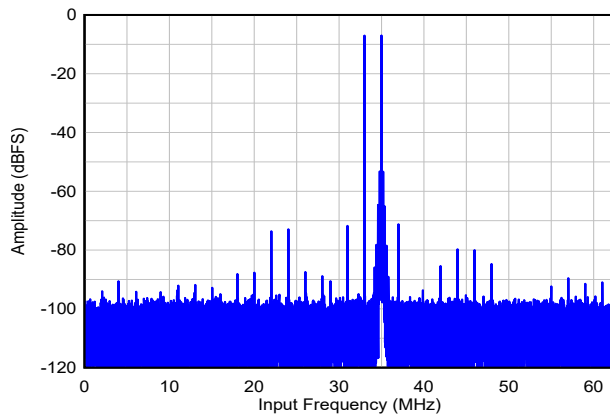
SNR = 59.1dBFS, SFDR = 66dBc, Non-HD23 = 71dBFS

Figure 5-50. Single Tone FFT at  $F_{IN} = 90\text{MHz}$



$A_{IN} = -7\text{dBFS/tone}$ , IMD3 = -84dBc

Figure 5-51. Two Tone FFT at  $F_{IN} = 10/12\text{MHz}$



$A_{IN} = -7\text{dBFS/tone}$ , IMD3 = -97dBc

Figure 5-52. Two Tone FFT at  $F_{IN} = 90/92\text{MHz}$

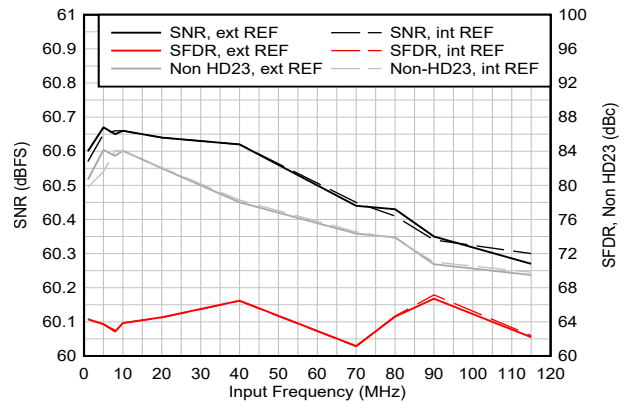


Figure 5-53. AC Performance vs Input Frequency

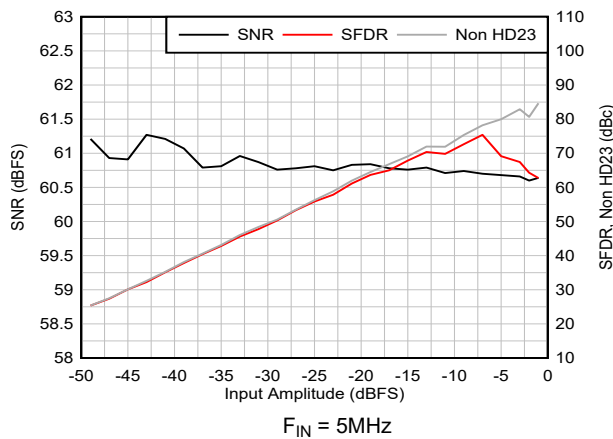


Figure 5-54. AC Performance vs Input Amplitude

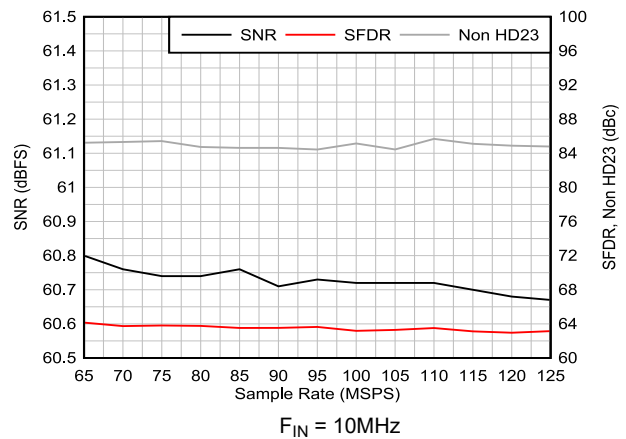
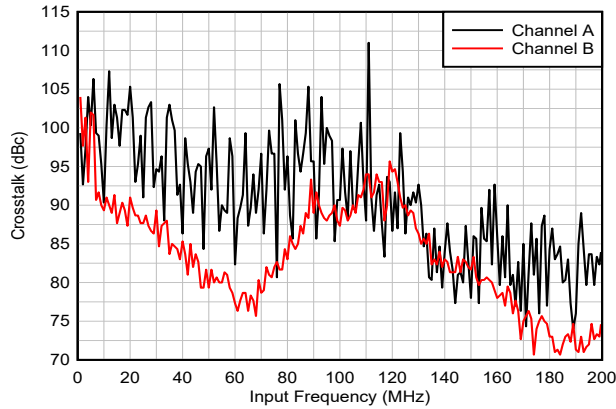


Figure 5-55. AC Performance vs Sampling Rate

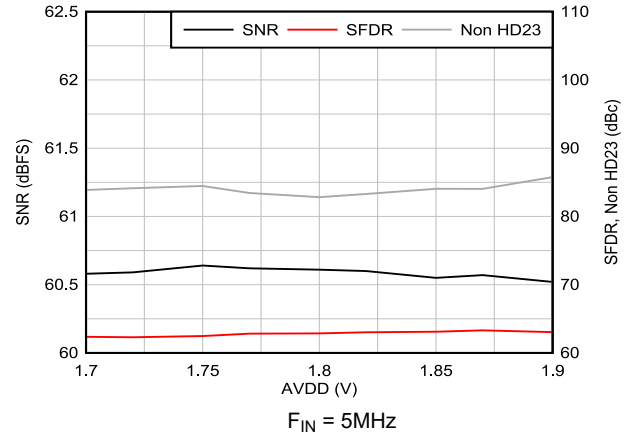
## 5.14 Typical Characteristics - 125MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input,  $AVDD = IOVDD = 1.8\text{V}$ , internal 1.2V voltage reference, unless otherwise noted.



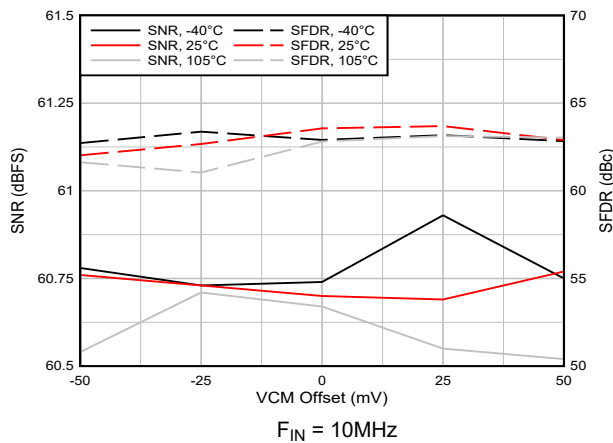
$F_{IN} = 5\text{MHz}$ ,  $A_{IN} = -1\text{dBFS}$  on aggressor channel

Figure 5-56. Crosstalk vs Input Frequency



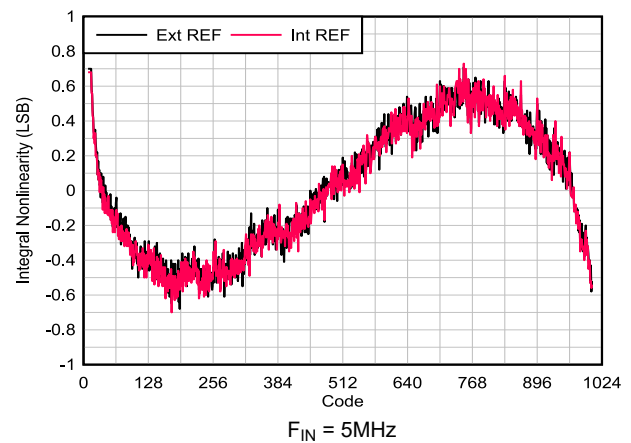
$F_{IN} = 5\text{MHz}$

Figure 5-57. AC Performance vs AVDD



$F_{IN} = 10\text{MHz}$

Figure 5-58. AC Performance vs VCM vs Temperature



$F_{IN} = 5\text{MHz}$

Figure 5-59. INL vs ADC Code

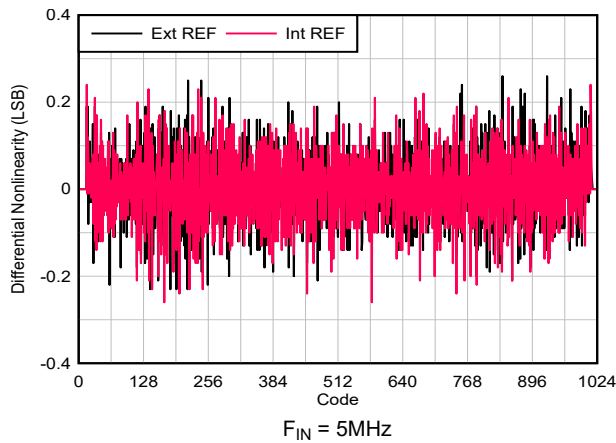


Figure 5-60. DNL vs ADC Code

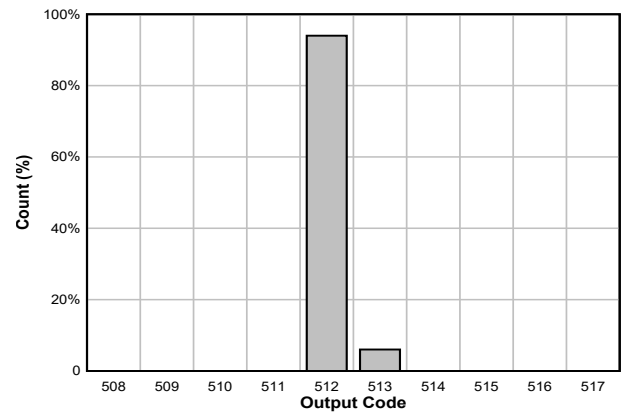


Figure 5-61. DC Offset Histogram

### 5.14 Typical Characteristics - 125MSPS (continued)

Typical values at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125MSPS,  $A_{IN} = -1\text{dBFS}$ , differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.

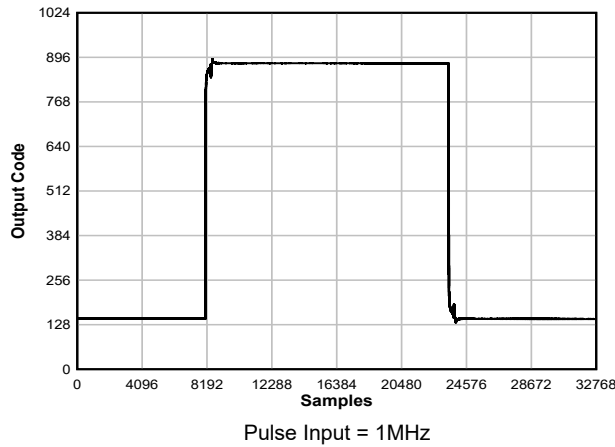


Figure 5-62. Pulse Response

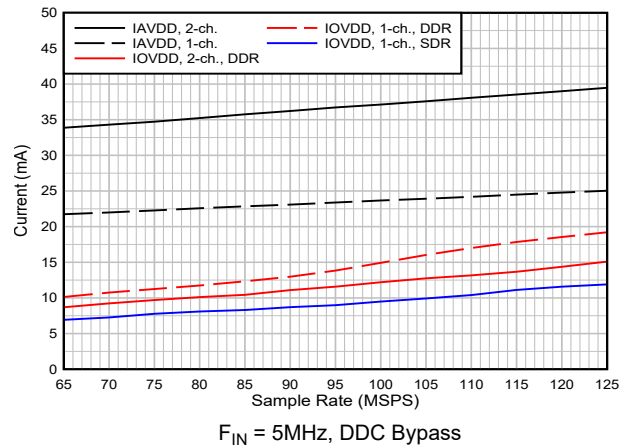


Figure 5-63. Current vs Sampling Rate

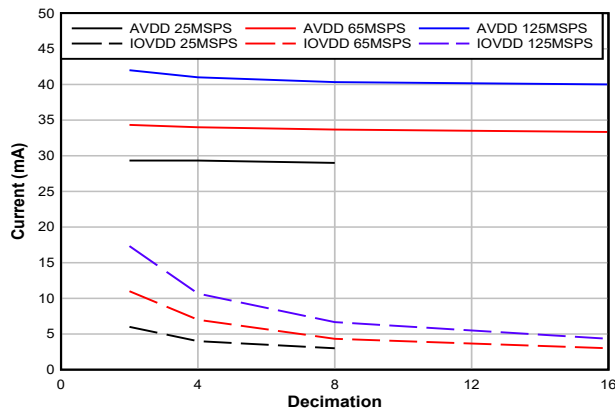


Figure 5-64. Current vs Decimation

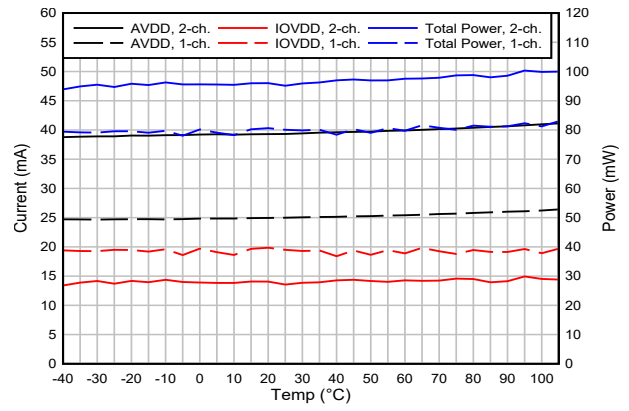


Figure 5-65. Current vs Temperature

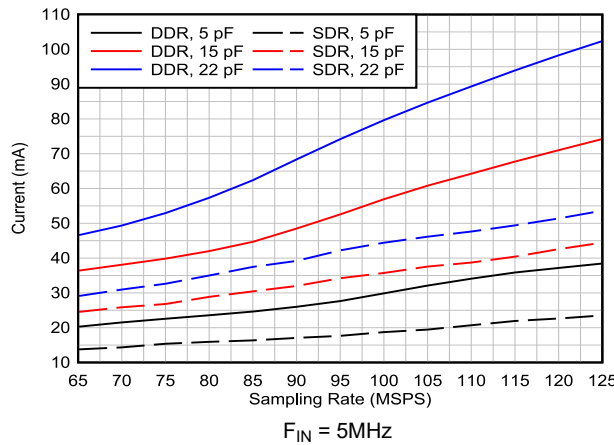


Figure 5-66.  $I_{IOVDD}$  Current vs Load Capacitance

## 6 Detailed Description

### 6.1 Overview

The ADC3910Dx and ADC3910Sx are a family of ultra-low power 10-bit high-speed dual and single channel analog-to-digital converters supporting sampling rates up to 125MSPS. With the inherent low latency architecture, the digital output result is available after only one clock cycle in low latency mode. The ADC3910Dx and ADC3910Sx has buffered analog inputs which eases design by isolating the input from the ADC sampling operation and supports single ended or differential input signaling. The ADC3910Dx and ADC3910Sx are equipped with an on-chip internal reference buffer but also supports use of an external, high precision 1.2V voltage reference.

The ADC3910Dx and ADC3910Sx also offers several digital features such as:

- Digital down converters that enables external anti-alias filter relaxation as well as output data rate reduction. The digital filter supports only real decimation.
- Digital comparators with a dedicated alert pin that can be used to interrupt the host when a programmed high or low threshold is crossed on any input channel.
- Statistics engine that provides min, max, sum, sum of samples squared, and threshold triggered counter, that gives additional sample details.

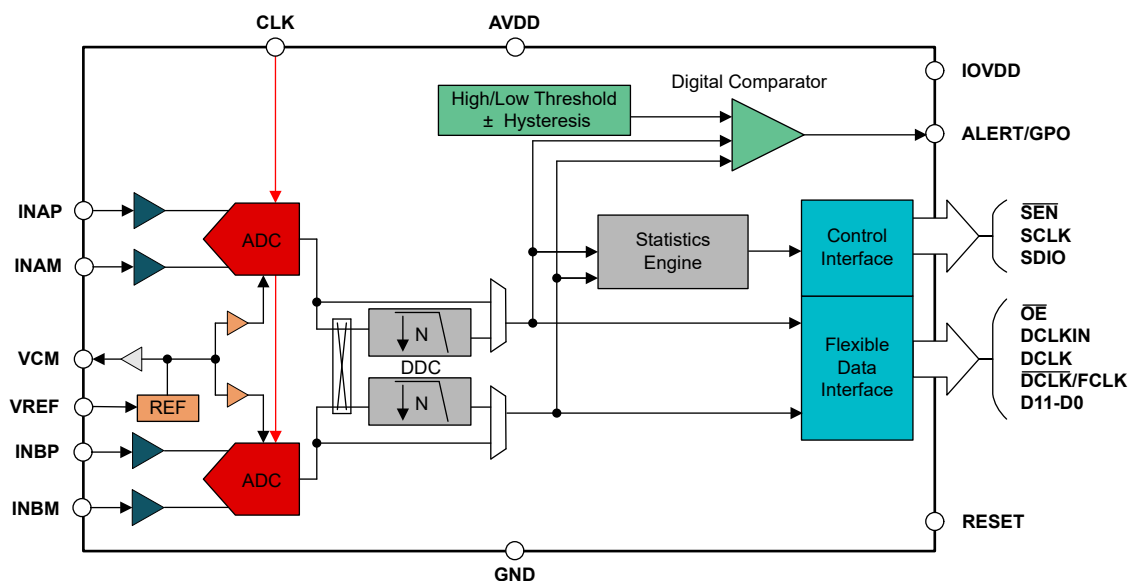
The CMOS output data interface can be configured in parallel or serial with the option of 1.8V to 3.3V logic. The device supports DDR, SDR and Serial CMOS modes with 2s Complement or Offset Binary format options. The ADC3910Dx and ADC3910Sx offers  $\overline{\text{DCLK}}$  as an alternate solution for designs that can not capture on the DCLK falling edge when using DDR interface.

Table 6-1 shows the pin mapping to supply.

**Table 6-1. Device Pin to Supply Mapping**

Power Supply	Device Pins
AVDD	$\overline{\text{OEN}}$ , DCLKIN, CLK, INxP M, RESET, SDIO, SCLK, SEN
IOVDD	D0-D11, DCLK, $\overline{\text{DCLK}}$  FCLK, ALERT

### 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 ADC Features

#### 6.3.1.1 Low Latency Mode

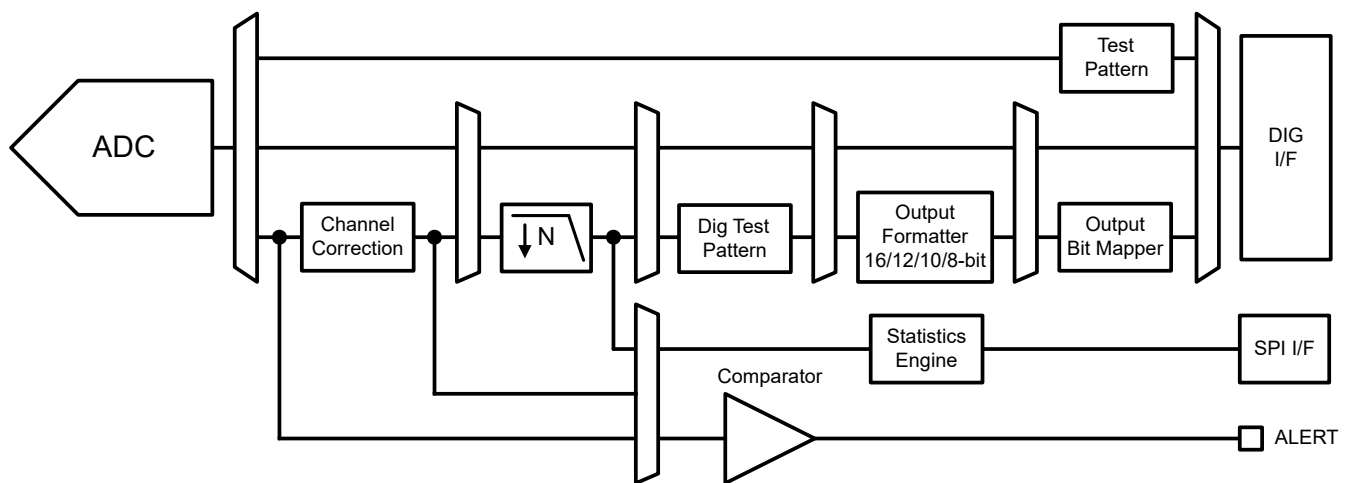
By default the ADC3910Dx and ADC3910Sx are in low latency mode where all digital features such as decimation, statistics engine and comparator are disabled and the interface is set to DDR, 10 output lanes. In this mode, latency between the ADC input and digital output is 1 clock cycle. Enabling any digital features or changing the interface mode adds latency to the device throughput.

#### 6.3.1.2 Full Digital Feature Mode

With the digital features enabled the ADC3910Dx and ADC3910Sx offers the ability to decimate, on-chip comparators, statistics engines and configurable alerts. See the [Digital Features](#) and [Digital Interface](#) sections for details on to set up each of these options.

#### Note

Enabling the digital features adds additional ADC latency depending on the configuration.



**Figure 6-1. Digital features block diagram**

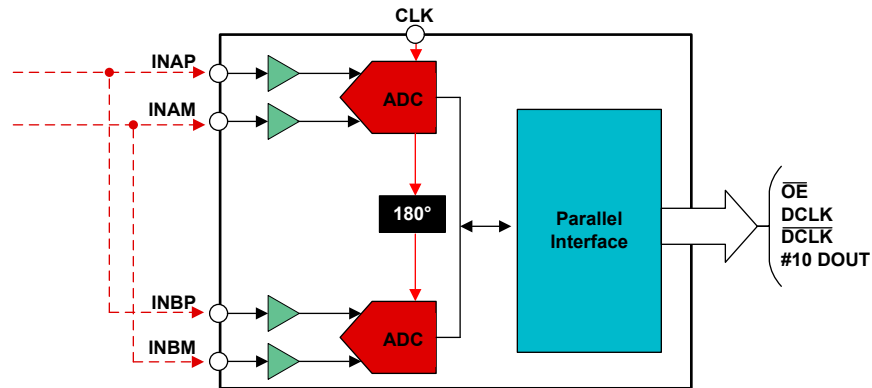
#### 6.3.1.3 Interleaving Mode

The ADC3910Dx can be used as a single-channel ADC where the sampling rate is equal to two times the clock frequency ( $F_S = 2 \times F_{CLK}$ ). This mode interleaves the two channels by sampling them out-of-phase. [Figure 6-2](#) shows block diagram when interleaving mode is selected. Operating in interleaving mode disables the digital down converter, statistics engine, and digital comparator. Interleaving mode supports only parallel output interface.

#### Note

Interleaving is only available on dual channel ADCs. Single channel ADCs do not have the ability to interleave.

Interleaving can be enabled in SPI register INTERLEAVE (0x84). Offset, gain, and timing controls are available in SPI registers OFFSET\_CHx, PROG\_GAIN\_CHx, IL\_GAIN\_CHx, and CLK\_TIM\_ADJ\_CHx (0x0D5-0x0DF) to minimize mismatches between the ADCs. Channel corrections (offset, gain) must be enabled in SPI register CORR\_CHx (0x0E0). Enabling channel corrections add several clock cycles of latency.



**Figure 6-2. Block Diagram of Interleaving Mode**

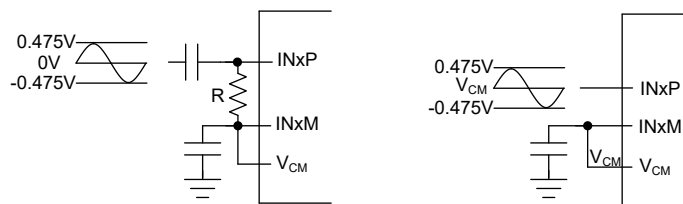
### 6.3.2 Analog Input

The analog inputs of ADC3910Dx and ADC3910Sx supports differential and single-ended configuration, with support for AC coupling and DC coupling. Analog inputs are designed for an input common mode voltage of 1.25V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The ADC3910Dx and ADC3910Sx has buffered analog inputs which eases design by isolating the input from the ADC sampling operation.

#### 6.3.2.1 Single Ended Input

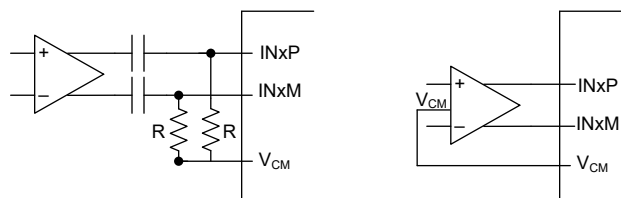
The ADC3910Dx and ADC3910Sx can be configured to operate in single ended mode using just the positive signal input. This operating mode must be enabled via SPI write to register 0x30B. The single ended signal is connected to the positive input of the ADC and negative input needs to be biased to  $V_{CM}$  as shown in [Figure 6-3](#).



**Figure 6-3. Single ended analog input: AC coupled (left) and DC coupled (right)**

#### 6.3.2.2 Differential Input

The ADC3910Dx and ADC3910Sx by default is configured to operate in differential mode with a swing of 1.9 Vpp as shown in [Figure 6-4](#).

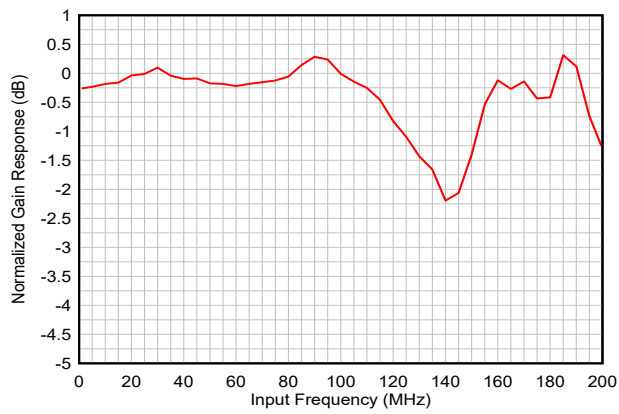


**Figure 6-4. Differential analog input: AC coupled (left) and DC coupled (right)**



### 6.3.2.3 Analog Input Bandwidth

Figure 6-5 shows the analog full power input bandwidth. The -3dB bandwidth is approximately 150MHz.



**Figure 6-5. ADC Analog Input Bandwidth Response**

### 6.3.3 Sampling Clock Input

The ADC3910Dx and ADC3910Sx has a single-ended sampling clock input. To maximize the ADC SNR performance, the external sampling clock can have low jitter with a high slew rate. The ADC3910Dx and ADC3910Sx can be AC or DC coupled externally. When AC coupling sampling clock needs to have a resistor divider such that the center voltage is around 0.9V and when DC coupling the sampling clock, center voltage needs to be around 0.9V as shown in Figure 6-6.

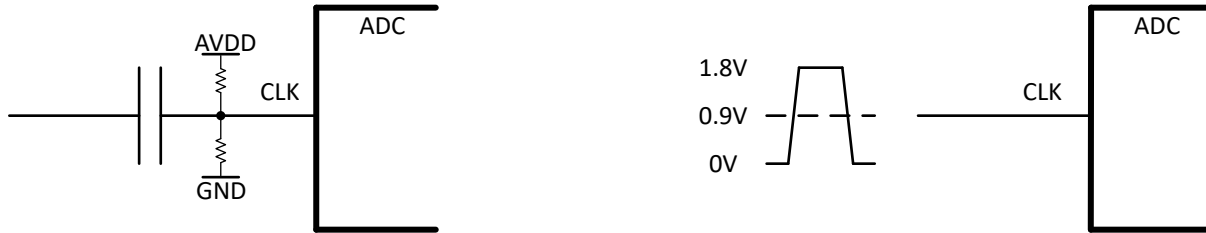


Figure 6-6. Sampling clock configuration: AC coupled (left) and DC coupled (right)

### 6.3.4 Voltage Reference

ADC3910Dx and ADC3910Sx by default is set to internal reference. For highest accuracy and lowest temperature drift, the ADC3910Dx and ADC3910Sx provides an option to supply a external reference voltage to the ADC. A 10  $\mu\text{F}$  and a 0.1  $\mu\text{F}$  ceramic bypass capacitor connected between VREF and GND pins, and placed as close to the pins as possible is recommended when using an external reference. Otherwise, the VREF pin should be connected to ground when using the internal reference. The internal reference circuitry of the ADC3910Dx and ADC3910Sx is shown in Figure 6-7.

#### Note

The voltage reference mode can be selected using SPI write in register in 0x30B.

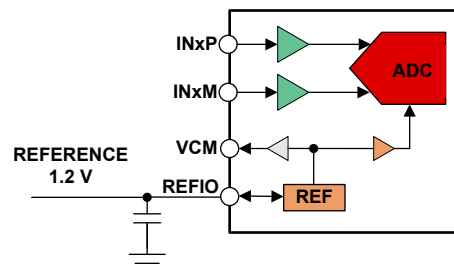
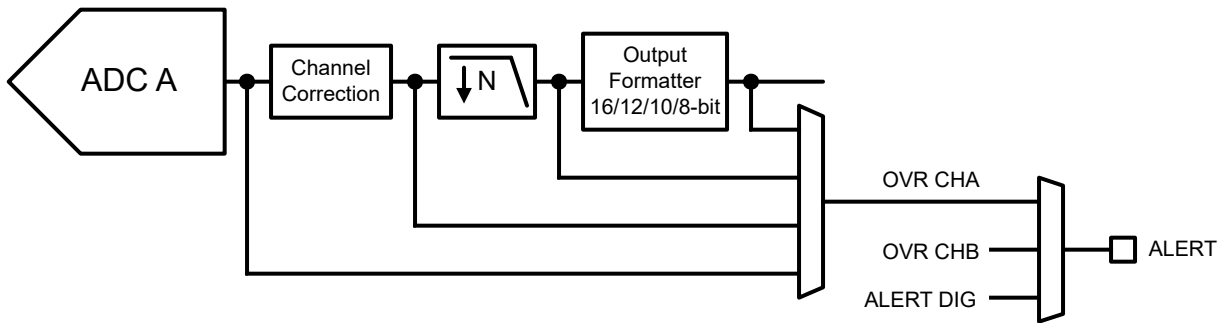


Figure 6-7. External 1.2 V reference

### 6.3.5 Over-range (OVR)

The ALERT by default is configured to trigger when either ADC channel A or ADC channel B detects a signal over-range on the input. The ALERT pin can also be configured via SPI write to register ALERT\_PIN\_SEL (0x09C) to ignore one of the ADC channels or to trigger when a digital alert is detected, including if an over-range is detected within a digital block. See the [Digital Alert](#) section to configure additional triggers in the digital features.



**Figure 6-8. Over-range block diagram**

### 6.3.6 Digital Features

#### 6.3.6.1 Digital Down Converter

The ADC3910Dx and ADC3910Sx has an optional dual on-chip digital down converters (DDC) that can be enabled via SPI register (0x0D4). It supports real decimation by 2, 4, 8, and 16. Real decimation operation is illustrated with an example in Figure 6-9. The output data rate is decimated. A decimation of 8 results in an output data rate  $F_{S,OUT} = F_S/8$  with a Nyquist zone of  $F_S/16$ .

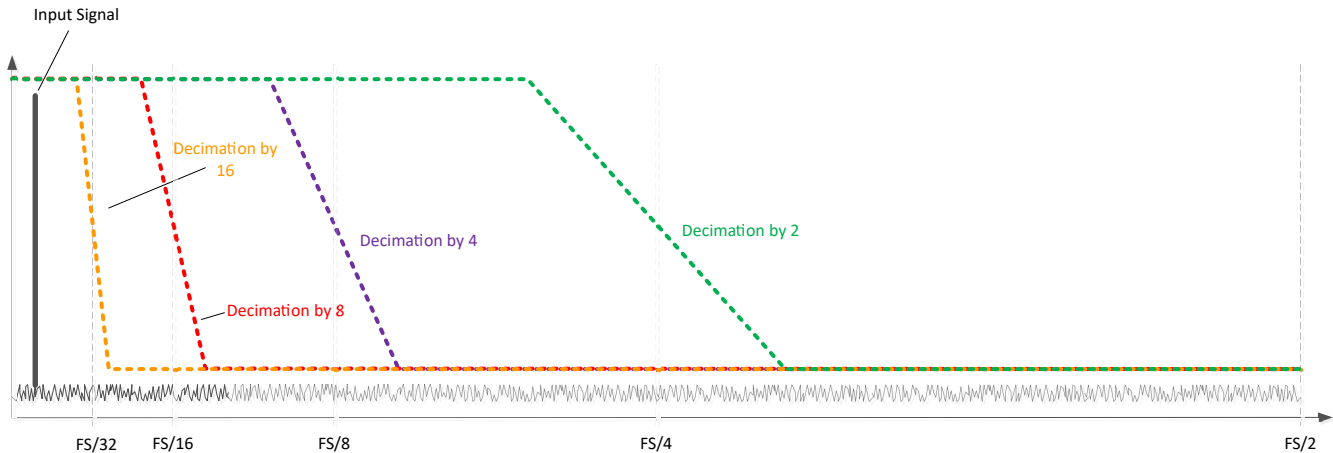


Figure 6-9. Real decimation illustration, default

##### 6.3.6.1.1 Digital Down Converter Data Select

Each digital comparator has the capability of selecting either channel with or without decimation data via SPI write (0x200, 0x203).

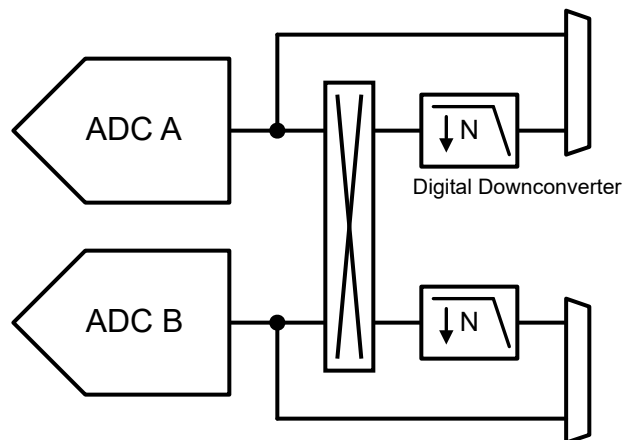


Figure 6-10. Digital down converter data multiplexer

##### 6.3.6.1.2 Decimation Filter

The ADC3910Dx and ADC3910Sx has a stop band rejection of at least 70dB, and a pass-band bandwidth of approximately 80%. Table 6-2 gives an overview of the pass-band bandwidth of the different decimation settings with respect to ADC sampling rate  $F_S$ .

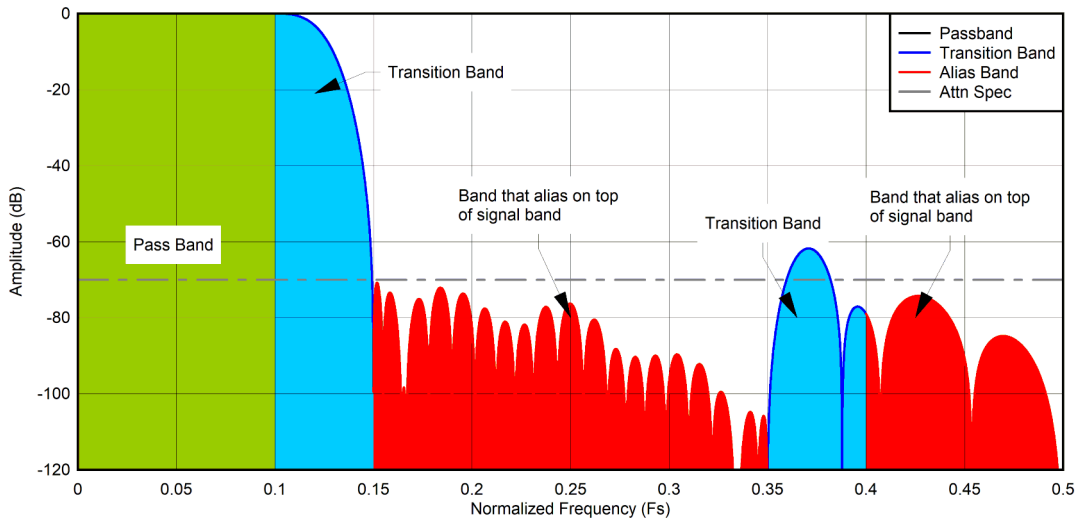
**Table 6-2. Decimation Filter Summary and Maximum Available Output Bandwidth**

REAL DECIMATION	DECIMATION SETTING (N)	OUTPUT RATE	OUTPUT BANDWIDTH	OUTPUT RATE (F <sub>S</sub> = 125MSPS)	OUTPUT BANDWIDTH (F <sub>S</sub> = 125MSPS)
Real	2	F <sub>S</sub> / 2	0.8 × F <sub>S</sub> / (2 × 2)	62.5MSPS	25MHz
	4	F <sub>S</sub> / 4	0.8 × F <sub>S</sub> / (4 × 2)	31.25MSPS	12.5MHz
	8	F <sub>S</sub> / 8	0.8 × F <sub>S</sub> / (8 × 2)	15.625MSPS	6.25MHz
	16	F <sub>S</sub> / 16	0.8 × F <sub>S</sub> / (16 × 2)	7.8125MSPS	3.125MHz

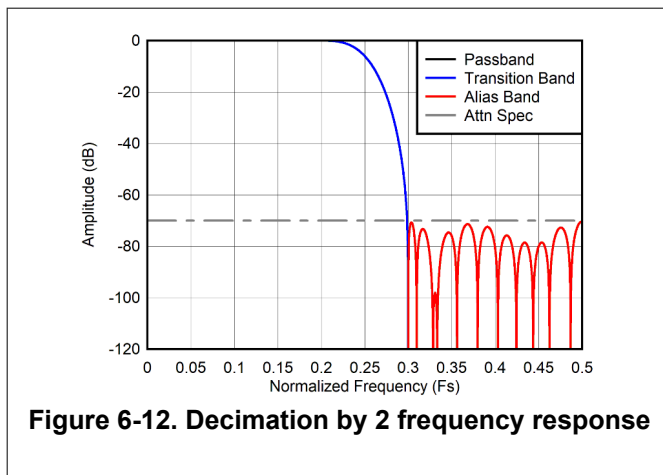
The decimation filter responses are normalized to the ADC sampling clock frequency F<sub>S</sub> and illustrated in Figure 6-12 to Figure 6-19. They are interpreted as follows:

Each figure contains the filter pass-band, transition band(s) and alias or stop-band(s) as shown in Figure 6-11. The x-axis shows the offset frequency normalized to the ADC sampling rate F<sub>S</sub>.

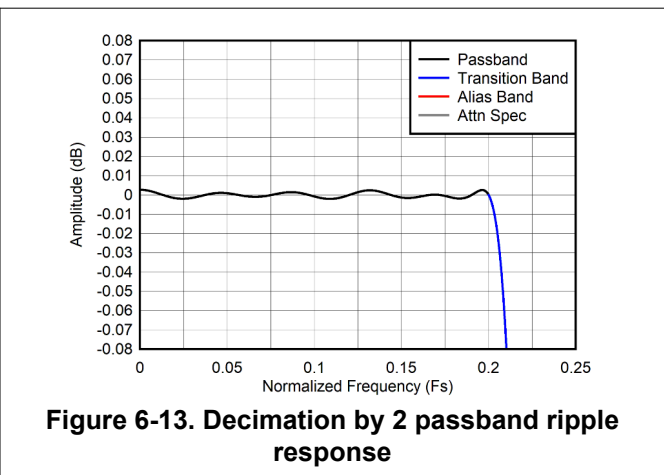
For example, in the divide-by-4 setup, the output data rate is F<sub>S</sub> / 4 with a Nyquist zone of F<sub>S</sub> / 8 or 0.125 × F<sub>S</sub>. The transition band (colored in blue) is centered around 0.125 × F<sub>S</sub> and the alias transition band is centered at 0.375 × F<sub>S</sub>. The stop-bands (colored in red), which alias on top of the pass-band, are centered at 0.25 × F<sub>S</sub> and 0.5 × F<sub>S</sub>.



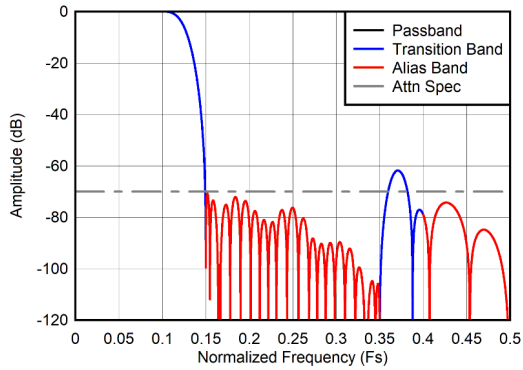
**Figure 6-11. Interpretation of the Decimation Filter Plots**



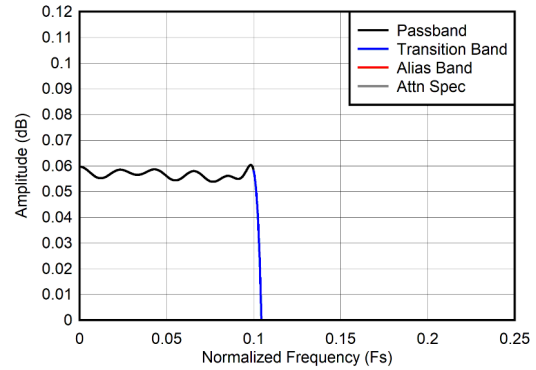
**Figure 6-12. Decimation by 2 frequency response**



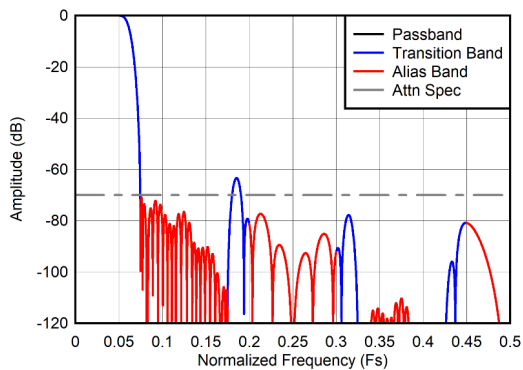
**Figure 6-13. Decimation by 2 passband ripple response**



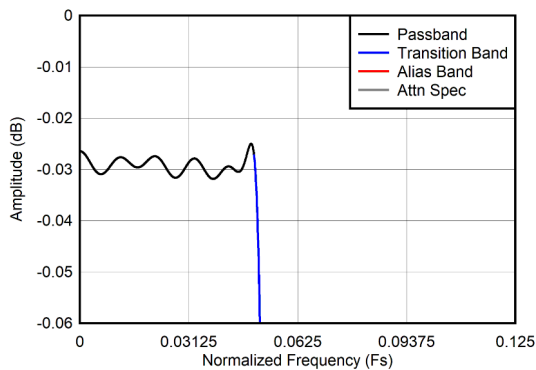
**Figure 6-14. Decimation by 4 frequency response**



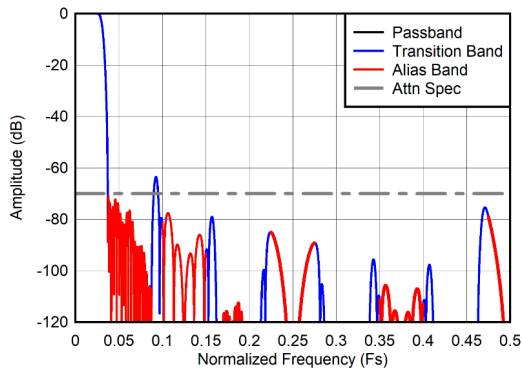
**Figure 6-15. Decimation by 4 passband ripple response**



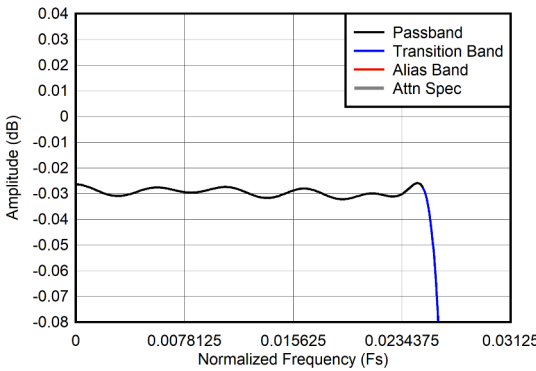
**Figure 6-16. Decimation by 8 frequency response**



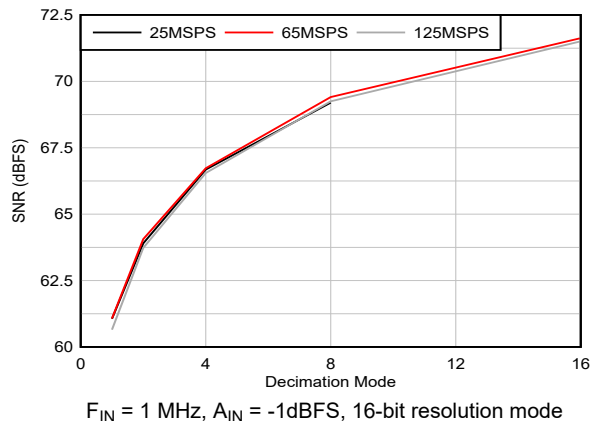
**Figure 6-17. Decimation by 8 passband ripple response**



**Figure 6-18. Decimation by 16 frequency response**



**Figure 6-19. Decimation by 16 passband ripple response**



**Figure 6-20. SNR Performance vs Decimation Mode**

#### 6.3.6.1.3 DDC Over-range

The ADC3910Dx and ADC3910Sx has an overrange indicator that can be enabled via SPI write to register 0x205-0x206 to protect the analog inputs from being saturated for extended period of time since latency is increased with decimation. When the alert pin is asserted, it stays high for one clock cycle of  $F_{OUT}$  ( $F_S$  divided by decimation factor) and then de-asserted.

#### 6.3.6.1.4 Output Formatting with Decimation

In serial CMOS mode, the ADC3910Dx and ADC3910Sx has a configurable output data mapping. Default bit size in serial CMOS is 10 bits wide and interface default is set to DDR. Interface options are double data rate (DDR), half double data rate (HDDR), and single data rate (SDR) via SPI write to register 0x098.

By default DDR mode clocks output data by alternating channel A data on the rising and channel B data on the falling edge of DCLK on the same lane. This behavior can be changed to clock all of channel A data first and then channel B data via SPI write to DDR\_MODE (0x0A6). HDDR mode clocks channel A data on separate output lanes from channel B data via SPI write to HDDR\_EN (0x098).

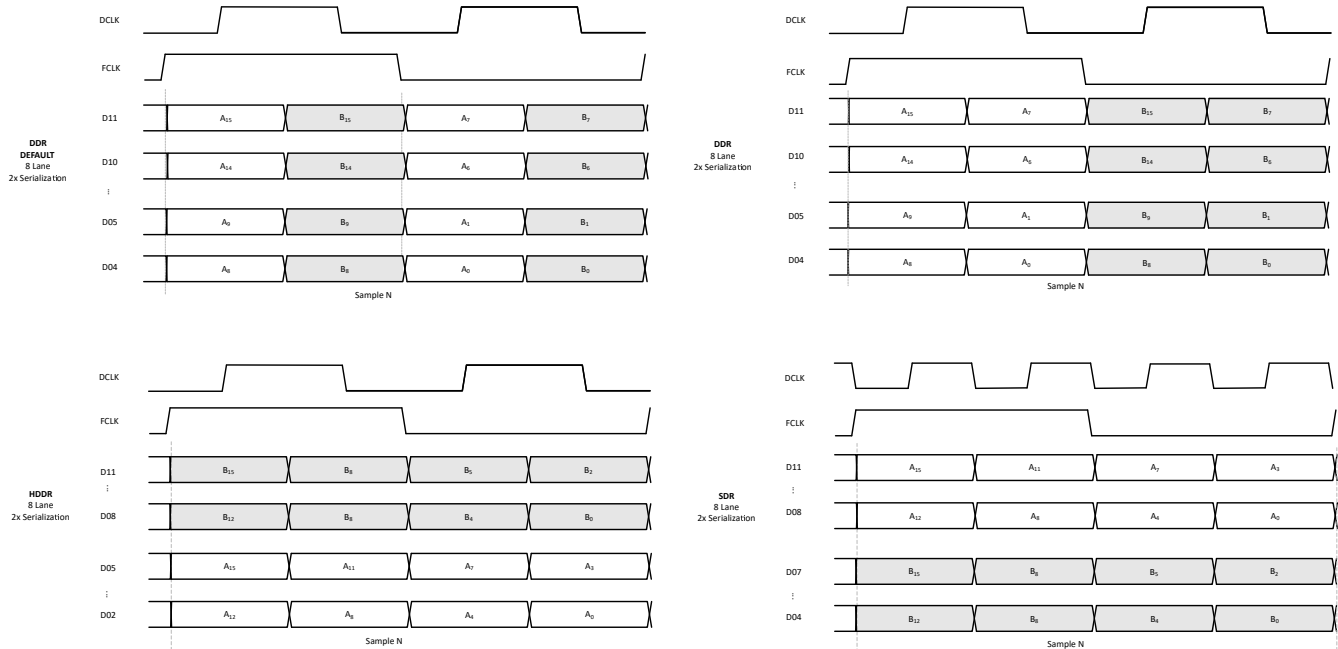
SDR mode clocks data only on rising edge; therefore, to clock both data samples in a cycle, requires double the data clock speed. The following diagrams show the different available configurations that can be programmed, and [Table 6-3](#) shows actual data and clock rates.

**Table 6-3. Serial CMOS Lane Rate Examples with Real Decimation and 12/16-bit Output Resolution**

Output Resolution	Decimation	Lanes	Serialization	DCLK	DCLK Divider	FCLK	
Register 0xA7	Register 0x200	Registers 0xAE...B3	Register 0xA6	Register 0xA8		Register 0x88	
8 bits	Bypass	8	1	$F_S$	/1	N/A	
10 bits		10	1	$F_S$	/1	N/A	
12 bits		12	1	$F_S$	/1	N/A	
	/2	12	1	$F_S / 2$	/2	N/A	
	/4	12	1	$F_S / 4$	/4	N/A	
	/8	12	1	$F_S / 8$	/8	N/A	
16 bits	/16	12	1	$F_S / 16$	/16	N/A	
	/2	8	2	$F_S$	/2	$F_S / 2$	
		/4	8	2	$F_S / 2$	/4	$F_S / 2$
			4	4	$F_S$		$F_S / 4$
	/8	8	2	$F_S / 4$	/8	$F_S / 2$	
		4	4	$F_S / 2$		$F_S / 4$	
		2	8	$F_S$		$F_S / 8$	
	/16	8	2	$F_S / 8$	/16	$F_S / 2$	
		4	4	$F_S / 4$		$F_S / 4$	
2		8	$F_S / 2$	$F_S / 8$			

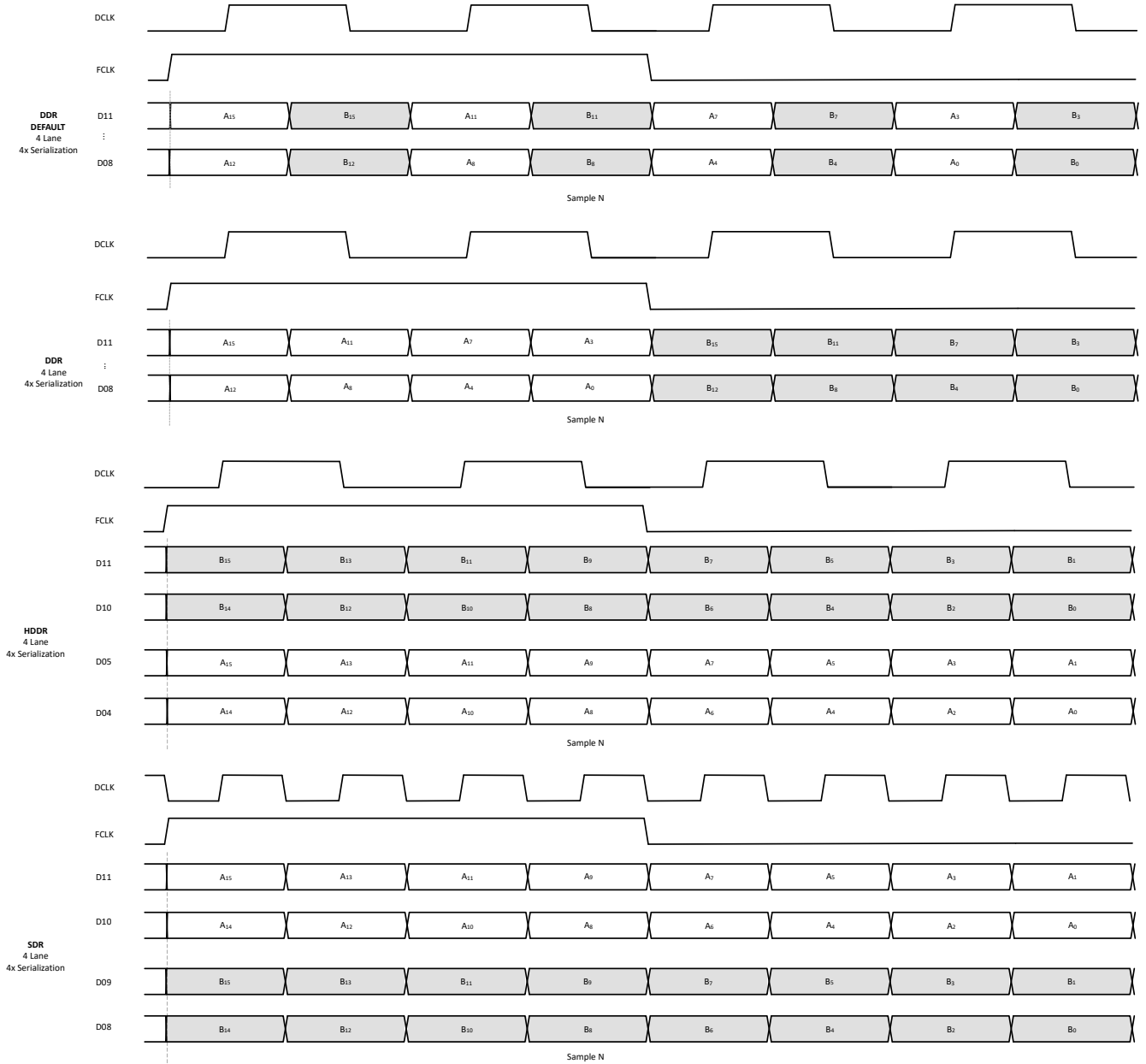
**Note**

16 bit resolution does not support a serialization factor of 1.

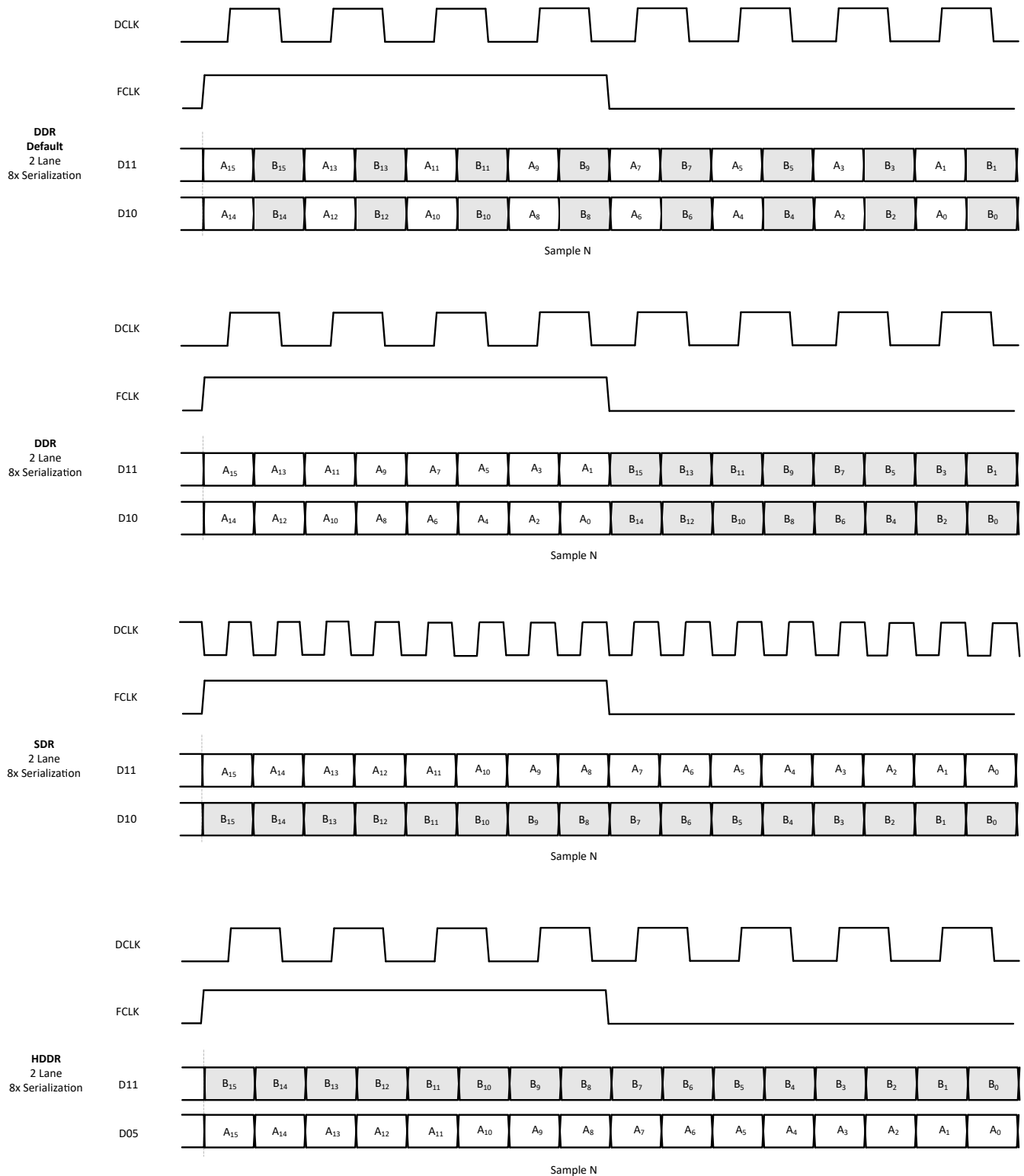


**Figure 6-21. 16 Bit, 8 Lanes, 2x Serialization**





**Figure 6-22. 16 Bit, 4 Lanes, 4x Serialization**



**Figure 6-23. 16 Bit, 2 Lanes, 8x Serialization**

### 6.3.6.2 Digital Comparator

The ADC3910Dx and ADC3910Sx has two internal digital comparators. The digital comparator controls the output ALERT pin buffer. ALERT pin can be configured as open-drain or push-pull using the ALERT\_OD (0x090) register. Figure 6-24 shows the block diagram for the digital comparator.

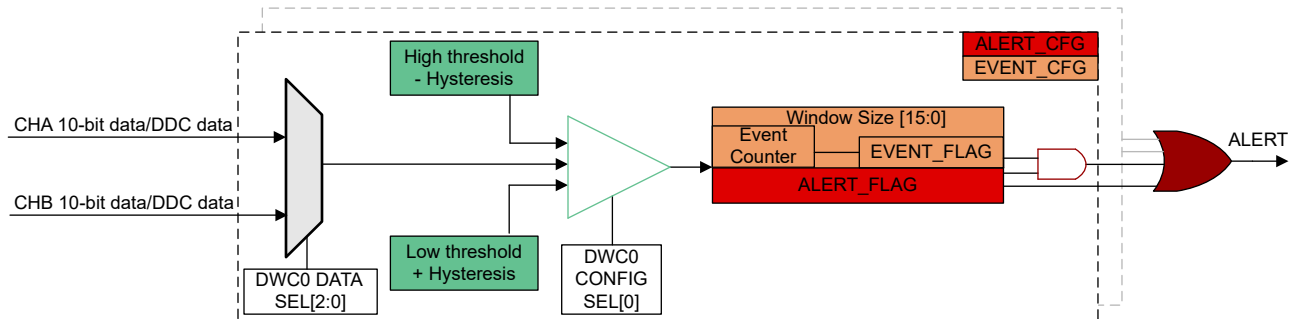


Figure 6-24. Digital Comparator Block Diagram

#### 6.3.6.2.1 Comparator Data Select

Each digital comparator has the capability of selecting either channel with or without decimation data via SPI write (0x201, 0x203).

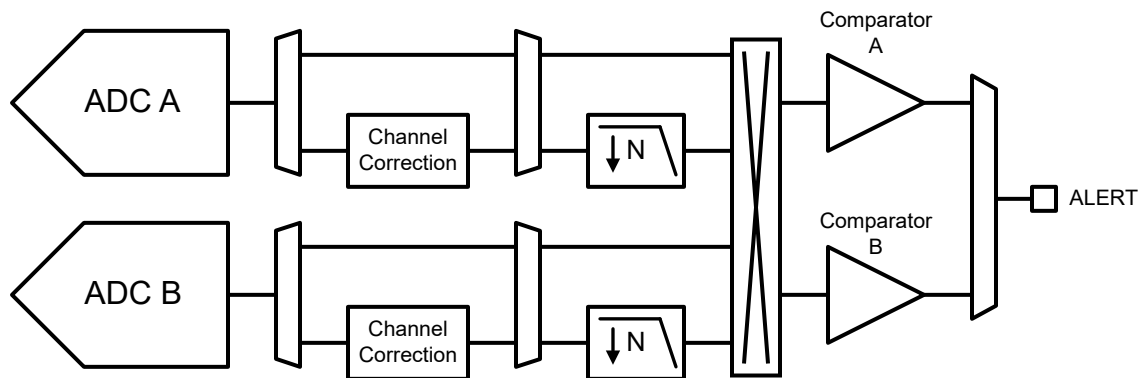


Figure 6-25. Comparator multiplexer

#### 6.3.6.2.2 Comparator High and Low Threshold

The digital comparator high-side threshold, low-side threshold and hysteresis (optional) parameters are independently programmed for each digital comparator (COMP\_THRESHOLD\_HI\_CHx, COMP\_THRESHOLD\_LO\_CHx, COMP\_HYSTERESIS\_CHx) via SPI write to registers 0x0C8-0x0D3.

#### 6.3.6.2.3 Comparator Configuration Compare Mode

The digital comparator can be configured to either standard compare or slew compare via SPI write SLEW\_CHx (0x0D3).

*Standard Compare* level based:

- COMP\_THRESHOLD\_HI\_CHx - COMP\_HYSTERESIS\_CHx
- COMP\_THRESHOLD\_LO\_CHx + COMP\_HYSTERESIS\_CHx

*Slew Compare* to detect based on difference between subsequent samples:

- Current sample - Previous sample > COMP\_THRESHOLD\_HI\_CHx
- Current sample - Previous sample < COMP\_THRESHOLD\_LO\_CHx

**Note**

Hysteresis must be set to 0 in slew compare mode.

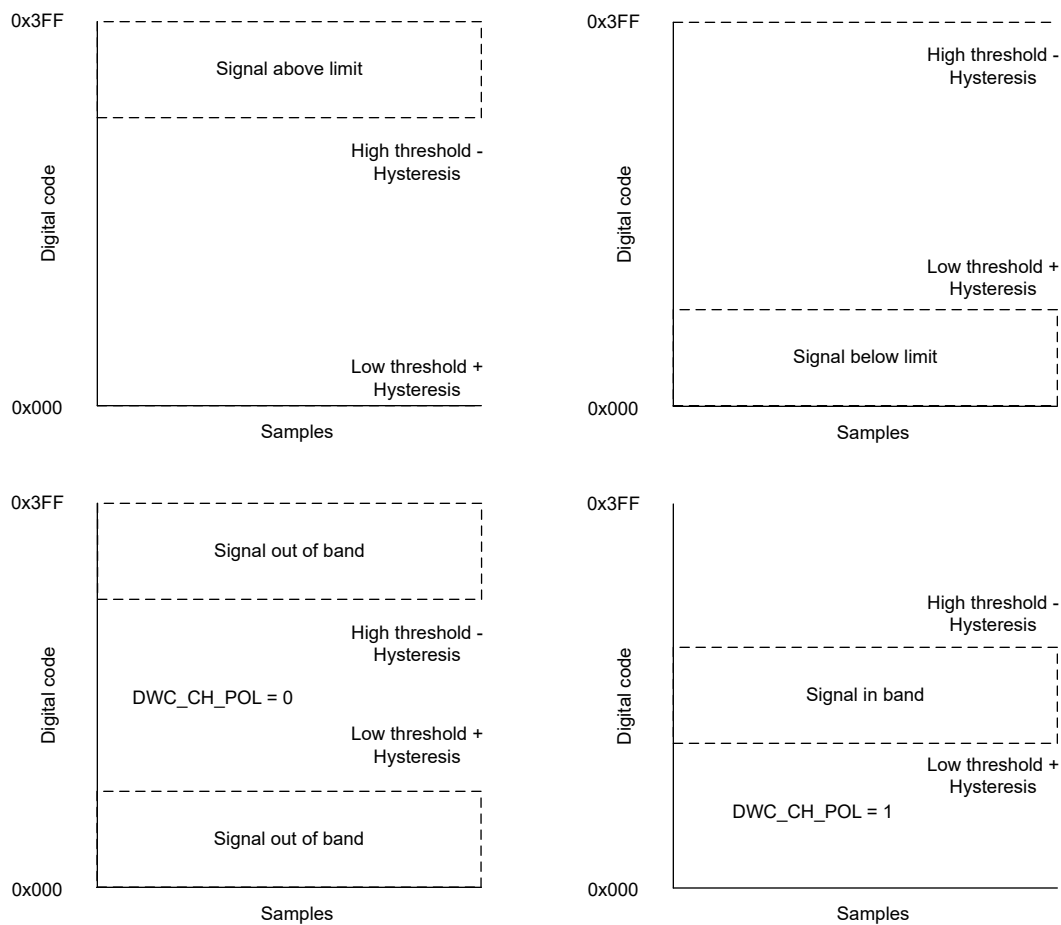
**6.3.6.2.4 Comparator Event Configuration**

Figure 6-26 shows the digital comparator monitor events that can be configured as triggers.

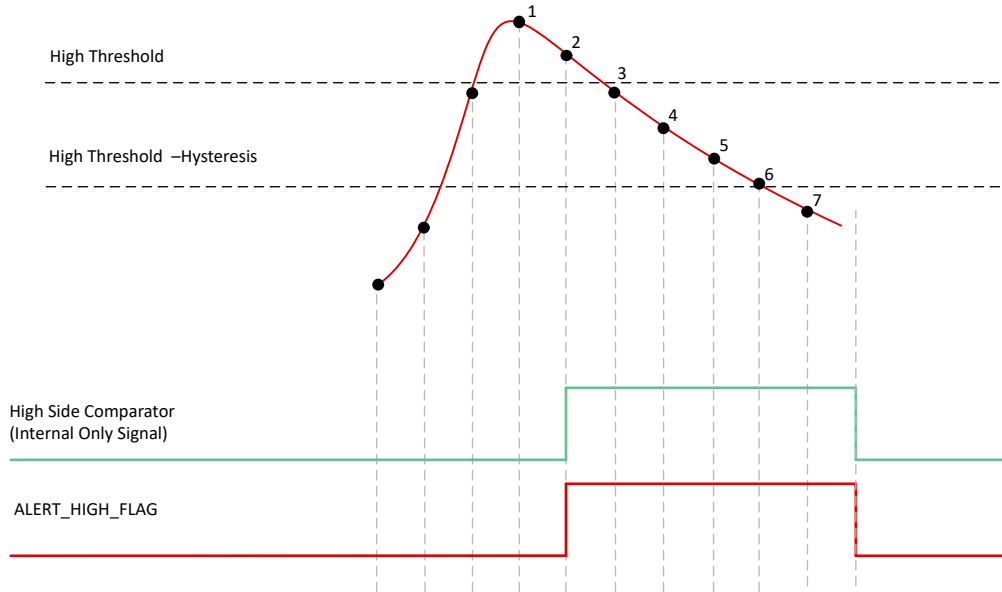
The digital comparator has two options for asserting ALERT pin: event-based or window-based monitoring.

In event-based monitoring, the ALERT pin is asserted when an event is triggered based on the comparator configuration seen in Figure 6-27.

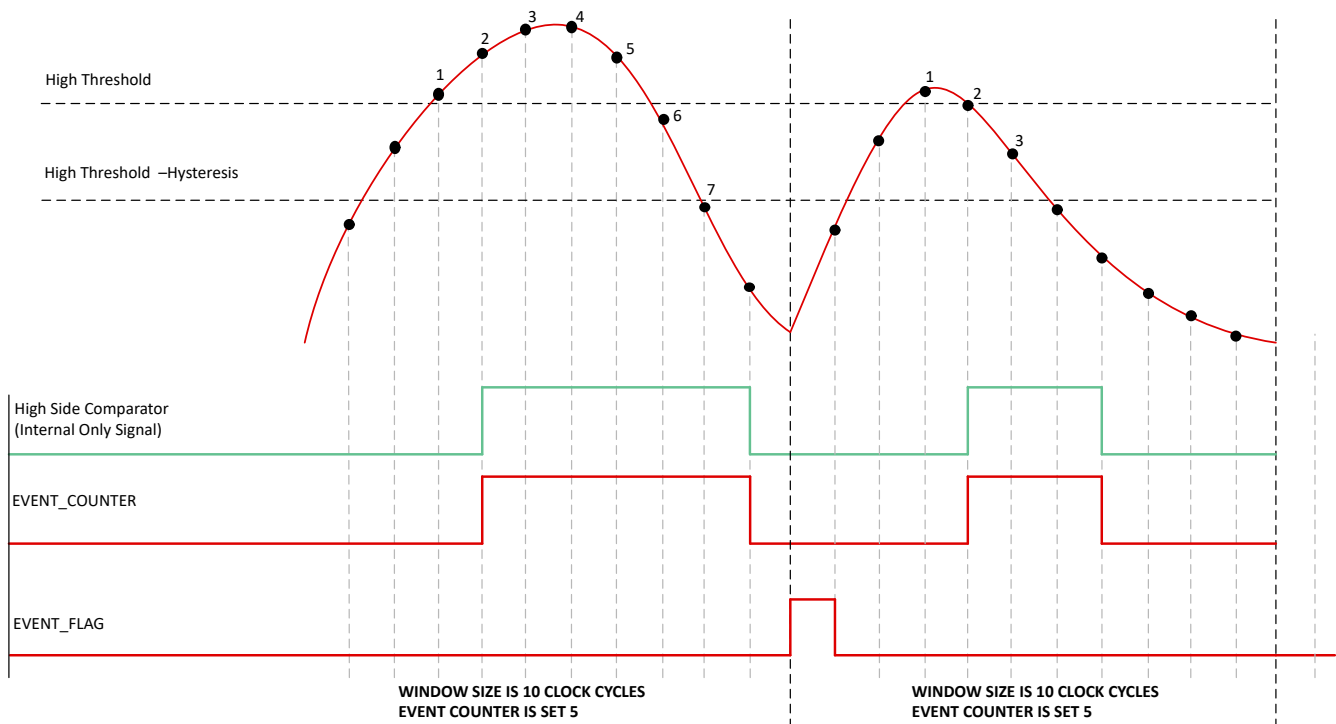
In window-based monitoring, the ALERT pin is only asserted when the number of event triggers recorded in CNT\_MODE\_x (0x1EA) crosses the threshold set in SPI register ALERT\_THRESHOLD (0x1EC-0x1ED). Window-based monitoring is enabled in SPI register CNT\_EN (0x1EA). Figure 6-28 shows an example of window-based monitoring.



**Figure 6-26. Digital Comparator Event Monitoring**



**Figure 6-27. Event Monitoring**

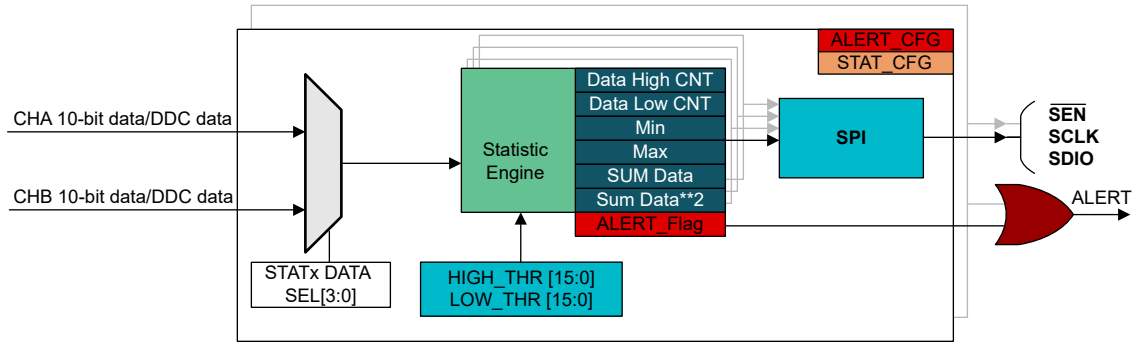


**Figure 6-28. Window Monitoring**

### 6.3.6.3 Statistics Engine

The ADC3910Dx and ADC3910Sx has two internal statistic engines that can be enabled via SPI write to register 0x1A4. It collects the following statistics within a window when enabled:

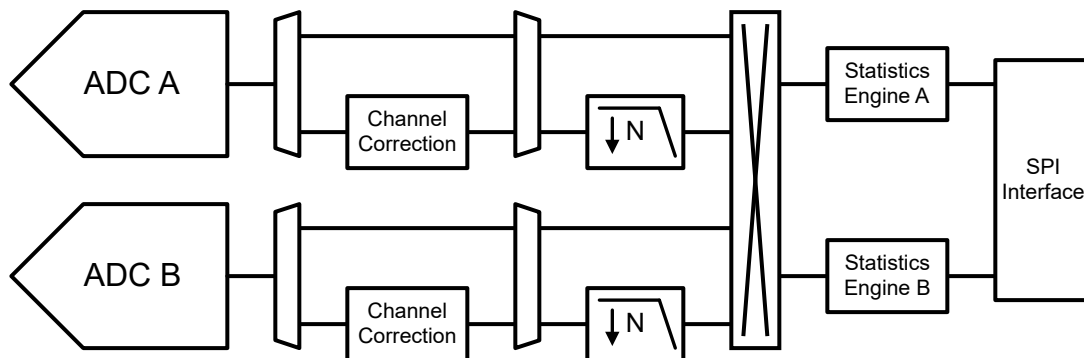
- Count samples above or below high and low thresholds
- Minimum and maximum sample values
- Summation of samples
- Summation of the squares of samples for power measurements



**Figure 6-29. Statistics Engine Block Diagram**

### 6.3.6.3.1 Statistics Engine Data Select

Each statistics engine has the capability of selecting either channel with or without decimation data via SPI write (0x201, 0x204).



**Figure 6-30. Statistics engine data multiplexer**

### 6.3.6.3.2 Window Configuration

The window size is configured in `STATS_WINDOW_SIZE_CHx` (0x1A0-0x1A3) in steps of 256 samples. Minimum window size is 256 samples up to a maximum of  $256 * 2^{16}$  samples. The device records the statistics for the current window (N) and up to 3 previous windows (N-1, N-2, N-3). By default the statistics engine continuously collects data when enabled and the ADCs are sampling or the single shot mode enabled in `1SHOT_CHx` (0x1A4) to collect data over a single window.

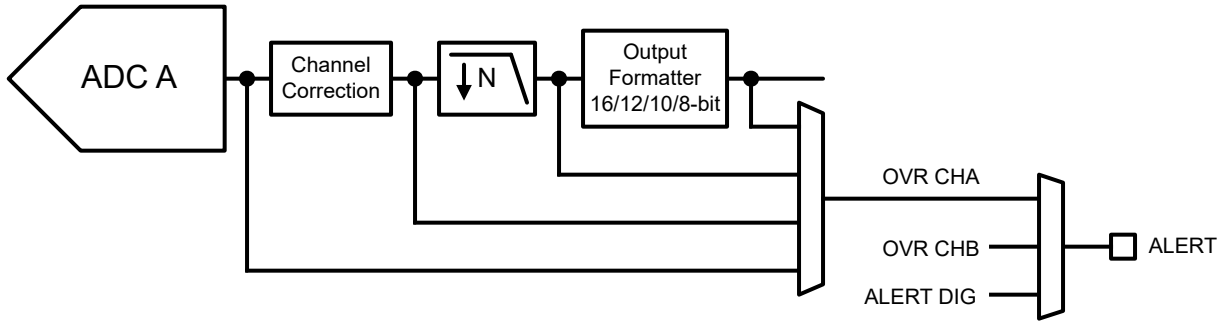
### 6.3.6.4 Digital Alerts

The digital alert functionality can be used in conjunction with the comparator to monitor input signal conditions or to detect over-ranging in the ADC or digital blocks. The alert function can be configured in several different ways via the SPI registers. These registers are enabled with bit masks so the behavior of multiple sources can be used to trigger the ALERT pin.

Available Alert triggers:

- Greater than, equal to, or less than either comparator's high or low threshold
- All ones or all zeros detected by either comparator
- Statistics engine window complete
- Over-range in the ADC, channel corrections, decimation or output formatter blocks

See register 0x1B4 for full list of available alert triggers.



**Figure 6-31. Digital alert block diagram**

### 6.3.7 Digital Interface

The ADC39xx family supports multiple CMOS output modes - parallel DDR/HDDR, SDR, and serialized CMOS output formats. The output data can be configured to two's complement (default) or offset binary via SPI write (0x30A).

#### 6.3.7.1 Parallel CMOS Output

The ADC3910Dx and ADC3910Sx supports double data rate (DDR), half double data rate (HDDR), and single data rate (SDR). In DDR/HDDR mode, the device generates the output data clock along with inverse data clock. Single channel ADCs can use SDR mode where data is output on the rising edge of the clock.

By default, DDR mode clocks output data by alternating channel A data on the rising and channel B data on the falling edge on the same lane. This behavior can be changed to clock all of channel A data first and then channel B data via SPI write to DDR\_MODE (0x0A6). HDDR mode clocks channel A data on separate output lanes from channel B data via SPI write to HDDR\_EN (0x098).

For receivers that cannot clock data on the falling edge of data clock, inverse data clock can be used to clock data on rising edge.

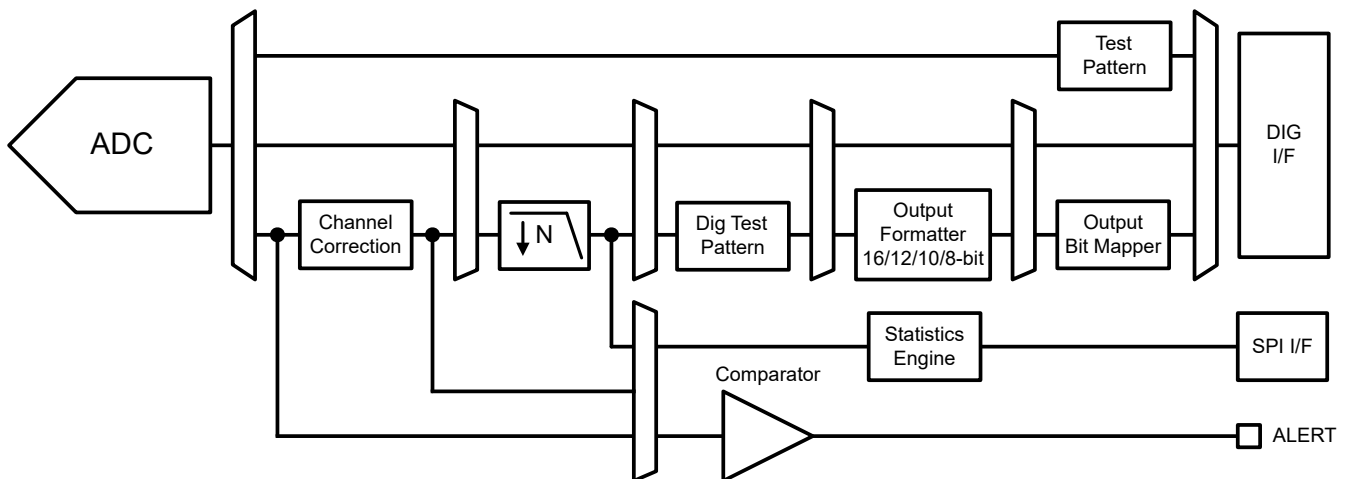
See [Section 5.11](#) section for timing diagrams for parallel CMOS output.

#### 6.3.7.2 Serialized CMOS Output

In this operation, the output data is serialized and transmitted over fewer lanes. Due to CMOS output speed limitation, the operation is only available for reduced output data rates. See the [Section 6.3.6.1.4](#) section for details on serial CMOS output.

### 6.3.8 Test Patterns

To enable in-circuit testing of the digital interface, the following test patterns are supported and enabled via SPI register writes. There are 2 test pattern generators available in the device. One located in the digital block when using the DDC, statistics engine or comparator functions and a second available in low latency (digital bypassed) mode.



**Figure 6-32. Test pattern block diagram**



### 6.3.8.1 Bypass Test Pattern

The test pattern for low latency mode (digital bypassed) is enabled in SPI register TEST\_PAT\_CHx (0x91) and configured in SPI register TEST\_PATTERN\_CHx (0x092).

### 6.3.8.2 Digital Test Pattern

The digital test pattern is enabled in SPI register DIG\_PAT\_EN (0x0A6) and configured in SPI registers DIG\_PATTERN\_MODE\_CHx (0x0A1) and DIG\_PATTERN\_CHx (0x0A2-0x0A5). The test pattern is 16 bits wide. In 10 bit mode the MSB 10 bits are send out.

- RAMP Pattern: The step size can be configured as 1 (at 16 bit level) or the value assigned written in DIG\_PAT\_CHx. To generate a ramp with step size of 1 in 10 bit mode the step size must be programmed to 64 in DIG\_PAT\_CHx.
- Custom Pattern: Configured in the DIG\_PAT\_CHx register
- Toggle Pattern: Either toggle between DIG\_PAT\_CHx and bitwise inversion of DIG\_PAT\_CHx or toggle between DIG\_PAT\_CHx and 0.

## 6.4 Device Functional Modes

### 6.4.1 Normal Operation

In normal operating mode, the entire ADC full scale range gets converted to a digital output with 10-bit resolution. The output is available in as little as 1 clock cycle on the digital outputs.

### 6.4.2 Power Down Options

A global or fast power down mode can be enabled via SPI as well as using the power down pin (OENZ/PDN). There is an internal pull-down resistor on the OENZ/PDN input pin, and the pin is active HIGH. The pin needs to be pulled high externally to enter power down mode. The SPI register map provides the capability to enable or disable individual blocks directly or via PDN pin mask to trade off power consumption vs wake up time as shown in the [Timing Requirements](#) table.

## 6.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI). After initial power up, the default operating configuration is shown in Table 6-4.

**Table 6-4. Default device configuration after power up**

FEATURE	DEFAULT
Signal Input	Differential
Reference	Internal
Channel Corrections	Disabled
Decimation	Disabled
Comparators	Disabled
Statistics Engine	Disabled
Interface	DDR, 10 lanes
Output Format	Two's Complement

### 6.5.1 Configuration using the SPI interface

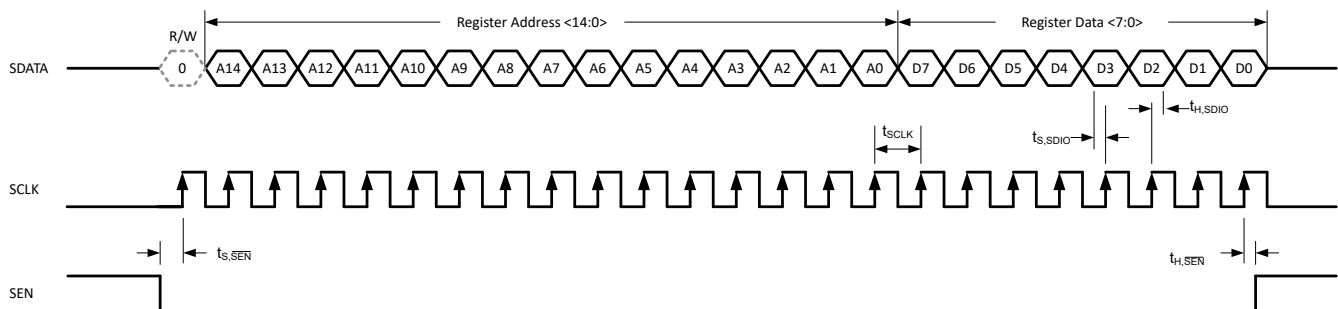
The device has a set of internal registers that can be accessed by the serial interface formed by the  $\overline{\text{SEN}}$  (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when  $\overline{\text{SEN}}$  is low. Serial data input are latched at every SCLK rising edge when  $\overline{\text{SEN}}$  is active (low). The serial data is loaded into the register at every 16th SCLK rising edge when  $\overline{\text{SEN}}$  is low. When the word length exceeds a multiple of 16bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active  $\overline{\text{SEN}}$  pulse. The interface can function with SCLK frequencies from 20MHz down to low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

#### 6.5.1.1 Register Write

The internal registers can be programmed following these steps:

1. Drive the  $\overline{\text{SEN}}$  pin low
2. Set the R/W bit to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[14:0]) whose content is written
4. Write the 8-bit data that are latched in on the SCLK rising edges

Figure 6-33 show the timing requirements for the serial register write operation.



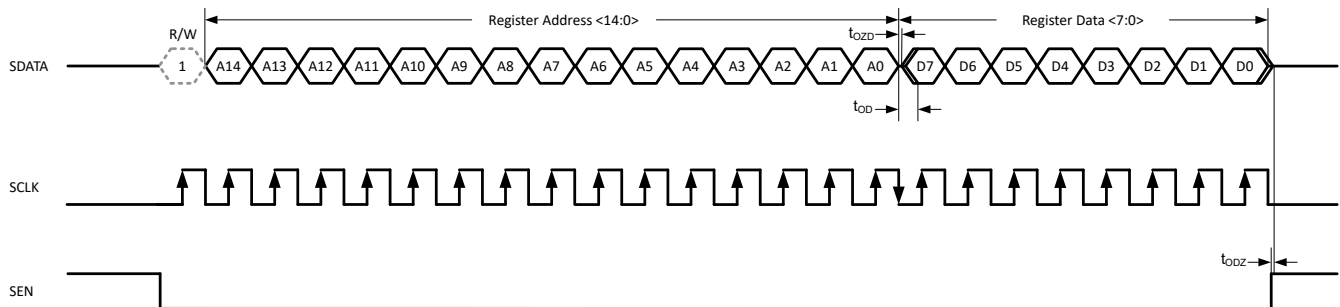
**Figure 6-33. Serial Register Write Timing Diagram**

### 6.5.1.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the  $\overline{\text{SEN}}$  pin low
2. Set the R/W bit to 1. This setting disables any further writes to the registers. Initiate a serial interface cycle specifying the address of the register (A[14:0]) whose content must be read
3. The device latches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
4. The external controller can capture the contents on the SCLK rising edge

Figure 6-34 show the timing requirements for the serial register Read operation.



**Figure 6-34. Serial Register Read Timing Diagram**

## 6.6 Register Maps

[Register Descriptions](#) lists the SPI registers. All register offset addresses not listed in [Register Descriptions](#) should be considered as reserved locations and the register contents should not be modified.

[Table 6-6](#) shows the codes that are used for access types in this section.

### 6.6.1 Register Descriptions

**Table 6-5. DEVICE Registers**

Address	Register Name
0h	RESET
38h	CFG_ALERT
39h	SPARE_REG
84h	INTERLEAVE
85h	REF_EQ
88h	DEV_CFG_1
89h	DEV_CFG_2
8Ah	CLK_CFG_1
8Bh	CLK_CFG_2
8Ch	PDN_CFG
8Dh	DEV_CFG_3
8Eh	CLK_CFG_3
8Fh	CLK_CFG_4
90h	PIN_CFG_1
91h	TEST_PAT_CFG
91h	TEST_PATTERN_CFG
92h	TEST_PATTERN_CHB_7:0
93h	TEST_PATTERN_CHB_13:8
94h	TEST_PATTERN_CHA_7:0
95h	TEST_PATTERN_CHA_13:8
97h	GLOBAL_PDN
98h	INTERFACE_CFG_1
9Ch	INTERFACE_CFG_2
9Eh	HFSB_FPDN_CFG
A0h	INTERFACE_CFG_3
A1h	DIG_PATTERN_EN
A2h	DIG_PATTERN_CHA_7:0
A3h	DIG_PATTERN_CHA_15:8
A4h	DIG_PATTERN_CHB_7:0
A5h	DIG_PATTERN_CHB_15:8
A6h	INTERFACE_CFG_4
A7h	OUTPUT_DATA_WIDTH
A8h	DCLK_DIVIDER
A Eh	OUTPUT_BIT_MAPPER_D0_D1
A Fh	OUTPUT_BIT_MAPPER_D2_D3
B0h	OUTPUT_BIT_MAPPER_D4_D5
B1h	OUTPUT_BIT_MAPPER_D6_D7
B2h	OUTPUT_BIT_MAPPER_D8_D9
B3h	OUTPUT_BIT_MAPPER_D10_D11

**Table 6-5. DEVICE Registers (continued)**

Address	Register Name
B6h	ROUND
C8h	COMP_THRESHOLD_HI_CHA_7:0
C9h	COMP_THRESHOLD_HI_CHA_11:8
CAh	COMP_THRESHOLD_HI_CHB_7:0
CBh	COMP_THRESHOLD_HI_CHB_11:8
CCh	COMP_THRESHOLD_LO_CHA_7:0
CDh	COMP_THRESHOLD_LO_CHA_11:8
CEh	COMP_THRESHOLD_LO_CHB_7:0
CFh	COMP_THRESHOLD_LO_CHB_11:8
D0h	COMP_HYSTERESIS_CHA_7:0
D1h	COMP_HYSTERESIS_CHA_11:8
D2h	COMP_HYSTERESIS_CHB_7:0
D3h	COMP_HYSTERESIS_CHB_11:8
D3h	COMP_SLEW
D4h	DECIMATION
D5h	PROG_GAIN_CHA
D6h	PROG_GAIN_CHB
D8h	IL_GAIN_CHA_7:0
D9h	IL_GAIN_CHA_15:8
DAh	IL_GAIN_CHB_7:0
DBh	IL_GAIN_CHB_15:8
DCh	OFFSET_CHA_7:0
DDh	OFFSET_CHA_15:8
DEh	OFFSET_CHB_7:0
DFh	OFFSET_CHB_15:8
E0h	CH_CORR_EN
200h	DDC_CFG_1
201h	STATS_COMP_DATA_SEL
202h	OUTPUT_DATA_SEL
203h	COMP_DDC_DATA_SEL
204h	OUTPUT_STATS_DATA_SEL
205h	OVR_CHB
206h	OVR_CHA
304h	CLK_TIM_ADJ_CHA
305h	CLK_TIM_ADJ_CHB
306h	DCLK_DLL_PD
307h	DIG_INPUT_CFG
309h	BUF_VCM_CURR
30Ah	BUF_CURR
30Bh	DEV_CFG_4
484h	GBL_CLK_CFG_1
4BEh	GBL_CLK_CFG_2
4BFh	GBL_CLK_CFG_3

Complex bit access types are encoded to fit into small table cells. [Table 6-6](#) shows the codes that are used for access types in this section.

**Table 6-6. Device Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 6.6.1.1 RESET Register (Address = 0h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-7. RESET Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESET	W	0h	This bit resets all internal registers to the default values and self clears to 0.
6:0	RESERVED	R	0h	

### 6.6.1.2 CFG\_ALERT Register (Address = 38h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-8. CFG\_ALERT Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	CFG_ALERT	R	0h	Indicates that the device is ready to be configured. The user can poll this bit before starting the device configuration. Alternatively, the user can wait for a fixed time (2000 clock cycles) after reset release before triggering device configuration

### 6.6.1.3 SPARE\_REG Register (Address = 39h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-9. SPARE\_REG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	SPARE_REG	R/W	0h	This field has no functionality and can be used for validating SPI writes.

### 6.6.1.4 INTERLEAVE Register (Address = 84h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-10. INTERLEAVE Register Field Descriptions**

Bit	Field	Type	Reset	Description
2	INTERLEAVE	R/W	0h	Enables interleaving mode where channels A and B are both sampling channel A input and channel B clock is 180 degrees out of phase with respect to channel A to achieve a 2x sampling rate. Only applies to dual channel devices. 0b = Interleaving mode disabled 1b = Interleaving mode enabled
1:0	RESERVED	R	0h	

#### 6.6.1.5 REF\_EQ Register (Address = 85h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-11. REF\_EQ Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	REF_EQ	R/W	0h	Enable when using external reference to improve temperature tracking. Internal bandgap is expected to have 7 mV of variation across the device operating temperature. 0b = Reference equalization disabled 1b = Reference equalization enabled
5:0	RESERVED	R	0h	

#### 6.6.1.6 CLK\_RESET Register (Address = 87h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-12. CLK\_RESET Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5:0	RESERVED	R	0h	

#### 6.6.1.7 DEV\_CFG\_1 Register (Address = 88h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-13. DEV\_CFG\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	FCLK_EN	R/W	0h	Enables frame clock output on DCLKZ pin. Must be enabled in Serial CMOS mode. 0b = Frame clock output on DCLKZ pin disabled 1b = Frame clock output on DCLKZ pin enabled
6	CNL_PDN	R/W	0h	Powers down internal non-linearity correction. Useful for input frequencies above 100 MHz and reduces current by 0.5 mA. 0b = Non-linearity correction enabled 1b = Non-linearity correction powered down
5	BUF_CHB	R/W	0h	Reduces current to ADC channel B input buffer which reduces buffer bandwidth. Recommended for input signals below 25 MHz and reduces current consumption by 2 mA. 0b = Input buffer full power mode 1b = Input buffer low power mode
4	BUF_CHA	R/W	0h	Reduces current to ADC channel A input buffer which reduces buffer bandwidth. Recommended for input signals below 25 MHz. Reduces current consumption by 2 mA. 0b = Input buffer full power mode 1b = Input buffer low power mode

**Table 6-13. DEV\_CFG\_1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3:0	RESERVED	R	0h	

### 6.6.1.8 DEV\_CFG\_2 Register (Address = 89h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-14. DEV\_CFG\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DCLK_FL_DLY__0	R/W	0h	Adjust the delay on the falling edge of DCLK where T is the period of DCLK. 0b = No adjustment 1b = T/20 (T/10 with HFSB = 1) 1010b = -T/10 (-T/5 with HFSB = 1) 1011b = -T/20 (-T/10 with HFSB = 1)
6	DIG_DCLK	R/W	0h	By default CLK is DCLK for digital blocks. Enable when CLK and DCLK are different and DCLKIN is used. 0b = CLK used as DCLK for digital blocks 1b = DCLKIN used as DCLK for digital blocks
5	DIG_DATA	R/W	0h	Data from digital block used as output data. 0b = Digital data to output data disabled 1b = Digital data to output data enabled
4:0	RESERVED	R	0h	

### 6.6.1.9 CLK\_CFG\_1 Register (Address = 8Ah) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-15. CLK\_CFG\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	DIG_CLK_SEL	R/W	0h	By default CLK is DCLK for digital blocks. Enable when CLK and DCLK are different and DCLKIN is used. 0b = CLK used as CLK for digital blocks 1b = Relatched CLK using DCLKIN used as CLK for digital blocks
4	RESERVED	R	0h	
3	CHB_CLK	R/W	0h	Enable when only ADC channel A is disabled, ADC channel B is enabled and HDDR interface mode is used.
2:1	DCLK_RISE_DLY	R/W	0h	Adjust the delay on the rising edge of DCLK where T is the period of DCLK. 00b = No adjustment 01b = T/20 (T/10 with HFSB = 1) 10b = -T/10 (-T/5 with HFSB = 1) 11b = -T/20 (-T/10 with HFSB = 1)
0	DCLK_FL_DLY__1	R/W	0h	Adjust the delay on the falling edge of DCLK where T is the period of DCLK. 0b = No adjustment 1b = T/20 (T/10 with HFSB = 1) 10b = -T/10 (-T/5 with HFSB = 1) 11b = -T/20 (-T/10 with HFSB = 1)

### 6.6.1.10 CLK\_CFG\_2 Register (Address = 8Bh) [Reset = 00h]

Return to the [Summary Table](#).



**Table 6-16. CLK\_CFG\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:4	DCLKZ_RISE_DLY	R/W	0h	Adjust the delay on the rising edge of DCLKZ where T is the period of DCLK. 00b = No adjustment 01b = T/20 (T/10 with HFSB = 1) 10b = -T/10 (-T/5 with HFSB = 1) 11b = -T/20 (-T/10 with HFSB = 1)
3	RESERVED	R	0h	
2:1	DCLKZ_FALL_DLY	R/W	0h	Adjust the delay on the falling edge of DCLKZ where T is the period of DCLK. 00b = No adjustment 01b = T/20 (T/10 with HFSB = 1) 10b = -T/10 (-T/5 with HFSB = 1) 11b = -T/20 (-T/10 with HFSB = 1)
0	RESERVED	R	0h	

**6.6.1.11 PDN\_CFG Register (Address = 8Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-17. PDN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	CHA_PDN	R/W	0h	Powers down ADC channel A. Reduces current by 12 mA. 0b = ADC channel A enabled 1b = ADC channel A powered down
6	CHB_PDN	R/W	0h	Powers down ADC channel B. Reduces current by 12 mA. 0b = ADC channel B enabled 1b = ADC channel B powered down
5	MASK_REF	R/W	0h	Fast power down mask control for reference amplifier. 0b = Reference amplifier powered down when fast power down is exercised. 1b = Reference amplifier NOT powered down when fast power down is exercised.
4	MASK_VCM	R/W	0h	Fast power down mask control for VCM buffer. 0b = VCM buffer powered down when fast power down is exercised. 1b = Reference amplifier NOT powered down when fast power down is exercised.
3	MASK_DLL	R/W	0h	Fast power down mask control for CLK DLL and DCLK DLL. 0b = DLLs powered down when fast power down is exercised. 1b = DLLs NOT powered down when fast power down is exercised.
2	SDR_CHB_SEL	R/W	0h	Selects the channel data to be sent out in SDR interface mode. Enable SDR with Channel B output when asserted. 0b = Channel A data 1b = Channel B data
1:0	RESERVED	R	0h	

**6.6.1.12 DEV\_CFG\_3 Register (Address = 8Dh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-18. DEV\_CFG\_3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	FORMAT	R/W	0h	Output Data Format when digital features are bypassed. 0b = Two's Complement 1b = Offset binary
5:4	RESERVED	R	0h	

**Table 6-18. DEV\_CFG\_3 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	DCLKZ_DLL	R/W	0h	Swap DCLKZ_OUT to DCLK output of DLL 0b = DCLKZ_OUT to DCLKZ output of DLL 1b = DCLKZ_OUT to DCLK output of DLL
2	DCLK_DLL	R/W	0h	Swap DCLK_OUT to DCLKZ output of DLL 0b = DCLK_OUT to DCLK output of DLL 1b = DCLK_OUT to DCLKZ output of DLL
1	ALERT_POL	R/W	0h	ALERT pin polarity 0b = ALERT pin active high 1b = ALERT pin active low
0	RESERVED	R	0h	

#### 6.6.1.13 CLK\_CFG\_3 Register (Address = 8Eh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-19. CLK\_CFG\_3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:6	DCLK_SYNC	R/W	0h	Used for DDR and SDR interface modes 00b = DDR Clocking mode (DCLKZ is inversion of DCLK) 01b = DDR Clocking 1010b = SDR Clocking (DCLKZ is same as DCLK) 1011b = DCLK/DCLKZ off
5:2	RESERVED	R	0h	
1	ADLL_BYP	R/W	0h	Bypass analog DLL. Enable this setting when ADC clock frequency below 25MHz. Reduces current by 1mA. 0b = Normal operation 1b = Analog DLL bypassed
0	RESERVED	R	0h	

#### 6.6.1.14 CLK\_CFG\_4 Register (Address = 8Fh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-20. CLK\_CFG\_4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	DCLK_DLL	R/W	0h	Enable when digital features are used
3:0	RESERVED	R	0h	

#### 6.6.1.15 PIN\_CFG\_1 Register (Address = 90h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-21. PIN\_CFG\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	ALERT_OD	R/W	0h	Alert output pin mode 0b = Push-pull 1b = Open-drain
6:4	RESERVED	R	0h	

**Table 6-21. PIN\_CFG\_1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3:1	CLK_PIN_STRENGTH	R/W	0h	DCLK and DCLKZ output pin strength 000b = 15/15 (default) 001b = 13/15 010b = 11/15 011b = 9/15 100b = 7/15 101b = 5/15 110b = 3/15 111b = 1/15
0	RESERVED	R	0h	

#### 6.6.1.16 TEST\_PAT\_CFG Register (Address = 91h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-22. TEST\_PAT\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	DATA_PIN_STRENGTH	R/W	0h	D11 to D0 output pin strength 0000b = 15/15 (default) 0001b = 14/15 0010b = 13/15 0011b = 12/15 0100b = 11/15 0101b = 10/15 0110b = 9/15 0111b = 8/15 1000b = 7/15 1001b = 6/15 1010b = 5/15 1011b = 4/15 1100b = 3/15 1101b = 2/15 1110b = 1/15 1111b = 0/15 (Tri-state)

#### 6.6.1.17 TEST\_PATTERN\_CFG Register (Address = 91h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-23. TEST\_PATTERN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	TOGGLE_PAT	R/W	0h	Toggle mode for test pattern. Enable to toggle all lanes in SDR mode, disable in DDR mode. 0b = Disable test pattern toggle 1b = Enable test pattern toggle
5	TEST_PAT_B	R/W	0h	Enables the test pattern in register 0x0092 0b = Channel B test pattern disabled 1b = Channel B test pattern enabled
4	TEST_PAT_A	R/W	0h	Enables the test pattern in register 0x0094 0b = Channel A test pattern disabled 1b = Channel A test pattern enabled
3:0	RESERVED	R	0h	

#### 6.6.1.18 TEST\_PATTERN\_CHB\_7:0 Register (Address = 92h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-24. TEST\_PATTERN\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	TEST_PATTERN_CHB_7:0	R/W	0h	

#### 6.6.1.19 TEST\_PATTERN\_CHB\_13:8 Register (Address = 93h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-25. TEST\_PATTERN\_CHB\_13:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:0	TEST_PATTERN_CHB_13:8	R/W	0h	

#### 6.6.1.20 TEST\_PATTERN\_CHA\_7:0 Register (Address = 94h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-26. TEST\_PATTERN\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	TEST_PATTERN_CHA_7:0	R/W	0h	

#### 6.6.1.21 TEST\_PATTERN\_CHA\_13:8 Register (Address = 95h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-27. TEST\_PATTERN\_CHA\_13:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:0	TEST_PATTERN_CHA_13:8	R/W	0h	

#### 6.6.1.22 GLOBAL\_PDN Register (Address = 97h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-28. GLOBAL\_PDN Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	PDN	R/W	0h	Global power down via SPI. 0b = Global power down disabled 1b = Global power down enabled.
4:0	RESERVED	R	0h	

#### 6.6.1.23 INTERFACE\_CFG\_1 Register (Address = 98h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-29. INTERFACE\_CFG\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	OENZ_PDN	R/W	0h	Overwrites OENZ control pin as either global or fast power down 0b = OENZ control pin functions as output enable 1b = OENZ control pin functions as power down. Power down options in register 0x009C determine the power down mode.
6	RESERVED	R	0h	

**Table 6-29. INTERFACE\_CFG\_1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5	HDDR_EN	R/W	0h	Enable HDDR interface mode 0b = HDDR interface mode disabled 1b = HDDR interface mode enabled
4	SDR_EN	R/W	0h	Enable SDR interface mode 0b = SDR interface mode disabled 1b = SDR interface mode enabled
3:0	ALERT_PIN_STRENGTH	R/W	0h	ALERT output pin strength 0000b = 15/15 (default) 0001b = 14/15 0010b = 13/15 0011b = 12/15 0100b = 11/15 0101b = 10/15 0110b = 9/15 0111b = 8/15 1000b = 7/15 1001b = 6/15 1010b = 5/15 1011b = 4/15 1100b = 3/15 1101b = 2/15 1110b = 1/15 1111b = 0/15 (Tri-state)

#### 6.6.1.24 INTERFACE\_CFG\_2 Register (Address = 9Ch) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-30. INTERFACE\_CFG\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	OENZ_GPDN	R/W	0h	Overwrites OENZ control pin as global power down. Global power down supersedes fast power down. 0b = OENZ control pin functions as output enable 1b = OENZ control pin functions as global power down
5	OENZ_FPDN	R/W	0h	Overwrites OENZ control pin as fast power down. Global power down supersedes fast power down. 0b = OENZ control pin functions as output enable 1b = OENZ control pin functions as fast power down
4:2	RESERVED	R	0h	
1:0	ALERT_PIN_SEL	R/W	0h	Alert output pin function. By default the ALERT output pin monitors overranging at the ADC core. 00b = Channel A overrange (OVR CHA)    Channel B overrange (OVR CHB) 01b = Channel A overrange (OVR CHA) 10b = Channel B overrange (OVR CHB) 11b = Digital Alerts

#### 6.6.1.25 HFSB\_FPDN\_CFG Register (Address = 9Eh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-31. HFSB\_FPDN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
6:5	HFSB_CONFIG	R/W	0h	DCLK generation block control. Used when global HFSB is 0 (CLK is greater than 65 MSPS) and DCLK is less than 65 MSPS, e.g. decimation. Forces half speed mode on DCLK generation block. 00b = Half speed mode for DCLK disabled 11b = Half speed mode for DCLK enabled

**Table 6-31. HFSB\_FPDN\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
4	PDN_FAST	R/W	0h	Fast power down via SPI. 0b = Fast power down disabled 1b = Fast power down enabled. Power down mask (register 0x008C) determines which internal blocks are powered down.
3:0	RESERVED	R	0h	

#### 6.6.1.26 INTERFACE\_CFG\_3 Register (Address = A0h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-32. INTERFACE\_CFG\_3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	CHB_SWAP	R/W	0h	Selects the channel data to send on Channel B output. Applicable in DDR interface mode and only available when digital enabled. 0b = Channel B data on channel B output 1b = Channel A data on channel B output
4	CHA_SWAP	R/W	0h	Selects the channel data to send on Channel A output. Applicable in DDR interface mode and only available when digital enabled. 0b = Channel A data on channel A output 1b = Channel B data on channel A output
3	OENZ_PIN_VAL	R/W	0h	Value to be overwritten on OENZ pin. Must enable OENZ overwrite in register 0x00A0, bit 2.
2	OENZ_PIN_OW	R/W	0h	OENZ pin overwrite 0b = Use value on OENZ pin 1b = Use value from OENZ_PIN_VAL. Ignore value on OENZ pin.
1:0	RESERVED	R	0h	

#### 6.6.1.27 DIG\_PATTERN\_EN Register (Address = A1h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-33. DIG\_PATTERN\_EN Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:3	DIG_PATTERN_MODE_C HB	R/W	0h	Enables test pattern output mode for channel B. 001b = Ramp pattern with step size of 1 010b = Ramp pattern with step size set in DIG PAT CHA 100b = Constant pattern using DIG PAT CHA 101b = Toggle pattern between DIG PAT CHA and bitwise inverted DIG PAT CHA 110b = Toggle pattern between DIG PAT CHA and 0
2:0	DIG_PATTERN_MODE_C HA	R/W	0h	Enables test pattern output mode for channel A. 001b = Ramp pattern with step size of 1 010b = Ramp pattern with step size set in DIG PAT CHA 100b = Constant pattern using DIG PAT CHA 101b = Toggle pattern between DIG PAT CHA and bitwise inverted DIG PAT CHA 110b = Toggle pattern between DIG PAT CHA and 0

#### 6.6.1.28 DIG\_PATTERN\_CHA\_7:0 Register (Address = A2h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-34. DIG\_PATTERN\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	DIG_PATTERN_CHA_7:0	R/W	0h	Used with DIG PAT MODE CHA to set constant custom pattern starting from MSB or sets ramp pattern increment step size.

**6.6.1.29 DIG\_PATTERN\_CHA\_15:8 Register (Address = A3h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-35. DIG\_PATTERN\_CHA\_15:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	DIG_PATTERN_CHA_15:8	R/W	0h	Used with DIG PAT MODE CHA to set constant custom pattern starting from MSB or sets ramp pattern increment step size.

**6.6.1.30 DIG\_PATTERN\_CHB\_7:0 Register (Address = A4h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-36. DIG\_PATTERN\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	DIG_PATTERN_CHB_7:0	R/W	0h	Used with DIG PAT MODE CHB to set constant custom pattern starting from MSB or sets ramp pattern increment step size.

**6.6.1.31 DIG\_PATTERN\_CHB\_15:8 Register (Address = A5h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-37. DIG\_PATTERN\_CHB\_15:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	DIG_PATTERN_CHB_15:8	R/W	0h	Used with DIG PAT MODE CHB to set constant custom pattern starting from MSB or sets ramp pattern increment step size.

**6.6.1.32 INTERFACE\_CFG\_4 Register (Address = A6h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-38. INTERFACE\_CFG\_4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	DDR_MODE	R/W	0h	Channel data output order. Applicable in DDR interface mode. 0b = Channel A data on rising edge and channel B on falling edge of DCLK 1b = Channel A data outputed first then channel B data
4:1	SERIALIZATION	R/W	0h	Serialization Factor 0000b = Parallel output 0001b = 2x serialization 0010b = 4x serialization 0011b = 8x serialization 0100b = 16x serialization
0	DIG_PAT_EN	R/W	0h	Enables the test patterns set in DIG PAT MODE CHA and DIG PAT MODE CHB. 0b = Normal output mode (test pattern disabled) 1b = Test pattern enabled

### 6.6.1.33 OUTPUT\_DATA\_WIDTH Register (Address = A7h) [Reset = 50h]

Return to the [Summary Table](#).

**Table 6-39. OUTPUT\_DATA\_WIDTH Register Field Descriptions**

Bit	Field	Type	Reset	Description
4:0	OUTPUT_DATA_WIDTH	R/W	Ah	Output resolution for lane optimization in serialization modes. 01000b = 8-bit 01010b = 10-bit 01100b = 12-bit 10000b = 16-bit

### 6.6.1.34 DCLK\_DIVIDER Register (Address = A8h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-40. DCLK\_DIVIDER Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	DCLK_DIVIDER	R/W	0h	Division of CLK to DCLK to match serialization and decimation data rates. Decimation and serialization factor (SERIALIZATION) must match. 0000b = Divide-by-1 0001b = Divide-by-2 0011b = Divide-by-4 0111b = Divide-by-8 1111b = Divide-by-16

### 6.6.1.35 OUTPUT\_BIT\_MAPPER\_D0\_D1 Register (Address = AEh) [Reset = D6h]

Return to the [Summary Table](#).

**Table 6-41. OUTPUT\_BIT\_MAPPER\_D0\_D1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	OUTPUT_BIT_MAPPER_D1	R/W	Dh	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)
3:0	OUTPUT_BIT_MAPPER_D0	R/W	6h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)



### 6.6.1.36 OUTPUT\_BIT\_MAPPER\_D2\_D3 Register (Address = AFh) [Reset = EBh]

Return to the [Summary Table](#).

**Table 6-42. OUTPUT\_BIT\_MAPPER\_D2\_D3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	OUTPUT_BIT_MAPPER_D3	R/W	Eh	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)
3:0	OUTPUT_BIT_MAPPER_D2	R/W	Bh	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

### 6.6.1.37 OUTPUT\_BIT\_MAPPER\_D4\_D5 Register (Address = B0h) [Reset = 84h]

Return to the [Summary Table](#).

**Table 6-43. OUTPUT\_BIT\_MAPPER\_D4\_D5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	OUTPUT_BIT_MAPPER_D5	R/W	8h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

**Table 6-43. OUTPUT\_BIT\_MAPPER\_D4\_D5 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3:0	OUTPUT_BIT_MAPPER_D4	R/W	4h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

**6.6.1.38 OUTPUT\_BIT\_MAPPER\_D6\_D7 Register (Address = B1h) [Reset = 86h]**

Return to the [Summary Table](#).

**Table 6-44. OUTPUT\_BIT\_MAPPER\_D6\_D7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	OUTPUT_BIT_MAPPER_D7	R/W	8h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)
3:0	OUTPUT_BIT_MAPPER_D6	R/W	6h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

**6.6.1.39 OUTPUT\_BIT\_MAPPER\_D8\_D9 Register (Address = B2h) [Reset = 92h]**

Return to the [Summary Table](#).

**Table 6-45. OUTPUT\_BIT\_MAPPER\_D8\_D9 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	OUTPUT_BIT_MAPPER_D9	R/W	9h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)
3:0	OUTPUT_BIT_MAPPER_D8	R/W	2h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

**6.6.1.40 OUTPUT\_BIT\_MAPPER\_D10\_D11 Register (Address = B3h) [Reset = 93h]**

Return to the [Summary Table](#).

**Table 6-46. OUTPUT\_BIT\_MAPPER\_D10\_D11 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	OUTPUT_BIT_MAPPER_D11	R/W	9h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

**Table 6-46. OUTPUT\_BIT\_MAPPER\_D10\_D11 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3:0	OUTPUT_BIT_MAPPER_D10	R/W	3h	These registers are used to reorder the output data bus. See the Output Bit Mapper on how to program. 0100b = Lane 0 (LSB) 0101b = Lane 1 0110b = Lane 2 0111b = Lane 3 1000b = Lane 4 1001b = Lane 5 1010b = Lane 6 1011b = Lane 7 1100b = Lane 8 1101b = Lane 9 1110b = Lane 10 1111b = Lane 11 (MSB)

#### 6.6.1.41 ROUND Register (Address = B6h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-47. ROUND Register Field Descriptions**

Bit	Field	Type	Reset	Description
4	ROUND	R/W	0h	The device uses a 16-bit resolution internally which can be useful for high decimation settings so that the quantization noise doesn't impact the ADC performance. 0b = Truncate 4 LSBs to reduce resolution from 16 bits to resolution specified in OUTPUT DATA WIDTH 1b = Round to reduce resolution from 16 bits to resolution specified in OUTPUT DATA WIDTH
3:0	RESERVED	R	0h	

#### 6.6.1.42 COMP\_THRESHOLD\_HI\_CHA\_7:0 Register (Address = C8h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-48. COMP\_THRESHOLD\_HI\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	COMP_THRESHOLD_HI_CHA_7:0	R/W	0h	Comparator high threshold for channel A

#### 6.6.1.43 COMP\_THRESHOLD\_HI\_CHA\_11:8 Register (Address = C9h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-49. COMP\_THRESHOLD\_HI\_CHA\_11:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	COMP_THRESHOLD_HI_CHA_11:8	R/W	0h	Comparator high threshold for channel A

#### 6.6.1.44 COMP\_THRESHOLD\_HI\_CHB\_7:0 Register (Address = CAh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-50. COMP\_THRESHOLD\_HI\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	COMP_THRESHOLD_HI_CHB_7:0	R/W	0h	Comparator high threshold for channel B

#### 6.6.1.45 COMP\_THRESHOLD\_HI\_CHB\_11:8 Register (Address = CBh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-51. COMP\_THRESHOLD\_HI\_CHB\_11:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	COMP_THRESHOLD_HI_CHB_11:8	R/W	0h	Comparator high threshold for channel B

#### 6.6.1.46 COMP\_THRESHOLD\_LO\_CHA\_7:0 Register (Address = CCh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-52. COMP\_THRESHOLD\_LO\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	COMP_THRESHOLD_LO_CHA_7:0	R/W	0h	Comparator low threshold for channel A

#### 6.6.1.47 COMP\_THRESHOLD\_LO\_CHA\_11:8 Register (Address = CDh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-53. COMP\_THRESHOLD\_LO\_CHA\_11:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	COMP_THRESHOLD_LO_CHA_11:8	R/W	0h	Comparator low threshold for channel A

#### 6.6.1.48 COMP\_THRESHOLD\_LO\_CHB\_7:0 Register (Address = CEh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-54. COMP\_THRESHOLD\_LO\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	COMP_THRESHOLD_LO_CHB_7:0	R/W	0h	Comparator low threshold for channel B

#### 6.6.1.49 COMP\_THRESHOLD\_LO\_CHB\_11:8 Register (Address = CFh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-55. COMP\_THRESHOLD\_LO\_CHB\_11:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	COMP_THRESHOLD_LO_CHB_11:8	R/W	0h	Comparator low threshold for channel B

#### 6.6.1.50 COMP\_HYSTERESIS\_CHA\_7:0 Register (Address = D0h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-56. COMP\_HYSTERESIS\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	COMP_HYSTERESIS_CHA_7:0	R/W	0h	Comparator hysteresis for channel A

#### 6.6.1.51 COMP\_HYSTERESIS\_CHA\_11:8 Register (Address = D1h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-57. COMP\_HYSTERESIS\_CHA\_11:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	COMP_HYSTERESIS_CHA_11:8	R/W	0h	Comparator hysteresis for channel A

#### 6.6.1.52 COMP\_HYSTERESIS\_CHB\_7:0 Register (Address = D2h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-58. COMP\_HYSTERESIS\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	COMP_HYSTERESIS_CHB_7:0	R/W	0h	Comparator hysteresis for channel A

#### 6.6.1.53 COMP\_HYSTERESIS\_CHB\_11:8 Register (Address = D3h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-59. COMP\_HYSTERESIS\_CHB\_11:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	COMP_HYSTERESIS_CHB_11:8	R/W	0h	Comparator hysteresis for channel A

#### 6.6.1.54 COMP\_SLEW Register (Address = D3h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-60. COMP\_SLEW Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	SLEW_CHB	R/W	0h	Comparison method for channel B 0b = Standard compare (THRESHOLD HI CHB - HYSTERESIS CHB, THRESHOLD LO CHB + HYSTERESIS CHB) 1b = Slew compare (current sample - previous sample > THRESHOLD HI CHB, current sample - previous sample < THRESHOLD LO CHB) HYSTERESIS CHB must be set to 0.
4	SLEW_CHA	R/W	0h	Comparison method for channel A 0b = Standard compare (THRESHOLD HI CHA - HYSTERESIS CHA, THRESHOLD LO CHA + HYSTERESIS CHA) 1b = Slew compare (current sample - previous sample > THRESHOLD HI CHA, current sample - previous sample < THRESHOLD LO CHA) HYSTERESIS CHA must be set to 0.
3:0	RESERVED	R	0h	

#### 6.6.1.55 DECIMATION Register (Address = D4h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-61. DECIMATION Register Field Descriptions**

Bit	Field	Type	Reset	Description
3	DDC_CHB	R/W	0h	Channel B decimation 0b = Decimation disabled 1b = Decimation enabled
2	DDC_CHA	R/W	0h	Channel A decimation 0b = Decimation disabled 1b = Decimation enabled
1:0	RESERVED	R	0h	

**6.6.1.56 PROG\_GAIN\_CHA Register (Address = D5h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-62. PROG\_GAIN\_CHA Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	PROG_GAIN_CHA	R/W	0h	Programmable gain for channel A. Effective gain = (PROG GAIN CHA * 256 + IL GAIN CHA)/2**15.

**6.6.1.57 PROG\_GAIN\_CHB Register (Address = D6h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-63. PROG\_GAIN\_CHB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	PROG_GAIN_CHB	R/W	0h	Programmable gain for channel B. Effective gain = (PROG GAIN CHB * 256 + IL GAIN CHB)/2**15

**6.6.1.58 IL\_GAIN\_CHA\_7:0 Register (Address = D8h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-64. IL\_GAIN\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	IL_GAIN_CHA__7:0	R/W	0h	Interleaving gain for channel A. Effective gain = (PROG GAIN CHA * 256 + IL GAIN CHA)/2**15

**6.6.1.59 IL\_GAIN\_CHA\_15:8 Register (Address = D9h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-65. IL\_GAIN\_CHA\_15:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	IL_GAIN_CHA__15:8	R/W	0h	Interleaving gain for channel A. Effective gain = (PROG GAIN CHA * 256 + IL GAIN CHA)/2**15

**6.6.1.60 IL\_GAIN\_CHB\_7:0 Register (Address = DAh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-66. IL\_GAIN\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	IL_GAIN_CHB__7:0	R/W	0h	Interleaving gain for channel B. Effective gain = (PROG GAIN CHB * 256 + IL_GAIN_CHB)/2**15

**6.6.1.61 IL\_GAIN\_CHB\_15:8 Register (Address = DBh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-67. IL\_GAIN\_CHB\_15:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	IL_GAIN_CHB__15:8	R/W	0h	Interleaving gain for channel B. Effective gain = (PROG GAIN CHB * 256 + IL_GAIN_CHB)/2**15

**6.6.1.62 OFFSET\_CHA\_7:0 Register (Address = DCh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-68. OFFSET\_CHA\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	OFFSET_CHA__7:0	R/W	0h	Channel A offset. Effective offset = OFFSET_CHA/2**15

**6.6.1.63 OFFSET\_CHA\_15:8 Register (Address = DDh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-69. OFFSET\_CHA\_15:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	OFFSET_CHA__15:8	R/W	0h	Channel A offset. Effective offset = OFFSET_CHA/2**15

**6.6.1.64 OFFSET\_CHB\_7:0 Register (Address = DEh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-70. OFFSET\_CHB\_7:0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	OFFSET_CHB__7:0	R/W	0h	Channel B offset. Effective offset = OFFSET_CHB/2**15

**6.6.1.65 OFFSET\_CHB\_15:8 Register (Address = DFh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-71. OFFSET\_CHB\_15:8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	OFFSET_CHB__15:8	R/W	0h	Channel B offset. Effective offset = OFFSET_CHB/2**15

**6.6.1.66 CH\_CORR\_EN Register (Address = E0h) [Reset = 3h]**

Return to the [Summary Table](#).



**Table 6-72. CH\_CORR\_EN Register Field Descriptions**

Bit	Field	Type	Reset	Description
1	CORR_CHB__15:8	R/W	1h	Channel corrections for channel B (PROG GAIN CHB, IL GAIN CHB, OFFSET CHB) 0b = Channel corrections enabled 1b = Channel corrections disabled
0	CORR_CHA__7:0	R/W	1h	Channel corrections for channel A (PROG GAIN CHA, IL GAIN CHA, OFFSET CHA) 0b = Channel corrections enabled 1b = Channel corrections disabled

**6.6.1.67 DDC\_CFG\_1 Register (Address = 200h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-73. DDC\_CFG\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:3	DDC_DATA_SEL_CHA	R/W	0h	Data select for channel A decimation 000b = ADC channel A (default) 001b = ADC channel B
2:0	DECIMATION	R/W	0h	Real decimation setting. This applies to both channels. 000b = Bypass mode (no decimation) 001b = Decimation by 2 010b = Decimation by 4 011b = Decimation by 8 100b = Decimation by 16

**6.6.1.68 STATS\_COMP\_DATA\_SEL Register (Address = 201h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-74. STATS\_COMP\_DATA\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:3	STATS_DATA_SEL_CHA	R/W	0h	Data select for channel A statistics engine 000b = Channel A digital downconverter 001b = ADC channel B 100b = Average of channel A and channel B data 101b = Channel A correction block 110b = Channel B correction block
2:0	COMP_DATA_SEL_CHA	R/W	0h	Data select for channel A comparator 000b = Channel A digital downconverter 001b = ADC channel B 100b = Average of channel A and channel B data 101b = Channel A correction block 110b = Channel B correction block

**6.6.1.69 OUTPUT\_DATA\_SEL Register (Address = 202h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-75. OUTPUT\_DATA\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
2:0	OUTPUT_DATA_SEL_CHA	R/W	0h	Data select for channel A output 000b = Channel A digital downconverter 001b = ADC channel B 100b = Average of channel A and channel B data 101b = Channel A correction block 110b = Channel B correction block

### 6.6.1.70 COMP\_DDC\_DATA\_SEL Register (Address = 203h) [Reset = 21h]

Return to the [Summary Table](#).

**Table 6-76. COMP\_DDC\_DATA\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:3	COMP_DATA_SEL_CHB	R/W	1h	Data select for channel B comparator 000b = Channel A digital downconverter 001b = ADC channel B (default) 100b = Average of channel A and channel B data 101b = Channel A correction block 110b = Channel B correction block
2:0	DDC_DATA_SEL_CHB	R/W	1h	Data select for channel B decimation 000b = ADC channel A 001b = ADC channel B (default)

### 6.6.1.71 OUTPUT\_STATS\_DATA\_SEL Register (Address = 204h) [Reset = 21h]

Return to the [Summary Table](#).

**Table 6-77. OUTPUT\_STATS\_DATA\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:3	OUTPUT_DATA_SEL_CHB	R/W	1h	Data select for channel B output 000b = Channel A digital downconverter 001b = ADC channel B (default) 100b = Average of channel A and channel B data 101b = Channel A correction block 110b = Channel B correction block
2:0	STATS_DATA_SEL_CHB	R/W	1h	Data select for channel B statistics engine 000b = Channel A digital downconverter 001b = ADC channel B (default) 100b = Average of channel A and channel B data 101b = Channel A correction block 110b = Channel B correction block

### 6.6.1.72 OVR\_CHB Register (Address = 205h) [Reset = F0h]

Return to the [Summary Table](#).

**Table 6-78. OVR\_CHB Register Field Descriptions**

Bit	Field	Type	Reset	Description
6:3	OVR_CHB	R/W	Fh	Channel B overrange control. This register is a mask with all sources enabled by default. Bit 0: Truncation overrange Bit 1: Channel Correction overrange Bit 2: Decimation overrange Bit 3: ADC overrange
2:0	RESERVED	R	0h	

### 6.6.1.73 OVR\_CHA Register (Address = 206h) [Reset = Fh]

Return to the [Summary Table](#).

**Table 6-79. OVR\_CHA Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	OVR_CHA	R	Fh	Channel A overrange control. This register is a mask with all sources enabled by default. Bit 0: Truncation overrange Bit 1: Channel Correction overrange Bit 2: Decimation overrange Bit 3: ADC overrange

#### 6.6.1.74 CLK\_TIM\_ADJ\_CHA Register (Address = 304h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-80. CLK\_TIM\_ADJ\_CHA Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:1	CLK_TIM_ADJ_CHA	R/W	0h	ADC channel A sampling edge adjustment. Used in interleaved mode to reduce interleaving spur. Min. step size is 1 ps and adjustment range is 15 ps.
0	RESERVED	R	0h	

#### 6.6.1.75 CLK\_TIM\_ADJ\_CHB Register (Address = 305h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-81. CLK\_TIM\_ADJ\_CHB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DCLK_OUT	R/W	0h	DCLK output disable 0b = DCLK output enabled 1b = DCLK output disabled
6:0	CLK_TIM_ADJ_CHB	R/W	0h	ADC channel B sampling edge adjustment. Used in interleaved mode to reduce interleaving spur. Min. step size is 1 ps and adjustment range is 15 ps.

#### 6.6.1.76 DCLK\_DLL\_PD Register (Address = 306h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-82. DCLK\_DLL\_PD Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	DCLKDLL_PD	R/W	0h	DCLK DLL power down and bypass. Useful in SDR interface mode and reduces current by 1 mA. 0b = DCLK DLL enabled 1b = DCLK DLL power down and bypassed

#### 6.6.1.77 DIG\_INPUT\_CFG Register (Address = 307h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-83. DIG\_INPUT\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
4	DCLKZ_OUT	R/W	0h	DCLKZ output disable 0b = DCLKZ output enabled 1b = DCLKZ output disabled
3	DIG_INPUT	R/W	0h	Disables data inputs to digital block. 0b = Data inputs enabled to digital blocks 1b = Data input disabled to digital blocks
2:0	RESERVED	R	0h	

#### 6.6.1.78 BUF\_VCM\_CURR Register (Address = 309h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-84. BUF\_VCM\_CURR Register Field Descriptions**

Bit	Field	Type	Reset	Description
5:4	BUF_CURR_CHB__1:0	R/W	0h	ADC channel B input buffer PTAT current source mask LSB's used for gain tracking across temperature for stability. 00b = 19.9uA (default) 01b = 26.5uA 10b = 13.3uA 11b = 19.9uA 100b = 29.9uA 101b = 36.5uA 110b = 23.3uA 111b = 29.9uA 1000b = 6.6uA 1001b = 13.2uA 1010b = 0uA 1011b = 6.6uA 1100b = 16.6uA 1101b = 23.2uA 1110b = 10uA 1111b = 16.6uA
3:0	VCM_CURR	R/W	0h	VCM buffer PTAT current source mask used for gain tracking across temperature for stability. 0000b = 19.9uA (default) 0001b = 26.5uA 0010b = 13.3uA 0011b = 19.9uA 0100b = 29.9uA 0101b = 36.5uA 0110b = 23.3uA 0111b = 29.9uA 1000b = 6.6uA 1001b = 13.2uA 1010b = 0uA 1011b = 6.6uA 1100b = 16.6uA 1101b = 23.2uA 1110b = 10uA 1111b = 16.6uA

**6.6.1.79 BUF\_CURR Register (Address = 30Ah) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-85. BUF\_CURR Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	FORMAT_DIG	R/W	0h	Output Data Format when digital features are used. 0b = Two's Complement 1b = Offset binary

**Table 6-85. BUF\_CURR Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5:2	BUF_CURR_CHA	R/W	0h	ADC channel A input buffer PTAT current source mask used for gain tracking across temperature for stability. 0000b = 19.9uA (default) 0001b = 26.5uA 0010b = 13.3uA 0011b = 19.9uA 0100b = 29.9uA 0101b = 36.5uA 0110b = 23.3uA 0111b = 29.9uA 1000b = 6.6uA 1001b = 13.2uA 1010b = 0uA 1011b = 6.6uA 1100b = 16.6uA 1101b = 23.2uA 1110b = 10uA 1111b = 16.6uA
1:0	BUF_CURR_CHB_3:2	R/W	0h	ADC channel B input buffer PTAT current source mask LSB's used for gain tracking across temperature for stability. 00b = 19.9uA (default) 01b = 26.5uA 10b = 13.3uA 11b = 19.9uA 100b = 29.9uA 101b = 36.5uA 110b = 23.3uA 111b = 29.9uA 1000b = 6.6uA 1001b = 13.2uA 1010b = 0uA 1011b = 6.6uA 1100b = 16.6uA 1101b = 23.2uA 1110b = 10uA 1111b = 16.6uA

**6.6.1.80 DEV\_CFG\_4 Register (Address = 30Bh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-86. DEV\_CFG\_4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
6	EXT_REF	R/W	0h	Selects the voltage reference option 0b = Internal reference 1b = External reference
5	SE_EN	R/W	0h	Single ended analog input for ADC channels A and B. In this mode the SNR reduces by 3-dB. 0b = Differential input 1b = Single ended input
4	SINGLE_CH	R/W	0h	Disables ADC channel B 0b = ADC channel B enabled 1b = ADC channel B disabled (enforced on single channel devices)
3	RESERVED	R	0h	
2	HALF_SPEED	R/W	0h	Half speed mode (HFSB). Enable when sample clock is less than 65 MSPS. 0b = Half speed mode disabled 1b = Half speed mode enabled (enforced on 25MSPS and 65MSPS devices)
1	RESERVED	R	0h	

**Table 6-86. DEV\_CFG\_4 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
0	8BIT_EN	R/W	0h	ADC resolution 0b = 10-bit resolution 1b = 8-bit resolution

#### 6.6.1.81 GBL\_CLK\_CFG\_1 Register (Address = 484h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-87. GBL\_CLK\_CFG\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
1	CLK_GBL	R/W	0h	Global clock enable. Controls clock for digital block 0b = Gates clock to digital 1b = Ungates clock to digital
0	RESERVED	R	0h	

#### 6.6.1.82 GBL\_CLK\_CFG\_2 Register (Address = 4BEh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-88. GBL\_CLK\_CFG\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:6	CLK_STATS	R/W	0h	Controls clock to statistics engine 00b = Disables clock to statistics engine 11b = Enables clock to statistics engine
5:4	CLK_COMP	R/W	0h	Controls clock to comparator 00b = Disables clock to comparator 11b = Enables clock to comparator
3:2	CLK_DEC	R/W	0h	Controls clock to decimation 00b = Disables clock to decimation 11b = Enables clock to decimation
1:0	CLK_CC	R/W	0h	Controls clock to channel corrections 00b = Disables clock to channel corrections 11b = Enables clock to channel corrections

#### 6.6.1.83 GBL\_CLK\_CFG\_3 Register (Address = 4BFh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-89. GBL\_CLK\_CFG\_3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
1:0	CLK_OUT	R/W	0h	Controls clock to digital output block 00b = Disables clock to digital output 11b = Enables clock to digital output

## 6.6.2 Statistics Engine Register Map

**Table 6-90. Statistics Engine Registers**

Address	Register Name
E4h	STATS_HI_COUNT_N_CHA_7:0
E5h	STATS_HI_COUNT_N_CHA_15:8
E6h	STATS_HI_COUNT_N_CHA_16
E8h	STATS_HI_COUNT_N_CHB_7:0
E9h	STATS_HI_COUNT_N_CHB_15:8
EAh	STATS_HI_COUNT_N_CHB_16
ECh	STATS_LO_COUNT_N_CHA_7:0
EDh	STATS_LO_COUNT_N_CHA_15:8
EEh	STATS_LO_COUNT_N_CHA_16
F0h	STATS_LO_COUNT_N_CHB_7:0
F1h	STATS_LO_COUNT_N_CHB_15:8
F2h	STATS_LO_COUNT_N_CHB_16
F4h	STATS_SUM_N_CHA_7:0
F5h	STATS_SUM_N_CHA_15:8
F6h	STATS_SUM_N_CHA_23:16
F7h	STATS_SUM_N_CHA_27:24
F8h	STATS_SUM_N_CHB_7:0
F9h	STATS_SUM_N_CHB_15:8
FAh	STATS_SUM_N_CHB_23:16
FBh	STATS_SUM_N_CHB_27:24
FCh	STATS_SUM_POW_N_CHA_7:0
FDh	STATS_SUM_POW_N_CHA_15:8
FEh	STATS_SUM_POW_N_CHA_23:16
FFh	STATS_SUM_POW_N_CHA_31:24
100h	STATS_SUM_POW_N_CHA_39:32
104h	STATS_SUM_POW_N_CHB_7:0
105h	STATS_SUM_POW_N_CHB_15:8
106h	STATS_SUM_POW_N_CHB_23:16
107h	STATS_SUM_POW_N_CHB_31:24
108h	STATS_SUM_POW_N_CHB_39:32
10Ah	STATS_MAX_N_CHA_7:0
10Bh	STATS_MAX_N_CHA_11:8
10Ch	STATS_MAX_N_CHB_7:0
10Dh	STATS_MAX_N_CHB_11:8
10Eh	STATS_MIN_N_CHA_7:0
10Fh	STATS_MIN_N_CHA_11:8
110h	STATS_MIN_N_CHB_7:0
111h	STATS_HI_COUNT_N1_CHA_7:0_MIN_N_CHB_11:8
112h	STATS_HI_COUNT_N1_CHA_15:8
113h	STATS_HI_COUNT_N1_CHA_16
114h	STATS_HI_COUNT_N1_CHB_7:0
115h	STATS_HI_COUNT_N1_CHB_15:8
116h	STATS_HI_COUNT_N1_CHB_16
118h	STATS_LO_COUNT_N1_CHA_7:0

**Table 6-90. Statistics Engine Registers (continued)**

Address	Register Name
119h	STATS_LO_COUNT_N1_CHA_15:8
11Ah	STATS_LO_COUNT_N1_CHA_16
11Ch	STATS_LO_COUNT_N1_CHB_7:0
11Dh	STATS_LO_COUNT_N1_CHB_15:8
11Eh	STATS_LO_COUNT_N1_CHB_16
120h	STATS_SUM_N1_CHA_7:0
121h	STATS_SUM_N1_CHA_15:8
122h	STATS_SUM_N1_CHA_23:16
123h	STATS_SUM_N1_CHA_27:24
124h	STATS_SUM_N1_CHB_7:0
125h	STATS_SUM_N1_CHB_15:8
126h	STATS_SUM_N1_CHB_23:16
127h	STATS_SUM_N1_CHB_27:24
128h	STATS_SUM_POW_N1_CHA_7:0
129h	STATS_SUM_POW_N1_CHA_15:8
12Ah	STATS_SUM_POW_N1_CHA_23:16
12Bh	STATS_SUM_POW_N1_CHA_31:24
12Ch	STATS_SUM_POW_N1_CHA_39:32
130h	STATS_SUM_POW_N1_CHB_7:0
131h	STATS_SUM_POW_N1_CHB_15:8
132h	STATS_SUM_POW_N1_CHB_23:16
133h	STATS_SUM_POW_N1_CHB_31:24
134h	STATS_SUM_POW_N1_CHB_39:32
136h	STATS_MAX_N1_CHA_7:0
137h	STATS_MAX_N1_CHA_11:8
138h	STATS_MAX_N1_CHB_7:0
139h	STATS_MAX_N1_CHB_11:8
13Ah	STATS_MIN_N1_CHA_7:0
13Bh	STATS_MIN_N1_CHA_11:8
13Ch	STATS_MIN_N1_CHB_7:0
13Dh	STATS_HI_COUNT_N2_CHB_3:0_MIN_N1_CHB_11:8
13Eh	STATS_HI_COUNT_N2_CHB_11:4
13Fh	STATS_HI_COUNT_N2_CHB_16:12
140h	STATS_HI_COUNT_N2_CHA_7:0
141h	STATS_HI_COUNT_N2_CHA_15:8
142h	STATS_HI_COUNT_N2_CHA_16
144h	STATS_LO_COUNT_N2_CHA_7:0
145h	STATS_LO_COUNT_N2_CHA_15:8
146h	STATS_LO_COUNT_N2_CHA_16
148h	STATS_LO_COUNT_N2_CHB_7:0
149h	STATS_LO_COUNT_N2_CHB_15:8
14Ah	STATS_LO_COUNT_N2_CHB_16
14Ch	STATS_SUM_N2_CHA_7:0
14Dh	STATS_SUM_N2_CHA_15:8
14Eh	STATS_SUM_N2_CHA_23:16



**Table 6-90. Statistics Engine Registers (continued)**

Address	Register Name
14Fh	STATS_SUM_N2_CHA_27:24
150h	STATS_SUM_N2_CHB_7:0
151h	STATS_SUM_N2_CHB_15:8
152h	STATS_SUM_N2_CHB_23:16
153h	STATS_SUM_N2_CHB_27:24
154h	STATS_SUM_POW_N2_CHA_7:0
155h	STATS_SUM_POW_N2_CHA_15:8
156h	STATS_SUM_POW_N2_CHA_23:16
157h	STATS_SUM_POW_N2_CHA_31:24
158h	STATS_SUM_POW_N2_CHA_39:32
15Ch	STATS_SUM_POW_N2_CHB_7:0
15Dh	STATS_SUM_POW_N2_CHB_15:8
15Eh	STATS_SUM_POW_N2_CHB_23:16
15Fh	STATS_SUM_POW_N2_CHB_31:24
160h	STATS_SUM_POW_N2_CHB_39:32
162h	STATS_MAX_N2_CHA_7:0
163h	STATS_MAX_N2_CHA_11:8
164h	STATS_MAX_N2_CHB_7:0
165h	STATS_MAX_N2_CHB_11:8
166h	STATS_MIN_N2_CHA_7:0
167h	STATS_MIN_N2_CHA_11:8
168h	STATS_MIN_N2_CHB_7:0
169h	STATS_HI_COUNT_N3_CHB_3:0_MIN_N2_CHB_11:8
16Ah	STATS_HI_COUNT_N3_CHB_11:4
16Bh	STATS_HI_COUNT_N3_CHB_16:12
16Ch	STATS_HI_COUNT_N3_CHA_7:0
16Dh	STATS_HI_COUNT_N3_CHA_15:8
16Eh	STATS_HI_COUNT_N3_CHA_16
170h	STATS_LO_COUNT_N3_CHA_7:0
171h	STATS_LO_COUNT_N3_CHA_15:8
172h	STATS_LO_COUNT_N3_CHA_16
174h	STATS_LO_COUNT_N3_CHB_7:0
175h	STATS_LO_COUNT_N3_CHB_15:8
176h	STATS_LO_COUNT_N3_CHB_16
178h	STATS_SUM_N3_CHA_7:0
179h	STATS_SUM_N3_CHA_15:8
17Ah	STATS_SUM_N3_CHA_23:16
17Bh	STATS_SUM_N3_CHA_27:24
17Ch	STATS_SUM_N3_CHB_7:0
17Dh	STATS_SUM_N3_CHB_15:8
17Eh	STATS_SUM_N3_CHB_23:16
17Fh	STATS_SUM_N3_CHB_27:24
180h	STATS_SUM_POW_N3_CHA_7:0
181h	STATS_SUM_POW_N3_CHA_15:8
182h	STATS_SUM_POW_N3_CHA_23:16

**Table 6-90. Statistics Engine Registers (continued)**

Address	Register Name
183h	STATS_SUM_POW_N3_CHA_31:24
184h	STATS_SUM_POW_N3_CHA_39:32
188h	STATS_SUM_POW_N3_CHB_7:0
189h	STATS_SUM_POW_N3_CHB_15:8
18Ah	STATS_SUM_POW_N3_CHB_23:16
18Bh	STATS_SUM_POW_N3_CHB_31:24
18Ch	STATS_SUM_POW_N3_CHB_39:32
18Eh	STATS_MAX_N3_CHA_7:0
18Fh	STATS_MAX_N3_CHA_11:8
190h	STATS_MAX_N3_CHB_7:0
191h	STATS_MAX_N3_CHB_11:8
192h	STATS_MIN_N3_CHA_7:0
193h	STATS_MIN_N3_CHA_11:8
194h	STATS_MIN_N3_CHB_7:0
195h	STATS_MIN_N3_CHB_11:8
198h	STATS_THRESHOLD_HI_CHA_7:0
199h	STATS_THRESHOLD_HI_CHA_11:8
19Ah	STATS_THRESHOLD_HI_CHB_7:0
19Bh	STATS_THRESHOLD_HI_CHB_11:8
19Ch	STATS_THRESHOLD_LO_CHA_7:0
19Dh	STATS_THRESHOLD_LO_CHA_11:8
19Eh	STATS_THRESHOLD_LO_CHB_7:0
19Fh	STATS_THRESHOLD_LO_CHB_11:8
1A0h	STATS_WINDOW_SIZE_CHA_7:0
1A1h	STATS_WINDOW_SIZE_CHA_15:8
1A2h	STATS_WINDOW_SIZE_CHB_7:0
1A3h	STATS_WINDOW_SIZE_CHB_15:8
1A4h	STATS_ENABLE

**Table 6-91. DeviceStats Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

**6.6.2.1 0x0E4 Register (Address = E4h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-92. 0x0E4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N_C HA__7:0	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N

#### 6.6.2.2 0x0E5 Register (Address = E5h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-93. 0x0E5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N_C HA__15:8	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N

#### 6.6.2.3 0x0E6 Register (Address = E6h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-94. 0x0E6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_HI_COUNT_N_C HA__16	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N

#### 6.6.2.4 0x0E8 Register (Address = E8h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-95. 0x0E8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N_C HB__7:0	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N

#### 6.6.2.5 0x0E9 Register (Address = E9h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-96. 0x0E9 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N_C HB__15:8	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N

#### 6.6.2.6 0x0EA Register (Address = EAh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-97. 0x0EA Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_HI_COUNT_N_C HB__16	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N

#### 6.6.2.7 0x0EC Register (Address = ECh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-98. 0x0EC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N_C HA__7:0	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N

#### 6.6.2.8 0x0ED Register (Address = EDh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-99. 0x0ED Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N_C HA__15:8	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N

#### 6.6.2.9 0x0EE Register (Address = EEh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-100. 0x0EE Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N_C HA__16	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N

#### 6.6.2.10 0x0F0 Register (Address = F0h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-101. 0x0F0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N_C HB__7:0	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N

#### 6.6.2.11 0x0F1 Register (Address = F1h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-102. 0x0F1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N_C HB__15:8	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N

#### 6.6.2.12 0x0F2 Register (Address = F2h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-103. 0x0F2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N_C HB__16	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N

#### 6.6.2.13 0x0F4 Register (Address = F4h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-104. 0x0F4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N_CHA__7: 0	R	0h	Summation of samples on channel A in window N

**6.6.2.14 0x0F5 Register (Address = F5h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-105. 0x0F5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N_CHA__1 5:8	R	0h	Summation of samples on channel A in window N

**6.6.2.15 0x0F6 Register (Address = F6h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-106. 0x0F6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N_CHA__2 3:16	R	0h	Summation of samples on channel A in window N

**6.6.2.16 0x0F7 Register (Address = F7h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-107. 0x0F7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N_CHA__2 7:24	R	0h	Summation of samples on channel A in window N

**6.6.2.17 0x0F8 Register (Address = F8h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-108. 0x0F8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N_CHB__7: 0	R	0h	Summation of samples on channel B in window N

**6.6.2.18 0x0F9 Register (Address = F9h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-109. 0x0F9 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N_CHB__1 5:8	R	0h	Summation of samples on channel B in window N

**6.6.2.19 0x0FA Register (Address = FAh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-110. 0x0FA Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N_CHB_2 3:16	R	0h	Summation of samples on channel B in window N

#### 6.6.2.20 0x0FB Register (Address = FBh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-111. 0x0FB Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N_CHB_2 7:24	R	0h	Summation of samples on channel B in window N

#### 6.6.2.21 0x0FC Register (Address = FCh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-112. 0x0FC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HA__7:0	R	0h	Summation of samples**2 on channel A in window N. Useful for power measurements.

#### 6.6.2.22 0x0FD Register (Address = FDh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-113. 0x0FD Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HA__15:8	R	0h	Summation of samples**2 on channel A in window N. Useful for power measurements.

#### 6.6.2.23 0x0FE Register (Address = FEh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-114. 0x0FE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HA__23:16	R	0h	Summation of samples**2 on channel A in window N. Useful for power measurements.

#### 6.6.2.24 0x0FF Register (Address = FFh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-115. 0x0FF Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HA__31:24	R	0h	Summation of samples**2 on channel A in window N. Useful for power measurements.

#### 6.6.2.25 0x100 Register (Address = 100h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-116. 0x100 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HA__39:32	R	0h	Summation of samples**2 on channel A in window N. Useful for power measurements.

**6.6.2.26 0x104 Register (Address = 104h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-117. 0x104 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HB__7:0	R	0h	Summation of samples**2 on channel B in window N. Useful for power measurements.

**6.6.2.27 0x108 Register (Address = 108h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-118. 0x108 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N_C HB__39:32	R	0h	Summation of samples**2 on channel B in window N. Useful for power measurements.

**6.6.2.28 0x10A Register (Address = 10Ah) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-119. 0x10A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N_CHA__7: 0	R	0h	Maximum value on channel A in window N

**6.6.2.29 0x10B Register (Address = 10Bh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-120. 0x10B Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N_CHA__11: :8	R	0h	Maximum value on channel A in window N

**6.6.2.30 0x10C Register (Address = 10Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-121. 0x10C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N_CHB__7: 0	R	0h	Maximum value on channel B in window N

**6.6.2.31 0x10D Register (Address = 10Dh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-122. 0x10D Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N_CHB__11:8	R	0h	Maximum value on channel B in window N

#### 6.6.2.32 0x10E Register (Address = 10Eh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-123. 0x10E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N_CHA__7:0	R	0h	Minimum value on channel A in window N

#### 6.6.2.33 0x10F Register (Address = 10Fh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-124. 0x10F Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MIN_N_CHA__11:8	R	0h	Minimum value on channel A in window N

#### 6.6.2.34 0x110 Register (Address = 110h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-125. 0x110 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N_CHB__7:0	R	0h	Minimum value on channel B in window N

#### 6.6.2.35 0x111 Register (Address = 111h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-126. 0x111 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	STATS_HI_COUNT_N1_CHA__7:0	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-1
3:0	STATS_MIN_N_CHB__11:8	R	0h	Minimum value on channel B in window N

#### 6.6.2.36 0x112 Register (Address = 112h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-127. 0x112 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N1_CHA__15:8	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-1

#### 6.6.2.37 0x113 Register (Address = 113h) [Reset = 00h]

Return to the [Summary Table](#).



**Table 6-128. 0x113 Register Field Descriptions**

Bit	Field	Type	Reset	Description
4:0	STATS_HI_COUNT_N1_C HA__16	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-1

#### 6.6.2.38 0x114 Register (Address = 114h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-129. 0x114 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N1_C HB__7:0	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-1

#### 6.6.2.39 0x115 Register (Address = 115h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-130. 0x115 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N1_C HB__15:8	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-1

#### 6.6.2.40 0x116 Register (Address = 116h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-131. 0x116 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_HI_COUNT_N1_C HB__16	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-1

#### 6.6.2.41 0x118 Register (Address = 118h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-132. 0x118 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N1_ CHA__7:0	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-1

#### 6.6.2.42 0x119 Register (Address = 119h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-133. 0x119 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N1_ CHA__15:8	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-1

#### 6.6.2.43 0x11A Register (Address = 11Ah) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-134. 0x11A Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N1_CHA__16	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-1

#### 6.6.2.44 0x11C Register (Address = 11Ch) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-135. 0x11C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N1_CHB__7:0	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-1

#### 6.6.2.45 0x11D Register (Address = 11Dh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-136. 0x11D Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N1_CHB__15:8	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-1

#### 6.6.2.46 0x11E Register (Address = 11Eh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-137. 0x11E Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N1_CHB__16	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-1

#### 6.6.2.47 0x120 Register (Address = 120h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-138. 0x120 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N1_CHA__7:0	R	0h	Summation of samples on channel A in window N-1

#### 6.6.2.48 0x121 Register (Address = 121h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-139. 0x121 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N1_CHA__15:8	R	0h	Summation of samples on channel A in window N-1

#### 6.6.2.49 0x122 Register (Address = 122h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-140. 0x122 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N1_CHA__ 23:16	R	0h	Summation of samples on channel A in window N-1

**6.6.2.50 0x123 Register (Address = 123h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-141. 0x123 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N1_CHA__ 27:24	R	0h	Summation of samples on channel A in window N-1

**6.6.2.51 0x124 Register (Address = 124h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-142. 0x124 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N1_CHB__ 7:0	R	0h	Summation of samples on channel B in window N-1

**6.6.2.52 0x125 Register (Address = 125h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-143. 0x125 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N1_CHB__ 15:8	R	0h	Summation of samples on channel B in window N-1

**6.6.2.53 0x126 Register (Address = 126h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-144. 0x126 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N1_CHB__ 23:16	R	0h	Summation of samples on channel B in window N-1

**6.6.2.54 0x127 Register (Address = 127h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-145. 0x127 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N1_CHB__ 27:24	R	0h	Summation of samples on channel B in window N-1

**6.6.2.55 0x128 Register (Address = 128h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-146. 0x128 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HA__7:0	R	0h	Summation of samples**2 on channel A in window N-1. Useful for power measurements.

**6.6.2.56 0x129 Register (Address = 129h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-147. 0x129 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HA__15:8	R	0h	Summation of samples**2 on channel A in window N-1. Useful for power measurements.

**6.6.2.57 0x12A Register (Address = 12Ah) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-148. 0x12A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HA__23:16	R	0h	Summation of samples**2 on channel A in window N-1. Useful for power measurements.

**6.6.2.58 0x12B Register (Address = 12Bh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-149. 0x12B Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HA__31:24	R	0h	Summation of samples**2 on channel A in window N-1. Useful for power measurements.

**6.6.2.59 0x12C Register (Address = 12Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-150. 0x12C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HA__39:32	R	0h	Summation of samples**2 on channel A in window N-1. Useful for power measurements.

**6.6.2.60 0x130 Register (Address = 130h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-151. 0x130 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HB__7:0	R	0h	Summation of samples**2 on channel B in window N-1. Useful for power measurements.

**6.6.2.61 0x131 Register (Address = 131h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-152. 0x131 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HB__15:8	R	0h	Summation of samples**2 on channel B in window N-1. Useful for power measurements.

**6.6.2.62 0x132 Register (Address = 132h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-153. 0x132 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HB__23:16	R	0h	Summation of samples**2 on channel B in window N-1. Useful for power measurements.

**6.6.2.63 0x133 Register (Address = 133h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-154. 0x133 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HB__31:24	R	0h	Summation of samples**2 on channel B in window N-1. Useful for power measurements.

**6.6.2.64 0x134 Register (Address = 134h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-155. 0x134 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N1_C HB__39:32	R	0h	Summation of samples**2 on channel B in window N-1. Useful for power measurements.

**6.6.2.65 0x136 Register (Address = 136h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-156. 0x136 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N1_CHA__ 7:0	R	0h	Maximum value on channel A in window N-1

**6.6.2.66 0x137 Register (Address = 137h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-157. 0x137 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N1_CHA__ 11:8	R	0h	Maximum value on channel A in window N-1

**6.6.2.67 0x138 Register (Address = 138h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-158. 0x138 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N1_CHB__ 7:0	R	0h	Maximum value on channel B in window N-1

**6.6.2.68 0x139 Register (Address = 139h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-159. 0x139 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N1_CHB__ 11:8	R	0h	Maximum value on channel B in window N-1

**6.6.2.69 0x13A Register (Address = 13Ah) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-160. 0x13A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N1_CHA__7: 0	R	0h	Minimum value on channel A in window N-1

**6.6.2.70 0x13B Register (Address = 13Bh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-161. 0x13B Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MIN_N1_CHA__1 1:8	R	0h	Minimum value on channel A in window N-1

**6.6.2.71 0x13C Register (Address = 13Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-162. 0x13C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N1_CHB__7: 0	R	0h	Minimum value on channel B in window N-1

**6.6.2.72 0x13D Register (Address = 13Dh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-163. 0x13D Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	STATS_HI_COUNT_N2_C HB__3:0	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-2
3:0	STATS_MIN_N1_CHB__1 1:8	R	0h	Minimum value on channel B in window N-1

### 6.6.2.73 0x13E Register (Address = 13Eh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-164. 0x13E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N2_C HB__11:4	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-2

### 6.6.2.74 0x13F Register (Address = 13Fh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-165. 0x13F Register Field Descriptions**

Bit	Field	Type	Reset	Description
4:0	STATS_HI_COUNT_N2_C HB__16:12	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-2

### 6.6.2.75 0x140 Register (Address = 140h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-166. 0x140 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N2_C HA__7:0	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-2

### 6.6.2.76 0x141 Register (Address = 141h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-167. 0x141 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N2_C HA__15:8	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-2

### 6.6.2.77 0x142 Register (Address = 142h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-168. 0x142 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_HI_COUNT_N2_C HA__16	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-2

### 6.6.2.78 0x144 Register (Address = 144h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-169. 0x144 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N2_C CHA__7:0	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-2

### 6.6.2.79 0x145 Register (Address = 145h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-170. 0x145 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N2_CHA__15:8	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-2

### 6.6.2.80 0x146 Register (Address = 146h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-171. 0x146 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N2_CHA__16	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-2

### 6.6.2.81 0x148 Register (Address = 148h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-172. 0x148 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N2_CHB__7:0	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-2

### 6.6.2.82 0x149 Register (Address = 149h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-173. 0x149 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N2_CHB__15:8	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-2

### 6.6.2.83 0x14A Register (Address = 14Ah) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-174. 0x14A Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N2_CHB__16	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-2

### 6.6.2.84 0x14C Register (Address = 14Ch) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-175. 0x14C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N2_CHA__7:0	R	0h	Summation of samples on channel A in window N-2



### 6.6.2.85 0x14D Register (Address = 14Dh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-176. 0x14D Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N2_CHA__ 15:8	R	0h	Summation of samples on channel A in window N-2

### 6.6.2.86 0x14E Register (Address = 14Eh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-177. 0x14E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N2_CHA__ 23:16	R	0h	Summation of samples on channel A in window N-2

### 6.6.2.87 0x14F Register (Address = 14Fh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-178. 0x14F Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N2_CHA__ 27:24	R	0h	Summation of samples on channel A in window N-2

### 6.6.2.88 0x150 Register (Address = 150h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-179. 0x150 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N2_CHB__ 7:0	R	0h	Summation of samples on channel B in window N-2

### 6.6.2.89 0x151 Register (Address = 151h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-180. 0x151 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N2_CHB__ 15:8	R	0h	Summation of samples on channel B in window N-2

### 6.6.2.90 0x152 Register (Address = 152h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-181. 0x152 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N2_CHB__ 23:16	R	0h	Summation of samples on channel B in window N-2

### 6.6.2.91 0x153 Register (Address = 153h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-182. 0x153 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N2_CHB__ 27:24	R	0h	Summation of samples on channel B in window N-2

### 6.6.2.92 0x154 Register (Address = 154h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-183. 0x154 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HA__7:0	R	0h	Summation of samples**2 on channel A in window N-2. Useful for power measurements.

### 6.6.2.93 0x155 Register (Address = 155h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-184. 0x155 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HA__15:8	R	0h	Summation of samples**2 on channel A in window N-2. Useful for power measurements.

### 6.6.2.94 0x156 Register (Address = 156h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-185. 0x156 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HA__23:16	R	0h	Summation of samples**2 on channel A in window N-2. Useful for power measurements.

### 6.6.2.95 0x157 Register (Address = 157h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-186. 0x157 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HA__31:24	R	0h	Summation of samples**2 on channel A in window N-2. Useful for power measurements.

### 6.6.2.96 0x158 Register (Address = 158h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-187. 0x158 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HA__39:32	R	0h	Summation of samples**2 on channel A in window N-2. Useful for power measurements.

### 6.6.2.97 0x15C Register (Address = 15Ch) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-188. 0x15C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HB__7:0	R	0h	Summation of samples**2 on channel B in window N-2. Useful for power measurements.

### 6.6.2.98 0x15D Register (Address = 15Dh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-189. 0x15D Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HB__15:8	R	0h	Summation of samples**2 on channel B in window N-2. Useful for power measurements.

### 6.6.2.99 0x15E Register (Address = 15Eh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-190. 0x15E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HB__23:16	R	0h	Summation of samples**2 on channel B in window N-2. Useful for power measurements.

### 6.6.2.100 0x15F Register (Address = 15Fh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-191. 0x15F Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HB__31:24	R	0h	Summation of samples**2 on channel B in window N-2. Useful for power measurements.

### 6.6.2.101 0x160 Register (Address = 160h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-192. 0x160 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N2_C HB__39:32	R	0h	Summation of samples**2 on channel B in window N-2. Useful for power measurements.

### 6.6.2.102 0x162 Register (Address = 162h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-193. 0x162 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N2_CHA__ 7:0	R	0h	Maximum value on channel A in window N-2

### 6.6.2.103 0x163 Register (Address = 163h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-194. 0x163 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N2_CHA__ 11:8	R	0h	Maximum value on channel A in window N-2

### 6.6.2.104 0x164 Register (Address = 164h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-195. 0x164 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N2_CHB__ 7:0	R	0h	Maximum value on channel B in window N-2

### 6.6.2.105 0x165 Register (Address = 165h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-196. 0x165 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N2_CHB__ 11:8	R	0h	Maximum value on channel B in window N-2

### 6.6.2.106 0x166 Register (Address = 166h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-197. 0x166 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N2_CHA__7: 0	R	0h	Minimum value on channel A in window N-2

### 6.6.2.107 0x167 Register (Address = 167h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-198. 0x167 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MIN_N2_CHA__1 1:8	R	0h	Minimum value on channel A in window N-2

### 6.6.2.108 0x168 Register (Address = 168h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-199. 0x168 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N2_CHB__7: 0	R	0h	Minimum value on channel B in window N-2

### 6.6.2.109 0x169 Register (Address = 169h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-200. 0x169 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:4	STATS_HI_COUNT_N3_C HB__3:0	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-3
3:0	STATS_MIN_N2_CHB__1 1:8	R	0h	Minimum value on channel B in window N-2

### 6.6.2.110 0x16A Register (Address = 16Ah) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-201. 0x16A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N3_C HB__11:4	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-3

### 6.6.2.111 0x16B Register (Address = 16Bh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-202. 0x16B Register Field Descriptions**

Bit	Field	Type	Reset	Description
4:0	STATS_HI_COUNT_N3_C HB__16:12	R	0h	Number of samples on channel B above STATS THRESHOLD HI CHB counted in window N-3

### 6.6.2.112 0x16C Register (Address = 16Ch) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-203. 0x16C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N3_C HA__7:0	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-3

### 6.6.2.113 0x16D Register (Address = 16Dh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-204. 0x16D Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_HI_COUNT_N3_C HA__15:8	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-3

### 6.6.2.114 0x16E Register (Address = 16Eh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-205. 0x16E Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_HI_COUNT_N3_C HA__16	R	0h	Number of samples on channel A above STATS THRESHOLD HI CHA counted in window N-3

**6.6.2.115 0x170 Register (Address = 170h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-206. 0x170 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N3_ CHA__7:0	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-3

**6.6.2.116 0x171 Register (Address = 171h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-207. 0x171 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N3_ CHA__15:8	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-3

**6.6.2.117 0x172 Register (Address = 172h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-208. 0x172 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N3_ CHA__16	R	0h	Number of samples on channel A below STATS THRESHOLD LO CHA counted in window N-3

**6.6.2.118 0x174 Register (Address = 174h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-209. 0x174 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N3_ CHB__7:0	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-3

**6.6.2.119 0x175 Register (Address = 175h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-210. 0x175 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_LO_COUNT_N3_ CHB__15:8	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-3

**6.6.2.120 0x176 Register (Address = 176h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-211. 0x176 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	STATS_LO_COUNT_N3_CHB__16	R	0h	Number of samples on channel B below STATS THRESHOLD LO CHB counted in window N-3

**6.6.2.121 0x178 Register (Address = 178h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-212. 0x178 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N3_CHA__7:0	R	0h	Summation of samples on channel A in window N-3

**6.6.2.122 0x179 Register (Address = 179h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-213. 0x179 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N3_CHA__15:8	R	0h	Summation of samples on channel A in window N-3

**6.6.2.123 0x17A Register (Address = 17Ah) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-214. 0x17A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N3_CHA__23:16	R	0h	Summation of samples on channel A in window N-3

**6.6.2.124 0x17B Register (Address = 17Bh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-215. 0x17B Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N3_CHA__27:24	R	0h	Summation of samples on channel A in window N-3

**6.6.2.125 0x17C Register (Address = 17Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-216. 0x17C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N3_CHB__7:0	R	0h	Summation of samples on channel B in window N-3

**6.6.2.126 0x17D Register (Address = 17Dh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-217. 0x17D Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N3_CHB__ 15:8	R	0h	Summation of samples on channel B in window N-3

**6.6.2.127 0x17E Register (Address = 17Eh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-218. 0x17E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_N3_CHB__ 23:16	R	0h	Summation of samples on channel B in window N-3

**6.6.2.128 0x17F Register (Address = 17Fh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-219. 0x17F Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_SUM_N3_CHB__ 27:24	R	0h	Summation of samples on channel B in window N-3

**6.6.2.129 0x180 Register (Address = 180h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-220. 0x180 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HA__7:0	R	0h	Summation of samples**2 on channel A in window N-3. Useful for power measurements.

**6.6.2.130 0x181 Register (Address = 181h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-221. 0x181 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HA__15:8	R	0h	Summation of samples**2 on channel A in window N-3. Useful for power measurements.

**6.6.2.131 0x182 Register (Address = 182h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-222. 0x182 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HA__23:16	R	0h	Summation of samples**2 on channel A in window N-3. Useful for power measurements.

**6.6.2.132 0x183 Register (Address = 183h) [Reset = 00h]**

Return to the [Summary Table](#).



**Table 6-223. 0x183 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HA__31:24	R	0h	Summation of samples**2 on channel A in window N-3. Useful for power measurements.

**6.6.2.133 0x184 Register (Address = 184h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-224. 0x184 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HA__39:32	R	0h	Summation of samples**2 on channel A in window N-3. Useful for power measurements.

**6.6.2.134 0x188 Register (Address = 188h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-225. 0x188 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HB__7:0	R	0h	Summation of samples**2 on channel B in window N-3. Useful for power measurements.

**6.6.2.135 0x189 Register (Address = 189h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-226. 0x189 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HB__15:8	R	0h	Summation of samples**2 on channel B in window N-3. Useful for power measurements.

**6.6.2.136 0x18A Register (Address = 18Ah) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-227. 0x18A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HB__23:16	R	0h	Summation of samples**2 on channel B in window N-3. Useful for power measurements.

**6.6.2.137 0x18B Register (Address = 18Bh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-228. 0x18B Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HB__31:24	R	0h	Summation of samples**2 on channel B in window N-3. Useful for power measurements.

**6.6.2.138 0x18C Register (Address = 18Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-229. 0x18C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_SUM_POW_N3_C HB__39:32	R	0h	Summation of samples**2 on channel B in window N-3. Useful for power measurements.

**6.6.2.139 0x18E Register (Address = 18Eh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-230. 0x18E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N3_CHA__ 7:0	R	0h	Maximum value on channel A in window N-3

**6.6.2.140 0x18F Register (Address = 18Fh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-231. 0x18F Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N3_CHA__ 11:8	R	0h	Maximum value on channel A in window N-3

**6.6.2.141 0x190 Register (Address = 190h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-232. 0x190 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MAX_N3_CHB__ 7:0	R	0h	Maximum value on channel B in window N-3

**6.6.2.142 0x191 Register (Address = 191h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-233. 0x191 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MAX_N3_CHB__ 11:8	R	0h	Maximum value on channel B in window N-3

**6.6.2.143 0x192 Register (Address = 192h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-234. 0x192 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N3_CHA__7: 0	R	0h	Minimum value on channel A in window N-3

**6.6.2.144 0x193 Register (Address = 193h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-235. 0x193 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MIN_N3_CHA__1 1:8	R	0h	Minimum value on channel A in window N-3

**6.6.2.145 0x194 Register (Address = 194h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-236. 0x194 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_MIN_N3_CHB__7: 0	R	0h	Minimum value on channel B in window N-3

**6.6.2.146 0x195 Register (Address = 195h) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-237. 0x195 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_MIN_N3_CHB__1 1:8	R	0h	Minimum value on channel B in window N-3

**6.6.2.147 0x198 Register (Address = 198h) [Reset = FFh]**

Return to the [Summary Table](#).

**Table 6-238. 0x198 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_THRESHOLD_HI_ CHA__7:0	R/W	FFh	Statistics engine high threshold for channel A

**6.6.2.148 0x199 Register (Address = 199h) [Reset = Fh]**

Return to the [Summary Table](#).

**Table 6-239. 0x199 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_THRESHOLD_HI_ CHA__11:8	R/W	Fh	Statistics engine high threshold for channel A

**6.6.2.149 0x19A Register (Address = 19Ah) [Reset = FFh]**

Return to the [Summary Table](#).

**Table 6-240. 0x19A Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_THRESHOLD_HI_ CHB__7:0	R/W	FFh	Statistics engine high threshold for channel B

**6.6.2.150 0x19B Register (Address = 19Bh) [Reset = Fh]**

Return to the [Summary Table](#).

**Table 6-241. 0x19B Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_THRESHOLD_HI_CHB__11:8	R/W	Fh	Statistics engine high threshold for channel B

**6.6.2.151 0x19C Register (Address = 19Ch) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-242. 0x19C Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_THRESHOLD_LO_CHA__7:0	R/W	0h	Statistics engine low threshold for channel A

**6.6.2.152 0x19D Register (Address = 19Dh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-243. 0x19D Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_THRESHOLD_LO_CHA__11:8	R/W	0h	Statistics engine low threshold for channel A

**6.6.2.153 0x19E Register (Address = 19Eh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-244. 0x19E Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_THRESHOLD_LO_CHB__7:0	R/W	0h	Statistics engine low threshold for channel B

**6.6.2.154 0x19F Register (Address = 19Fh) [Reset = 0h]**

Return to the [Summary Table](#).

**Table 6-245. 0x19F Register Field Descriptions**

Bit	Field	Type	Reset	Description
3:0	STATS_THRESHOLD_LO_CHB__11:8	R/W	0h	Statistics engine low threshold for channel B

**6.6.2.155 0x1A0 Register (Address = 1A0h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-246. 0x1A0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_WINDOW_SIZE_CHA__7:0	R/W	0h	Statistics engine window size for channel A. Minimum size is 256 samples. Maximum size is $256 * 2^{16}$ .

**6.6.2.156 0x1A1 Register (Address = 1A1h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-247. 0x1A1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_WINDOW_SIZE_CHA__15:8	R/W	0h	Statistics engine window size for channel A. Minimum size is 256 samples. Maximum size is $256 * 2^{16}$ .

**6.6.2.157 0x1A2 Register (Address = 1A2h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-248. 0x1A2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_WINDOW_SIZE_CHB__7:0	R/W	0h	Statistics engine window size for channel B. Minimum size is 256 samples. Maximum size is $256 * 2^{16}$ .

**6.6.2.158 0x1A3 Register (Address = 1A3h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-249. 0x1A3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	STATS_WINDOW_SIZE_CHB__15:8	R/W	0h	Statistics engine window size for channel B. Minimum size is 256 samples. Maximum size is $256 * 2^{16}$ .

**6.6.2.159 0x1A4 Register (Address = 1A4h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-250. 0x1A4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
5	STATS_CHB	R/W	0h	Channel B statistics engine 0b = Statistics engine disabled 1b = Statistics engine enabled
4	STATS_CHA	R/W	0h	Channel A statistics engine 0b = Statistics engine disabled 1b = Statistics engine enabled
3:2	RESERVED	R	0h	
1	1SHOT_CHB	R/W	0h	Channel B statistics engine data collection method. By default the statistics engine is continuously collecting data when enabled. There is also the option for a single shot (1 window only) data collection. 0b = Continuous data collection 1b = Single shot data collection
0	1SHOT_CHA	R/W	0h	Channel A statistics engine data collection method. By default the statistics engine is contiguously collecting data when enabled. There is also the option for a single shot (1 window only) data collection. 0b = Continuous data collection 1b = Single shot data collection

### 6.6.3 Alerts Register Map

**Table 6-251. ALERT Registers**

Address	Register Name
1AFh	ALERT_PULSE_WIDTH
1B4h	ALERT_INVERT_7:0
1B5h	ALERT_INVERT_15:8
1B6h	ALERT_INVERT_18:16
1C0h	ALERT_TRIG_7:0
1C1h	ALERT_TRIG_15:8
1C2h	ALERT_TRIG_18:16
1CCh	ALERT_STICKY_7:0
1CDh	ALERT_STICKY_15:8
1CEh	ALERT_STICKY_18:16
1D8h	ALERT_STICKY_CLR_7:0
1D9h	ALERT_STICKY_CLR_15:8
1DAh	ALERT_STICKY_CLR_18:16
1E4h	ALERT_CNT_7:0
1E5h	ALERT_CNT_15:8
1EAh	ALERT_CNT
1ECh	ALERT_THRESHOLD_7:0
1EDh	ALERT_THRESHOLD_15:8

#### 6.6.3.1 0x1AF Register (Address = 1AFh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-252. 0x1AF Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_PULSE_WIDTH	R/W	0h	ALERT pulse width = 2 <sup>ALERTPULSE_WIDTH</sup> + 1 CLK cycles. Minimum width is 1 CLK cycle.

#### 6.6.3.2 0x1B4 Register (Address = 1B4h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-253. 0x1B4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_INVERT_7:0	R/W	0h	Invert signals routed to ALERT pin. This register is a mask so multiple signals can be inverted simultaneously by enabling the corresponding bit. Bit 0: Equal to THRESHOLD HI CHA Bit 1: Greater than THRESHOLD HI CHA Bit 2: Less than THRESHOLD LO CHA Bit 3: All ones Bit 4: All zeros Bit 5: Less than THRESHOLD HI CHA Bit 6: Greater than THRESHOLD LO CHA Bit 7: Equal to THRESHOLD HI CHB Bit 8: Greater than THRESHOLD HI CHB Bit 9: Less than THRESHOLD LO CHB Bit 10: All ones Bit 11: All zeros Bit 12: Less than THRESHOLD HI CHB Bit 13: Greater than THRESHOLD LO CHB Bit 14: ADC channel A overrange Bit 15: ADC channel B overrange Bit 16: Statistics engine window complete

### 6.6.3.3 0x1B5 Register (Address = 1B5h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-254. 0x1B5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_INVERT__15:8	R/W	0h	Invert signals routed to ALERT pin. This register is a mask so multiple signals can be inverted simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask. See register 0x1B4 for bit mask.

### 6.6.3.4 0x1B6 Register (Address = 1B6h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-255. 0x1B6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
2:0	ALERT_INVERT__18:16	R/W	0h	Invert signals routed to ALERT pin. This register is a mask so multiple signals can be inverted simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.5 0x1C0 Register (Address = 1C0h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-256. 0x1C0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_TRIG__7:0	R/W	0h	Signals set as triggers for ALERT pin. This register is a mask so multiple signals can be triggered simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.6 0x1C1 Register (Address = 1C1h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-257. 0x1C1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_TRIG__15:8	R/W	0h	Signals set as triggers for ALERT pin. This register is a mask so multiple signals can be triggered simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.7 0x1C2 Register (Address = 1C2h) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-258. 0x1C2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	ALERT_TRIG__18:16	R/W	0h	Signals set as triggers for ALERT pin. This register is a mask so multiple signals can be triggered simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.8 0x1CC Register (Address = 1CCh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-259. 0x1CC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_STICKY__7:0	R/W	0h	Signals set as sticky for ALERT pin, that is, once triggered remains triggered until cleared in ALERT STICKY CLR MASK. This register is a mask so multiple signals can be set as sticky simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.9 0x1CD Register (Address = 1CDh) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-260. 0x1CD Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_STICKY__15:8	R/W	0h	Signals set as sticky for ALERT pin, that is, once triggered remains triggered until cleared in ALERT STICKY CLR MASK. This register is a mask so multiple signals can be set as sticky simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.10 0x1CE Register (Address = 1CEh) [Reset = 0h]

Return to the [Summary Table](#).

**Table 6-261. 0x1CE Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	ALERT_STICKY__18:16	R/W	0h	Signals set as sticky for ALERT pin, that is, once triggered remains triggered until cleared in ALERT STICKY CLR MASK. This register is a mask so multiple signals can be set as sticky simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.11 0x1D8 Register (Address = 1D8h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-262. 0x1D8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_STICKY_CLR__7:0	R/W	0h	Signals set as sticky for ALERT pin. This register is a mask so multiple signals can be set as sticky simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.12 0x1D9 Register (Address = 1D9h) [Reset = 00h]

Return to the [Summary Table](#).

**Table 6-263. 0x1D9 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_STICKY_CLR__15:8	R/W	0h	Signals set as sticky for ALERT pin. This register is a mask so multiple signals can be set as sticky simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

### 6.6.3.13 0x1DA Register (Address = 1DAh) [Reset = 0h]

Return to the [Summary Table](#).



**Table 6-264. 0x1DA Register Field Descriptions**

Bit	Field	Type	Reset	Description
0	ALERT_STICKY_CLR__1 8:16	R/W	0h	Signals set as sticky for ALERT pin. This register is a mask so multiple signals can be set as sticky simultaneously by enabling the corresponding bit. See register 0x1B4 for bit mask.

**6.6.3.14 0x1E4 Register (Address = 1E4h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-265. 0x1E4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_CNT__7:0	R/W	0h	Counter of the input alerts cross the threshold before the output alert is triggered

**6.6.3.15 0x1E5 Register (Address = 1E5h) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-266. 0x1E5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_CNT__15:8	R/W	0h	Counter of the input alerts cross the threshold before the output alert is triggered

**6.6.3.16 0x1EA Register (Address = 1EAh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-267. 0x1EA Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	CNT_MODE_B	R/W	0h	Sets the ALERT count mode for channel B 0b = Level-based count 1b = Rise-based count
6	CNT_MODE_A	R/W	0h	Sets the ALERT count mode for channel A 0b = Level-based count 1b = Rise-based count
5:1	RESERVED	R	0h	
0	CNT_EN	R/W	0h	Enables alert window mode. In this mode alert is triggered when input triggers cross (alert_thres) number of time in alert_cnt window 0b = Disable alert window mode 1b = Enable alert window mode

**6.6.3.17 0x1EC Register (Address = 1ECh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-268. 0x1EC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0	ALERT_THRESHOLD__7: 0	R/W	0h	Sets the threshold the count of input alerts must cross before the output alert is triggered

**6.6.3.18 0x1ED Register (Address = 1EDh) [Reset = 00h]**

Return to the [Summary Table](#).

**Table 6-269. 0x1ED Register Field Descriptions**

Bit	Field	Type	Reset	Description
7:0 5:8	ALERT_THRESHOLD__1	R/W	0h	Sets the threshold the count of input alerts must cross before the output alert is triggered

## 7 Application Information Disclaimer

### Note

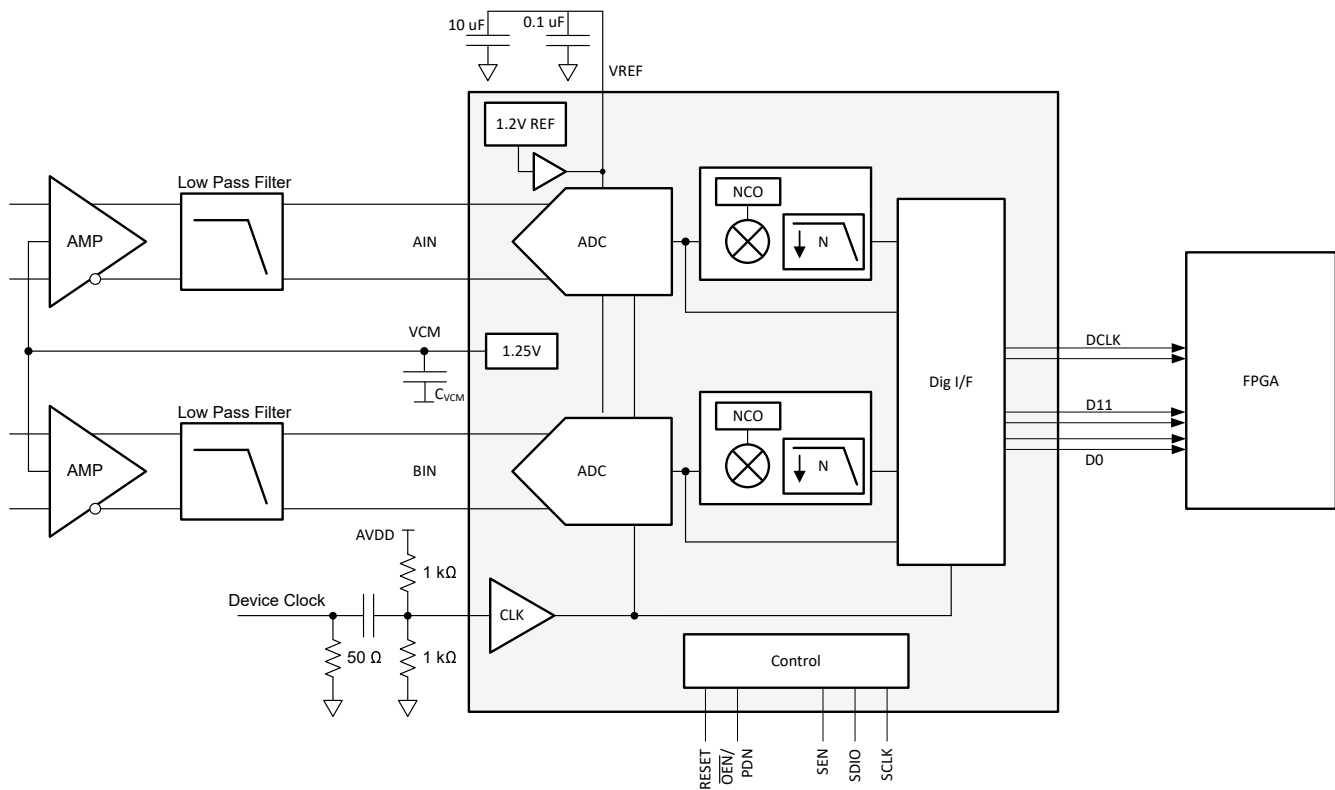
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The ADC3910D125 can be used in a wide range of applications including radio receivers, LiDAR low latency control loops, laser scanners, global positioning systems and detection equipment. The Typical Applications section describe one configuration that meets the needs of a number of these applications.

### 7.2 Typical Application

A spectrum analyzer is a typical frequency domain application for the ADC3910D125. The front end circuitry is similar to several other systems such as software defined radio (SDR), sonar, radar or communications. Some applications require frequency coverage including DC or near DC, which is included in this example.



**Figure 7-1. Typical configuration for a spectrum analyzer with DC support**

#### 7.2.1 Design Requirements

Frequency domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone to under sampling in higher Nyquist zones. If a low input frequency is supported, then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA). If low frequency support is not needed, then AC coupling and use of a balun may be more suitable.

The internal reference is used since DC precision is not needed. However, the ADC AC performance is highly dependent on the quality of the external clock source. If in-band interferes can be present, then the ADC

SFDR performance is a key care about as well. A higher ADC sampling rate is desirable to relax the external anti-aliasing filter. An internal decimation filter can be used to reduce the digital output rate afterwards.

**Table 7-1. Design key care abouts**

FEATURE	DESCRIPTION
Signal Bandwidth	DC to 30MHz
Input Driver	Single ended to differential signal conversion and DC coupling
Clock Source	External clock with low jitter

When designing the amplifier/filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3910D125 input full-scale is 1.9 V<sub>PP</sub>. When factoring in approximately 1dB for insertion loss of the filter, then the amplifier needs to deliver close to 2.1 V<sub>PP</sub>. The amplifier distortion performance degrades with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The ADC3910D125 provides an output common mode voltage of 1.25V and the THS4541 for example can only swing within 250mV of its negative supply. A unipolar 3.3V amplifier power supply limits the maximum voltage swing to approximately 2.8 V<sub>PP</sub>. Hence, if a larger output swing is required (factoring in filter insertion loss) then a negative supply for the amplifier is needed in order to eliminate that limitation. Additionally, input voltage protection diodes may be needed to protect the ADC from over-voltage events.

**Table 7-2. Output voltage swing of THS4541 vs power supply**

DEVICE	MIN OUTPUT VOLTAGE	MAX SWING WITH 3.3V/ 0V SUPPLY
THS4541	VS- + 250mV	2.8 V <sub>PP</sub>

## 7.2.2 Detailed Design Procedure

### 7.2.2.1 Input Signal Path

The THS4541 provides a good low power option to drive the ADC inputs. [Table 7-3](#) provides an overview of the THS4541 with power consumption and usable frequency.

**Table 7-3. Fully Differential Amplifier Options**

DEVICE	CURRENT (IQ) PER CHANNEL	USABLE FREQUENCY RANGE
THS4541	10mA	< 70MHz

The low pass filter design (topology, filter order) is driven by the application. However, when designing the low pass filter, the optimum load impedance for the amplifier must also be taken into consideration.

### 7.2.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 20MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (that is, square wave vs sine wave).

Termination of the clock input needs to be considered for long clock traces.

### 7.2.2.3 Voltage Reference

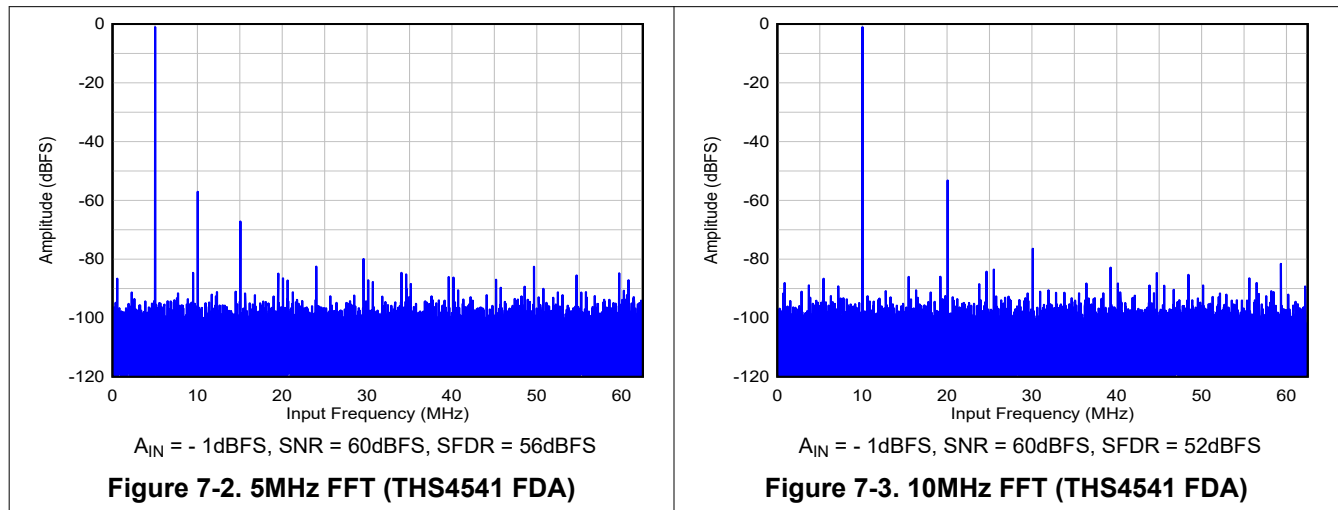
The ADC3910D125 provides two different options for supplying the voltage reference to the ADC. An external 1.2V reference can be directly connected to the VREF input or the internal 1.2V reference can be enabled to generate a reference voltage. For best performance, the reference noise needs to be filtered by connecting a 10μF and a 0.1μF ceramic bypass capacitor to the VREF pin when using an external reference and can be connected to ground when the internal reference is used.

#### Note

The voltage reference mode can be selected using SPI writes.

### 7.2.3 Application Curves

The following FFT plots show the performance of THS4541 driving the ADC3910D125 operated at 125MSPS with a full-scale input at -1dBFS.



### 7.3 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied the internal band gap reference powers up and settle out in approximately 2ms.
2. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up capacitor calibration is initiated. The calibration takes approximately 200000 clock cycles.
3. Begin programming using SPI interface.

#### 7.3.1 Register Initialization During Operation

If required, the serial interface registers can be cleared and reset to default settings during operation either:

- Through a hardware reset or
- By applying a software reset. When using the serial interface, set the RESET bit (register address 0x00) high. This setting initializes the internal registers to the default values, and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

After hardware or software reset the wait time is also approximately 200000 clock cycles before the SPI registers can be programmed.

## 7.4 Power Supply Recommendations

The ADC requires two different power-supplies. The AVDD rail provides power for the internal analog and digital circuits and the ADC itself while the IOVDD rail powers the digital interface. Power sequencing is not required.

The AVDD power supply must be low noise to achieve data sheet performance. In applications operating near DC, the 1/f noise contribution of the power supply also needs to be considered. The ADC is designed for very good PSRR which aids with the power supply filter design.

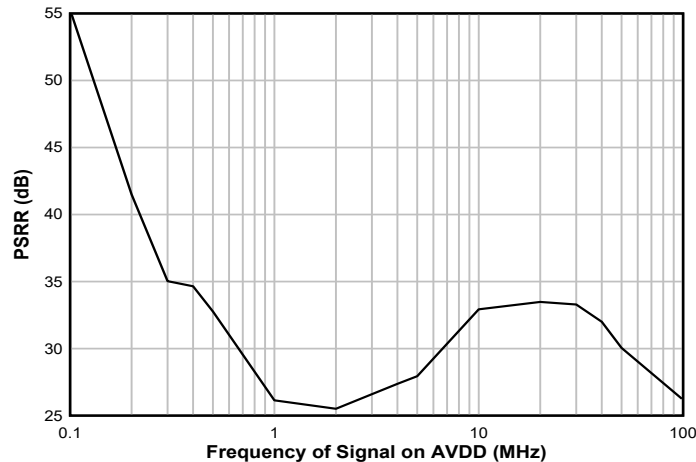


Figure 7-4. Power supply rejection ratio (PSRR) vs frequency

There are two recommended power-supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to make sure switching noise is minimized to prevent degraded ADC performance.

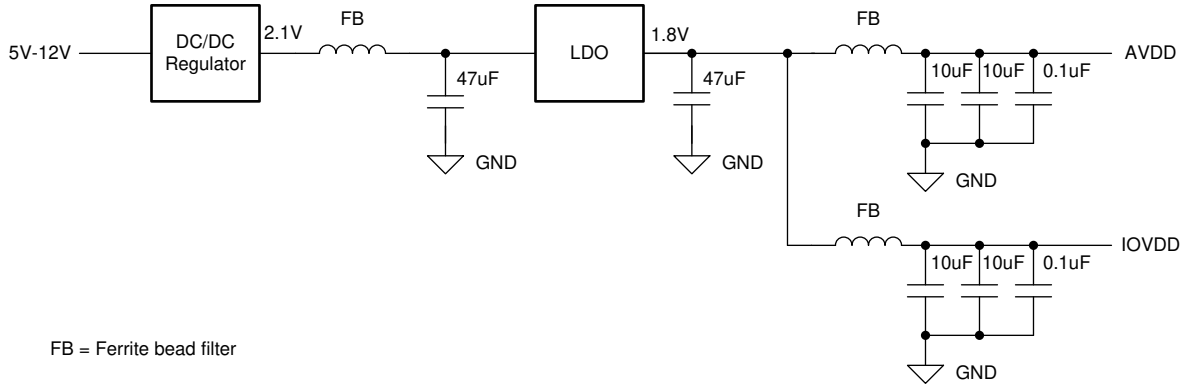
TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62821, and similar devices.

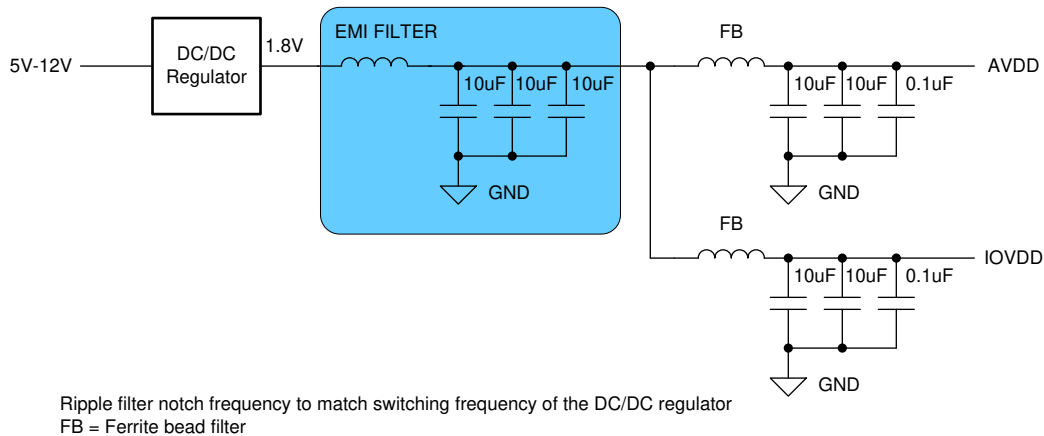
Recommended low dropout (LDO) linear regulators include the TPS7A4701, TPS7A90, LP5901, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. [Figure 7-5](#) and [Figure 7-6](#) illustrate the two approaches.

AVDD and IOVDD supply voltages should not be shared to prevent digital switching noise from coupling into the analog signal chain.



**Figure 7-5. Example: LDO Linear Regulator Approach**



**Figure 7-6. Example: Switcher-Only Approach**

## 7.5 Layout

### 7.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
  - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
2. Digital output interface
  - Traces should be as short as possible to reduce capacitive load seen by the CMOS outputs.
  - Series resistance should be used to reduce instantaneous current demand and improve signal integrity.
3. Power and ground connections
  - Provide low resistance connection paths to all power and ground pins.
  - Use power and ground planes instead of traces.
  - Avoid narrow, isolated paths which increase the connection resistance.
  - Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

### 7.5.2 Layout Example

The following screen shot shows the top layer of the [ADC3910D125EVM](#).

- Signal inputs are routed as different signal and along with clock input on the top layer avoiding vias.
- Serial CMOS output interface lanes with isolation resistor.
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

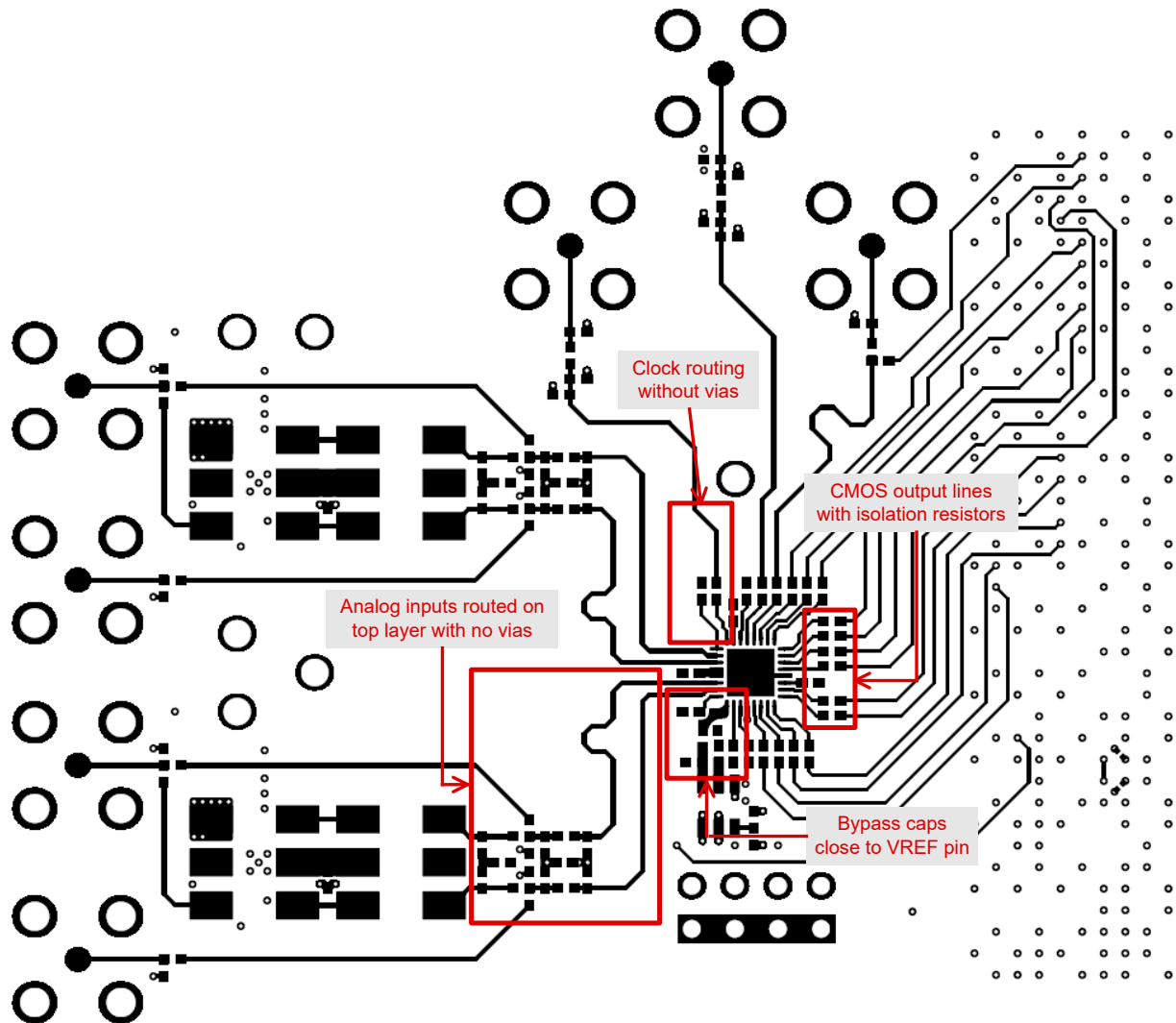


Figure 7-7. Layout Example: top layer of ADC3910D125EVM



## 8 Device and Documentation Support

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.

WEBENCH® is a registered trademark of Texas Instruments.

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### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (December 2023) to Revision A (May 2024)</b>	<b>Page</b>
• Deleted the Product preview note from the <i>Package Information</i> table.....	1
• Added I <sub>AVDD</sub> , I <sub>IOVDD</sub> max for all devices in the family.....	6
• Changed ADC3910D125 P <sub>DIS</sub> from 92mW to 97mW.....	6
• Added DNL, INL, offset min and max for 25/65MSPS.....	6
• Changed 25MSPS GAIN <sub>ERR</sub> , Ext. Ref. from ±1.3%FSR to ±0.2%FSR.....	6
• Added GAIN <sub>ERR</sub> , Ext. Ref. min and max for 25/65MSPS.....	6
• Changed 25MSPS GAIN <sub>ERR</sub> , Int. Ref. from ±1.3%FSR to ±0.8%FSR.....	6
• Changed 65MSPS GAIN <sub>ERR</sub> , Ext. Ref. from ±1.3%FSR to ±0.2%FSR.....	6
• Changed 65MSPS GAIN <sub>ERR</sub> , Int. Ref. from ±1.3%FSR to ±0.8%FSR.....	6
• Changed 125MSPS GAIN <sub>ERR</sub> , Ext. Ref. from ±1.3%FSR to ±0.3%FSR.....	6
• Changed 125MSPS GAIN <sub>ERR</sub> , Int. Ref. from ±1.3%FSR to ±0.8%FSR.....	6
• Added SNR, SFDR, SPUR min for 25MSPS.....	9
• Added SNR, SFDR, SPUR min for 65MSPS.....	9
• Updated interface timings.....	12
• Removed setup/hold naming in timing diagrams.....	14
• Added 8-bit, 12-bit modes. Updated Lane Rate Examples table.....	39

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC3910D025IRSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D1
ADC3910D025IRSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D1
<a href="#">ADC3910D025IRSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D1
ADC3910D025IRSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D1
ADC3910D065IRSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D2
ADC3910D065IRSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D2
<a href="#">ADC3910D065IRSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D2
ADC3910D065IRSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391D2
<a href="#">ADC3910D125IRSMR</a>	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	AZ391D3
ADC3910D125IRSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	AZ391D3
<a href="#">ADC3910D125IRSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	AZ391D3
ADC3910D125IRSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	AZ391D3
ADC3910S025IRSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S1
ADC3910S025IRSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S1
<a href="#">ADC3910S025IRSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S1
ADC3910S025IRSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S1
ADC3910S065IRSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S2
ADC3910S065IRSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S2
<a href="#">ADC3910S065IRSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S2
ADC3910S065IRSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S2
ADC3910S125IRSMR	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S3
ADC3910S125IRSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S3
<a href="#">ADC3910S125IRSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S3
ADC3910S125IRSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AZ391S3

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

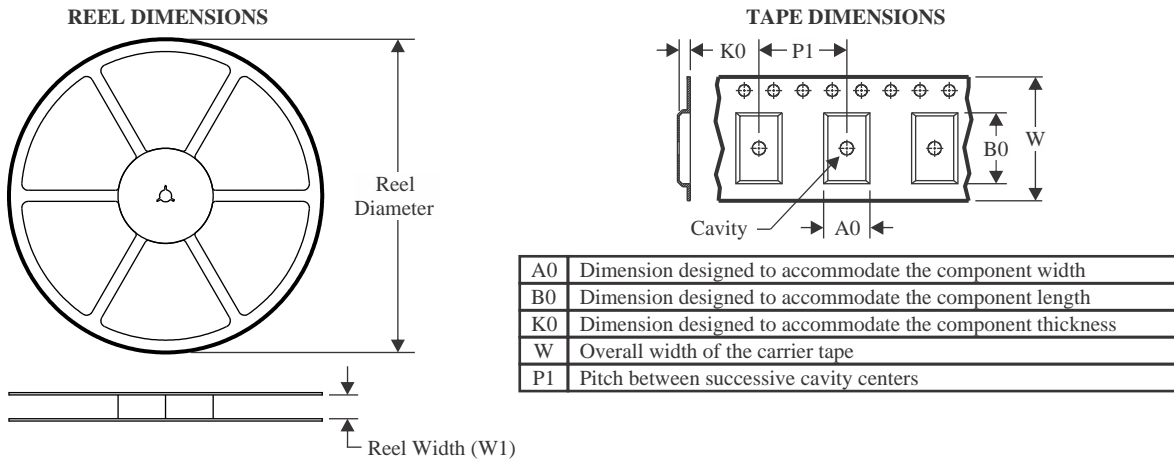
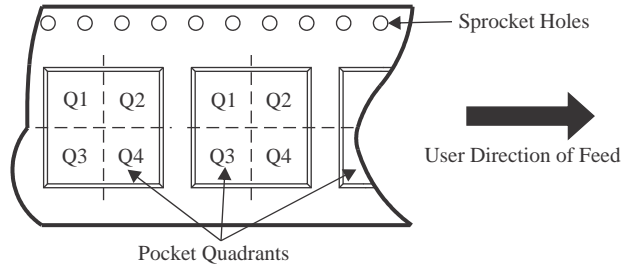
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3910D025IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910D025IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910D065IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910D065IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910D125IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910D125IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910S025IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910S025IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910S065IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910S065IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910S125IRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADC3910S125IRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3910D025IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3910D025IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3910D065IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3910D065IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3910D125IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3910D125IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3910S025IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3910S025IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3910S065IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3910S065IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
ADC3910S125IRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
ADC3910S125IRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

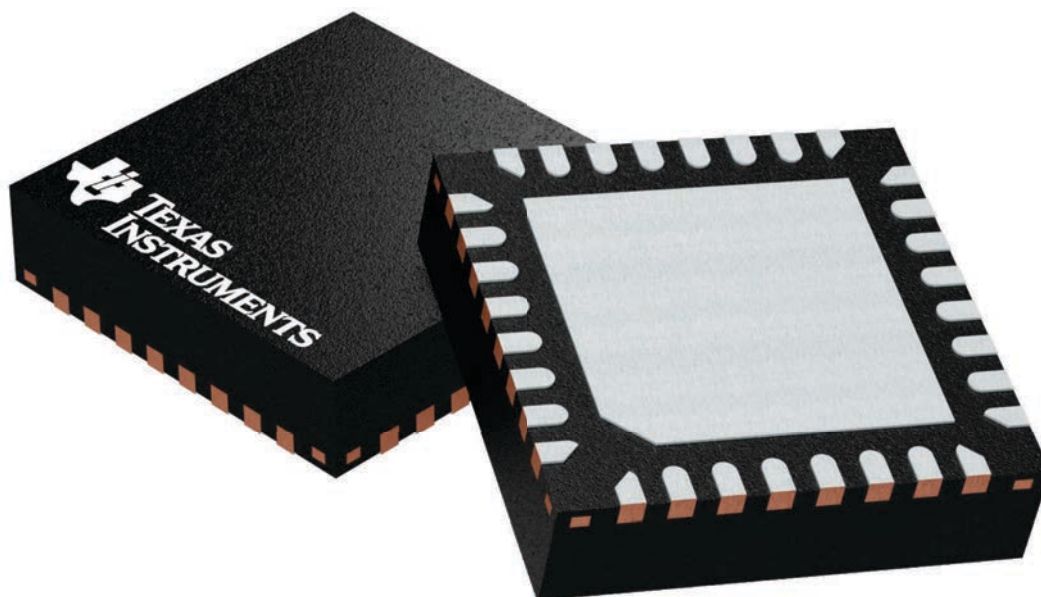
**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

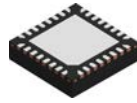
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

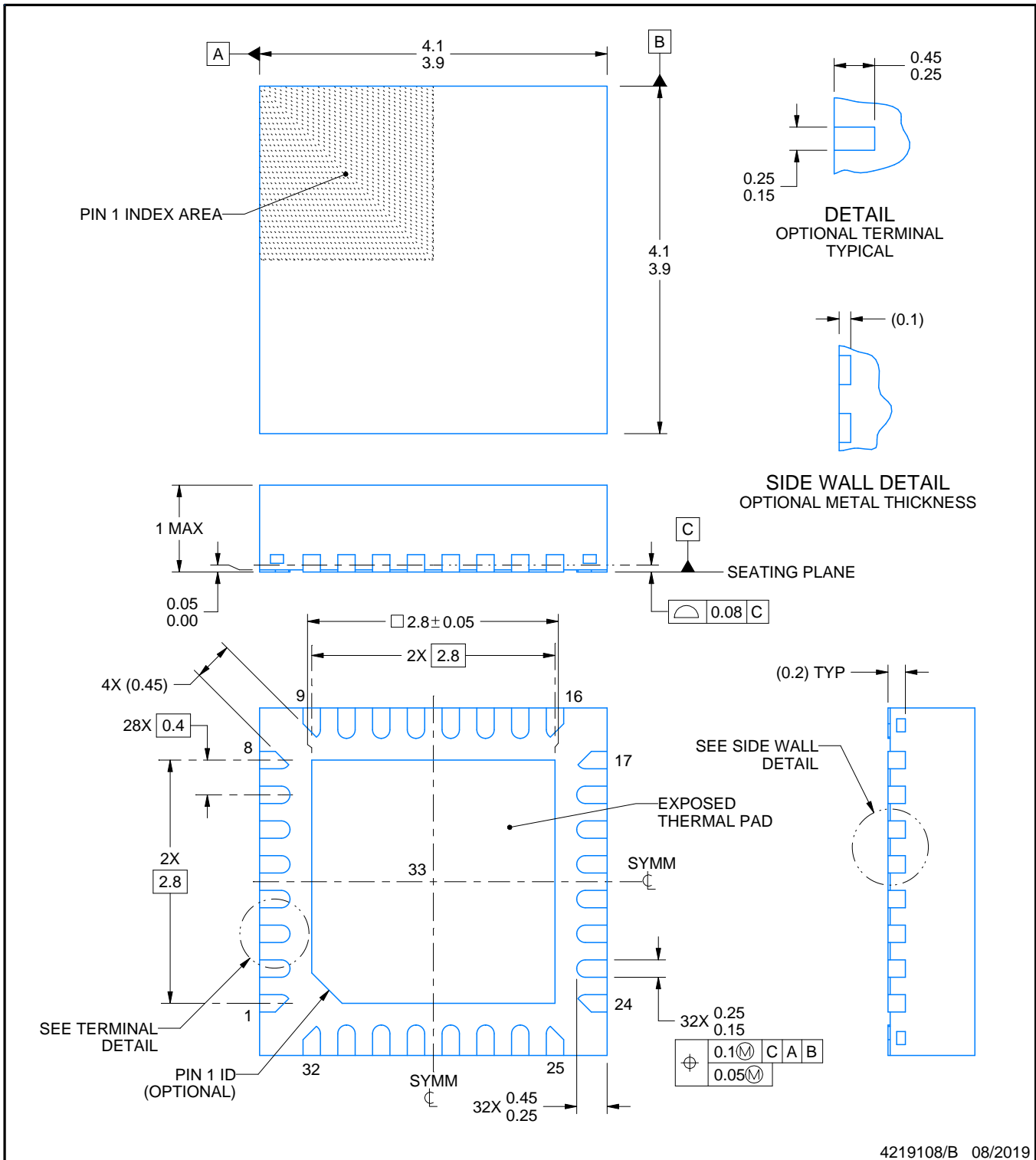
# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

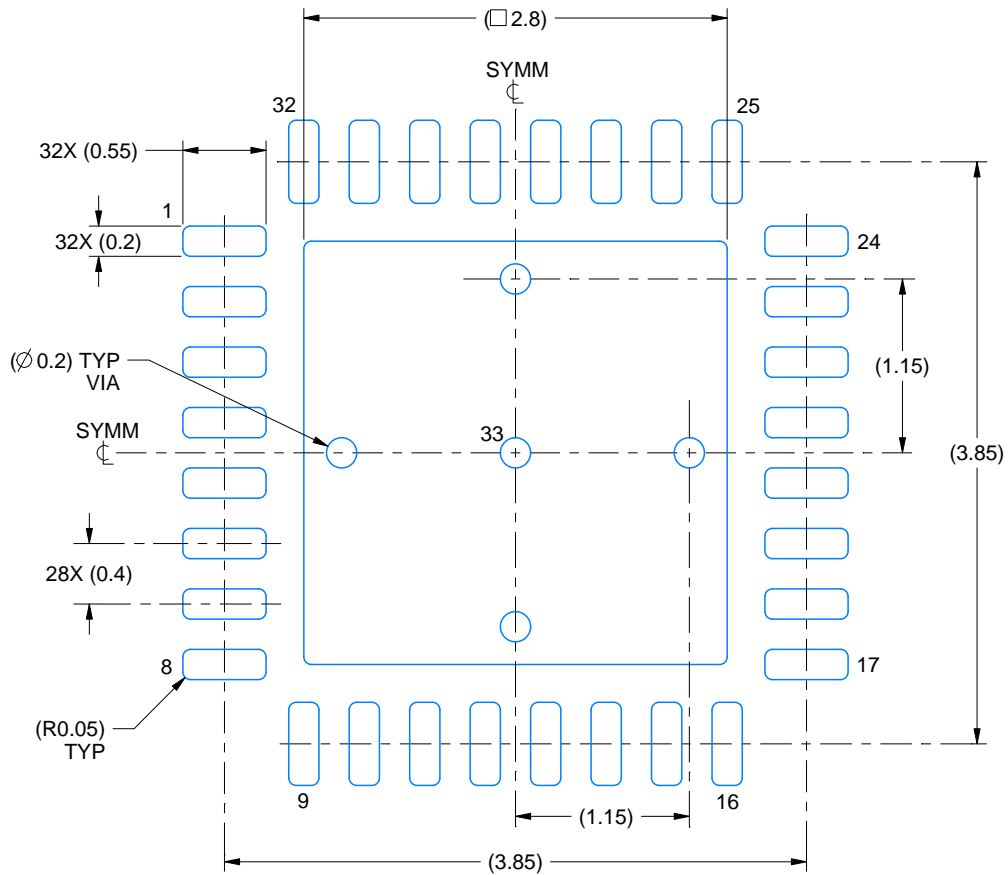


# EXAMPLE BOARD LAYOUT

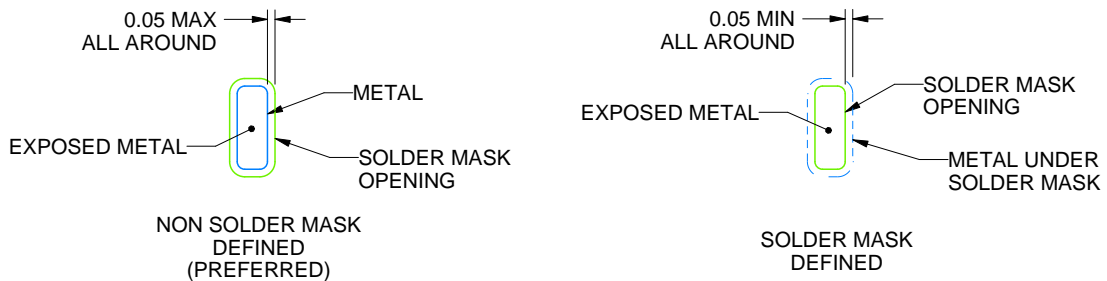
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

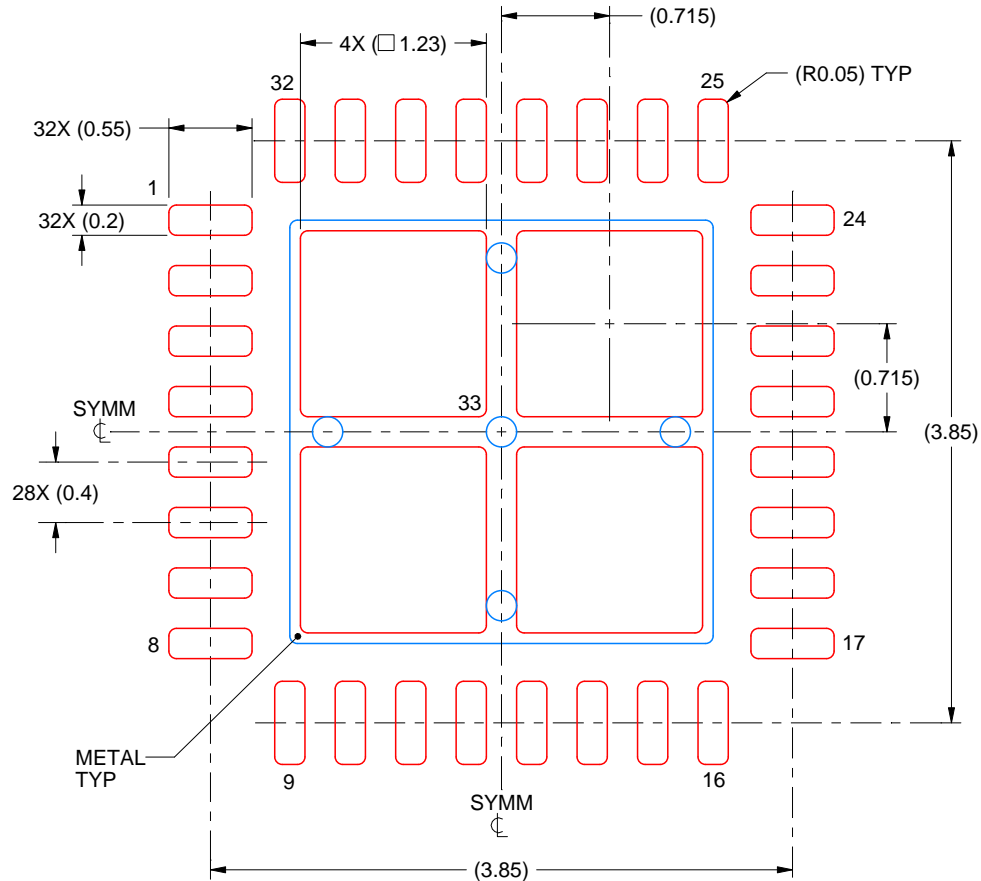
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025