Drill Table: Top Layer to Bottom Layer

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance (+)	Hole Tolerance (-)	Hole Length	Routed Path Length
[8] ◇	13	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
[8] ▽	2365	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
[8] ⊠	267	12.20mil (0.310mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
[8] E	10	15.00mil (0.381mm)	PTH	Round	Top Layer - Bottom Layer	0.00mil (0.000mm)	15.00mil (0.381mm)	-	-
◎	6	23.62mil (0.600mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
⧓	2	23.62mil (0.600mm)	PTH	Slot	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	51.18mil (1.300mm)	27.56mil (0.700mm)
▣	2	33.47mil (0.850mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
▼	4	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
○	1	80.00mil (2.032mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
□	8	118.11mil (3.000mm)	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
☼	18	32.00mil (0.813mm)	NPTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
✱	6	40.16mil (1.020mm)	NPTH	Round	Top Layer - Bottom Layer	2.00mil (0.051mm)	2.00mil (0.051mm)	-	-
✪	4	126.00mil (3.200mm)	NPTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
	2706 Total								

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

NOTE :
1. THIS IS AN IMPEDANCE CONTROLLED BOARD.
2. EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

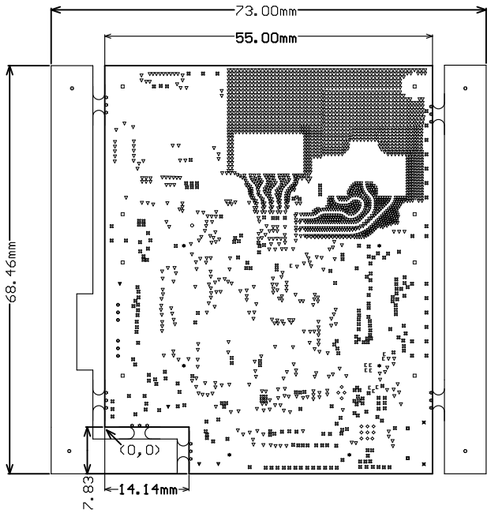
IMPEDANCE TABLE : [6]

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	9.3 MILS	5.3 MILS	50 OHM	LAYER-2 (GND LAYER)

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP AND BOTTOM	5.2 MILS	5 MILS	100 OHM	LAYER-2 AND LAYER-7
L3 & L6	4.8 MILS	7.2 MIL	100 OHM	LAYER-2,LAYER 7
TOP,L5	6 MILS	-	50 OHM	LAYER-2, LAYER 6

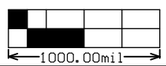
NOTES:

1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
3. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL.
5. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL.
6. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3, 6 & 8.
7. FOR ACCURACY OF THE ANTENNA DIMENSION, NEED TO BE MEASURE THE ANTENNA DIMENSIONS ON ONE BAORD AS PER ANTENNA DOCUMENT(Visio-IWR_60GHz4).
8. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER.
9. INTENTIONAL ONE NET ANTENNA VIA IS PRESENT IN DESIGN.
10. VIA HOLE OFFSET SHALL BE WITHIN 1MILS OF ITS ORIGINAL LOCATION



LAYER STACK-UP :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	1	
[6] 1	Top Layer	Copper	1.60mil		
	Dielectric 1	Isola FR408HR (DUAL PLY, 2x1067, SPREAD GLASS)	5.00mil	3.33	
2	L2_GND	Copper	1.40mil		
	Dielectric 2	PCL370HR	5.50mil	4.17	
[6] 3	L3_SIGNAL 1	Copper	1.40mil		
	Dielectric 3	PCL370HR	10.00mil	4.17	
4	L4_SIGNAL 2	Copper	1.40mil		
	Dielectric 4	PCL370HR	5.50mil	4.17	
5	L5_SIGNAL 3	Copper	1.40mil		
	Dielectric 5	PCL370HR	10.00mil	4.17	
[6] 6	L6_SIGNAL 4	Copper	1.40mil		
	Dielectric 6	PCL370HR	5.50mil	4.17	
7	L7_GND	Copper	1.40mil		
	Dielectric 7	PCL370HR	5.00mil	4.17	
[6] 8	Bottom Layer	Copper	1.60mil		
	Bottom Solder	Solder Resist	0.80mil	1	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 3.9 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.127mm (5.0MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☐ FR-4 High Tg ☒ OTHER REFER STACK-UP
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 57.37 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☐ MATTE ☒ SEMI-GLOSS
SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☐ ENEPIG
☒ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____
ARRAY/PANEL: ☒ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☐ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 1 & 6 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: IWR6843 LOW COST EVM
DESIGNED FOR: Public Release
FILE NAME: PROC116A_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC116 / REV: A / SVN REV: Not In VersionControl
LAYER NAME = [illegible] Dimensions	TID #: N/A
PLOT NAME = Fabrication Drawing 1	GENERATED : 19-10-2021 18:44:01 / TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Chethan Kumar Y.B	Mistral
SCALE: 1.00	ALTIUM DESIGNER VERSION: 19.1.9.167