

1

2

3

4

5

6

A

B

C

D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		2.80mil		
	Dielectric 1	FR-4 High Tg	10.00mil	4.2	
2	GND Layer		1.40mil		
	Dielectric 2	FR-4 High Tg	31.00mil	4.2	
3	Signal Layer 1		1.40mil		
	Dielectric 3	FR-4 High Tg	10.00mil	4.2	
4	Bottom Layer		2.80mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
⊕	3	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
■	1	7.88mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
◇	4	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	
▽	23	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	9	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
□	3	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	4	98.43mil (2.500mm)	PTH	Round	Top Layer - Bottom Layer	
○	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	
	51 Total					

71.12mm

88.90mm

1000.00mil

ALL ARTWORK VIEWED FROM TOP SIDE

BOARD #: SR019

REV: A

SUN REV: Not in version control

LAYER NAME = 06059-0143

TID #: N/A

PLOT NAME = Fabrication Drawing

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TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE:
.PRJ_Title

DESIGNED FOR:
Public Release

FILE NAME:
SR019A.PcbDoc

ENGINEER:
Marshall Beck

LAYOUT BY:
Marshall Beck

SCALE: 1.00

ALTUM DESIGNER VERSION:
22.1.2.22