User's Guide

ADCxxDJxx00RF/SE Evaluation Module

ABSTRACT

The ADCxxDJxx00RFEVM/SEEVM is an evaluation board used to evaluate the ADC12DJ5200RF, ADC12DJ4000RF, ADC08DJ5200RF, ADC12DJ5200SE analog-to-digital converters (ADC) from Texas Instruments. The ADC12DJ5200RF and SE is a dual-channel, 12/08-bit ADC, capable of operating at sampling rates up to 5.2 and 4 Giga-samples per second (GSPS) in dual-channel mode, or 10.4 and 8 GSPS in single-channel mode. The ADC12DJ5200RF/SE, ADC12DJ4000RF, ADC08DJ5200RF output data is transmitted over a standard JESD204C high-speed serial interface. This evaluation board also includes the following important features:

- Transformer-coupled signal input network allowing a single-ended signal source from 500 kHz to 9 GHz. ADC12DJ5200SE has an internal balun in the ADC chip.
- The LMX2594 clock synthesizer generates the ADC sampling clock
- The LMK04828, LMK61E2 and LMX2594 onboard system clock generator generates SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the ADC performance with an external low-noise clock source
- LM95233 temperature sensor
- High-speed serial data output over a High Pin Count FMC+ interface connector

Note

To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in Table 8-1).

- Device register programming through USB connector and FTDI USB-to-SPI bus translator

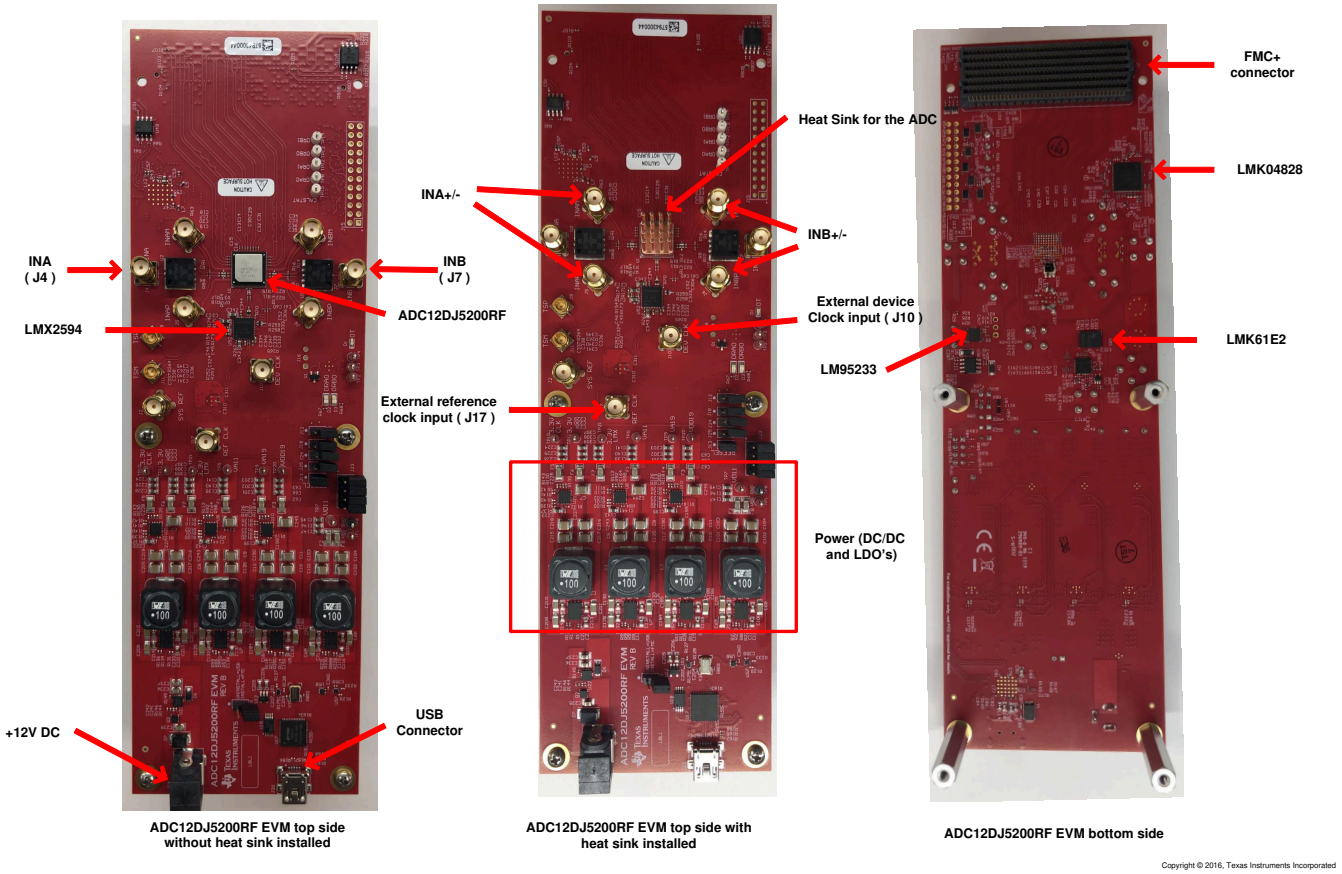

Figure 1-1. EVM Orientation

The digital data from the ADCxxDJxx00RFEVM/SEEVM board is quickly and easily captured with the TSW14J57EVM data capture boards.

Note

The TSW14J57EVM cannot be used for JMODES that use 64b/66b encoding, or serial rates above 15 Gbps.

The TSW14J57EVM captures the high-speed serial data, decodes the data, stores the data in memory, and then uploads it to a connected PC through a USB interface for analysis. The High-Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDC Pro software, the TSW14J57 device is automatically configured to support a wide range of operating speeds of the ADCxxDJxx00RFEVM/SEEVM, but the device may not cover the full operating range of the ADC device. Serial data rates of 15 Gbps down to 1 Gbps are supported.

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1 Trademarks

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2 Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

2.1 Evaluation Board Feature Identification Summary

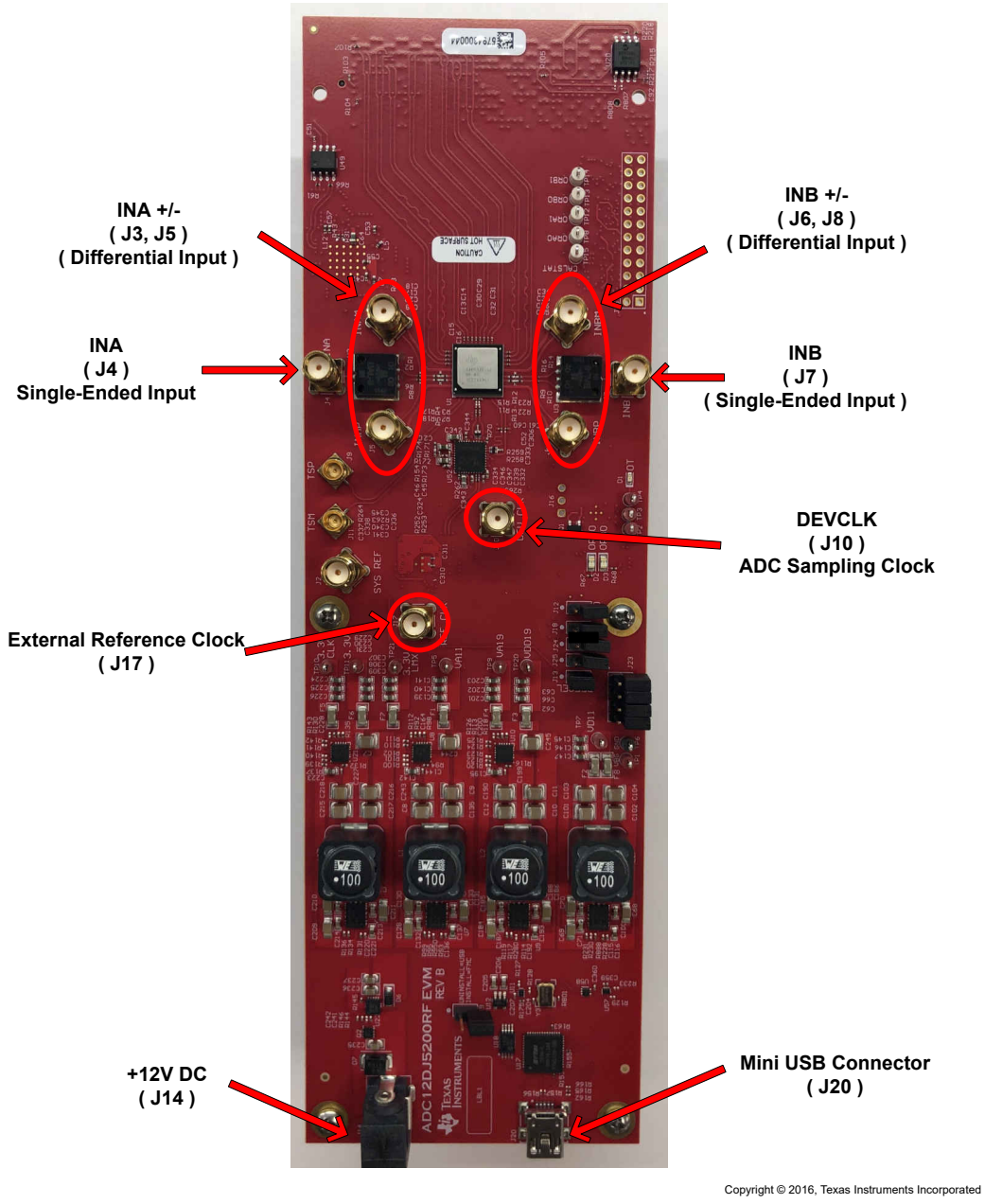

Figure 2-1. EVM Feature Locations

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14J57EVM data capture board and related items
- High-Speed Data Converter Pro software.
- PC computer running Microsoft® Windows® 7, or 10
- Two low-noise signal generator one for DEVCLK (Sampling clock) second for providing reference signal. TI recommends the following generators:
  - Rohde & Schwarz® SMA100B
  - Rohde & Schwarz® SMA100A
- One low-noise signal generator for analog input. TI recommends the following generators:
  - Rohde & Schwarz® SMA100B
  - Rohde & Schwarz® SMA100A
- Bandpass filter for analog input signal (2897 MHz or desired frequency). The following filters are recommended:
  - Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
  - Trilithic™ 5VH-series tunable BPF
  - K&L Microwave™ BT-series tunable BPF
  - TTE KC6 or KC7-series fixed BPF
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the ADCxxDJxx00RFEVM/SEEVM has an external clocking solution. A few small board modifications enable onboard clocking. If onboard clocking is used, the following equipment is recommended.

- One low-noise signal generators. TI recommends similar models to the analog input source.
- A bandpass filter for the analog input. TI recommends a filter similar to the analog-input path filter.

Note

The frequency of clock source used to drive the external reference clock (labeled REF CLK J17) displayed on the first page of the GUI under Reference Clock. The reference clock frequency is calculated by the GUI using JMODE and the sampling frequency (Fs) entered by the user. The reference clock generator and device clock generator must be frequency-locked using a common 10-MHz reference.

3 Setup Procedure

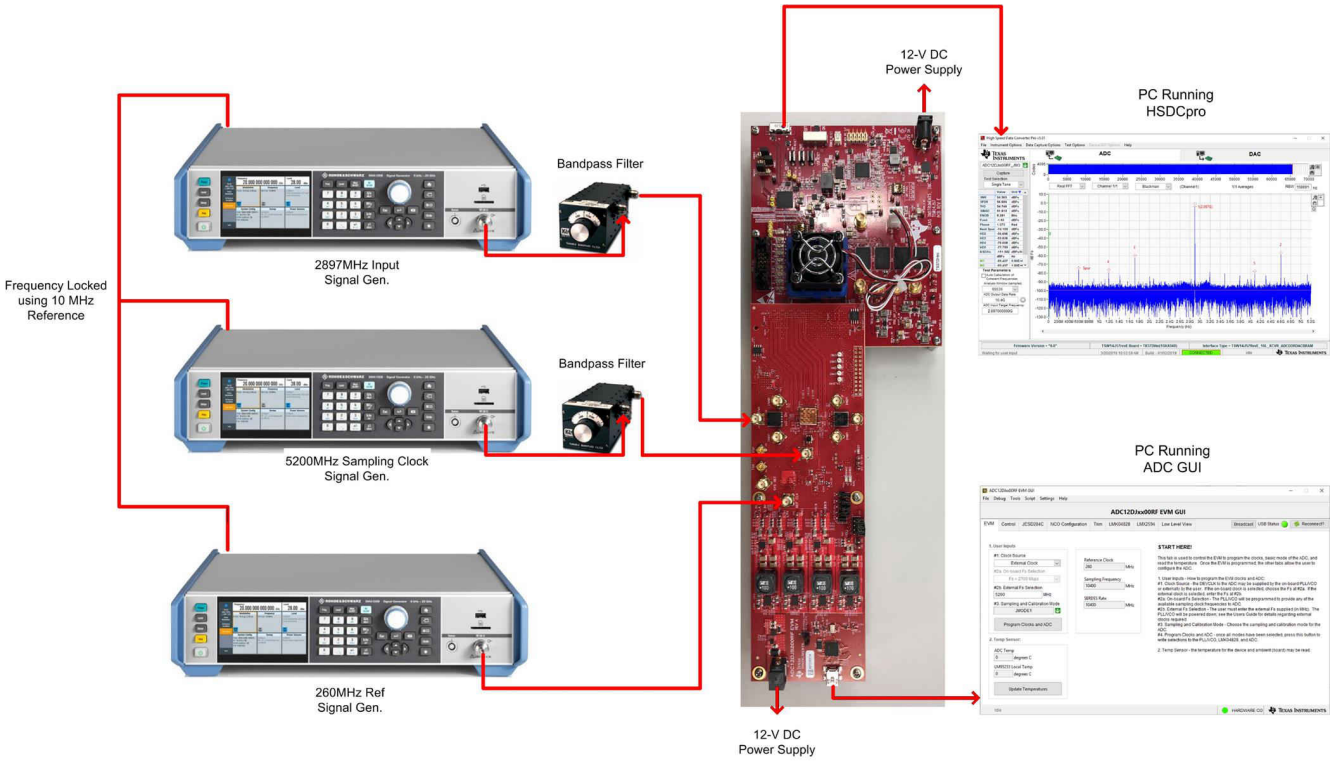

Figure 3-1. EVM Test Setup

Note

The HSDC Pro software must be installed before connecting the TSW14J57EVM to the PC for the first time.

3.1 Install the High Speed Data Converter (HSDC) Pro Software

1. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Install the Configuration GUI Software

1. Download the Configuration GUI software from the EVM tool folder at ADC12DJ5200RF GUI.
2. Extract files from the .zip file.
3. Run the executable file (`setup.exe`), and follow the instructions.

3.3 Connect the EVM and TSW14J57EVM

With the power off, connect the ADCxxDJxx00RFEVM/SEEVM to the TSW14J57EVM through the FMC connector as shown in Figure 3-1. Ensure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14J57EVM is in the off position. Connect the power cable to a 12-V DC (minimum 4A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector.
2. Confirm that the power switch for the ADC12DJ5200EVMs power supply is in the off position. Connect the power cable to a 12-V DC (minimum 2 A) power supply. Make sure the proper supply polarity by confirming

that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector.

CAUTION

Make sure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage.

Leave the power switches in the off position until directed later.

3.5 Connect the Signal Generators to the EVM (RF Outputs Disabled Until Directed)

Connect a signal generator to the VIN input of the ADC12DJ5200RFEVM through a bandpass filter and attenuator at the SMA connector. This must be a low-noise signal generator. TI recommends a bandpass filter to filter the signal from the generator. Configure the signal generator for 2897 MHz, 6 dBm.

Note: ADC12DJ5200SE has an integrated input balun and extenal balun is not required. When using ADC12DJ5200SEEVM INAP(connector J5) should be used Channel A input and INBP(J6) should be used for channel B input. To appply an analog input signal use a bandpass filter to filter the signal from the generator. Configure the signal generator for 2897 MHz, 0 dBm.

When External Clocking is Used

1. Connect a signal generator to the DEVCLK input of the EVM through a bandpass filter. This signal generator must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for the desired clock frequency in the range of 0.8 to 5.2 GHz. For best performance when using an RF signal generator, the power input to the CLK SMA connector must be 10 dBm (2.0 Vpp into 50 Ω). The signal generator must increase above 10 dBm by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2 dB, the signal generator must be set to 10 dBm + 2 dB = 12 dBm.

1. Connect a signal generator to the reference signal input of the EVM at REF CLK(J17). Configure the signal generator for the desired (260MHz) clock frequency. Set the output power to approximately 6–9 dBm.

Note

a. The Reference clock frequency can be obtained from the ADC12DJ5200EVM GUI. Once the ADC12DJ5200EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown with red square in Figure 3-2
b. Ensure that the DEVCLK and Reference clock sources are frequency-locked using a common 10-MHz reference to ensure functionality. Frequency locking the input signal generator to the other generators can also be done if coherent sampling is desired.
c. Do not turn on the RF output of any signal generator at this time.
d. When using the ADC in single-input mode, the device uses both edges of DEVCLK for sampling.

3.6 Turn On the TSW14J57EVM Power and Connect to the PC

1. Turn on the power switch of the TSW14J57EVM.
2. Connect a mini-USB cable from the PC to the TSW14J57EVM.
3. If this is the first time connecting the TSW14J57EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the TSW14J57EVM user's guide for specific instructions.

3.7 Turn On the ADC12DJ5200RFEVM/SEEVM Power Supplies and Connect to the PC

1. Turn on the 12-V power supply to power up the EVM.
2. Connect the EVM to the PC with the mini-USB cable.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to VIN. If external clocking is used, turn on the RF signal outputs connected to DEVCLK and Reference clock.

3.9 Open the ADC12DJ5200RFEVM/SEEVM GUI and Program the ADC and Clocks

The Device Configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

Note

The max clock rate supported by ADC12DJ4000RF is 4000 MHz and only 8-bit mode are suppored by ADC08DJ5200RF. All the 12-bit and 15-bit modes are disabled on ADC08DJ5200RF.

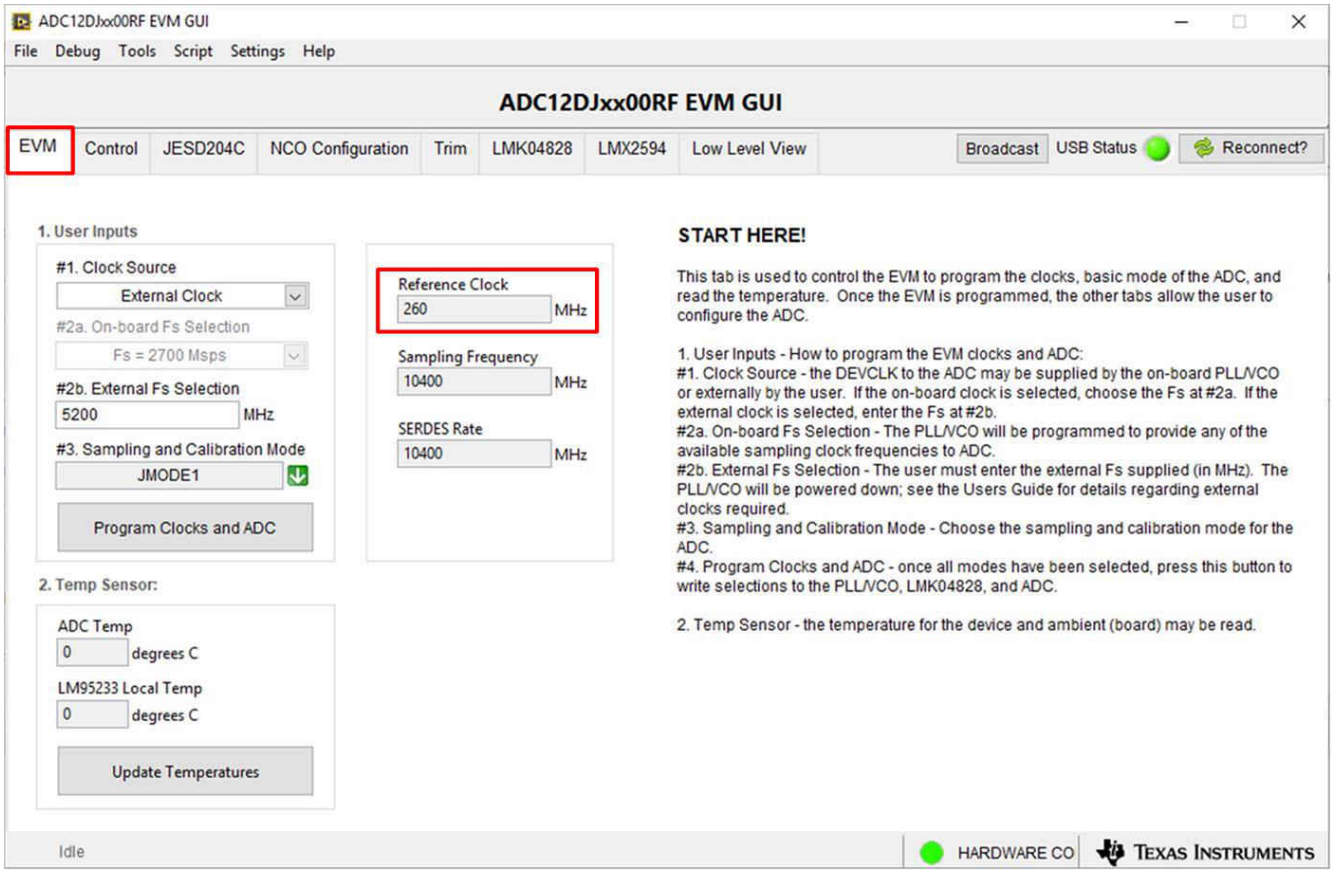

Figure 3-2. Configuration GUI EVM Tab

Figure 3-2 and Figure 3-3 show the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the ADC12DJ5200RF/SE, LMK04828, LMK61E2, and LMX2594. The register map for each device is provided in the device data sheet (ADC12DJ5200RF/SE 10.4-GSPS Single Channel or 5.2-GSPS Dual Channel, 12-bit, RF, LMK0482xB Ultra Low-Noise JESD204B Cmplnt Clck Jitter Cleaner w/ Dual Loop PLLs, and LMX2594 15-GHz Wideband PLLatinum™ RF Synthesizer, respectively).

1. Open the ADC12DJ5200RFEVM GUI.
2. Select the external clock as the clock source.
3. Enter Fs = 5200 MHz MSPS as the external Fs selection.
4. Select JMODE1 for the sampling and Calibration mode.
5. Click *Program Clocks and ADC* (Note: This action will overwrite any previous device register settings.)
6. The Reference frequency required by the EVM is shown under indicator Reference Clock.

3.10 Calibrate the ADC Device on the EVM

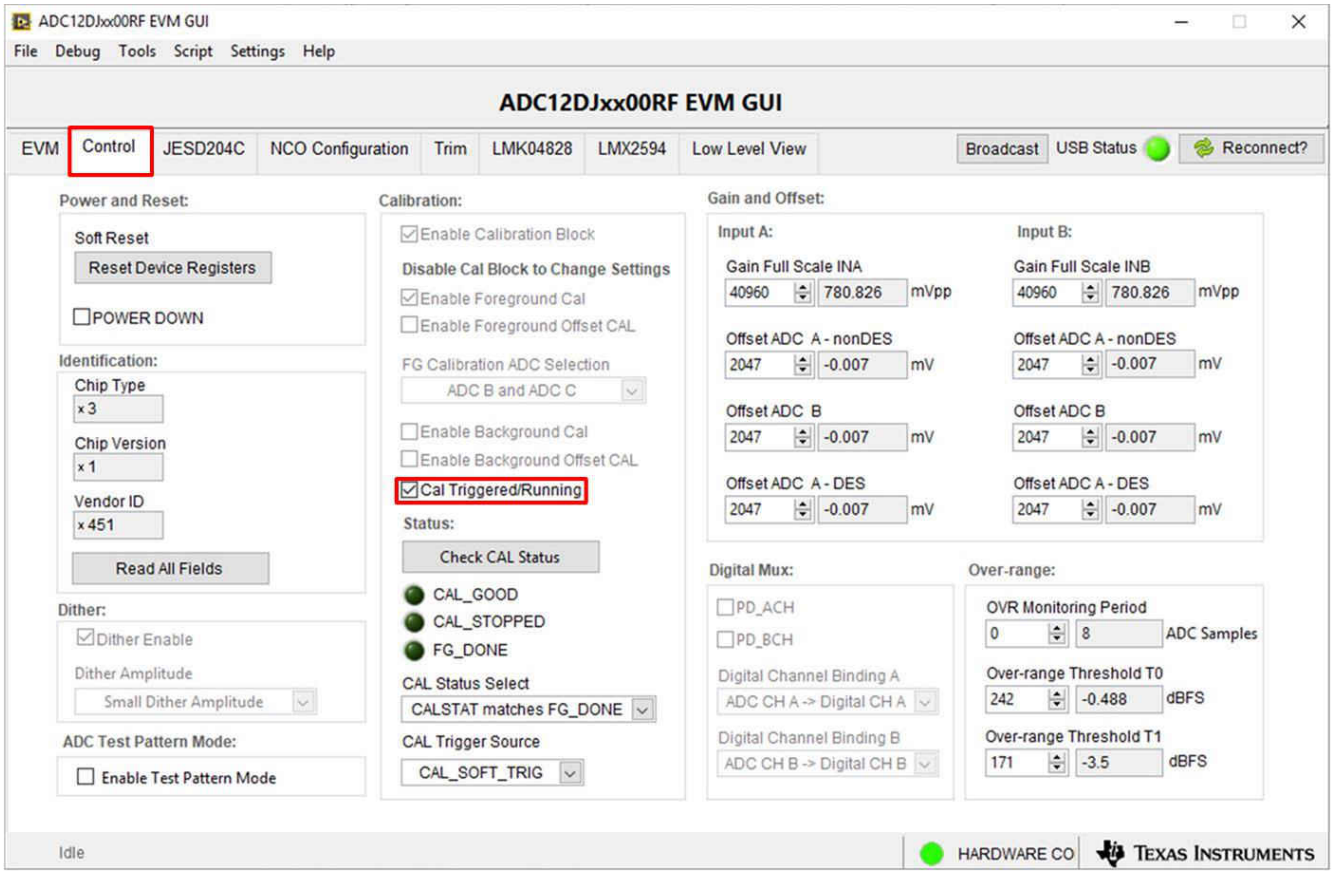

Figure 3-3. Configuration GUI ADC Control

1. With the EVM GUI open on the PC, navigate to the *Control* tab.
2. To calibrate the ADC, click *Cal Triggered/Running* once, then click it again. This will stop and re-start the Calibration engine.

Note

This calibrate button executes a calibration sequence that is required for full performance. This calibration is performed automatically during the Section 3.9 step but must be performed again, any time the sampling rate changes, after significant temperature change of the ADC, or after exiting the power-down mode. See the ADC12DJ5200RF/SE device data sheet, (SLVSEN9) for details regarding the necessary calibration sequence.

3. To enable background calibration, use the following steps:

- Navigate to the *JESD204C* tab and click on *JESD Block Enable* to stop the JESD204C block.
- Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
- Click on *Enable Background Cal*.
- If background offset calibration is desired also, click on *Enable Background Offset Cal*.
- Click on *Enable Calibration Block* to re-enable the calibration subsystem
- Navigate to the *JESD204C* tab and click on *JESD Block Enable* to re-start the JESD204C block.
- Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

4. To disable background calibration, use the following steps:
   - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to stop the JESD204C block.
   - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
   - If background offset calibration was enabled, click on *Enable Background Offset Cal* to disable the feature.
   - Click on *Enable Background Cal* to disable the feature.
   - Click on *Enable Calibration Block* to re-enable the calibration subsystem.
   - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to re-start the JESD204C block.
   - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

3.11 Open the HSDC Software and Load the FPGA Image to the TSW14J57EVM

1. Open the HSDC Pro software.
2. Click *OK* to confirm the serial number of the TSW14J57EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the ADC12DJ5200RFEVM/SEEVM.
3. Select the ADC12DJxx00RF_JMODE1 device from the ADC select drop-down in the top left corner.
4. When prompted, click *Yes* to update the firmware.

Note

If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See Section 7 for more details.

5. Enter the ADC Output Data Rate ($f_{(SAMPLE)}$) as "10400M" or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.12 Capture Data Using the HSDC Pro Software

The following steps show how to capture data using the HSDC Pro software (see Figure 3-4):

1. Select the test to perform.
2. Select the data view.
3. Select the channel to view.
4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable Continuous Capture or FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value less than the number of total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

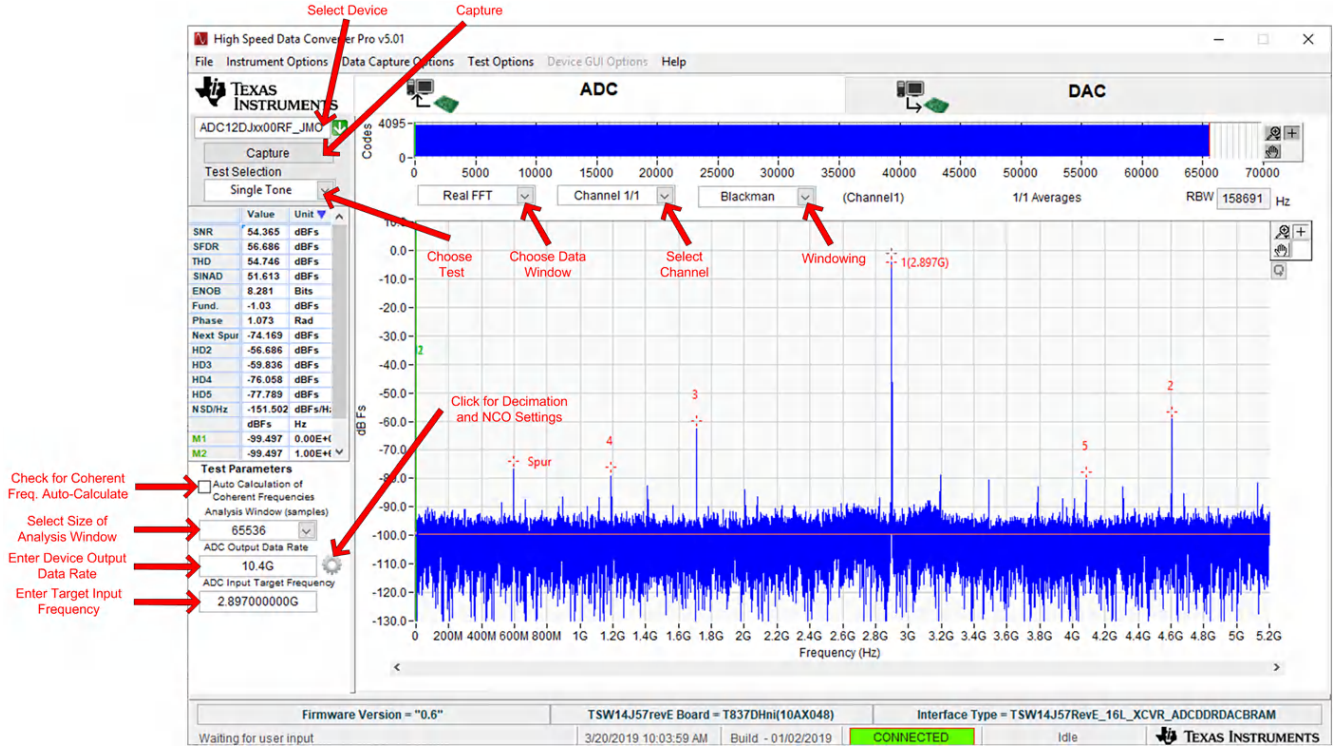

Figure 3-4. High Speed Data Converter Pro (HSDC) GUI

When using decimation and NCO features, click the gear symbol to access the *Additional Device Parameters* dialog box to enter the following details:

1. ADC Sampling Rate
2. ADC Input Signal Frequency
3. NCO Frequency
4. Decimation Factor

The HSDC Pro GUI will calculate the *ADC Output Data Rate* based on these inputs. The *Fundamental and Harmonic* frequency locations will also be calculated and identified in the FFT display.

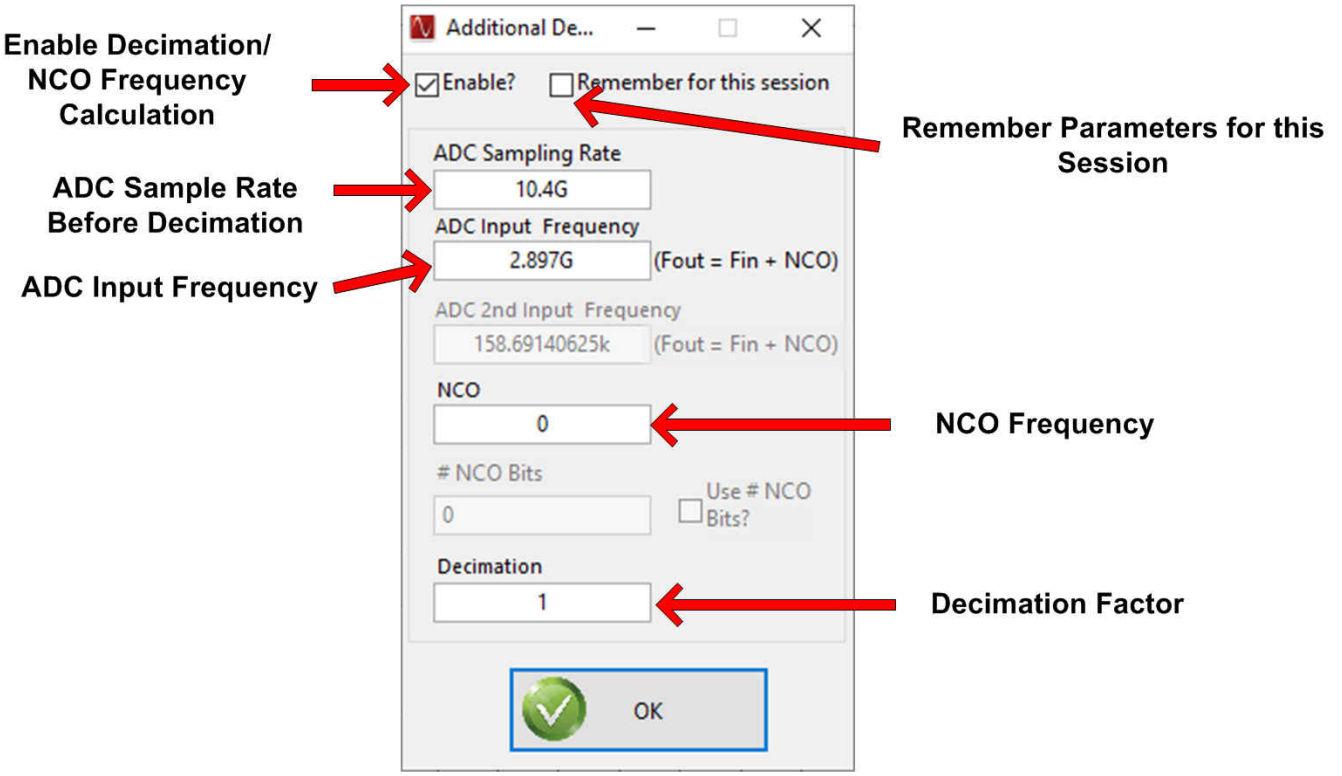

Figure 3-5. Additional Device Parameters Dialog Box

4 Device Configuration

The ADC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

For more information about the registers in the ADC device, see the ADC12DJ5200RF/SE device data sheet.

4.1 Supported JESD204C Device Features

The ADC device supports some configuration of the JESD204C interface. Due to limitations in the TSW14J57EVM firmware, all JESD204C link features of the ADC device are not supported. Table 4-1 lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204C Device

JESD204C Feature	Supported by ADC Device	Supported by TSW14J57EVM	Supported by TSW14J58EVM
Number of lanes per link (L)	L = 1, 2, 3, 4, 6, 8(1)	L = 1, 2, 3, 4, 6, 8 supported	L = 1, 2, 3, 4, 6, 8 supported
Total number of lanes active	2, 4, 6, 8, 12, 16	2, 4, 6, 8, 12, 16	2, 4, 6, 8, 12, 16
Number of frames per multiframe (K)	K_{min} = 3–256,(1) K_{max} = 256, K_{step} = 1 or 2	Most values of K supported, constrained by requirement that $K \times F = 4^n$	Most values of K supported, constrained by requirement that $K \times F = 4^n$
Scrambling	Supported	Supported	Supported
Test patterns	PRBS7, PRBS9, PRBS15, PBRS23, PRBS31, Ramp, Transport Layer test, D21.5, K28.5, Repeat ILA, Modified RPAT, Serial Out 0, Serial Out 1, Clock test, ADC Test Pattern(1)	ILA, Ramp, Long/Short Transport	ILA, Ramp, Long/Short Transport
Speed	Lane rates from 0.8 to 17.12 Gbps(1)	Lane rates from 2 to 15 Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.	Lane rates from 0.6 to 17.16Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204C settings. Once the settings are changed, re-enable the JESD204 block.

4.2 Tab Organization

Control of the ADC device features are available in the EVM, Control, JESD204C, NCO Configuration tabs.

4.3 Low-Level Control

The *Low Level View* tab, illustrated in Figure 4-1, allows configuration of the devices at the bit-field level. At any time, the controls in Table 4-2 can be used to configure or read from the device.

Table 4-2. Low-Level Controls

Control	Description
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the register data cluster • The value column shows the value of the register at the time the GUI was last updated • The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the *Write Data* field
Write all button	Update all registers shown in the register map summary with the values shown in the *Register Map* summary
Read register button	Read from the register highlighted in the *Register Map* summary and display the results in the *Read Data* field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the *Register Map* summary and display the current state of the hardware
Load Configuration button	Load a configuration file from disk and register address/data values in the file
Save Configuration button	Save a configuration file to disk that contains the current state of the configuration registers
Register Data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the *Block* drop-down box using the address and write data information

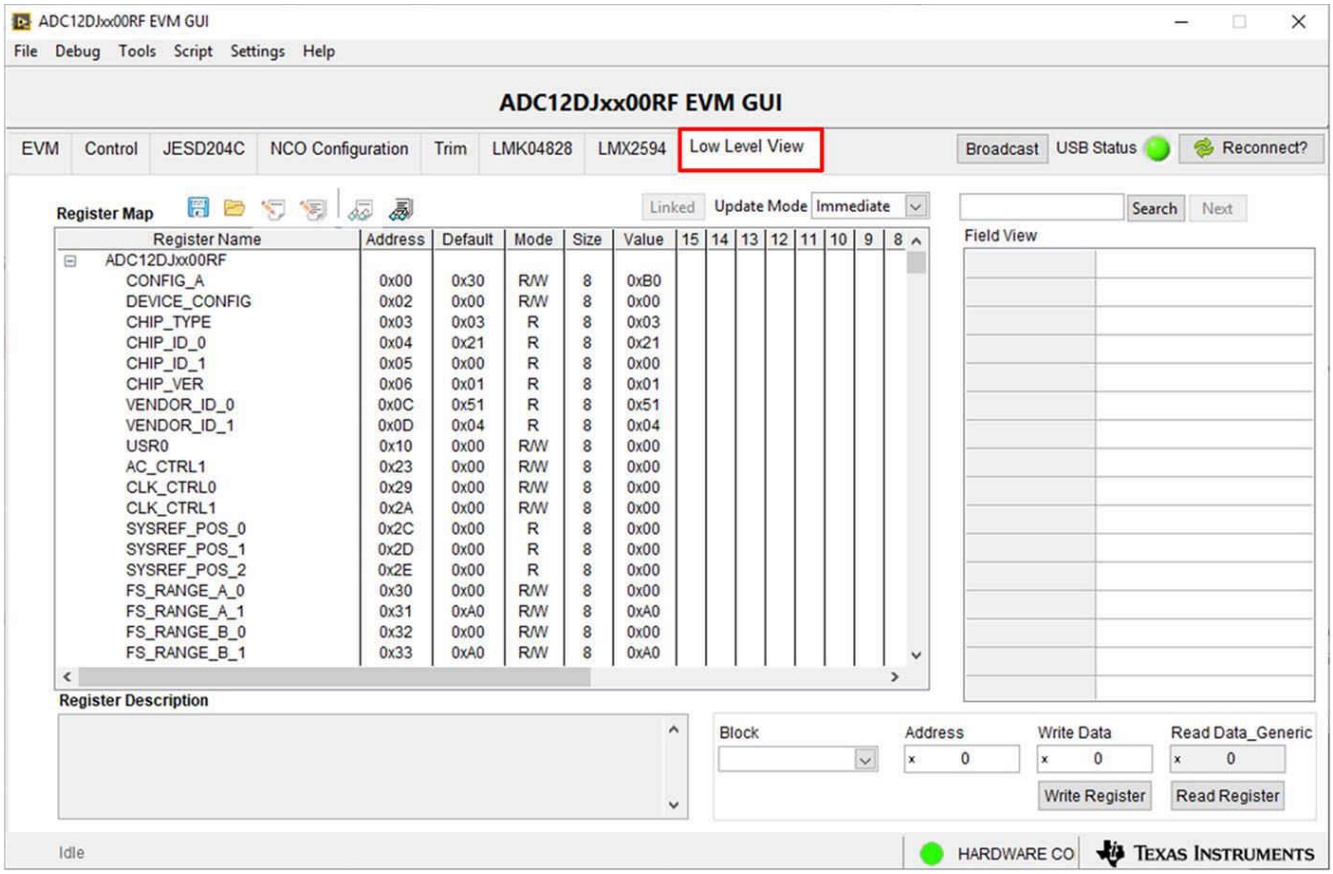

Figure 4-1. Low-Level Register Control Tab

5 Troubleshooting the ADC12DJ5200RFEVM/SEEVM

Table 5-1 lists some troubleshooting procedures.

Table 5-1. Troubleshooting

Issue	Troubleshoot
General problems	• Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J57EVM. Verify that the power switch is in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. • Ensure the board-to-board FMC+ connection is secure. • Try pressing the CPU_RESET button on the TSW14J57EVM. Also try clicking *Instrument Options* → *Reset Board* after changing the ADC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.
TSW14J57 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J57EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the ADC device internal registers are configured properly. • If LEDs are not blinking, reprogram the ADC EVM devices. • Try pressing the CPU_RESET button on the TSW14J57EVM. • Try capturing data in HSDC Pro to force an LED status update
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a *USB serial device* is recognized when the EVM is connected to the PC. • Verify that the green *USB Status* LED light in the top right corner of the GUI is lit. If it is not lit, click the *Reconnect FTDI* button. • Try restarting the configuration GUI.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description *ADC12DJ5200RF* .
HSDC Pro software is not capturing good data or analysis results are incorrect.	• Verify that the TSW14J57EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC software. • Check that the proper ADC device mode is selected. The mode should match in HSDC Pro and the ADC GUI. • Check that the analysis parameters are properly configured.
HSDC Pro software gives a time-out error when capturing data	• Try to reprogram the LMK device and reset the JESD204 link. • Verify that the ADC sampling rate is correctly set in the HSDC software. • Try pressing the *CPU_RESET* button on the TSW14J57EVM. Also try clicking *Instrument Options* → *Reset Board* after changing the ADC configuration. Try to recapture again. • Select *Instrument Options* → *Download Firmware* and download 'TSW14J57RevE_16L_XCVR_ADCDDRDACBRAM.rbf'. Try to capture again.
Sub-optimal measured performance	• Try clicking *Cal Triggered/Running* button 2× to re-calibrate the ADC in the current operating conditions. It is located on the *Control* tab of the configuration GUI. • Check that the spectral analysis parameters are properly configured. • Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

6 References

This section provides references to technical documents and user's guides.

6.1 Technical Reference Documents

- ADC12DJ5200RF device data sheet
- ADC12DJ5200SE device data sheet
- TSW14J57EVM user’s guide
- TSW14J56EVM user’s guide
- High-Speed Data Converter Pro GUI User's Guide, also available in the help menu of the software
- LMK04828 data sheet
- LMX2594 data sheet
- FTDI USB to Serial Driver Installation Manual (www.ftdichip.com/Support/Documents/InstallGuides.htm)

6.2 TSW14J57EVM Operation

Refer to the TSW14J57EVM user guide for configuration and status information.

7 HSDC Pro Settings for Optional ADC Device Configuration

This appendix provides settings for optional ADC device configuration in HSDC Pro.

7.1 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter on the *JESD204C* tab in the *Configuration* GUI. This parameter must be matched by the receiving device, and the SYSREF frequency must also be programmed to a compatible frequency. Ensure that the K value complies with the *K Min* and *Step* values for the selected JMODE. Refer to the ADC12DJ5200RF/SE operating modes table in the data sheet.

7.2 Customizing the EVM for Optional Clocking Support

The ADC12DJ5200RFEVM/SEEVM can be clocked using 3 different methods: external clock option, onboard clock option and external reference clock option.

7.2.1 External Clocking Option (Default)

By default, the EVM is configured to use the external clock option. The user provide and external clock signal for both the ADC sampling clock(DEVCLK at J10) and also the Reference clock(REF CLK at J17) which feed into the LMK04828 and is used in clock distribution mode and provides the FPGA reference clock, FPGA SYSREF signal and ADC SYSREF signal. If coherent sampling is desired the external clocking has to be used. Figure 7-1 shows the block diagram of external clocking option:

The EVM can be configured to use external clocks with the following steps (see Figure 7-4):

1. Modify the hardware:
   a. Remove R171 and R174, populate C2 and C3.
   b. Remove C52 and C306, populate C60 and C61
   c. Install Jumper J13

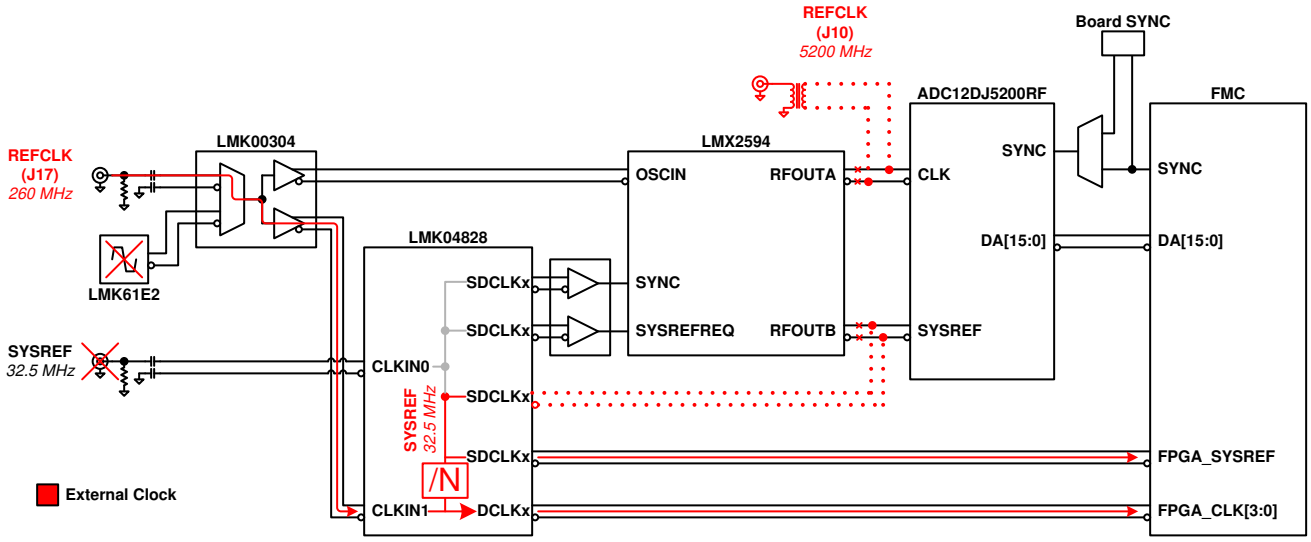

Figure 7-1. ADC12DJ5200RFEVM/SEEVM Clocking System Block Diagram

7.2.2 Onboard Clocking Option

All the required clocking is generated on the EVM and no external clock signal is required. The LMK61E2 generates the reference frequency LMK00304 make two copies of the reference signal and sends the one copy to LMX2594 to generate the sampling clock for the ADC and LMK04828 uses the second copy in clock distribution mode to provides the FPGA reference clock, FPGA SYSREF signal and ADC SYSREF signal. Figure 7-2 shows the block diagram of onboard clocking option:

The EVM can be configured to use onboard clocking option with the following steps (see Figure 7-5):

- Remove C2 and C3, populate R171 and R174
- Remove C60 and C61, populate C52 and C306
- Uninstall Jumper J13

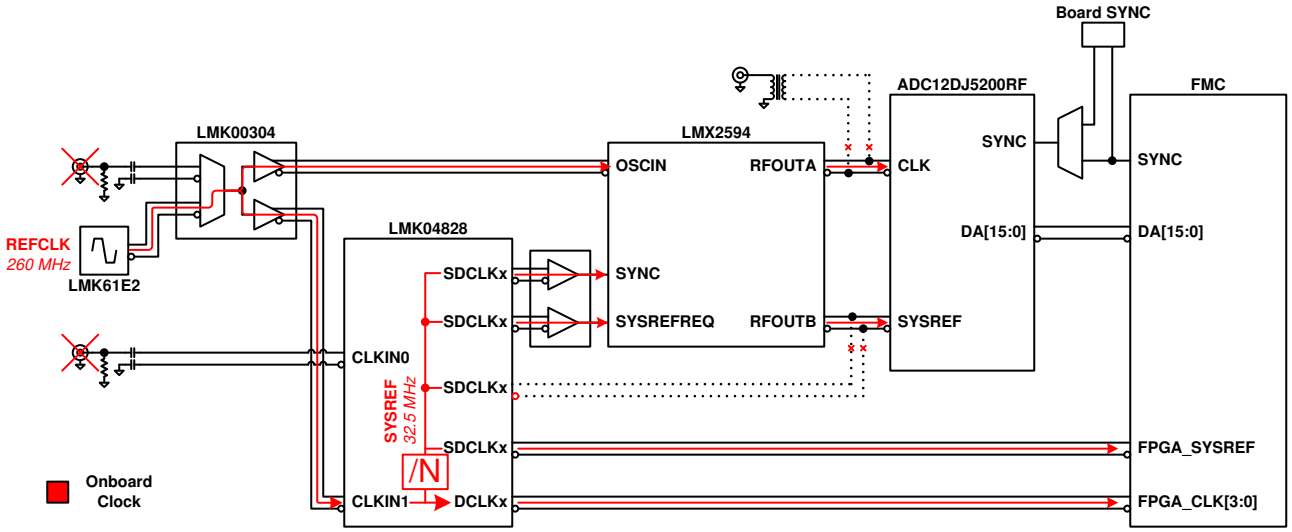

Figure 7-2. Onboard Clocking System Block Diagram

7.2.3 External Reference Clocking Option

The Reference clock(J17) is provided by an external source. The LMK00304 make two copies of the reference signal and sends the one copy to LMX2594 to generate the sampling clock for the ADC and LMK04828 uses the second copy in clock distribution mode to provides the FPGA reference clock, FPGA SYSREF signal. The ADC SYSREF signal is generated by the LMX2594. Figure 7-3 shows the block diagram of external reference clocking option:

The EVM can be configured to use external reference clocking option with the following steps (see Figure 7-5):

- Remove C2 and C3, populate R171 and R174
- Remove C60 and C61, populate C52 and C306
- Install Jumper J13

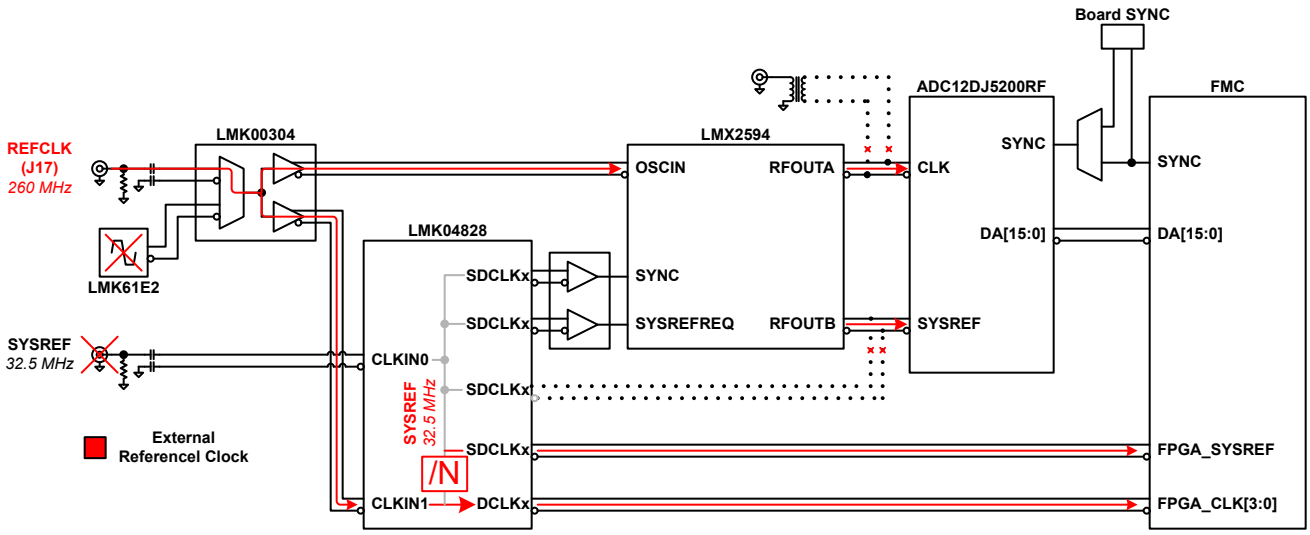

Figure 7-3. External Reference Clocking System Block Diagram

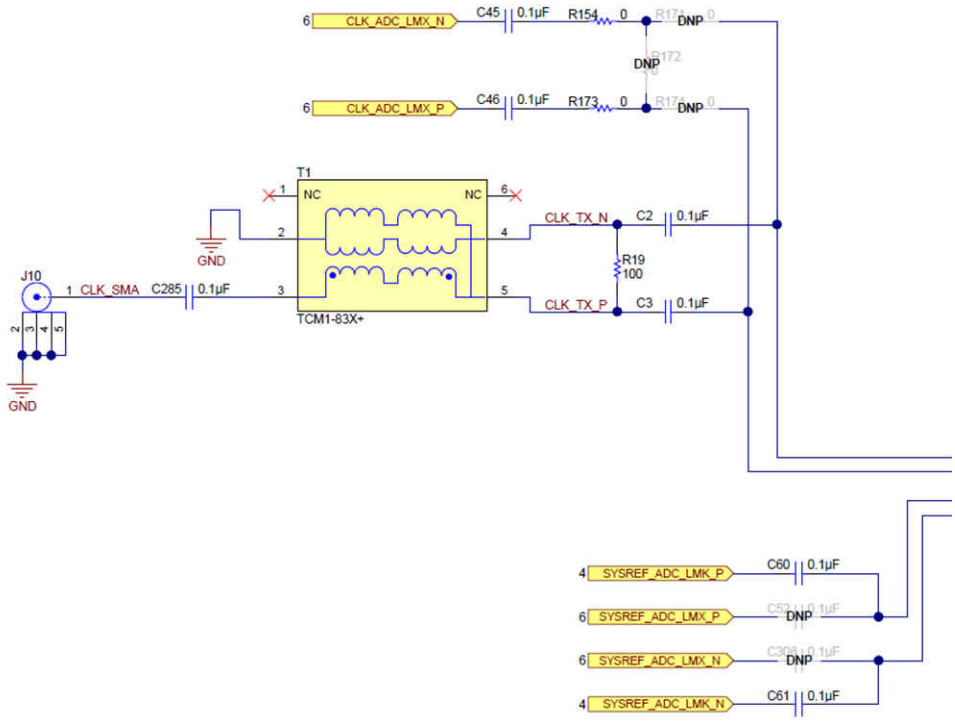

Figure 7-4. External Clock Configuration

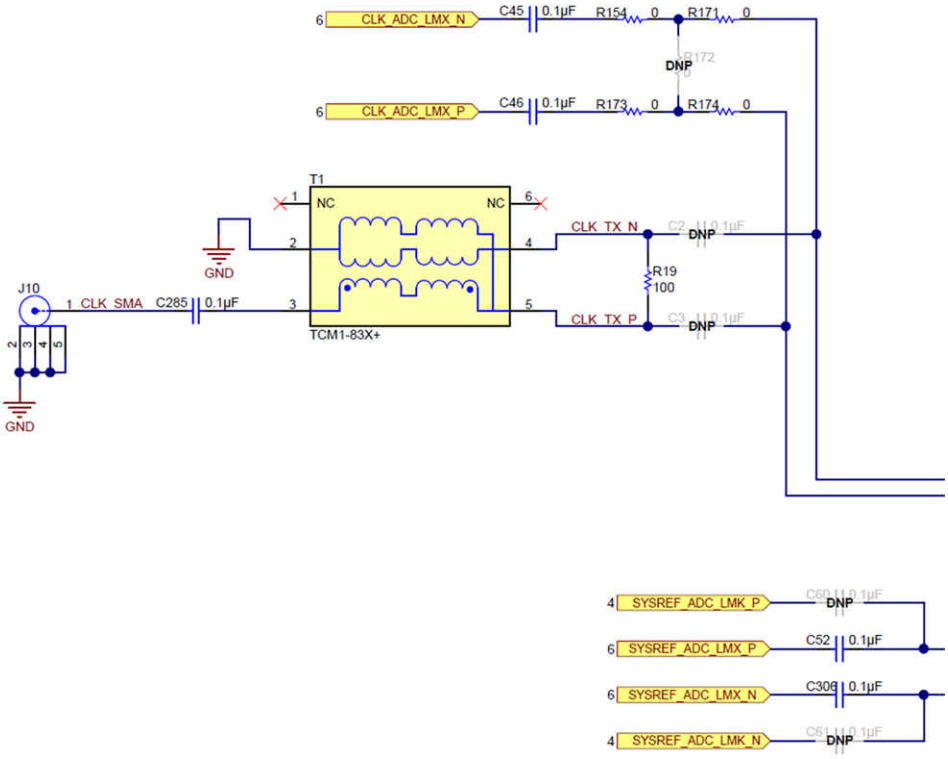

Figure 7-5. Onboard Clocking Configuration

8 Signal Routing

8.1 Signal Routing

Table 8-1 provides the signal routing details for the ADC12DJ5200RFEVM/SEEVM.

Table 8-1. ADCxxDJxx00RFEVM/SEEVM Signal Routing

JESD204C Output	Link	LID	FMC(+) Pins	FMC(+) Signal Names(1)
DA0	A	0	A10,A11	DP3_M2C
DA1	A	1	C6,C7	DP0_M2C
DA2	A	2	A6,A7	DP2_M2C
DA3	A	3	A2,A3	DP1_M2C
DB0	B	0	B12,B13	DP7_M2C_INV
DB1	B	1	A14,A15	DP4_M2C_INV
DB2	B	2	B16,B17	DP6_M2C_INV
DB3	B	3	A18,A19	DP5_M2C_INV
DA4	A	4	Z12,Z13	DP11_M2C
DA5	A	5	Y10,Y11	DP10_M2C
DA6	A	6	B8,B9	DP8_M2C
DA7	A	7	B4,B5	DP9_M2C
DB4	B	4	Y14,Y15	DP12_M2C_INV
DB5	B	5	Z16,Z17	DP13_M2C_INV
DB6	B	6	Y18,Y19	DP14_M2C_INV
DB7	B	7	Y22,Y23	DP15_M2C_INV

(1) Red items with _INV in the signal name are inverted with respect to standard FMC polarity.

A Analog Inputs

Table A-1 provides the different settings for setting the analog inputs path.

Table A-1. Analog Input Path

Coupling	Input	SMA to Use	R2, R6, R10, R14	R1, R8, R9, R16
AC (default) 5200RF	S/E Balun (500kHz to 9GHz)	INA(J4), INB(J7)	0 Ω	DNI
AC (default) 5200SE	Intergrated Balun	INAP(J5) INBP(J6)	DNI	R1, R16 = DNI C74, C75 = 0.1uF
AC	Differential 5200SE = N/A	INAP(J5), INAM(J3), INBP(J6), INBM(J8)	DNI	0.1 µF
DC	Differential 5200SE = N/A	INAP, INAM, INBP, INBM	DNI	0 Ω

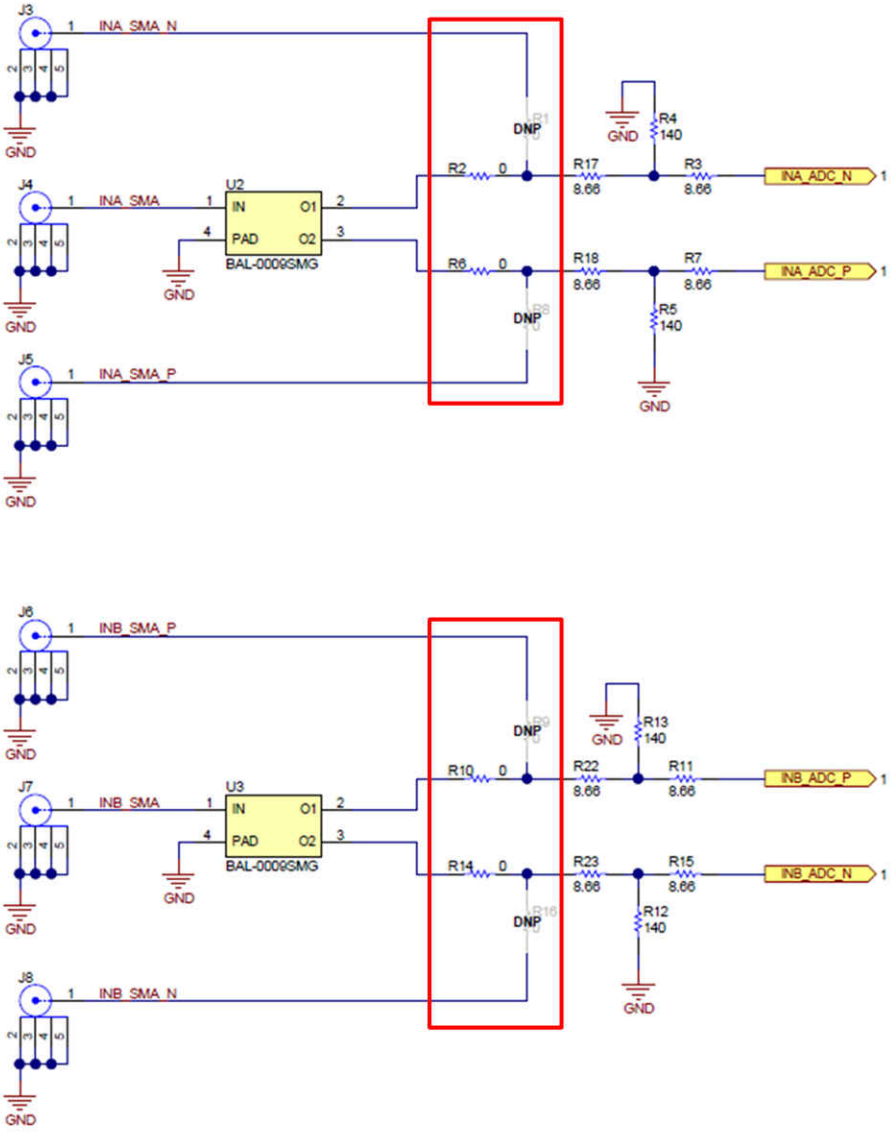

Figure A-1. Analog Input Path

A 3dB attenuation pad is added between the inputs and the ADC. The 3 dB pad helps with the flatness of the frequency response.

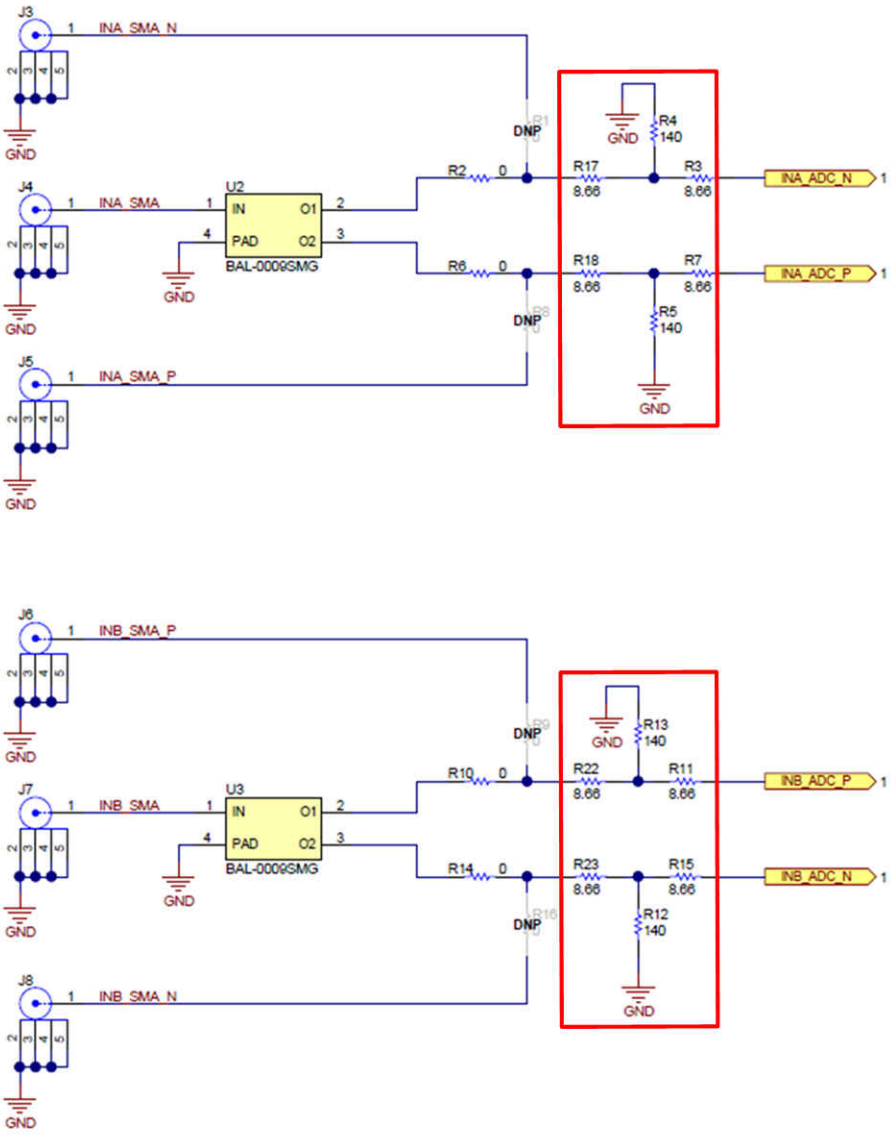

Figure A-2. 3 dB attenuation pad

B Jumpers and LEDs

10.1 Jumper settings

Table 10-1 shows the jumper settings and Table 10-2 shows the LED functionality.

Table 10-1. Jumper Settings

Label	Description	Function
J12	ADC power down jumper.	Installed: ADC powered down. Uninstalled: ADC powered up(default)
J13	Select the source for Reference clock signal	Installed: External Reference clock signal is selected(default). Uninstalled: Onboard reference signal (LMK61E2) is selected.
J18	When hardware calibration trigger option is enabled. The ADC's calibration routine is can be enable using external signal	Installed: ADC's calibration routine is triggered. Uninstalled: ADC's calibration routine is not triggered(default).
J19	Selects the source for SPI signals	Installed: SPI signals from FMC+ connector are controlling the devices on the EVM. Uninstalled: SPI signal from the onboard FTDI IC is controlling the devices on the EVMs

Table 10-2. LEDs

Label	Function
D1	High temp indicator
D2	High input power on channel A
D3	High input power on channel B

B Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2021) to Revision B (March 2023) **Page**

- Added ADC12DJ5200SEEVM to the User's Guide..... 1

Changes from Revision * (April 2019) to Revision A (June 2021) **Page**

- Changed the abstract to include additional devices..... 1
- Added a Note to Open the ADC12DJ5200RFEVM/SEEVM GUI and Program the ADC and Clocks 9

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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