



TPS7B4250-Q1 50mA、40V電圧トラッキングLDO、トラッキング許容誤差5mV

1 特長

- 車載アプリケーション用に認定済み
- AEC-Q100認定済み
 - デバイス温度グレード1: 動作時周囲温度範囲 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - デバイスHBM ESD分類レベル3A
 - デバイスCDM ESD分類レベルC6
- $-20\text{V} \sim 45\text{V}$ の広い入力電圧範囲
- 出力電流: 50mA
- 非常に低い出力トラッキング許容誤差: 5mV (最大値)
- 低いドロップアウト電圧: $I_{\text{OUT}} = 10\text{mA}$ のとき150mV
- 基準入力とイネーブル入力の結合
- 軽負荷時に40 μA の低い静止電流
- 非常に広いESR範囲
 - 1 $\mu\text{F} \sim 50\mu\text{F}$ のセラミック出力コンデンサ、ESR 1m $\Omega \sim 20\Omega$ で安定動作
- 逆極性保護
- 過熱保護
- 出力からグランドおよび電源への短絡保護
- SOT-23パッケージ

2 アプリケーション

- オフボード・センサの電源
- 高精度の電圧トラッキング

3 概要

TPS7B4250-Q1デバイスは、モノリシックな統合低ドロップアウト電圧トラッカです。このデバイスは、SOT-23パッケージで供給されます。TPS7B4250-Q1デバイスは、車載環境でオフボード・センサへ電源を供給するよう設計されています。このICには過負荷、過熱、逆極性、および出力からバッテリーおよびグランドへの短絡に対する保護機能が搭載されています。

調整入力ピンADJに印加される基準電圧によって、電源電圧が最大 $V_{\text{IN}} = 45\text{V}$ まで、50mAまでの負荷について高い精度でレギュレートされます。

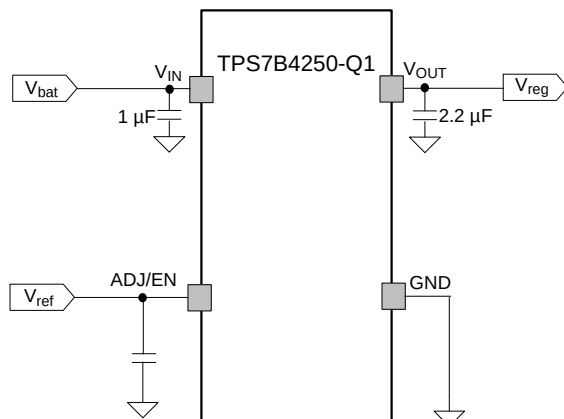
調整/イネーブル入力ピンのADJ/ENをLOWに設定すると、TPS7B4250-Q1デバイスはスタンバイ・モードに切り替わり、静止電流は最小値に減少します。

製品情報⁽¹⁾

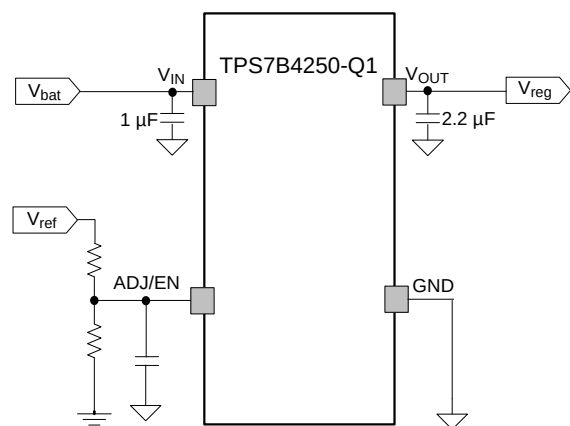
型番	パッケージ	本体サイズ(公称)
TPS7B4250-Q1	SOT-23 (5)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

基準電圧と等しい出力



基準電圧よりも低い出力



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

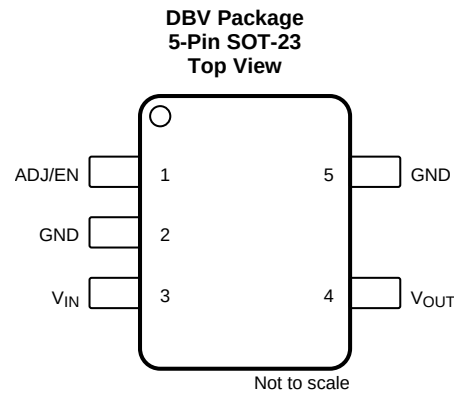
Revision B (July 2015) から Revision C に変更	Page
• データ・シートのタイトル 変更	1
• 追加「デバイスのサポート」および「ドキュメントの更新通知を受け取る方法」セクション	16

Revision A (November 2013) から Revision B に変更	Page
• HBM ESD分類レベルを2から3Aへ 変更	1
• CDM ESD分類レベルをC4からC6へ 変更	1
• 「ピン構成および機能」セクション、「ESD定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• Deleted the transient current and 107-pF capacitor for HBM table notes from the <i>ESD Ratings</i> table	5
• Changed input voltage symbol from V_{IN} to V_I for the $\Delta V_{O(\Delta V)}$ and $V_{dropout}$ parameters and the output voltage symbol from V_{OUT} to V_O for the I_L parameter in the Electrical Characteristics table	6
• Added I_O and C_O to the PSRR test condition in the <i>Electrical Characteristics</i> table	6
• Changed the max value for $V_{dropout}$ where $I_O = 10$ mA from 250 to 265 in the <i>Electrical Characteristics</i> table	6
• Deleted the $V_{ADJ} = 5$ V condition for the <i>Ground current vs Temperature</i> graph and changed the legend	7
• Changed the y axis units from mV to mA in the <i>Current-limit vs Temperature</i> graph	7
• Added the V_{ADJ} condition statement to the <i>Input Voltage vs Output Voltage</i> graph and changed the y-axis from I_O to V_O ..	7
• Changed the title of Figure 8 from <i>Input Voltage vs Output Voltage</i> to <i>Reference Voltage vs Output Voltage</i> , and changed the y-axis from I_O to V_O . Also added the V_I condition statement to the graph	7
• Changed the second y axis from I_O to V_I and removed the units in the <i>Line Transient</i>	7
• Deleted the units from the second y axis in the <i>Load Transient</i>	7
• Added the V_{ADJ} condition statement to the <i>Power-supply Rejection Ratio vs Frequency</i> graph	8
• Added resistor-divider values to the <i>Tracking LDO With Enable Circuit</i> figure	11

2013年10月発行のものから更新
Page

• ドキュメント全体でCDM ESD分類レベルをC3BからC4へ 変更	1
• Changed V_{OUT} min value from -0.3 to -1 in the <i>Absolute Maximum Ratings</i> table	5
• Added transient current flow to ESD rating in the <i>Absolute Maximum Ratings</i> table	5
• Changed HBM absolute maximum rating from 2 kV to 4 kV.....	5
• Deleted relevant ESR value from <i>Recommended Operating Conditions</i> table	5
• Added grater-than-or-equal-to ($\geq$) value to $V_{ADJ/EN}$ in condition statement of the <i>Electrical Characteristics</i> table	6
• Added $V_{ADJ} = 1.5$ V to both test conditions for V_{UVLO} parameter in the <i>Electrical Characteristics</i> table	6
• Changed max value for load regulation parameter from 3 to 4 in the <i>Electrical Characteristics</i> table	6
• Changed max value for the current consumption test condition where $I_O = 0.5$ mA from 80 to 90 in the <i>Electrical Characteristics</i> table	6
• Added the <i>Detailed Description</i> section.....	9
• Added the TPS7B4250 block diagram	9

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADJ/EN	1	I	This pin connects to the reference voltage. A low signal disables the IC and a high signal enables the device. Connected the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.
GND	2	G	Internally connected to pin 5
GND	5	G	Internally connected to pin 2
V _{IN}	3	I	This pin is the device supply. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.
V _{OUT}	4	O	V _{OUT} is an external capacitor that is required between V _{OUT} and GND with respect to the capacitance and ESR requirements given in the Recommended Operating Conditions .

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage, unregulated input, $V_{IN}^{(2)(3)}$	–20	45	V
Output voltage, regulated output, V_{OUT}	–1	22	V
Adjust input and enable input voltage, $ADJ/EN^{(2)(3)}$	–0.3	22	V
ADJ Voltage minus input voltage ($ADJ-V_{IN}$), $V_{IN} > 0$ V		7	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground, GND.
- (3) Absolute maximum voltage.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000
	Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V_{IN} Unregulated input	4	40	V
V_{OUT} regulated output	1.5	18	V
ADJ/EN Adjust input and enable input voltage	1.5	18	V
$ADJ-V_{IN}$ ADJ voltage minus input voltage		5	V
C_{OUT} Output capacitor requirements ⁽²⁾	1	50	μF
ESR_{COUT} Output ESR requirements	0.001	20	Ω
T_J Operating junction temperature	–40	150	°C

- (1) Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.
- (2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS7B4250-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).
- (2) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

TPS7B4250-Q1

JAJSC96C –OCTOBER 2013–REVISED SEPTEMBER 2016

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6.5 Electrical Characteristics
 $V_I = 13.5\text{ V}$, $18\text{ V} \geq V_{\text{ADJ/EN}} \geq 1.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	V_{IN} undervoltage detection	Ramp up V_I until the output turns on, $V_{\text{ADJ}} = 1.5\text{ V}$	3.65			V
		Ramp down V_I until the output turns off, $V_{\text{ADJ}} = 1.5\text{ V}$			3	
ΔV_O	Output-voltage tracking accuracy	$I_O = 100\text{ }\mu\text{A}$ to 1 mA , $V_I = 4\text{ V}$ to 40 V , $1.5\text{ V} < V_{\text{ADJ}} < V_I - 0.3\text{ V}$	–4		4	mV
		$I_O = 1\text{ mA}$ to 50 mA , $V_I = 4\text{ V}$ to 40 V , $1.5\text{ V} < V_{\text{ADJ}} < V_I - 1.5\text{ V}$	–5		5	
$\Delta V_{O(\Delta I_L)}$	Load regulation steady-state	$I_O = 1\text{ mA}$ to 30 mA			4	mV
$\Delta V_{O(\Delta V_I)}$	Line regulation steady-state	$I_O = 10\text{ mA}$, $V_I = 6\text{ V}$ to 40 V			3	mV
PSRR	Power-supply ripple rejection	Frequency = 100 Hz , $V_{\text{rip}} = 0.5\text{ V}_{\text{PP}}$, $I_O = 5\text{ mA}$, $C_O = 2.2\text{ }\mu\text{F}$		60		dB
V_{dropout}	Dropout voltage, $V_{\text{dropout}} = V_I - V_Q$	$I_O = 10\text{ mA}$, $V_I \geq 4\text{ V}^{(1)}$		150	265	mV
		$I_O = 50\text{ mA}$, $V_I \geq 4\text{ V}^{(1)}$		550	1000	
I_L	Output-current limitation	V_O short to GND	100		500	mA
I_R	Reverse current at V_{IN}	$V_I = 0\text{ V}$, $V_O = 20\text{ V}$, $V_{\text{ADJ}} = 5\text{ V}$	–5		0	μA
I_{RN1}	Reverse current at negative input voltage	$V_I = -20\text{ V}$, $V_O = 0\text{ V}$, $V_{\text{ADJ}} = 5\text{ V}$	–5		0	μA
I_{RN2}		$V_I = -20\text{ V}$, $V_O = 20\text{ V}$, $V_{\text{ADJ}} = 5\text{ V}$	–5		0	
T_{SD}	Thermal shutdown temperature	T_J increasing because of power dissipation generated by the IC		175		$^\circ\text{C}$
I_Q	Current consumption	$V_{\text{ADJ}} < 0.8\text{ V}$, $T_A \leq 85^\circ\text{C}^{(2)}$		7.5	15	μA
		$V_{\text{ADJ}} < 0.8\text{ V}$, $T_A \leq 125^\circ\text{C}$			20	
		$I_O = 0.5\text{ mA}$, $V_{\text{ADJ}} = 5\text{ V}$		40	90	
		$I_O = 30\text{ mA}$, $V_{\text{ADJ}} = 5\text{ V}$		150	350	
I_{ADJ}	Adjust-input and enable-input current	$V_{\text{ADJ}} = 5\text{ V}$			1	μA
$V_{\text{ADJ,low}}$	Adjust and enable low signal valid	$V_O = 0\text{ V}$			0.8	V
$V_{\text{ADJ,high}}$	Adjust and enable high signal valid	$ V_O - V_{\text{ADJ}} < 5\text{ mV}$	1.5		18	V

 (1) Measured when the output voltage V_Q has dropped 10 mV from the typical value.

(2) Ensured by design.

6.6 Typical Characteristics

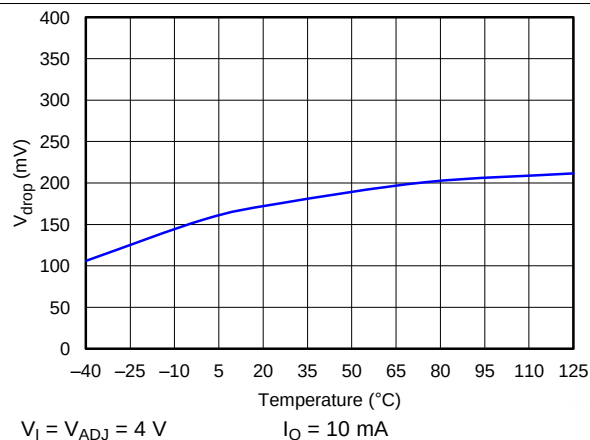


Figure 1. Dropout Voltage vs Temperature

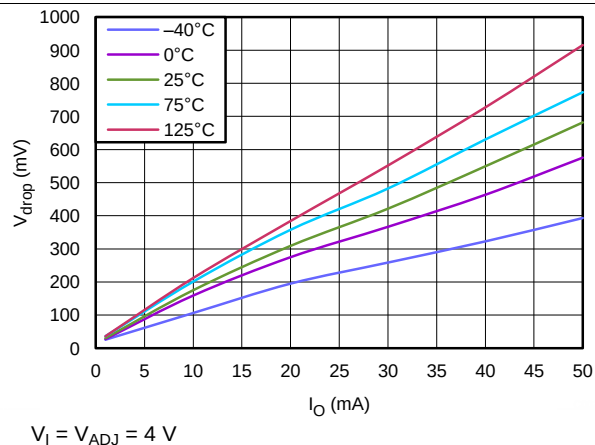


Figure 2. Dropout Voltage vs Output Current

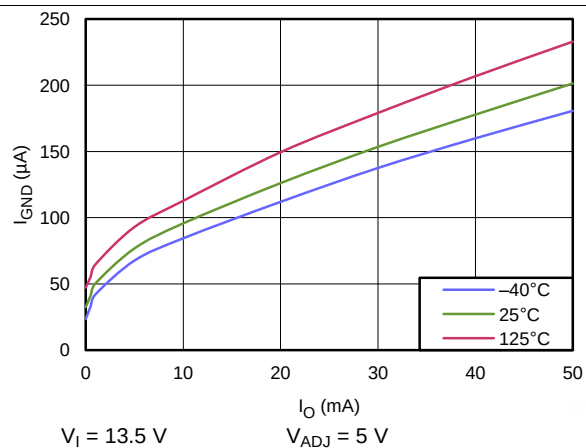


Figure 3. Ground Current vs Output Current

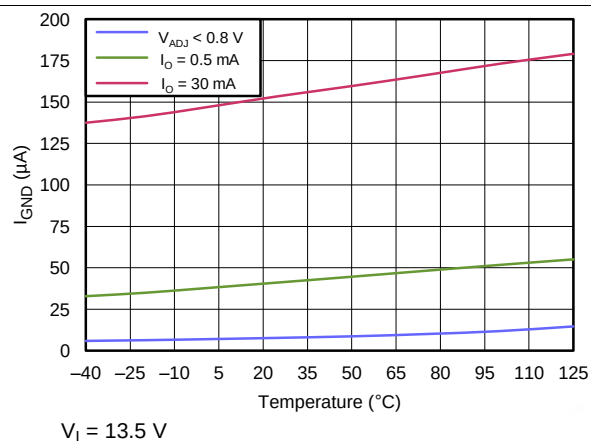


Figure 4. Ground Current vs Temperature

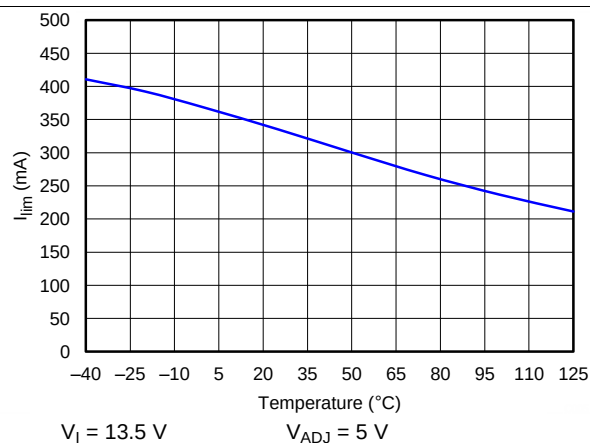


Figure 5. Current-limit vs Temperature

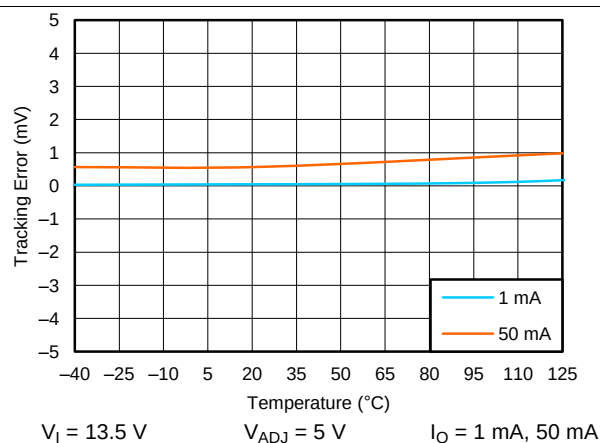


Figure 6. Tracking Error vs Temperature

Typical Characteristics (continued)

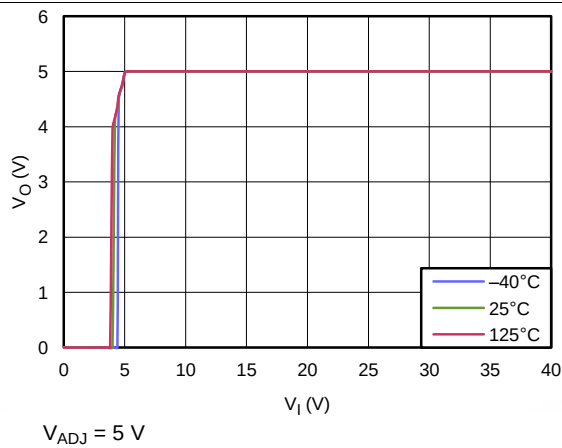


Figure 7. Input Voltage vs Output Voltage

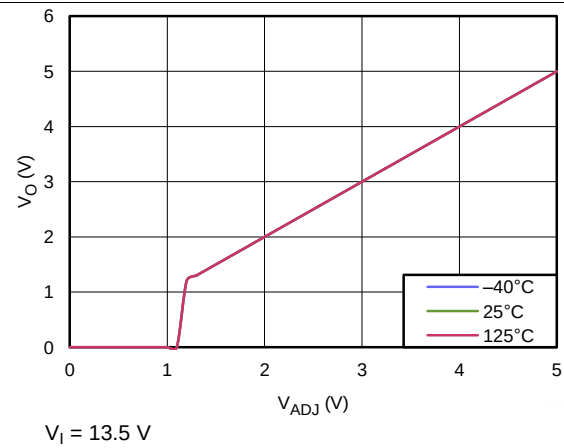


Figure 8. Reference Voltage vs Output Voltage

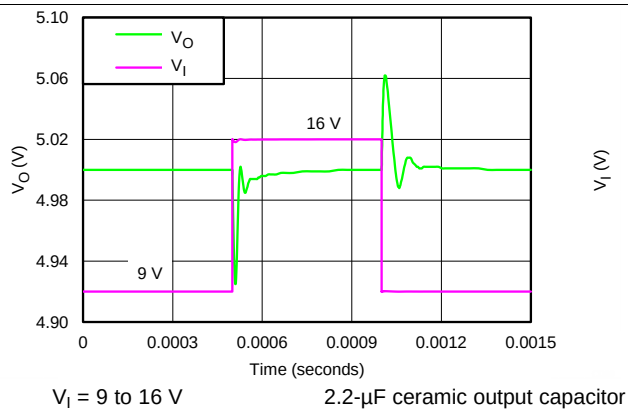


Figure 9. Line Transient

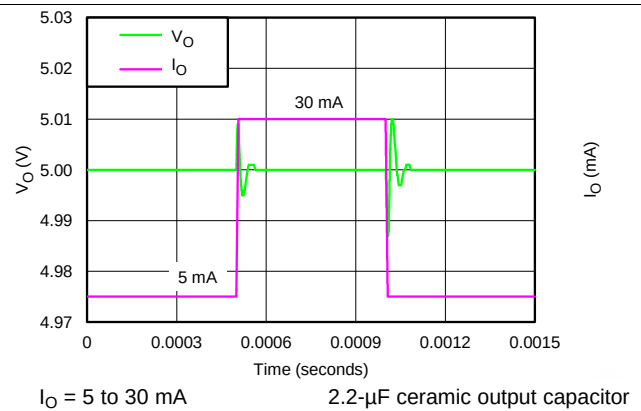


Figure 10. Load Transient

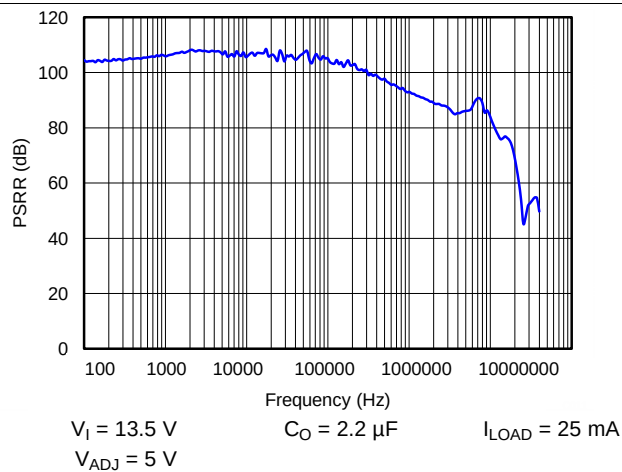


Figure 11. Power-Supply Rejection Ratio vs Frequency

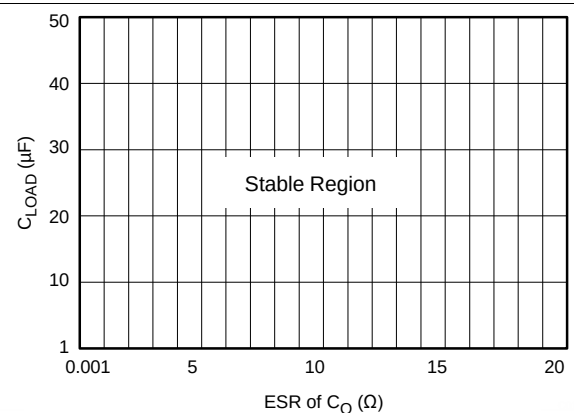


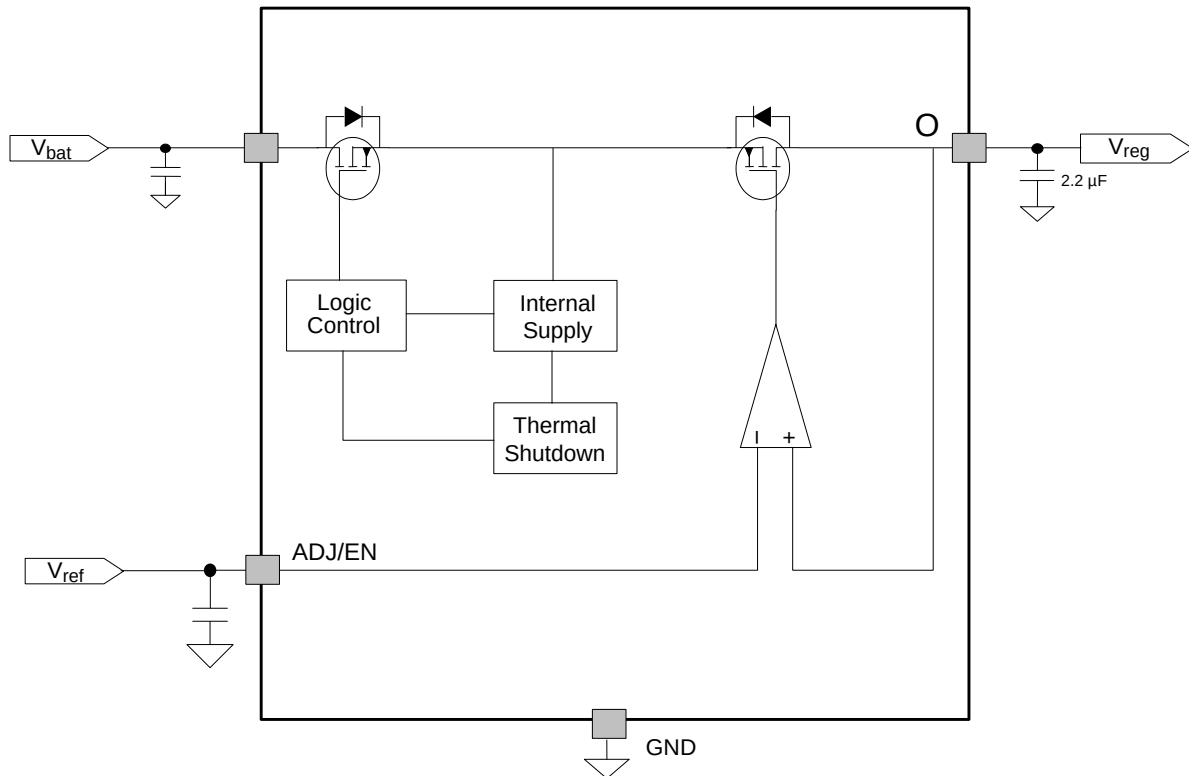
Figure 12. ESR Stability vs Load Capacitance

7 Detailed Description

7.1 Overview

The TPS7B4250-Q1 device is a monolithic integrated low-dropout voltage tracker with ultra-low tracking tolerance. Several types of protection circuits are also integrated in the device such as output current limitation, reverse polarity protection, and thermal shutdown in case of over temperature.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Regulated Output (V_{OUT})

V_{OUT} is the regulated output based on the reference voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft start to control the initial current through the pass element.

7.3.2 Undervoltage Shutdown

The device has an internally-fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on V_{IN} drops below UVLO. This activation ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up similar to a standard power-up sequence when the input voltage is above the required levels.

Feature Description (continued)

7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B4250-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B4250-Q1 device into thermal shutdown degrades device reliability.

7.3.4 V_{OUT} Short to Battery

The TPS7B4250-Q1 device survives a short to battery when the output is shorted to the battery as shown in Figure 13. No damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply at a lower voltage as shown in Figure 14. In this case the TPS7B4250-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on V_{OUT} which typically runs at 5 V. The continuous reverse current flows out through V_{IN} is less than 5 μ A.

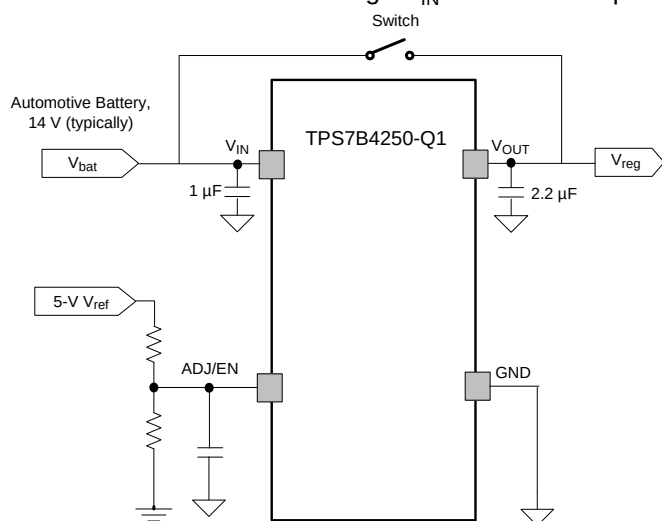


Figure 13. Output-Voltage Short to Battery

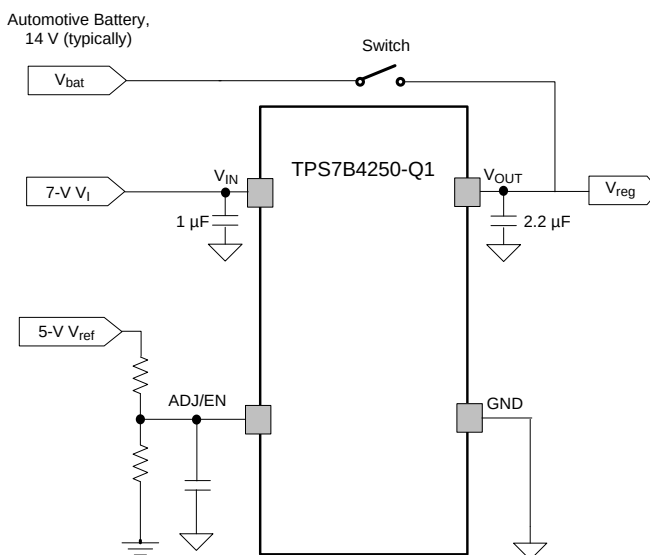


Figure 14. Output Voltage Higher than Input

7.3.5 Tracking Regulator with ENABLE Circuit

By pulling the reference voltage of the device below 0.8 V, the IC disables and enters a sleep state where the device draws 7.5 μ A (typical) from the power supply. In a real application, the reference voltage is generally sourced from another LDO voltage rail. A case where the device must be disabled without a shutdown of the reference voltage can occur. In such case, the device can be configured as shown in Figure 15. The TPS7A6650-Q1 device is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4250-Q1 device and also as a power supply to the ADC. In a configuration as shown in Figure 15, the status of the device is controlled by an MCU I/O.

Feature Description (continued)

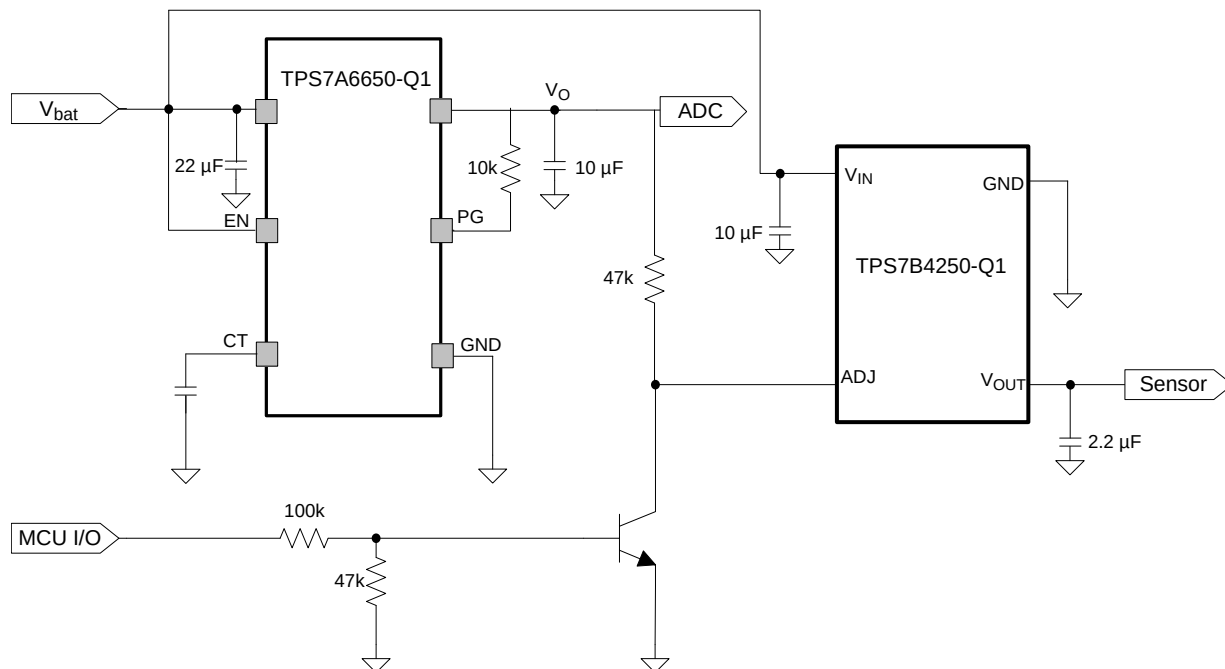


Figure 15. Tracking LDO With Enable Circuit

7.4 Device Functional Modes

7.4.1 Operation With $V_I < 4\text{ V}$

The device operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and operates at input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With ADJ/EN Control

The rising-edge threshold voltage of the ADJ/EN pin is 1.5 V (maximum). When the EN pin is held above that voltage and the input voltage is above the 4 V, the device becomes active. The enable falling edge is 0.8 V (minimum). When the EN pin is held below that voltage the device is disabled, the IC quiescent current is reduced in this state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. TI recommends a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

8.2 Typical Application

Figure 16 show typical application circuit for the TPS7B4250-Q1 device.

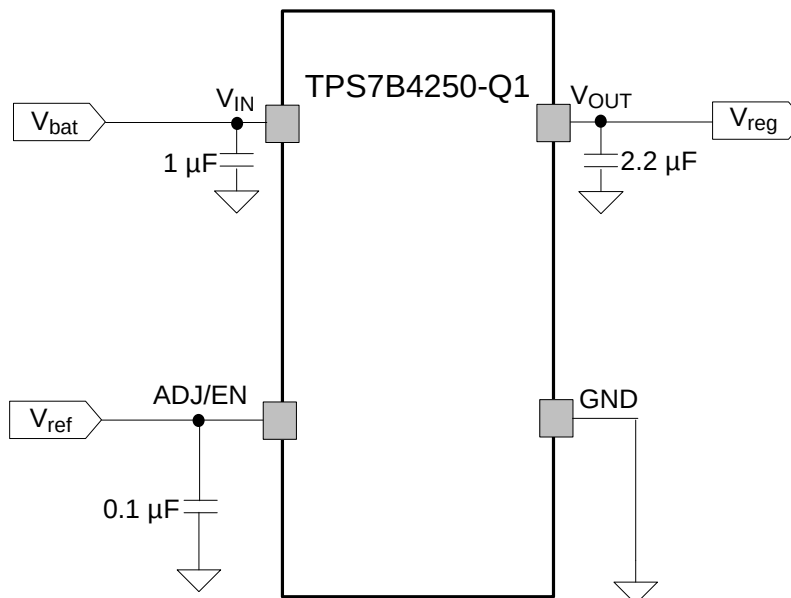


Figure 16. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	4 to 40 V
ADJ reference voltage	1.5 to 18 V
Output voltage	1.5 to 18 V
Output current rating	50 mA
Output capacitor range	1 µF to 50 µF
Output capacitor ESR range	1 mΩ to 20 Ω

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Reference voltage
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

8.2.2.1 External Capacitors

An input capacitor, C_I , is recommended to buffer line influences. Connect the capacitors close to the IC pins.

The output capacitor for the TPS7B4250-Q1 device is required for stability. Without the output capacitor, the regulator oscillates. The actual size and type of the output capacitor can vary based on the application load and temperature range. The effective series resistance (ESR) of the capacitor is also a factor in the IC stability. The worst case is determined at the minimum ambient temperature and maximum load expected. To ensure stability of TPS7B4250-Q1 device, the device requires an output capacitor between 1 μF and 50 μF with an ESR range between 0.001 Ω and 20 Ω that can cover most types of capacitor ESR variation under the recommend operating conditions. As a result, the output capacitor selection is flexible.

The capacitor must also be rated at all ambient temperature expected in the system. To maintain regulator stability down to -40°C , use a capacitor rated at that temperature.

8.2.3 Application Curves

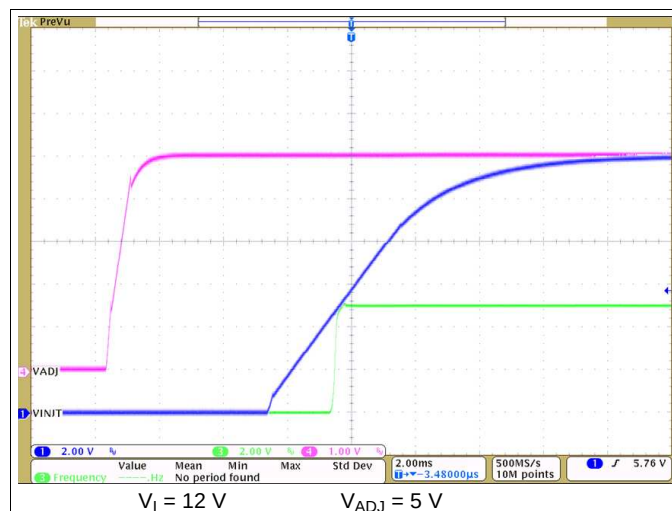


Figure 17. Power Up

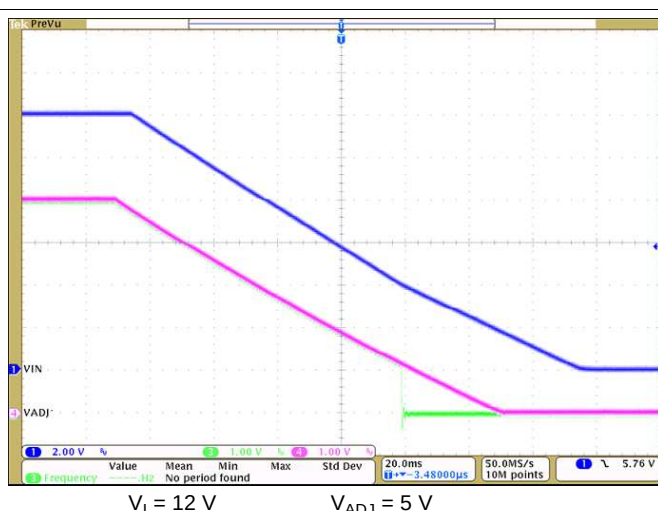


Figure 18. Power Down

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B4250-Q1 device, adding an electrolytic capacitor with a value of 10- μF and a ceramic bypass capacitor at the input is recommended.

10 Layout

10.1 Layout Guidelines

10.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4250-Q1 device are available in the [メカニカル、パッケージ、および注文情報](#) section and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7B4250 evaluation board, available at www.ti.com.

10.2 Layout Example

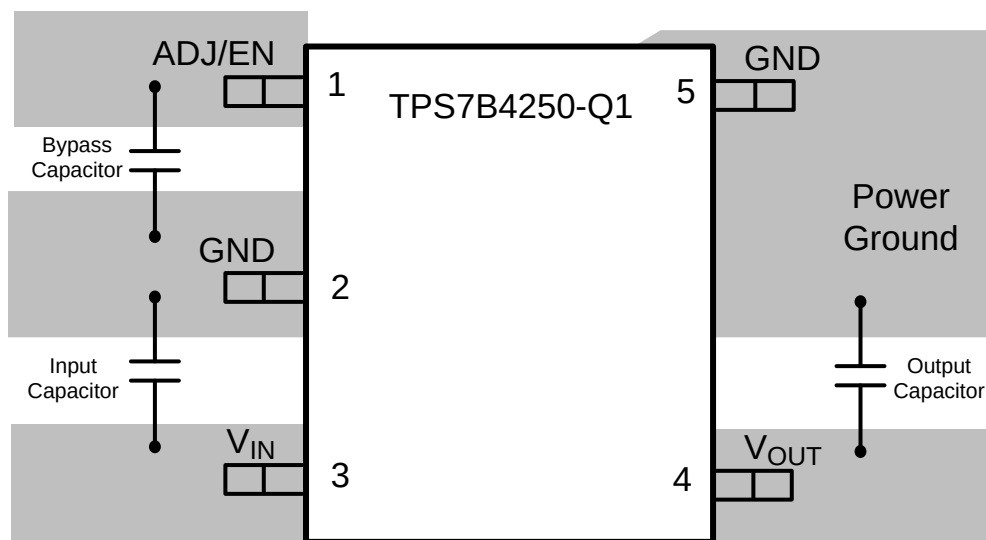


Figure 19. TPS7B4250-Q1 Layout Example

10.3 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with [Equation 1](#).

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage
- I_Q = quiescent current

(1)

As $I_Q \ll I_O$, the term $I_Q \times V_I$ in [Equation 1](#) can be ignored.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) with [Equation 2](#).

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- θ_{JA} = junction-to-junction-ambient air thermal impedance

(2)

A rise in junction temperature because of power dissipation can be calculated with [Equation 3](#).

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D)$$

(3)

For a given maximum junction temperature (T_{JM}), the maximum ambient air temperature (T_{AM}) at which the device can operate can be calculated with [Equation 4](#).

$$T_{AM} = T_{JM} - (\theta_{JA} \times P_D)$$

(4)

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

PSpiceモデルについては、[TPS7B4250 PSpiceトランジェント・モデル\(SLV976\)](#)を参照してください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください:

- 『[電圧トラッキングLDO用の各種アプリケーション](#)』(SLVA789)
- 『[TPS7B4250評価モジュール](#)』SLVU975
- 『[TPS7B4250-Q1 ピンFMEA](#)』(SLVA738)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B4250QDBVQ1	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7B4250QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PA3Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

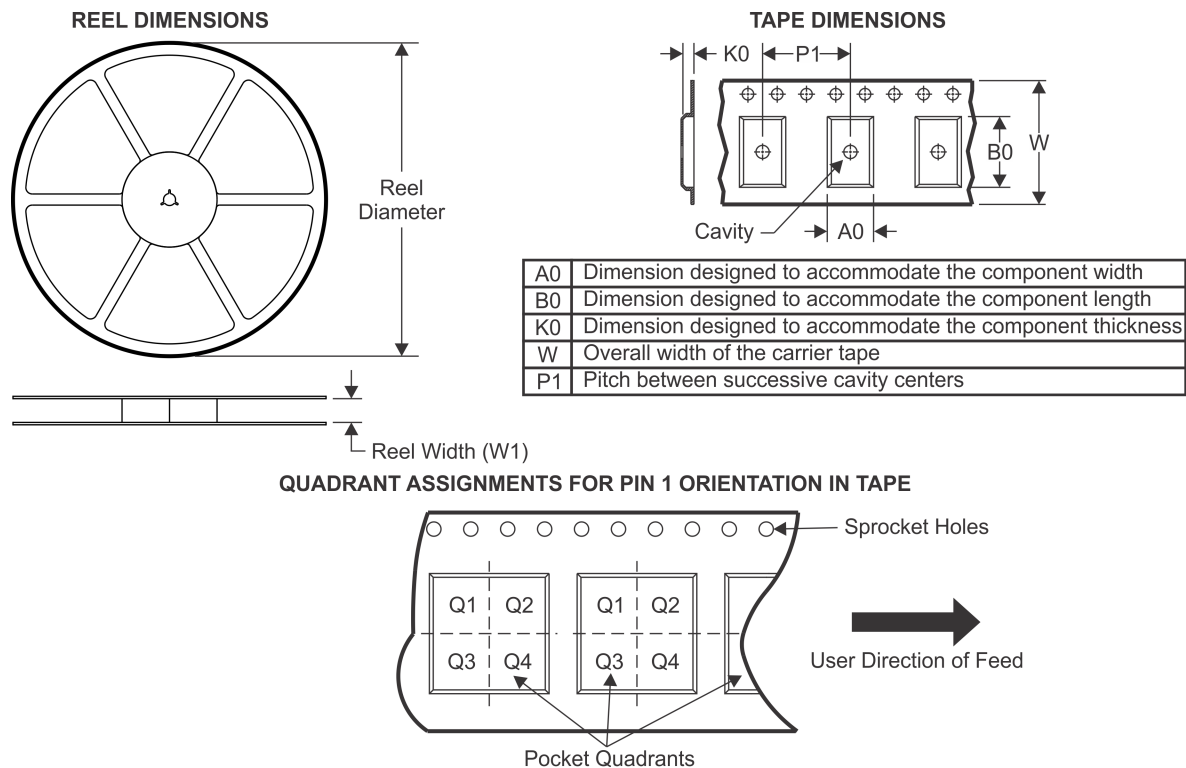
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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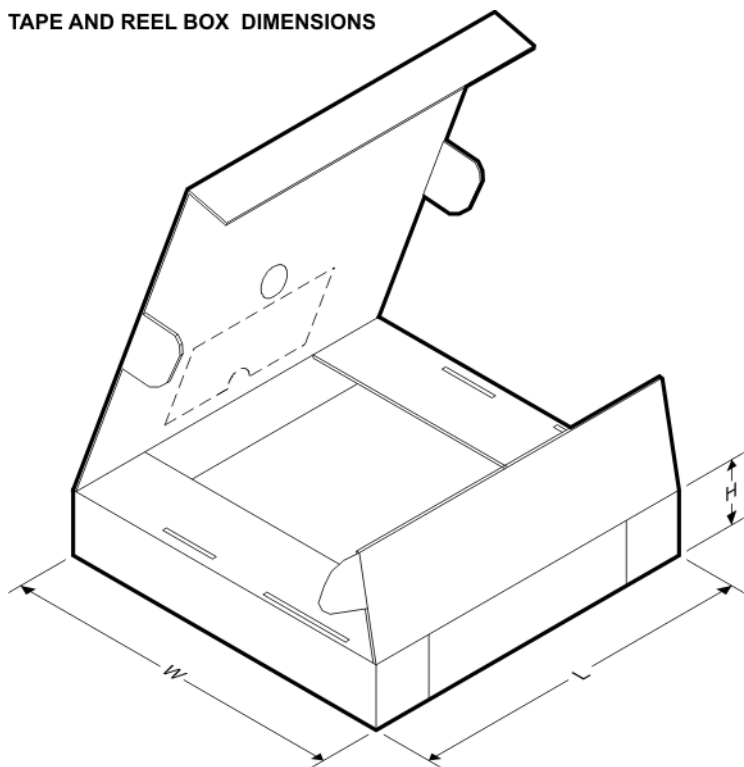
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4250QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4250QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



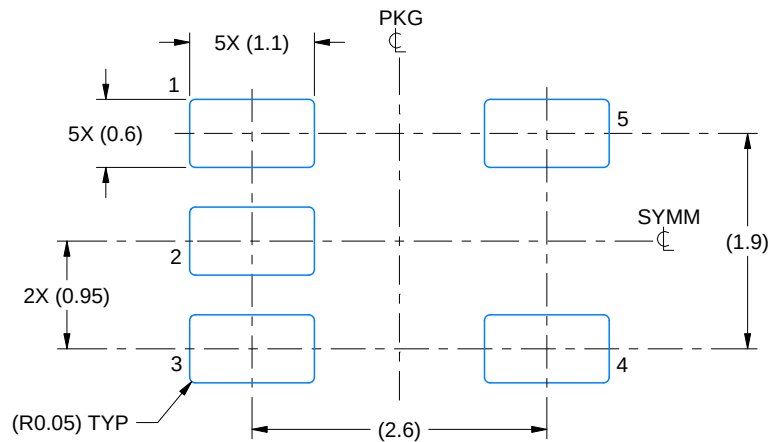
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

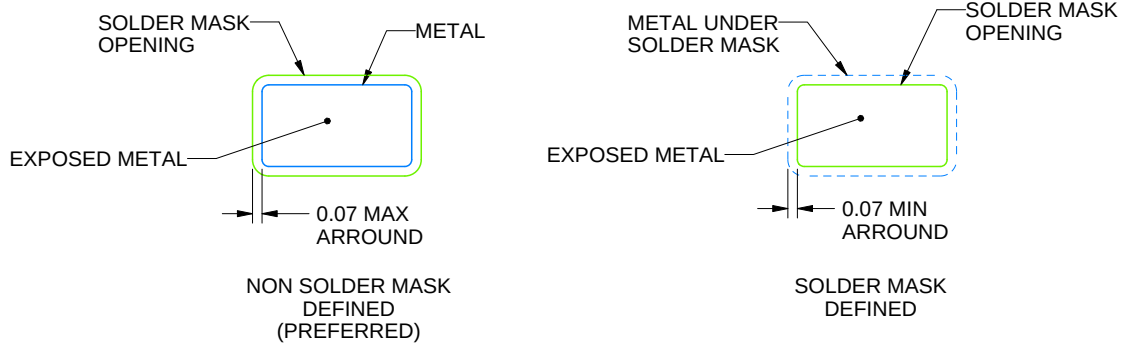
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

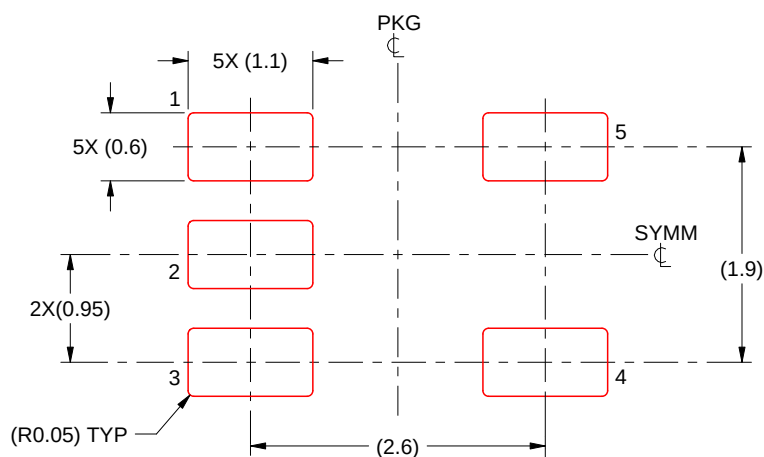
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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