

TPS73801-SEP 宇宙用強化プラスチックに搭載された 1A、低ノイズ、高速過渡応答、低ドロップアウト・レギュレータ

1 特長

- VID V62/18616
- 放射線耐性を強化
 - SEL、SE、SEGR 耐性:
LET = 43MeV-cm²/mg (最大値)
 - LET = 43MeV-cm²/mg まで、SET および SEFI 特性を評価済み
 - すべてのウェハー・ロットについて最大 20krad(Si) の吸収線量 (TID) を保証
 - 50krad(Si) まで、吸収線量 (TID) 特性を評価済み
- 宇宙向けに強化されたプラスチック
 - Au ボンド・ワイヤと NiPdAu リード仕上げ
 - モールド・コンパウンドの改良による低いガス放出
 - 単一の製造、アセンブリ、テスト施設
 - 長い製品ライフ・サイクル
 - 長期にわたる製品変更通知
 - 製品のトレーサビリティ
- 高速過渡応答に最適化
- 出力電流: 1A
- ドロップアウト電圧: 300mV
- 低ノイズ: 45μV_{RMS} (10Hz~100kHz)
- 静止電流: 1mA
- 保護ダイオード不要
- ドロップアウト時の静止電流制御
- 可変出力電圧: 1.21V~20V
- シャットダウン時の静止電流: 1μA 未満
- 10μF の出力コンデンサで安定動作
- セラミック・コンデンサで安定動作
- バッテリ逆接続保護
- 逆電流なし
- 熱制限

2 アプリケーション

- 低軌道 (LEO) 衛星用途のサポート
- RF、VCO、受信機、アンプ用の、放射線強化された低ノイズのリニア・レギュレータ電源
- クリーンなアナログ電源要件
- 人工衛星のペイロード
- コマンドとデータの処理 (C&DH)
- 光学画像処理のペイロード
- レーダー画像処理ペイロード
- 衛星用電源システム (EPS)

3 概要

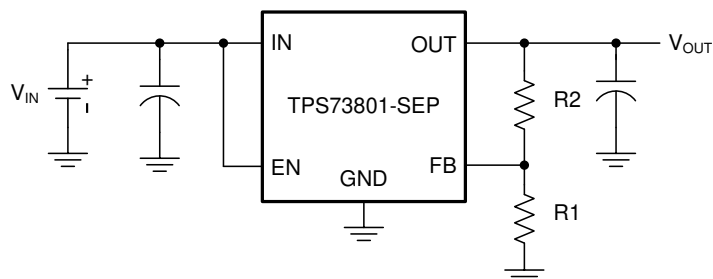
TPS73801-SEP は、高速過渡応答に最適化された低ドロップアウト (LDO) レギュレータです。このデバイスは、300mV のドロップアウト電圧で、1A の出力電流を供給できます。動作時の静止電流は 1mA で、シャットダウン時には 1μA 未満まで低減されます。静止電流は、その他の多くのレギュレータと比較して適切に制御されており、ドロップアウト時に増加することはありません。過渡応答が速いことに加え、出力ノイズが非常に小さいため、TPS73801-SEP レギュレータは高精度 RF 電源アプリケーションに理想的です。

出力電圧範囲は 1.21~20V であり、最小 10μF の出力コンデンサを使用して安定に動作します。小容量のセラミック・コンデンサを、ESR を追加しないで使用できます。内部保護回路として、バッテリ逆接続保護、電流制限、過熱制限、逆電流保護機能が搭載されています。TPS73801-SEP レギュレータは可変の 1.21V リファレンス電圧を備えており、6 ピンの TO-223 (DCQ) パッケージで供給されます。

製品情報

部品番号 ⁽¹⁾	グレード	パッケージ
TPS73801MDCQTPSEP	20krad(Si)	SOT-223 (6)
TPS73801MDCQPSEP	RLAT	6.55mm × 7.26mm 質量 = 119.8mg ⁽²⁾

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
- (2) 質量の精度は ±10% です。



概略回路図



Table of Contents

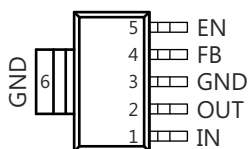
1 特長	1	8 Application and Implementation	14
2 アプリケーション	1	8.1 Application Information.....	14
3 概要	1	8.2 Typical Application.....	14
4 Revision History	2	9 Power Supply Recommendations	17
5 Pin Configuration and Functions	3	10 Layout	18
6 Specifications	4	10.1 Layout Guidelines.....	18
6.1 Absolute Maximum Ratings.....	4	10.2 Layout Example.....	18
6.2 ESD Ratings.....	4	10.3 Thermal Considerations.....	18
6.3 Recommended Operating Conditions.....	4	11 Device and Documentation Support	20
6.4 Thermal Information.....	4	11.1 Receiving Notification of Documentation Updates..	20
6.5 Electrical Characteristics.....	5	11.2 サポート・リソース.....	20
6.6 Typical Characteristics.....	7	11.3 Trademarks.....	20
7 Detailed Description	11	11.4 Electrostatic Discharge Caution.....	20
7.1 Overview.....	11	11.5 Glossary.....	20
7.2 Functional Block Diagram.....	11	12 Mechanical, Packaging, and Orderable Information	21
7.3 Feature Description.....	11		
7.4 Device Functional Modes.....	13		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2018) to Revision A (May 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• 「特長」セクションの「放射線耐性を強化」と「宇宙向けに強化されたプラスチック」の箇条書き項目を更新.....	1
• 「アプリケーション」セクションを更新.....	1
• 「製品情報」表にデバイスの質量と寸法を追加.....	1

5 Pin Configuration and Functions



**图 5-1. DCQ Package
SOT-223
Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	—	Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 μ F to 10 μ F is sufficient. The TPS73801-SEP regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
2	OUT	—	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 μ F is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
3	GND	—	Ground.
4	FB	I	Feedback. This is the input to the error amplifier. This pin is internally clamped to ± 7 V. It has a bias current of 3 μ A that flows into the pin. The FB pin voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
5	EN	I	Enable. The EN pin is used to put the TPS73801-SEP regulators into a low-power shutdown state. The output is off when the EN pin is pulled low. The EN pin can be driven either by 5-V logic or open-collector gate, normally several microamperes, and the EN pin current, typically 3 μ A. If unused, the EN pin must be connected to the IN pin. The device is in the low-power shutdown state if the EN pin is not connected.
6	GND	—	Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{IN} Input voltage	IN	–20	20	V
	OUT	–20	20	
	Input-to-output differential ⁽²⁾	–20	20	
	FB	–7	7	
	EN	–20	20	
t_{short}	Output short-circuit duration	Indefinite		
T_J	Operating virtual-junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT cannot exceed ± 20 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	$V_{OUT} + V_{DO}$	20	V
V_{IH}	EN high-level input voltage	2	20	V
V_{IL}	EN low-level input voltage		0.25	V
T_J	Recommended operating junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS73801-SEP	UNIT
		DCQ (SOT-223)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over operating temperature range $T_A = -55^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP ⁽⁹⁾	MAX	UNIT
V_{IN}	Input voltage ^{(1) (2)}		25°C	2.2	1.9	20	V
V_{FB}	FB pin voltage ^{(1) (3)}	$V_{IN} = 2.21\text{ V}$, $I_{LOAD} = 1\text{ mA}$	25°C	1.192	1.21	1.228	V
		$V_{IN} = 2.5\text{ V}$ to 20 V , $I_{LOAD} = 1\text{ mA}$ to 1 A	Full range	1.174	1.21	1.246	
	Line regulation ⁽¹⁾	$\Delta V_{IN} = 2.21\text{ V}$ to 20 V , $I_{LOAD} = 1\text{ mA}$	Full range		1.5	5	mV
	Load regulation ⁽¹⁾	$V_{IN} = 2.5\text{ V}$, $\Delta I_{LOAD} = 1\text{ mA}$ to 1 A	25°C		2	8	mV
			Full range			18	
V_{DO}	Dropout voltage ^{(2) (5) (4)} $V_{IN} = V_{OUT(NOMINAL)}$	$I_{LOAD} = 1\text{ mA}$	25°C		0.02	0.06	V
			Full range			0.10	
		$I_{LOAD} = 100\text{ mA}$	25°C		0.1	0.17	
			Full range			0.22	
		$I_{LOAD} = 500\text{ mA}$	25°C		0.19	0.27	
			Full range			0.35	
I_{GND}	GND pin current ^{(4) (6)} $V_{IN} = V_{OUT(NOMINAL)} + 1$	$I_{LOAD} = 1\text{ A}$	25°C		0.24	0.30	mA
			Full range			0.40	
		$I_{LOAD} = 0\text{ mA}$	Full range		1	1.5	
			Full range		1.1	1.6	
		$I_{LOAD} = 100\text{ mA}$	Full range		3.8	5.5	
			Full range		15	25	
V_N	Output voltage noise	$C_{OUT} = 10\text{ }\mu\text{F}$, $I_{LOAD} = 1\text{ A}$, $B_W = 10\text{ Hz}$ to 100 kHz	25°C		45		μV_{RMS}
I_{FB}	FB pin bias current ^{(1) (7)}		25°C		3	10	μA
V_{EN}	Shutdown threshold	$V_{OUT} = \text{OFF to ON}$	Full range		0.9	2	V
		$V_{OUT} = \text{ON to OFF}$	Full range	0.15	0.75		
I_{EN}	EN pin current	$V_{EN} = 0\text{ V}$	25°C		0.01	1	μA
		$V_{EN} = 20\text{ V}$	25°C		3	30	
	Quiescent current in shutdown	$V_{IN} = 6\text{ V}$, $V_{EN} = 0\text{ V}$	25°C		0.01	1	μA
PSRR	Ripple rejection ⁽¹⁰⁾	$V_{IN} - V_{OUT} = 1.5\text{ V}$ (avg), $V_{RIPPLE} = 0.5\text{ V}_{P-P}$, $f_{RIPPLE} = 120\text{ Hz}$, $I_{LOAD} = 0.75\text{ A}$	25°C	55	63		dB
I_{CL}	Current limit	$V_{IN} = 7\text{ V}$, $V_{OUT} = 0\text{ V}$	25°C		2		A
		$V_{IN} = V_{OUT(NOMINAL)} + 1$	Full range		1.6		
I_{REV}	Input reverse leakage current	$V_{IN} = -20\text{ V}$, $V_{OUT} = 0\text{ V}$	Full range			1	mA
I_{RO}	Reverse output current ⁽⁸⁾	$V_{OUT} = 1.21\text{ V}$, $V_{IN} < 1.21\text{ V}$	25°C		300	600	μA

- (1) The TPS73801-SEP is tested and specified for these conditions with the FB pin connected to the OUT pin.
- (2) Dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
- (3) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
- (4) To satisfy requirements for minimum input voltage, the TPS73801-SEP is tested and specified for these conditions with an external resistor divider (two 4.12-k Ω resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-mA DC load on the output.
- (5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to $V_{IN} - V_{DROPOUT}$.
- (6) GND pin current is tested with $V_{IN} = (V_{OUT(NOMINAL)} + 1\text{ V})$ and a current source load. The GND pin current decreases at higher input voltages.
- (7) FB pin bias current flows into the FB pin.
- (8) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

- (9) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
- (10) Parameter is specified by characterization and is not tested in production.

6.6 Typical Characteristics

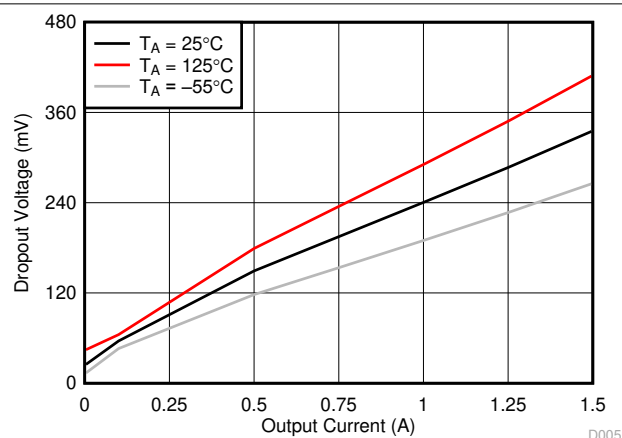


Figure 6-1. Dropout Voltage vs Output Current

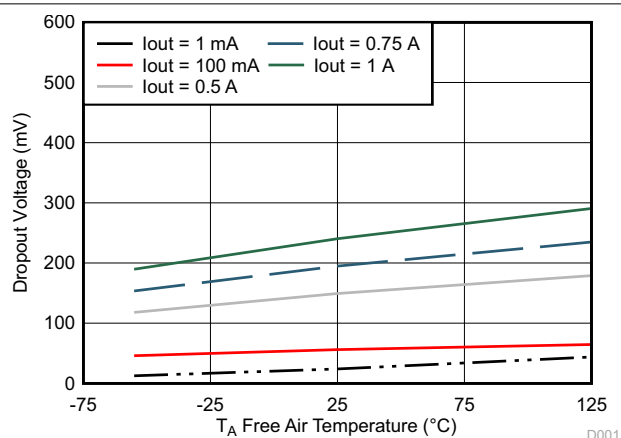


Figure 6-2. Dropout Voltage vs Temperature

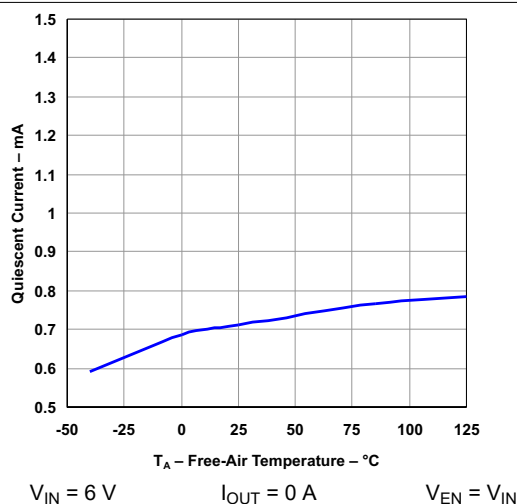


Figure 6-3. Quiescent Current vs Temperature

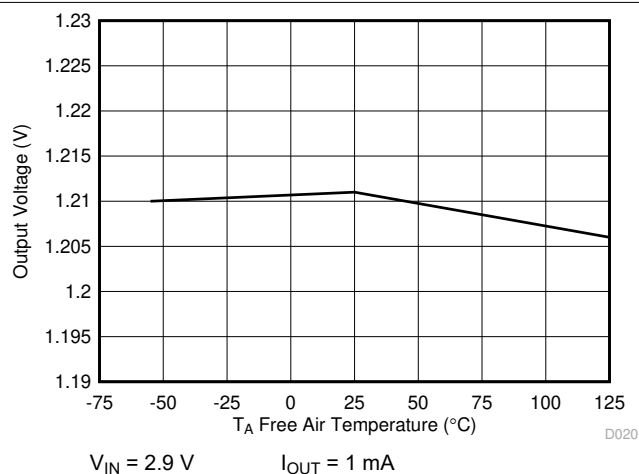


Figure 6-4. Output Voltage vs Temperature

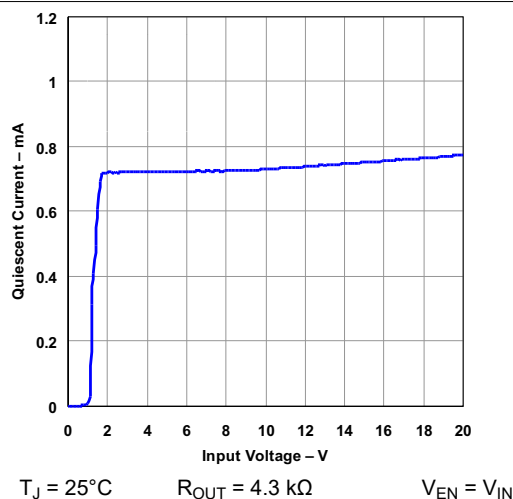


Figure 6-5. Quiescent Current vs Input Voltage

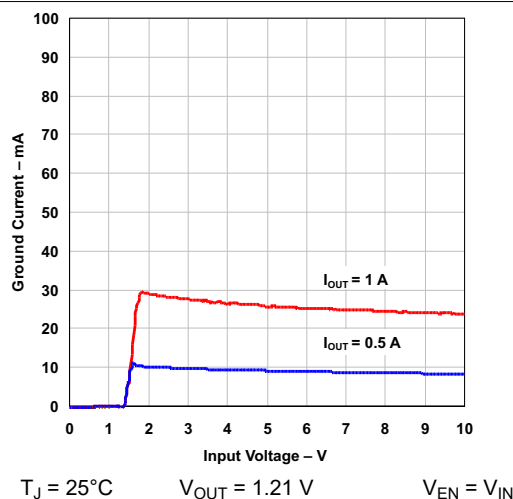


Figure 6-6. Ground Current vs Input Voltage

6.6 Typical Characteristics (continued)

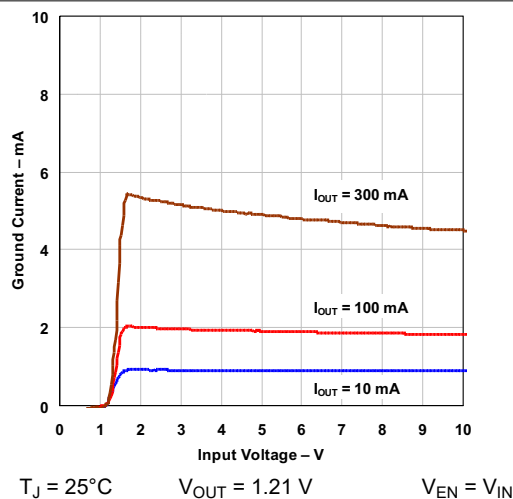


Figure 6-7. Ground Current vs Input Voltage

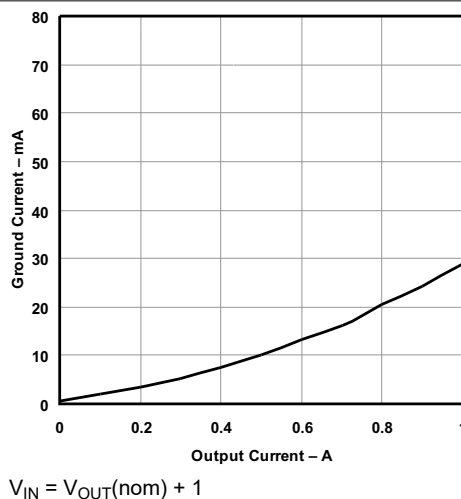


Figure 6-8. Ground Current vs Output Current

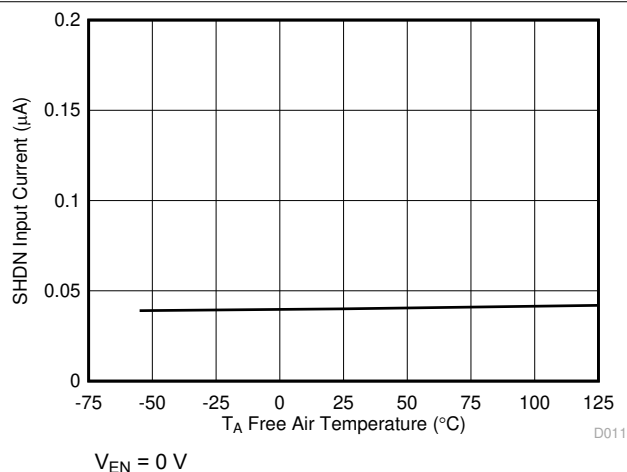


Figure 6-9. EN Input Current vs Temperature

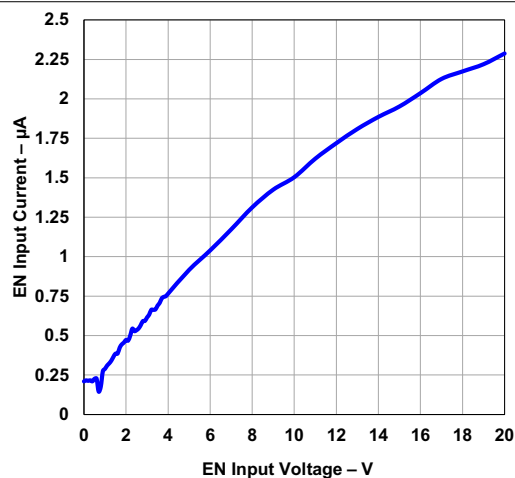


Figure 6-10. EN Input Current vs EN Input Voltage

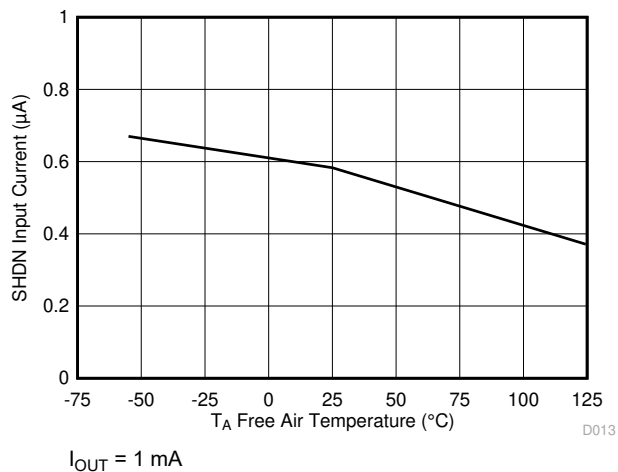


Figure 6-11. EN Threshold (Off to On) vs Temperature

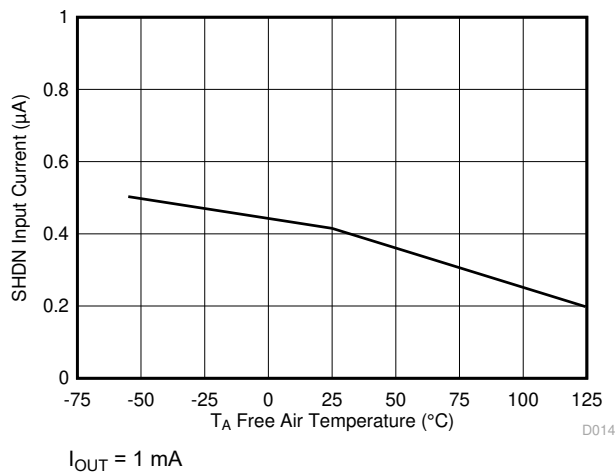


Figure 6-12. EN Threshold (On to Off) vs Temperature

6.6 Typical Characteristics (continued)

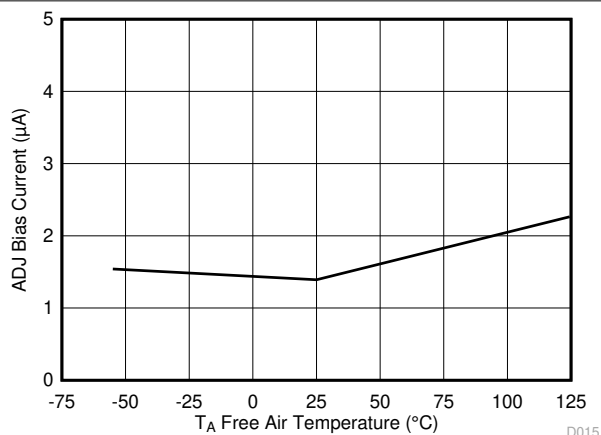


FIG 6-13. FB Bias Current vs Temperature

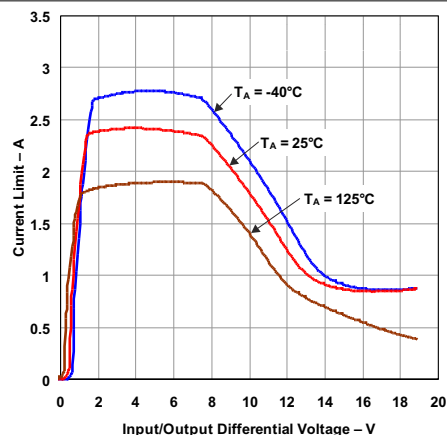


FIG 6-14. Current Limit vs Input/Output Differential Voltage

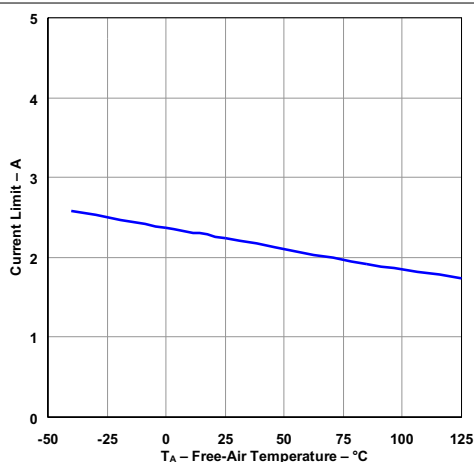


FIG 6-15. Current Limit vs Temperature

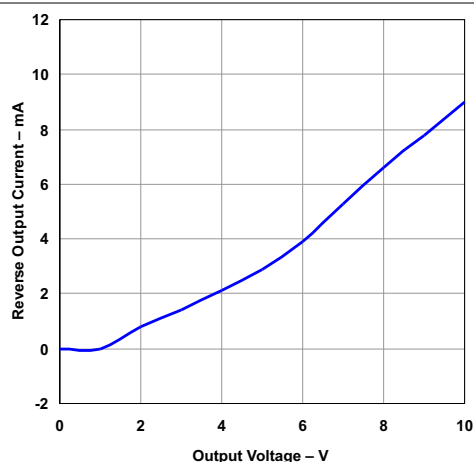


FIG 6-16. Reverse Output Current vs Output Voltage

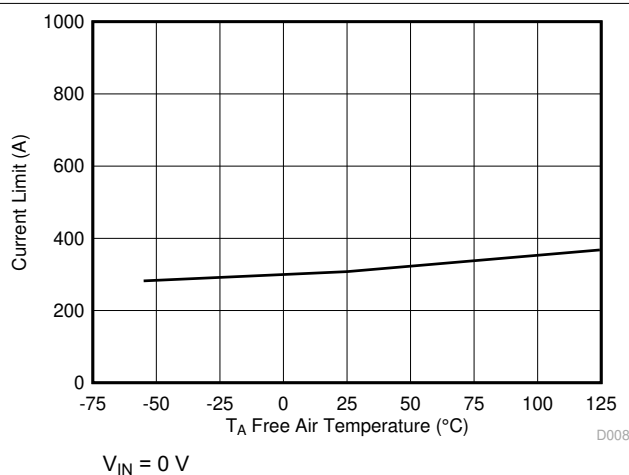


FIG 6-17. Reverse Output Current vs Temperature

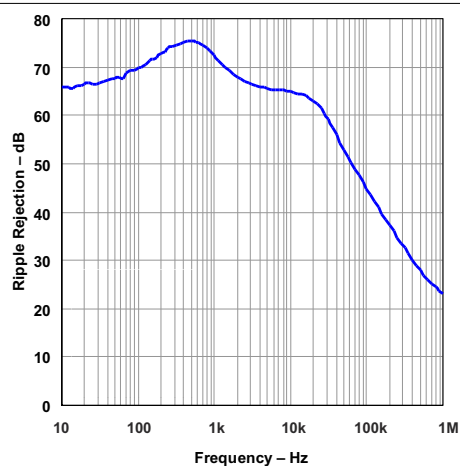
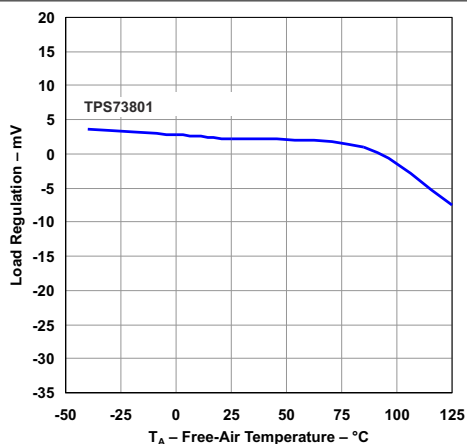
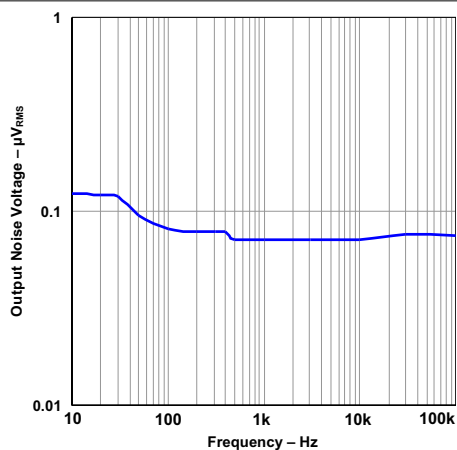
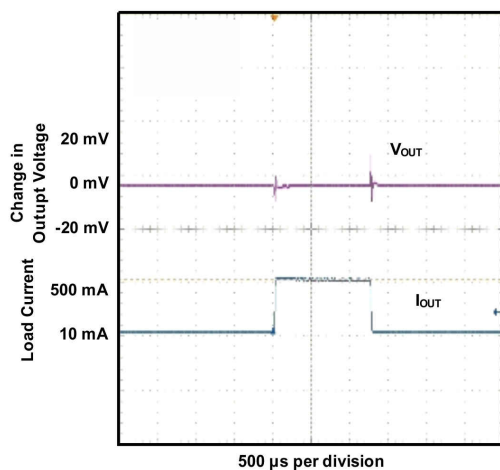
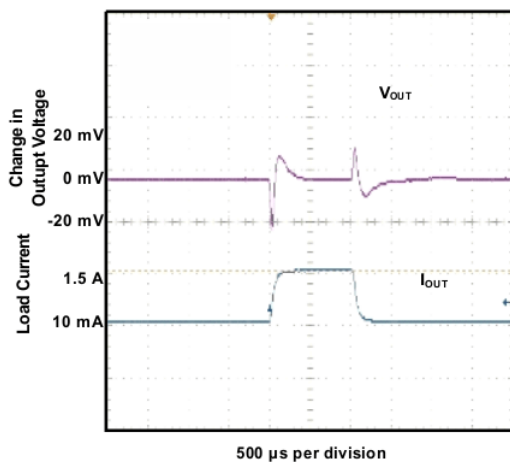


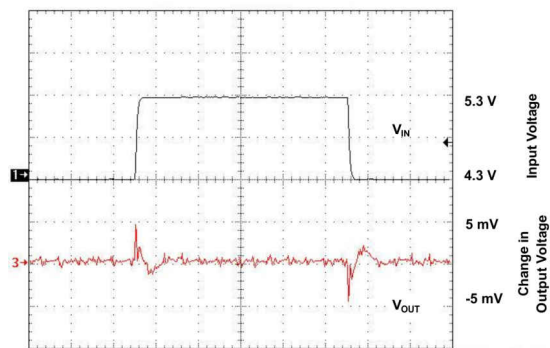
FIG 6-18. Ripple Rejection vs Frequency

6.6 Typical Characteristics (continued)


 $I_{OUT} = 1\text{ A}$
6-19. Load Regulation vs Temperature

 $C_{OUT} = 10\text{ }\mu\text{F}$ (ceramic)

 $I_{OUT} = 1\text{ A}$
6-20. Output Noise Voltage vs Frequency

 $V_{IN} = 4.3\text{ V}$ $C_{IN} = 10\text{ }\mu\text{F}$ $C_{OUT} = 10\text{ }\mu\text{F}$ (ceramic)

6-21. Load Transient Response

 $V_{IN} = 4.3\text{ V}$ $C_{IN} = 10\text{ }\mu\text{F}$ $C_{OUT} = 10\text{ }\mu\text{F}$ (ceramic)

6-22. Max Load Transient Response

 $I_{OUT} = 1.5\text{ A}$
 $C_{IN} = 10\text{ }\mu\text{F}$
 $C_{OUT} = 10\text{ }\mu\text{F}$ (ceramic)

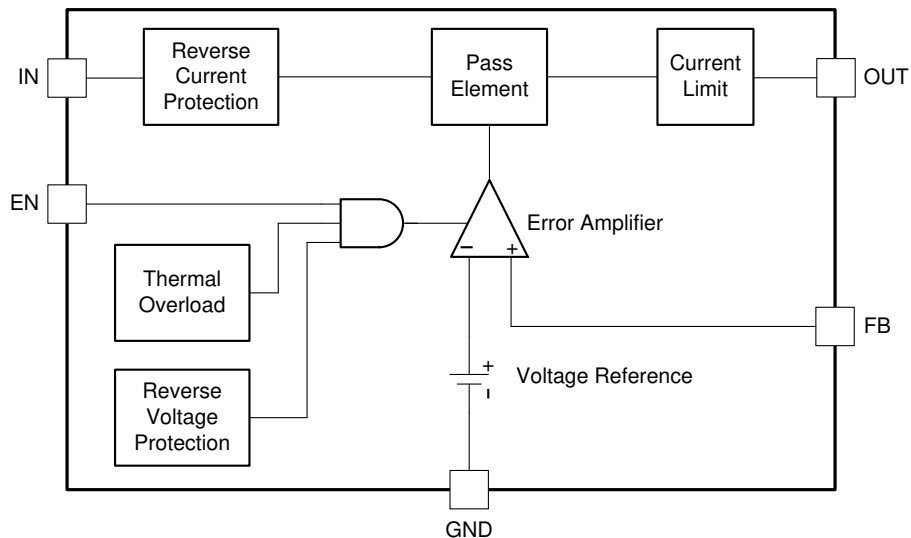
6-23. Line Transient Response

7 Detailed Description

7.1 Overview

The TPS73801-SEP is a 1-A LDO regulator optimized for fast transient response. The devices are capable of supplying 1 A at a dropout voltage of 300 mV. The low operating quiescent current (1 mA) drops to less than 1 μ A in shutdown. In addition to the low quiescent current, the TPS73801-SEP regulators incorporate several protection features which make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TPS73801-SEP acts as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20 V and still allow the device to start and operate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Operation

The TPS73801-SEP has an adjustable output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors as shown in [Figure 7-1](#). The device maintains the voltage at the FB pin at 1.21 V referenced to ground. The current in R1 is then equal to $(1.21 \text{ V} / R1)$, and the current in R2 is the current in R1 plus the FB pin bias current. The FB pin bias current, 3 μ A at 25°C, flows through R2 into the FB pin. The output voltage can be calculated using the formula shown in [Equation 1](#). The value of R1 should be less than 4.17 k Ω to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.

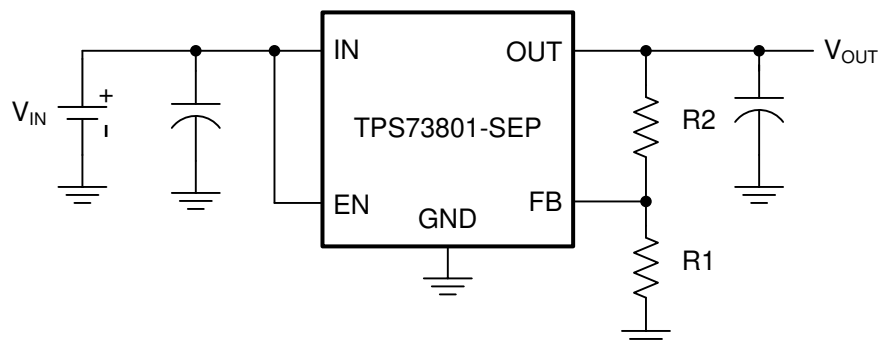


Figure 7-1. Adjustable Operation

The output voltage can be set using the following equations:

$$V_{OUT} = 1.21 V \left(1 + \frac{R_2}{R_1}\right) + I_{FB} \times R_2 \quad (1)$$

$$V_{FB} = 1.21 V \quad (2)$$

$$I_{FB} = 3 \mu A \text{ at } 25^\circ C \quad (3)$$

$$\text{Output Range} = 1.21 \text{ to } 20 V \quad (4)$$

7.3.2 Fixed Operation

The TPS73801-SEP can be used in a fixed voltage configuration. By connecting the FB pin to OUT, the TPS73801-SEP will regulate the output to 1.21 V. During fixed voltage operation, the FB pin can be used for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances (R_P) between the output and the load. This becomes more crucial with higher load currents.

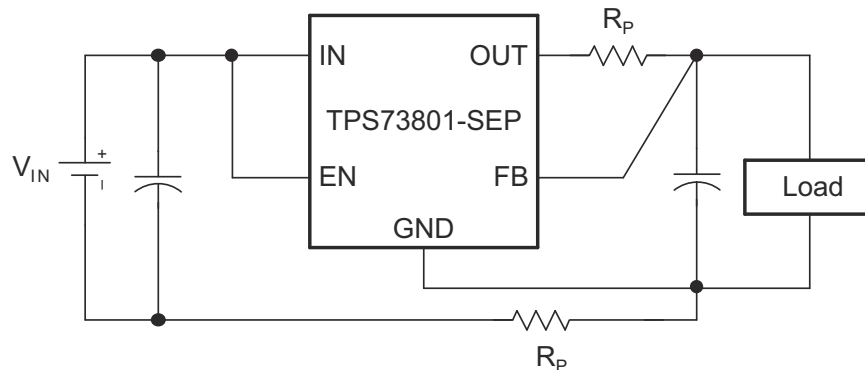


FIG 7-2. Kelvin Sense Connection

7.3.3 Overload Recovery

Like many IC power regulators, the TPS73801-SEP has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS73801-SEP.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

7.3.4 Output Voltage Noise

The TPS73801-SEP regulators have been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically $40 \text{ nV}/\sqrt{\text{Hz}}$ over this frequency bandwidth for the TPS73801-SEP. For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly. This results in RMS noise over the 10-Hz to 100-kHz bandwidth of $14 \mu\text{VRMS}$ for the TPS73801-SEP.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS73801-SEP. Power supply ripple rejection must also be considered; the TPS73801-SEP regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

7.3.5 Protection Features

The TPS73801-SEP regulators incorporate several protection features that make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TPS73801-SEP can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the EN pin turns off the device and stops the output from sourcing the short-circuit current.

The FB pin can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the FB pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the FB pin is connected to a resistor divider that would pull the FB pin above its 7-V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5 mA when the FB pin is at 7 V. The 13-V difference between OUT and FB pins divided by the 5-mA maximum current into the FB pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. When the IN pin of the TPS73801-SEP is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

7.4 Device Functional Modes

See the device modes in [表 7-1](#).

表 7-1. Device Modes

EN	DEVICE STATE
H	Regulated voltage
L	Shutdown

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Capacitance and Transient Response

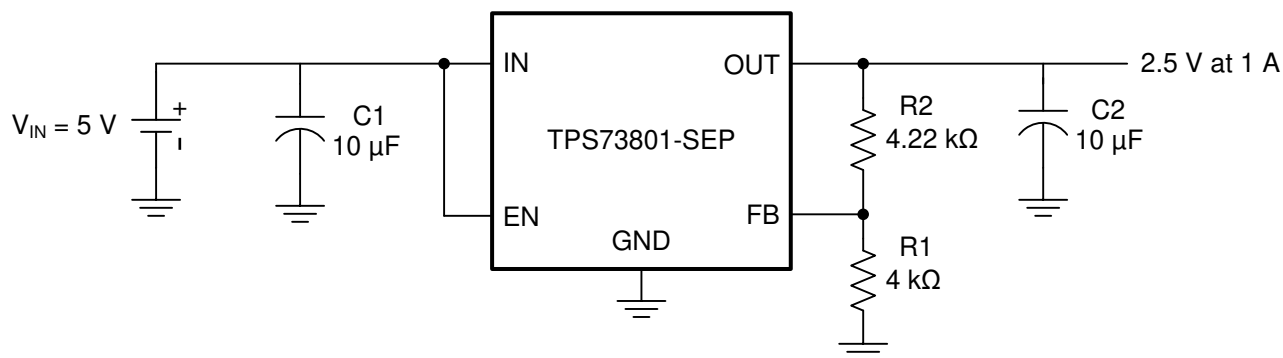
The TPS73801-SEP regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10 μF with an ESR of 3 Ω or less is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS73801-SEP, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10- μF Y5V capacitor can exhibit an effective value as low as 1 μF to 2 μF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

8.2 Typical Application

This section will highlight some of the design considerations when implementing this device in various applications.



All capacitors are ceramic.

8-1. Adjustable Output Voltage Operation

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	5 V
Output voltage (V_{OUT})	2.5 V
Output current (I_{OUT})	0 to 1 A
Load regulation	1%

8.2.2 Detailed Design Procedure

The TPS73801-SEP has an adjustable output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors R1 and R2 as shown in [Adjustable Output Voltage Operation](#). The device maintains the voltage at the FB pin at 1.21 V referenced to ground. The current in R1 is then equal to $(1.21 \text{ V} / R1)$, and the current in R2 is the current in R1 plus the FB pin bias current. The FB pin bias current, 3 μA at 25°C, flows through R2 into the FB pin. The output voltage can be calculated using 式 5.

$$V_{OUT} = 1.21 \text{ V} \left(1 + \frac{R2}{R1}\right) + I_{FB} \times R2 \quad (5)$$

The value of R1 should be less than 4.17 k Ω to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50 V, R1 will be set to 4.0 k Ω . R2 is then found to be 4.22 k Ω using the equation above.

$$V_{OUT} = 1.21 \text{ V} \left(1 + \frac{4.22 \text{ k}\Omega}{4.0 \text{ k}\Omega}\right) + 3 \mu\text{A} \times 4.22 \text{ k}\Omega \quad (6)$$

$$V_{OUT} = 2.50 \text{ V} \quad (7)$$

The adjustable device is tested and specified with the FB pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: $V_{OUT} / 1.21 \text{ V}$. For example, load regulation for an output current change of 1 mA to 1.5 A is –2 mV (typ) at $V_{OUT} = 1.21 \text{ V}$. At $V_{OUT} = 2.50 \text{ V}$, the typical load regulation is:

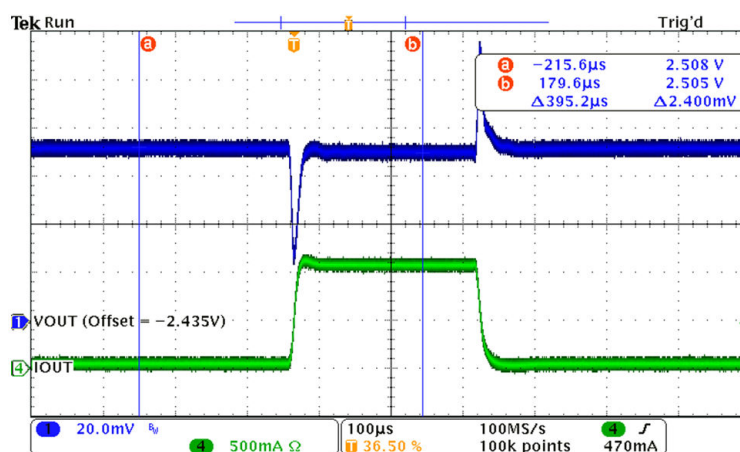
$$(2.50 \text{ V} / 1.21 \text{ V})(-2 \text{ mV}) = -4.13 \text{ mV} \quad (8)$$

☒ 8-2 shows the actual change in output is approximately 3 mV for a 1-A load step. The maximum load regulation at 25°C is –8 mV. At $V_{OUT} = 2.50 \text{ V}$, the maximum load regulation is:

$$(2.50 \text{ V} / 1.21 \text{ V})(-8 \text{ mV}) = -16.53 \text{ mV} \quad (9)$$

Since 16.53 mV is 0.7% of the 2.5-V output voltage, the load regulation will meet the design requirements.

8.2.3 Application Curve



8-2. 1-A Load Transient Response

9 Power Supply Recommendations

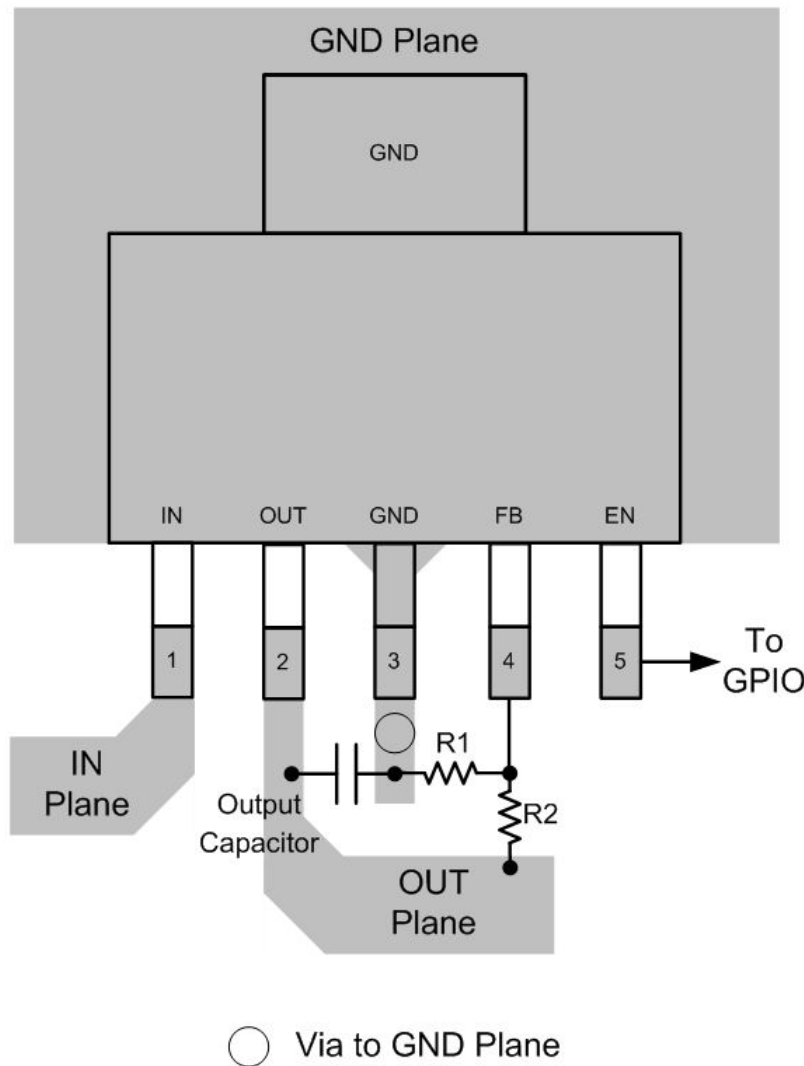
The device is designed to operate with an input voltage supply up to 20 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

1. For best performance, all traces should be as short as possible.
2. Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
3. A minimum output capacitor of 10 μF with an ESR of 3 Ω or less is recommended to prevent oscillations. X5R and X7R dielectrics are preferred.
4. Place the output capacitor as close as possible to the OUT pin of the device.
5. The tab of the DCQ package should be connected to ground.

10.2 Layout Example



10-1. SOT-223 Layout Example (DCQ)

10.3 Thermal Considerations

The power handling capability of the device is limited by the recommended maximum operating junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{\text{OUT}} (V_{\text{IN}} - V_{\text{OUT}})$
2. GND pin current multiplied by the input voltage: $I_{\text{GND}} \times V_{\text{IN}}$

The GND pin current can be found using the GND Pin Current graphs in [セクション 6.6](#) . Power dissipation is equal to the sum of the two components listed above.

The TPS73801-SEP series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

10.3.1 Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, an output current range of 0 mA to 500 mA, and a maximum ambient temperature of 50°C, what is the operating junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)}) \quad (10)$$

where

- $I_{OUT(MAX)} = 500 \text{ mA}$
- $V_{IN(MAX)} = 6 \text{ V}$
- I_{GND} at ($I_{OUT} = 500 \text{ mA}$, $V_{IN} = 6 \text{ V}$) = 10 mA

So,

$$P = 500 \text{ mA} \times (6 \text{ V} - 3.3 \text{ V}) + 10 \text{ mA} \times 6 \text{ V} = 1.41 \text{ W} \quad (11)$$

The thermal resistance of the DCQ package is 50.5°C/W. So the junction temperature rise above ambient is approximately equal to:

$$1.41 \text{ W} \times 50.5^\circ\text{C/W} = 71.2^\circ\text{C} \quad (12)$$

The junction temperature rise can then be added to the maximum ambient temperature to find the operating junction temperature (T_J):

$$T_J = 50^\circ\text{C} + 71.2^\circ\text{C} = 121.2^\circ\text{C} \quad (13)$$

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73801MDCQPSEP	Active	Production	SOT-223 (DCQ) 6	78 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
TPS73801MDCQPSEP.A	Active	Production	SOT-223 (DCQ) 6	78 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
TPS73801MDCQTPSEP	Active	Production	SOT-223 (DCQ) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
TPS73801MDCQTPSEP.A	Active	Production	SOT-223 (DCQ) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
V62/18616-01XE	Active	Production	SOT-223 (DCQ) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP
V62/18616-01XE-T	Active	Production	SOT-223 (DCQ) 6	78 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73801MDCQTPSEP	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73801MDCQTPSEP	SOT-223	DCQ	6	250	213.0	191.0	35.0

TUBE



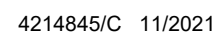
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS73801MDCQPSEP	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS73801MDCQPSEP.A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
V62/18616-01XE-T	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68



SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



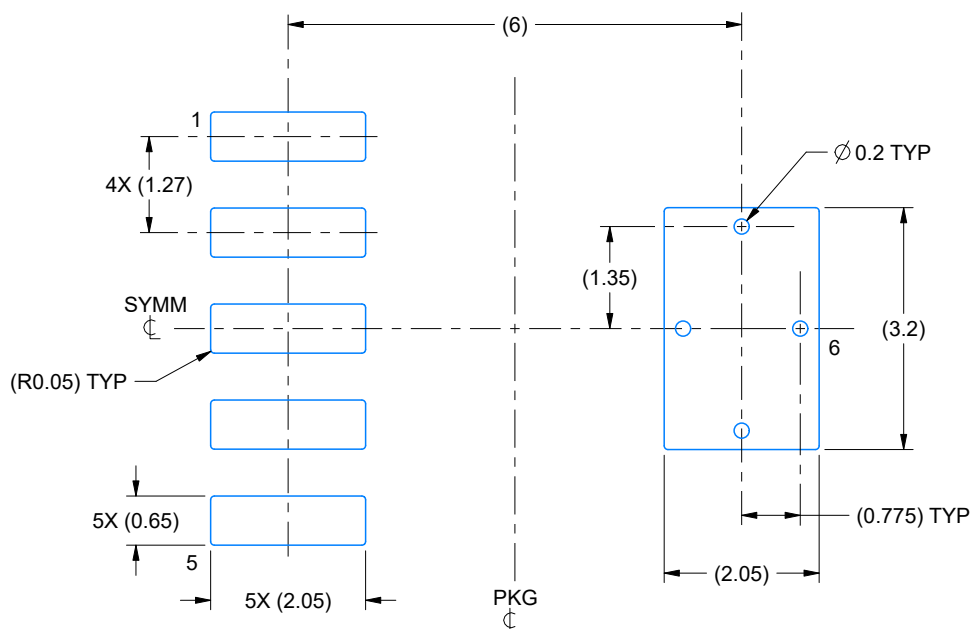
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

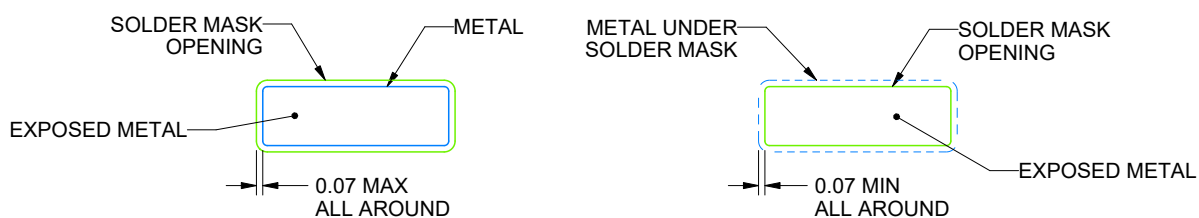
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

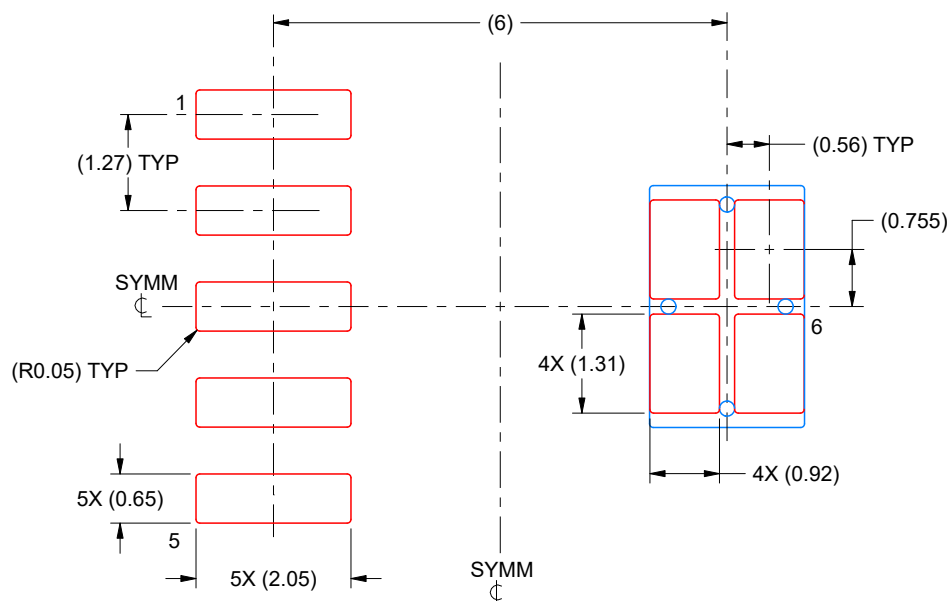
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含みいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月