TEXAS INSTRUMENTS
TPS62085, TPS62086, TPS62087
JAJSFU2C – OCTOBER 2013 – REVISED JANUARY 2021

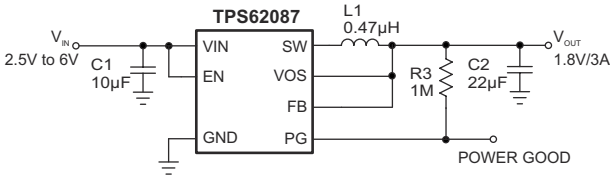
TPS6208x ヒカップ短絡保護搭載、2mm × 2mm VSON パッケージの 3A 降圧型コンバータ

1 特長

- DCS-Control™ トポロジ
- 最大 95% の効率
- ヒカップ短絡保護機能
- パワー・セーブ・モードにより軽負荷時の効率を向上
- 100% デューティ・サイクル動作による最小のドロップアウト電圧
- 2.5V～6.0V の入力電圧範囲
- 動作時静止電流：17μA
- 出力電圧は 0.8V～V_{IN} まで可変
- 1.8V～3.3V の固定出力電圧
- 出力放電
- パワー・グッド出力
- サーマル・シャットダウン保護機能
- 2mm × 2mm の VSON パッケージで供給
- WEBENCH Power Designer でカスタム設計を作成
  - TPS62085 WEBENCH® Power Designer
  - TPS62086 WEBENCH® Power Designer
  - TPS62087 WEBENCH® Power Designer

2 アプリケーション

- バッテリ駆動のアプリケーション
- ポイントオブロード
- プロセッサ用電源
- ハード・ディスク・ドライブ



代表的なアプリケーション回路図

3 概要

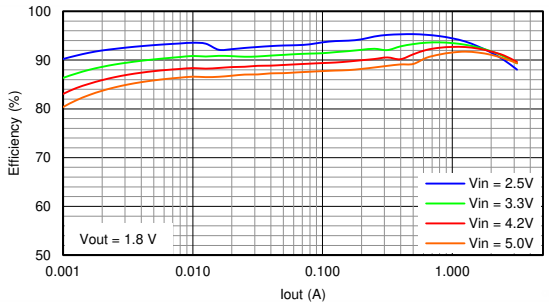
TPS62085、TPS62086、TPS62087 デバイスは高周波数の同期降圧型コンバータで、ソリューションの小型化と高効率のために最適化されています。入力電圧範囲は 2.5V～6.0V で、一般的なバッテリ・テクノロジをサポートします。
このデバイスは、広い出力電流範囲にわたって高い効率で降圧変換を行うことを主眼としています。中負荷から重負荷では PWM モードで動作し、軽負荷時には自動的に省電力モードへ移行するため、負荷電流の全範囲にわたって高効率が維持されます。

システム電源レールの要件に対処するため、内部補償回路は 10μF～150μF の範囲で、多くの外部出力コンデンサの値を選択できます。また、DCS-Control アーキテクチャにより、優れた負荷過渡性能と出力電圧レギュレーション精度を実現しています。このデバイスは、2mm × 2mm の VSON パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS62085	VSON (7)	2.00mm × 2.00mm
TPS62086		
TPS62087		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



標準的なアプリケーションの効率

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2018) to Revision C (January 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Changed maximum $I_{PG,LKG}$ specification up to 125°C T_J from 0.16 µA to 0.25 µA in *Electrical Characteristics* table ... 5

Changes from Revision A (June 2015) to Revision B (July 2018) — **Page**

- 「*特長*」の一覧でパッケージ名を QFN から VSON に変更 ... 1
- Webench のリンクをデータシートに追加 ... 1
- Added SW node AC value in *Absolute Maximum Ratings* table ... 4
- Changed f_{PFM} To: f_{PSM} in 式 1 ... 7
- Added 図 8-1 to *Power Save Mode* section ... 7
- Added 表 8-1 to *Power Good* section ... 9
- Changed Murata inductor part number in 表 9-4 ... 11

Changes from Revision * (October 2013) to Revision A (June 2015) — **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 ... 1

5 Device Options

PART NUMBER(1)	OUTPUT VOLTAGE
TPS62085RLT	Adjustable
TPS62086RLT	3.3 V
TPS62087RLT	1.8 V

(1) For detailed ordering information, please check the *セクション Mechanical, Packaging, and Orderable Information* section at the end of this datasheet.

6 Pin Configuration and Functions

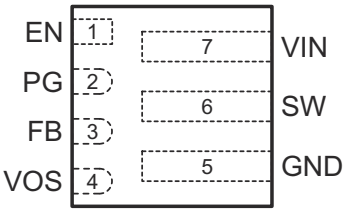


図 6-1. RLT Package 7-Pin VSON Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	IN	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. This pin has a pulldown resistor of typically 400 kΩ when the device is disabled.
FB	3	IN	Feedback pin. For the fixed output voltage versions this pin must be connected to the output voltage.
GND	5		Ground pin.
PG	2	OUT	Power good open drain output pin. The pullup resistor can not be connected to any voltage higher than 6 V. If unused, leave it floating.
SW	6	PWR	Switch pin of the power stage.
VIN	7	PWR	Input voltage pin.
VOS	4	IN	Output voltage sense pin. This pin must be directly connected to the output capacitor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage at Pins(2)	VIN, FB, VOS, EN, PG	–0.3	7	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 100ns)(3)	–3	11	
Temperature	Operating Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN(1)	NOM	MAX(1)	UNIT
V_{IN}	Input voltage range	2.5		6	V
I_{SINK_PG}	Sink current at PG pin			1	mA
V_{PG}	Pullup resistor voltage			6	V
T_J	Operating junction temperature	–40		125	°C

(1) Refer to *セクション 9* for further information.

7.4 Thermal Information

THERMAL METRIC		TPS6208x RLT [VSON] 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

7.5 Electrical Characteristics

T_J = –40 °C to 125 °C, and V_{IN} = 3.6 V. Typical values are at T_J = 25 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6	V
I_Q	Quiescent current into VIN	No load, device not switching T_J = –40 °C to 85 °C, V_{IN} = 2.5 V to 5.5 V		17	25	µA
I_{SD}	Shutdown current into VIN	EN = Low, T_J = –40 °C to 85 °C, V_{IN} = 2.5 V to 5.5 V		0.7	5	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis	V_{IN} rising		200		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage	V_{IN} = 2.5 V to 6.0 V	1.0			V
V_{IL}	Low-level input voltage	V_{IN} = 2.5 V to 6.0 V			0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01	0.16	µA
R_{PD}	Pulldown resistance at EN pin	EN = Low		400		kΩ
SOFT START, POWER GOOD						
t_{SS}	Soft-start time	Time from EN high to 95% of V_{OUT} nominal		0.8		ms
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal	93%	95%	98%	
		V_{OUT} falling, referenced to V_{OUT} nominal	88%	90%	93%	
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V, T_J = –40 °C to 85 °C		0.01	0.16	µA
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.25	µA
OUTPUT						
V_{OUT}	Output voltage range, TPS62085		0.8		V_{IN}	V
	Output voltage accuracy, TPS62086, TPS62087[1]	I_{OUT} = 1 A, V_{IN} ≥ V_{OUT} + 1 V, PWM mode	–1.0%		1.0%	
		I_{OUT} = 0 A, V_{IN} ≥ V_{OUT} + 1 V, PSM mode	–1.0%		2.1%	
V_{FB}	Feedback regulation voltage[1] [2]	I_{OUT} = 1A , V_{IN} ≥ V_{OUT} + 1 V, PWM mode	792	800	808	mV
		I_{OUT} = 0 A, V_{IN} ≥ V_{OUT} + 1 V, PSM mode	792	800	817	
$I_{FB,LKG}$	Feedback input leakage current	V_{FB} = 1 V		0.01	0.1	µA
R_{DIS}	Output discharge resistor	EN = LOW, V_{OUT} = 1.8 V		260		Ω
	Line regulation	I_{OUT} = 1 A, V_{IN} = 2.5 V to 6.0 V		0.02		%/V
	Load regulation	I_{OUT} = 0.5 A to 3 A		0.16		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET ON-resistance	I_{SW} = 500 mA		31	56	mΩ
	Low-side FET ON-resistance	I_{SW} = 500 mA		23	45	mΩ
I_{LIM}	High-side FET switch current limit		3.7	4.6	5.5	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A		2.4		MHz

(1) For more information, see *セクション 8.3.1*.
(2) Conditions: L = 0.47 µH, C_{OUT} = 22 µF

7.6 Typical Characteristics

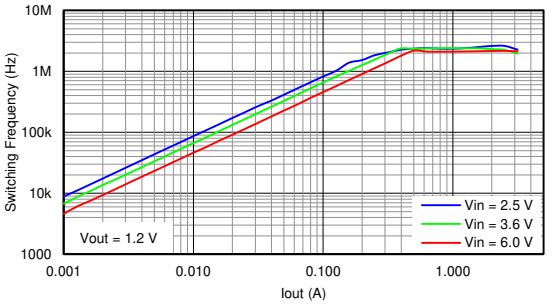


図 7-1. Switching Frequency

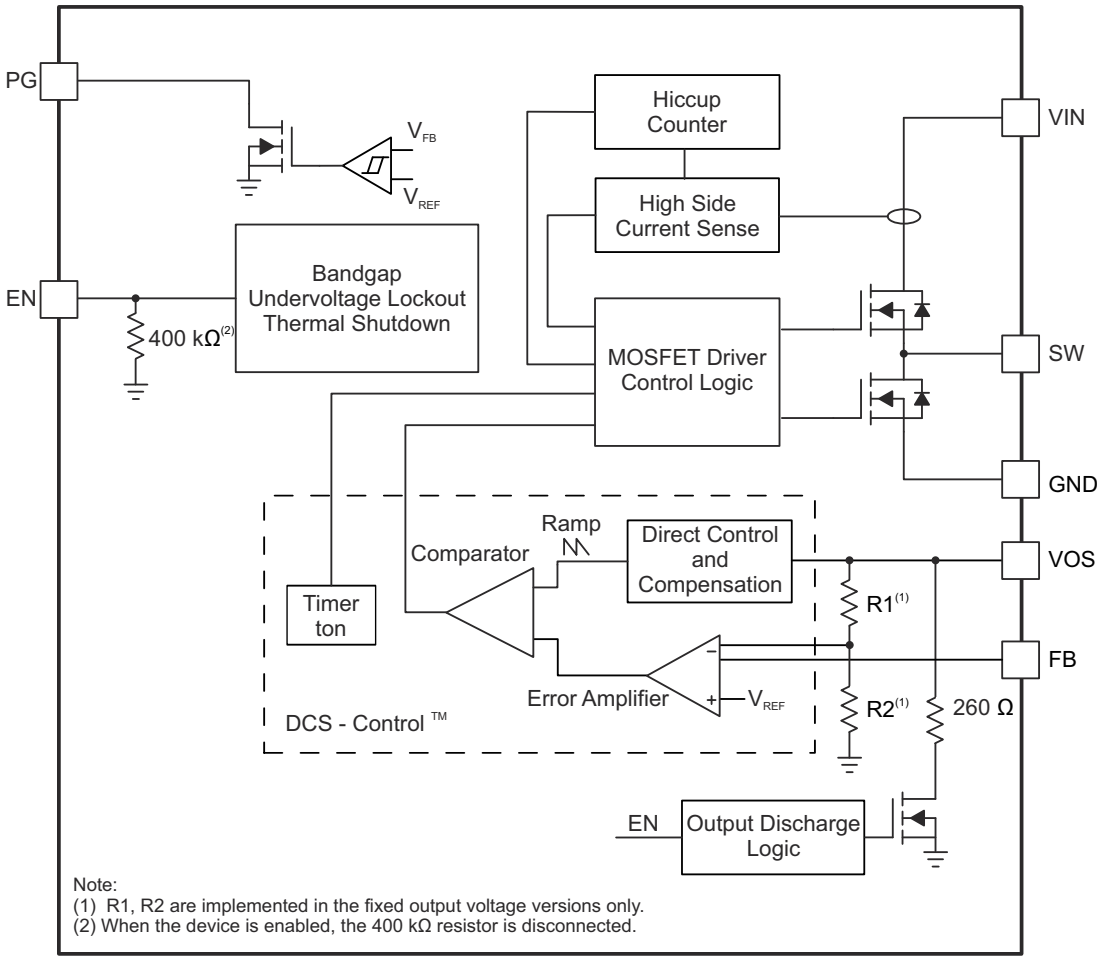
8 Detailed Description

8.1 Overview

The TPS62085, TPS62086, and TPS62087 synchronous step-down converters are based on the DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. Because DCS-Control supports both operation modes (PWM and PSM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. Fixed output voltage version provides smallest solution size combined with lowest no load current. The devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



Note:
(1) R1, R2 are implemented in the fixed output voltage versions only.
(2) When the device is enabled, the 400 kΩ resistor is disconnected.

8.3 Feature Description

8.3.1 Power Save Mode

As the load current decreases, the TPS62085, TPS62086, and TPS62087 enter Power Save Mode (PSM) operation. During Power Save Mode, the converter operates with reduced switching frequency and with a minimum quiescent current maintaining high efficiency. The power save mode occurs when the inductor current becomes discontinuous. Power Save Mode is based on a fixed on-time architecture, as related in 式 1. The

switching frequency over the whole load current range is also shown in Switching Frequency for a typical application.

$$t_{ON} = 420\ ns \times \frac{V_{OUT}}{V_{IN}}$$

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage, as shown in Load Regulation. This effect is minimized by increasing the output capacitor or inductor value. The output voltage accuracy in PSM operation is reflected in the electrical specification table and given for a 22-µF output capacitor.

During PAUSE period in PSM (shown in 図 8-1), the device does not change the PG pin state nor does it detect an UVLO event, in order to achieve a minimum quiescent current and maintain high efficiency at light loads.

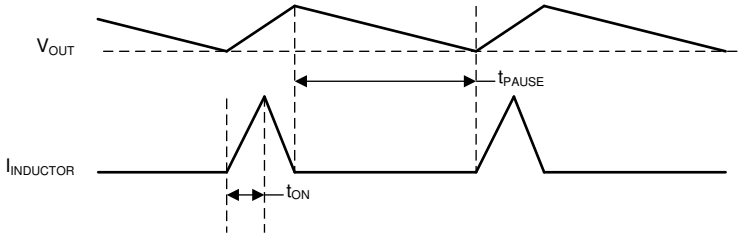


図 8-1. Power Save Mode Waveform Diagram

8.3.2 100% Duty Cycle Low Dropout Operation

The devices offer low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (2)$$

with

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

8.3.3 Soft Start

The TPS62085, TPS62086, and TPS62087 have an internal soft-start circuitry which monotonically ramps up the output voltage and reaches the nominal output voltage during a soft-start time of typically 0.8 ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and Hiccup Short-Circuit Protection

The switch current limit prevents the devices from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy

load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. When this switch current limits is triggered 32 times, the devices stop switching and enable the output discharge. The devices then automatically start a new start-up after a typical delay time of 66 µs has passed. This is named HICCUP short-circuit protection. The devices repeat this mode until the high load condition disappears.

8.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The devices are enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7 µA.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 260 Ω discharges the output through the VOS pin smoothly. The output discharge function also works when thermal shutdown, UVLO, or short-circuit protection are triggered.

An internal pulldown resistor of 400 kΩ is connected to the EN pin when the EN pin is LOW. The pulldown resistor is disconnected when the EN pin is HIGH.

8.4.2 Power Good

The TPS62085, TPS62086, and TPS62087 have a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 6 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. 表 8-1 shows the PG pin logic.

表 8-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} < V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.5\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 0.5\ V$	√	

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS62085 is a synchronous step-down converter in which output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference. The TPS62086 and TPS62087 devices provide a fixed output voltage which does not need an external resistor divider.

9.2 Typical Application

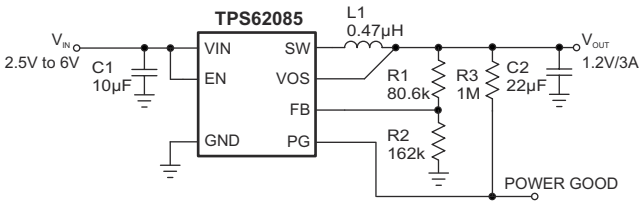


図 9-1. 1.2-V Output Voltage Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 6 V
Output voltage	1.2 V
Output ripple voltage	<20 mV
Maximum output current	3 A

表 9-2 lists the components used for the example.

表 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BR71A106ME51L	Murata
C2	22 µF, Ceramic capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L	Murata
L1	0.47 µH, Power Inductor, size 4 mm × 4 mm × 1.5 mm, XFL4015-471ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603; 0 Ω for TPS62086, TPS62087	Std
R2	162 kΩ, Chip resistor, 1/16 W, 1%, size 0603; open for TPS62086, TPS62087	Std
R3	1 MΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62085 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62086 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62087 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 式 3:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

R2 must not be higher than 180 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Lowest operating quiescent current and best output voltage accuracy are achieved with the fixed output voltage versions. For the fixed output voltage versions, the FB pin must be connected to the output.

9.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, 表 9-3 outlines possible inductor and capacitor value combinations for most applications.

表 9-3. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)				
	10	22	47	100	150
0.47		+(1)	+	+	+
1	+	+	+	+	+
2.2					

(1) Typical application configuration. Other '+' mark indicates recommended filter combinations.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

9.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 4 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (4)$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

TI recommends choosing the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of 式 4. A higher inductor value is also useful to lower ripple current but increases the transient response time as well. The following inductors are recommended to be used in designs.

表 9-4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS L × W × H [mm^3]	DC RESISTANCE [mΩ typical]	PART NUMBER
0.47	6.6	4 × 4 × 1.5	7.6	Coilcraft XFL4015-471
0.47	6.7	3.2 × 2.5 × 1.2	23	Murata DFE322512F-R47N
1	5.1	4 × 4 × 2	10.8	Coilcraft XFL4020-102

9.2.2.5 Capacitor Selection

The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 10 µF is sufficient, though a larger value reduces input current ripple.

The architecture of the TPS62085, TPS62086, and TPS62087 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended typical output capacitor value is 22 µF; this capacitance can vary over a wide range as outline in the output filter selection table. Output capacitors above 150 µF may be used with a reduced load current during startup to avoid triggering the short circuit protection.

A feed-forward capacitor is not required for device proper operation.

9.2.3 Application Curves

V_{IN} = 3.6 V, V_{OUT} = 1.2 V, T_A = 25°C, unless otherwise noted

表 9-5. Table of Graphs

		FIGURE
Efficiency	TPS62085, V_{OUT} = 0.95 V	Efficiency
	TPS62085, V_{OUT} = 1.2 V	Efficiency
	TPS62086, V_{OUT} = 3.3 V	Efficiency
	TPS62087, V_{OUT} = 1.8 V	Efficiency
Line Regulation	TPS62085	Line Regulation
Load Regulation	TPS62085	Load Regulation
Switching Frequency	TPS62085	Switching Frequency

表 9-5. Table of Graphs (continued)

		FIGURE
Waveforms	TPS62085, PWM Operation (Load = 3 A)	PWM Operation, Load = 3 A
	TPS62085, PSM Operation (Load = 100 mA)	PSM Operation, Load = 100 mA
	TPS62085, Load Sweep (Load = Open to 3 A)	Load Sweep, Load = Open to 3 A
	TPS62085, Start-Up (Load = 0.47 Ω)	Start-Up, Load = 0.47 Ω
	TPS62085, Start-Up (Load = Open)	Start-Up, Load = Open
	TPS62085, Shutdown (Load = 0.47 Ω)	Shutdown, Load = 0.47 Ω
	TPS62085, Shutdown (Load = Open)	Shutdown, Load = Open
	TPS62085, Load Transient (Load = 0.5 A to 3 A)	Load Transient, Load = 0.5 A to 3 A
	TPS62085, Load Transient (Load = 50 mA to 3 A)	Load Transient, Load = 50 mA to 3 A
	TPS62085, Output Short-Circuit Protection (Load = 0.47 Ω, Entry)	Output Short-Circuit Protection, Load = 0.47 Ω, Entry
	TPS62085, Output Short-Circuit Protection (Load = 0.47 Ω, Recovery)	Output Short-Circuit Protection, Load = 0.47 Ω, Recovery
	TPS62085, Output Short-Circuit Protection (Load = 0.47 Ω, HICCUP Zoom In)	Output Short-Circuit Protection, Load = 0.47 Ω, HICCUP Zoom In

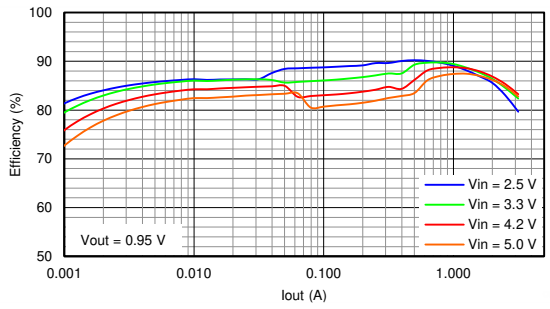


図 9-2. Efficiency

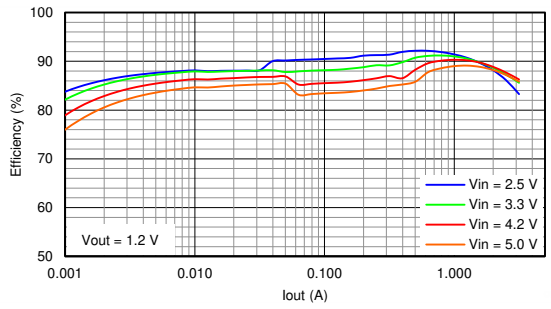


図 9-3. Efficiency

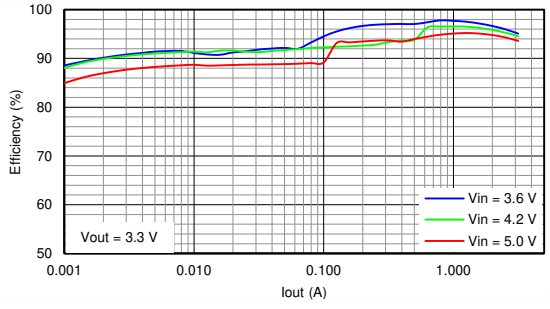


図 9-4. Efficiency

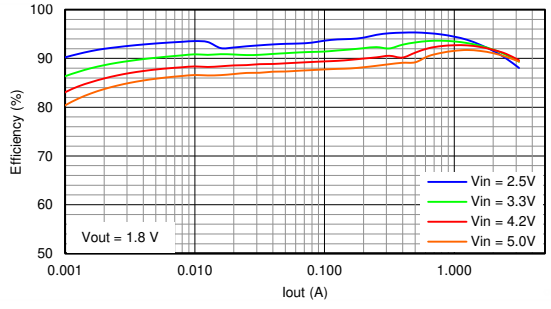


図 9-5. Efficiency

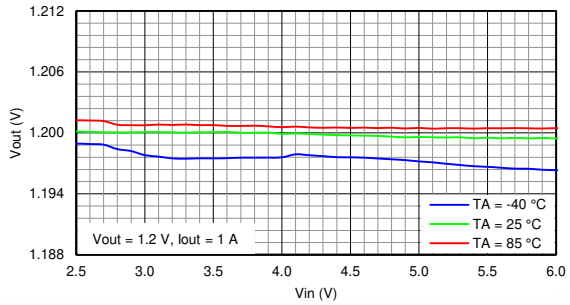


図 9-6. Line Regulation

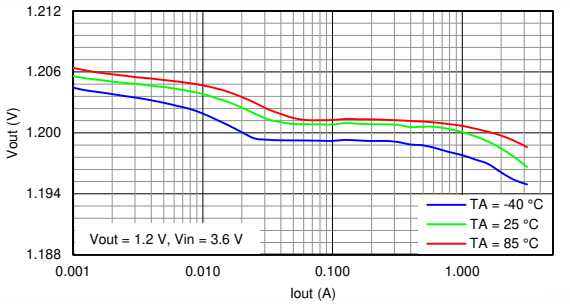


図 9-7. Load Regulation

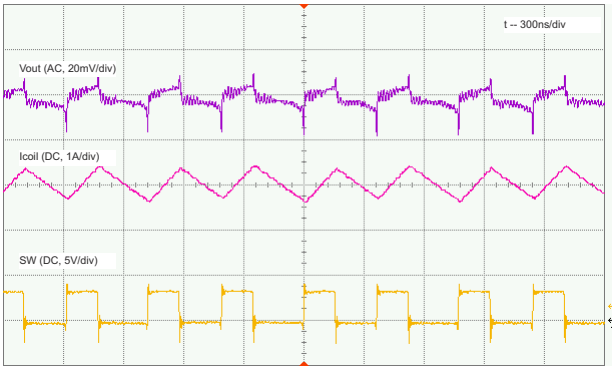


図 9-8. PWM Operation, Load = 3 A

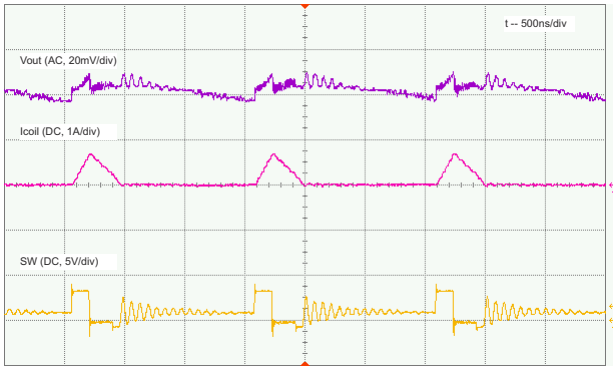


図 9-9. PSM Operation, Load = 100 mA

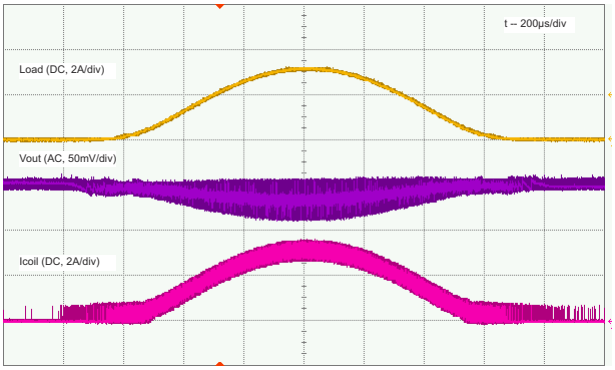


図 9-10. Load Sweep, Load = Open to 3 A

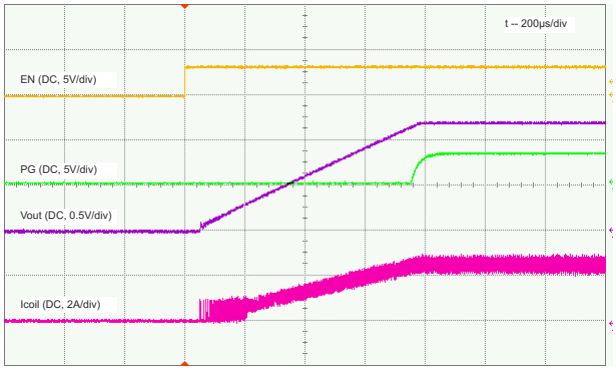


図 9-11. Start-Up, Load = 0.47 Ω

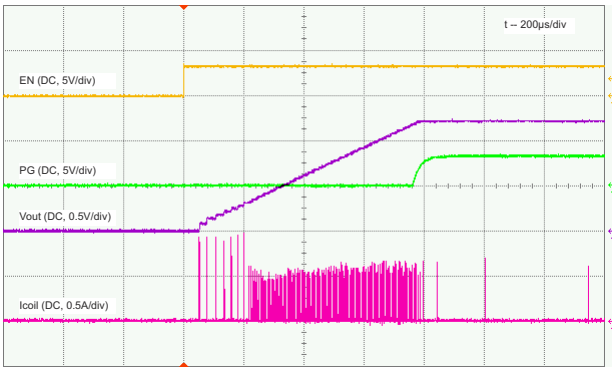


図 9-12. Start-Up, Load = Open

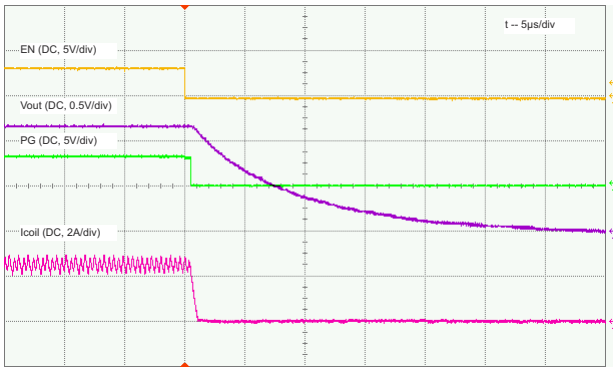


図 9-13. Shutdown, Load = 0.47 Ω

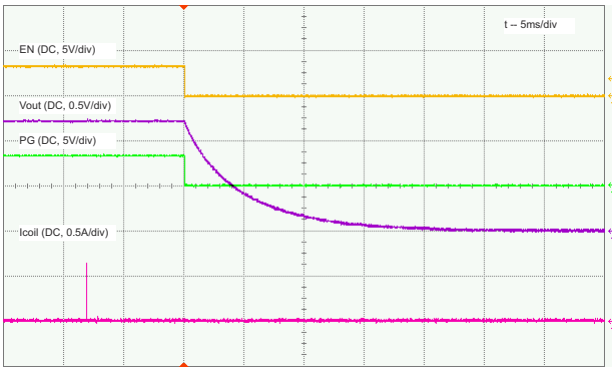


図 9-14. Shutdown, Load = Open

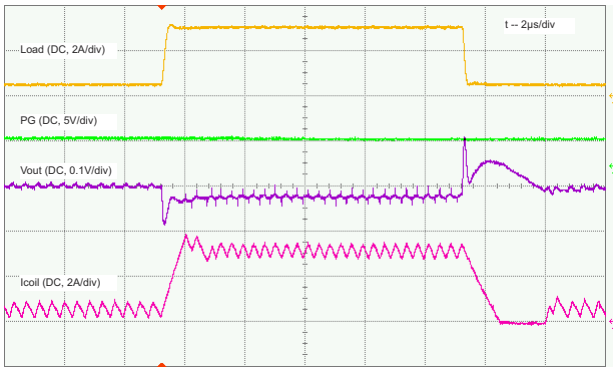


図 9-15. Load Transient, Load = 0.5 A to 3 A

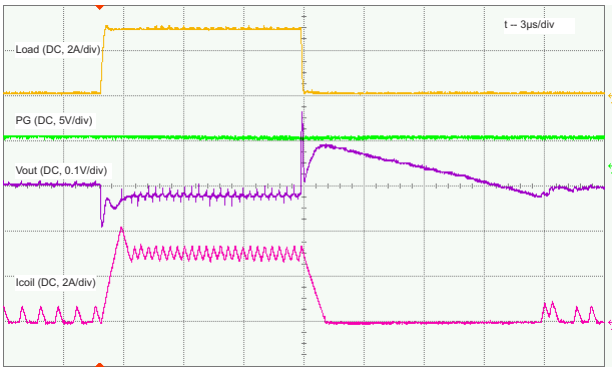


図 9-16. Load Transient, Load = 50 mA to 3 A

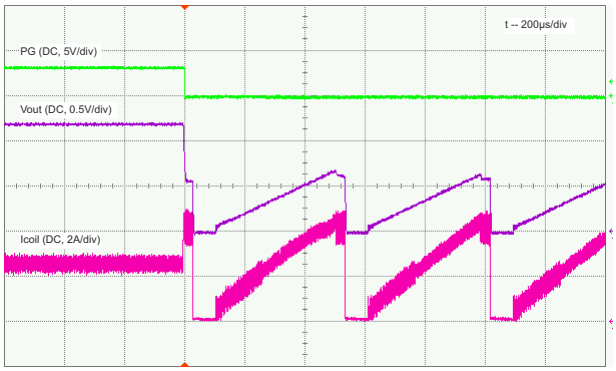


図 9-17. Output Short-Circuit Protection, Load = 0.47 Ω, Entry

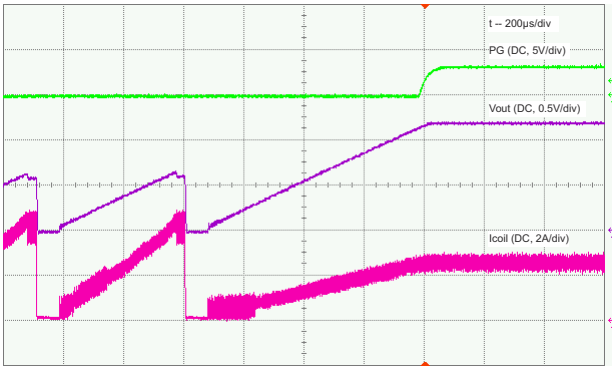


図 9-18. Output Short-Circuit Protection, Load = 0.47 Ω, Recovery

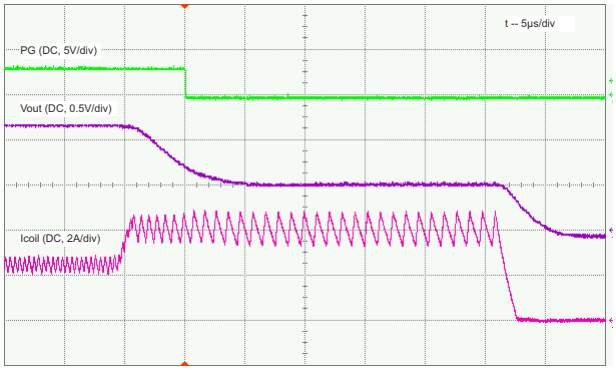


図 9-19. Output Short-Circuit Protection, Load = 0.47 Ω, HICCUP Zoom In

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 6 V. Ensure that the input power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62085, TPS62086, and TPS62087 devices.

The input and output capacitors and the inductor must be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. The low side of the input and output capacitors must be connected directly to the GND pin to avoid a ground potential shift. The sense traces connected to FB and VOS pins are signal traces. Special care must be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes. See 図 11-1 for the recommended PCB layout.

11.2 Layout Example

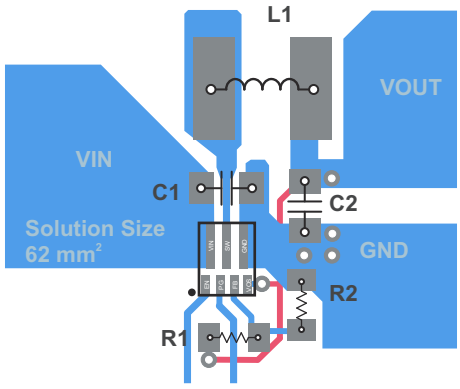


図 11-1. PCB Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in the *TPS62085EVM-169 Evaluation Module User's Guide* (SLVU809) provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the *Thermal Characteristics Application Notes*, SZZA017 and SPRA953.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62085 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62086 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62087 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *TPS62085EVM-169 Evaluation Module User's Guide*, SLVU809
- *Thermal Characteristics Application Note*, SZZA017
- *Thermal Characteristics Application Note*, SPRA953

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ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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TI E2E™ is a trademark of Texas Instruments.
WEBENCH® are registered trademarks of Texas Instruments.
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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62085RLTR	ACTIVE	VSON-HR	RLT	7	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	PD5Q	Samples
TPS62085RLTT	ACTIVE	VSON-HR	RLT	7	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	PD5Q	Samples
TPS62086RLTR	ACTIVE	VSON-HR	RLT	7	3000	RoHS & Green	Call TI | MATTE SN	Level-1-260C-UNLIM	-40 to 125	PD4Q	Samples
TPS62086RLTT	ACTIVE	VSON-HR	RLT	7	250	RoHS & Green	Call TI | MATTE SN	Level-1-260C-UNLIM	-40 to 125	PD4Q	Samples
TPS62087RLTR	ACTIVE	VSON-HR	RLT	7	3000	RoHS & Green	Call TI | MATTE SN	Level-1-260C-UNLIM	-40 to 125	PD3Q	Samples
TPS62087RLTT	ACTIVE	VSON-HR	RLT	7	250	RoHS & Green	Call TI | MATTE SN	Level-1-260C-UNLIM	-40 to 125	PD3Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

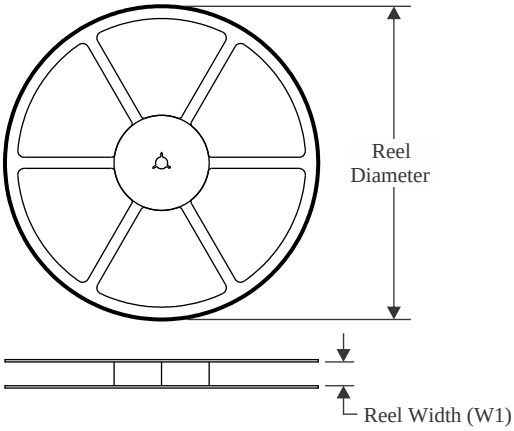
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

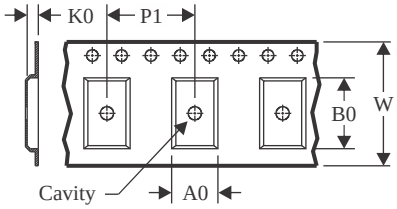
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

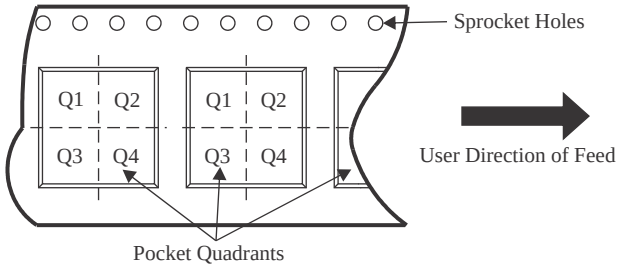


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

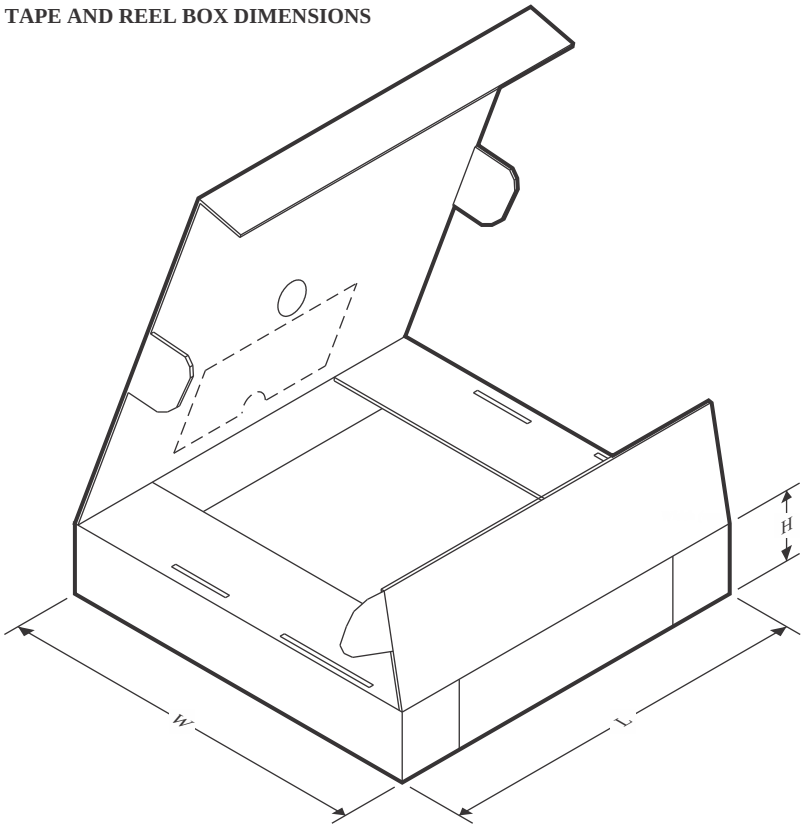
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62085RLTR	VSON-HR	RLT	7	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62085RLTT	VSON-HR	RLT	7	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

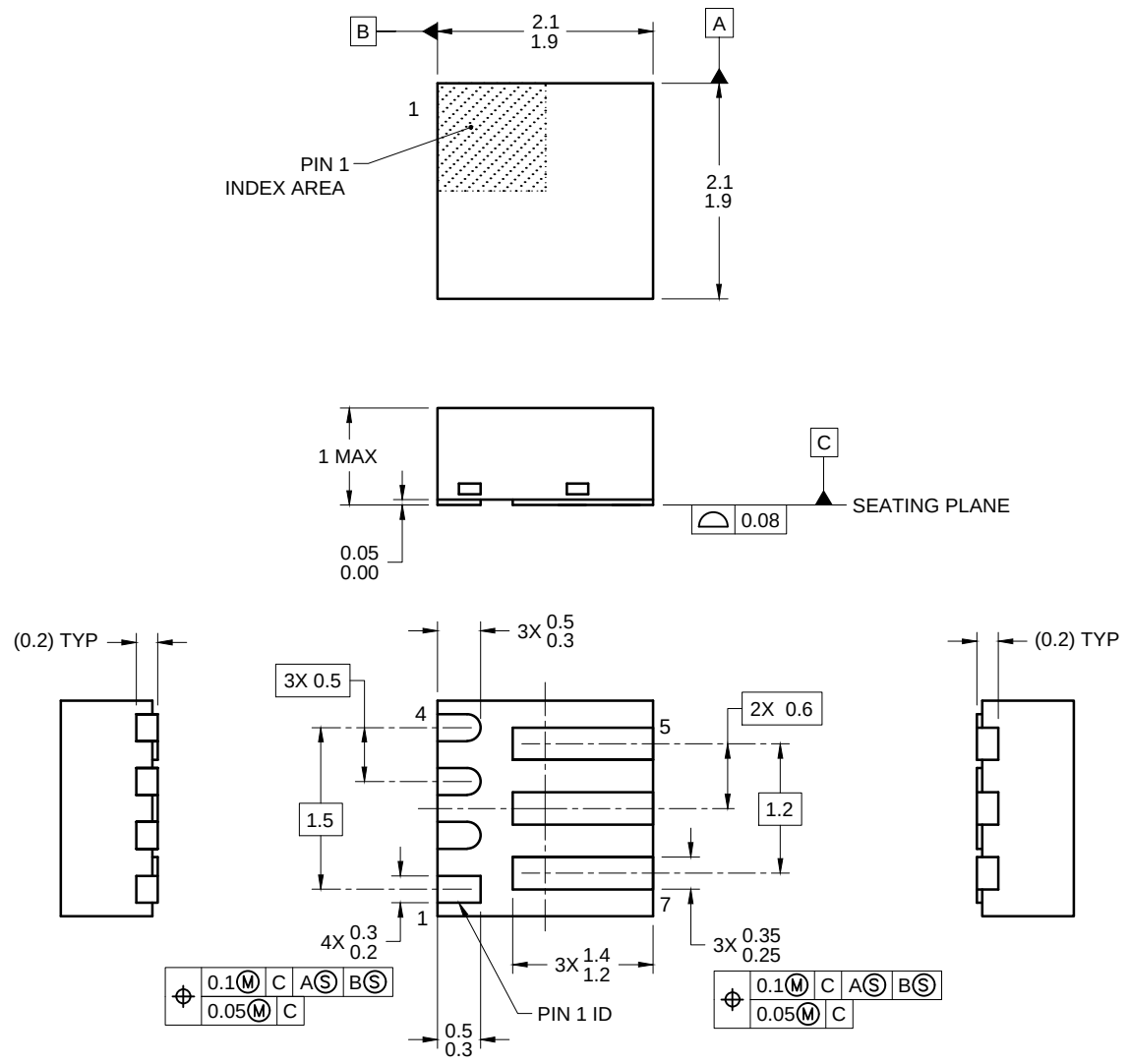
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62085RLTR	VSON-HR	RLT	7	3000	210.0	185.0	35.0
TPS62085RLTT	VSON-HR	RLT	7	250	210.0	185.0	35.0

PACKAGE OUTLINE

RLT0007A

VSON - 1 mm max height

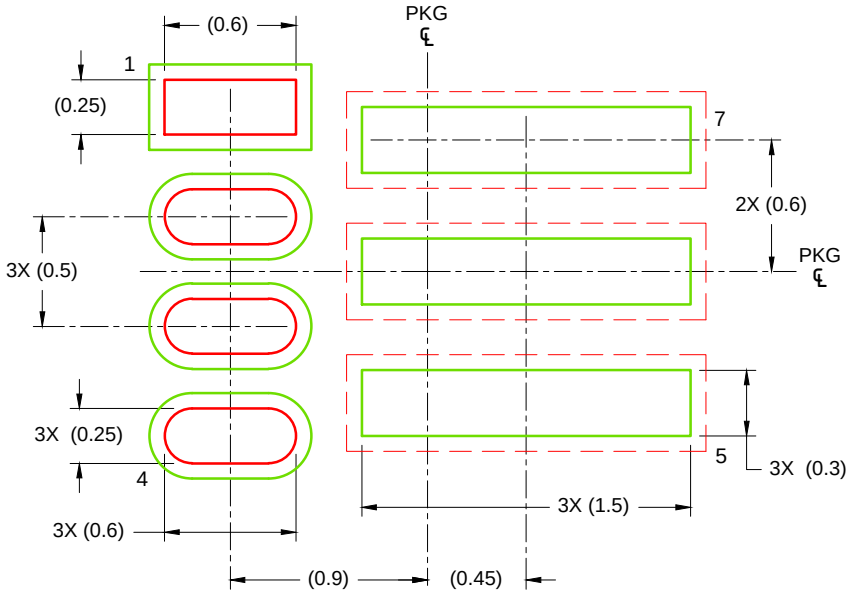
PLASTIC SMALL OUTLINE - NO LEAD



4220429/A 09/2014

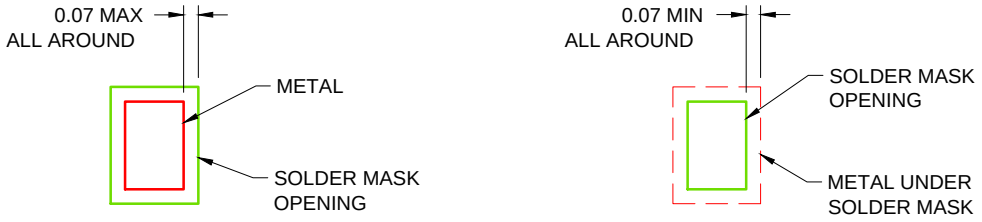
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



NON SOLDER MASK
DEFINED
PADS 1 - 4

SOLDER MASK
DEFINED
PADS 5 - 7

SOLDER MASK DETAILS

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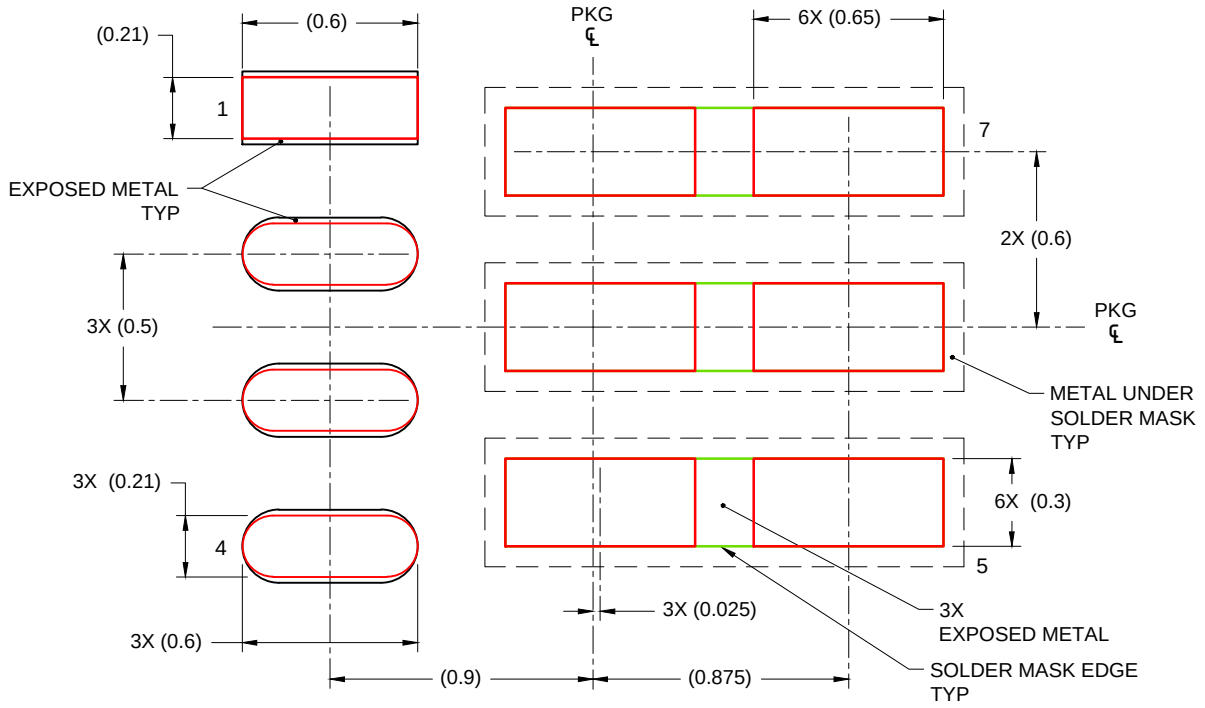
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias should not be placed on soldering pads unless they are plugged or plated shut.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR ALL EXPOSED PADS
85% PRINTED SOLDER COVERAGE BY AREA
SCALE: 40X

4220429/A 09/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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