TPS552892-Q1 車載用の 36V、8A で完全に統合された昇降圧コンバータ

1 特長

- AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40°C～+125°Cの動作時周囲温度範囲
- 広い入出力電圧範囲
  - 広い入力電圧範囲:3.0V～36V
  - プログラム可能な出力電圧範囲:0.8V～22V
  - ±1% の基準電圧精度
  - ケーブルの電圧ドループに対する可変出力電圧補償
  - ±5% 精度の出力電流監視
- 全負荷範囲にわたって高効率を実現
  - V_{IN} = 12V、V_{OUT} = 20V、I_{OUT} = 3A で 96% の効率
  - 軽負荷時の PFM および FPWM モードをプログラム可能
- 周波数干渉とクロストークを回避
  - クロック同期 (オプション)
  - プログラム可能なスイッチング周波数:200kHz～2.2MHz
- EMI 低減
  - プログラム可能な拡散スペクトラム (オプション)
  - リードレス・パッケージ
- 豊富な保護機能
  - 出力過電圧保護
  - ヒカップ・モードによる出力短絡保護
  - サーマル・シャットダウン保護機能
  - 8A の平均インダクタ電流制限
- 小型ソリューション・サイズ
  - 最大 2.2MHz のスイッチング周波数
  - 3.0mm × 5.0mm の HotRod™ QFN パッケージ

2 アプリケーション

- 先進運転支援システム (ADAS)
- ワイヤレス・チャージャ
- 車載用インフォテインメントおよびクラスタ

3 説明

TPS552892-Q1 は、バッテリ電圧やアダプタ電圧を複数の電源レール向けに変換するために最適化された、同期整流昇降圧コンバータです。TPS552892-Q1 は 4 個の MOSFET スイッチを内蔵しており、多様なアプリケーション向けのコンパクトなソリューションを実現します。TPS552892-Q1 は最大で 36V の入力電圧に対応できます。TPS552892-Q1 は、昇圧モードでの動作時に 12V 入力から 60W の供給が可能です。9V の入力電圧からは 45W を供給できます。

TPS552892-Q1 は平均電流モード制御方式を採用しています。スイッチング周波数は、外付け抵抗で 200kHz～2.2MHz に設定することも、外部クロックに同期させることもできます。TPS552892-Q1 は、ピーク EMI を最小限に抑えるための拡散スペクトラム・オプション機能も備えています。

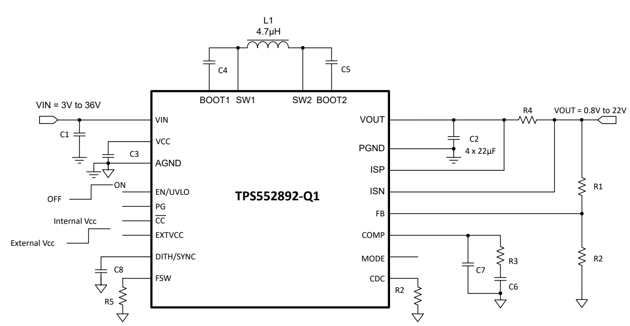
TPS552892-Q1 には、出力過電圧保護、平均インダクタ電流制限、サイクル単位のピーク電流制限、出力短絡からの保護機能があります。また TPS552892-Q1 は、持続的な過負荷状態での出力電流制限およびヒカップ・モード保護オプション機能により、安全な動作を保証します。

TPS552892-Q1 はスイッチング周波数が高いため、小型のインダクタとコンデンサを使用できます。本デバイスは、3.0mm × 5.0mm の QFN パッケージで供給されます。

製品情報

部品番号	パッケージ (1)	本体サイズ
TPS552892-Q1	VQFN-HR	3.0mm × 5.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

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4 Revision History

DATE	REVISION	NOTES
April 2023	*	Initial release

5 Pin Configuration and Functions

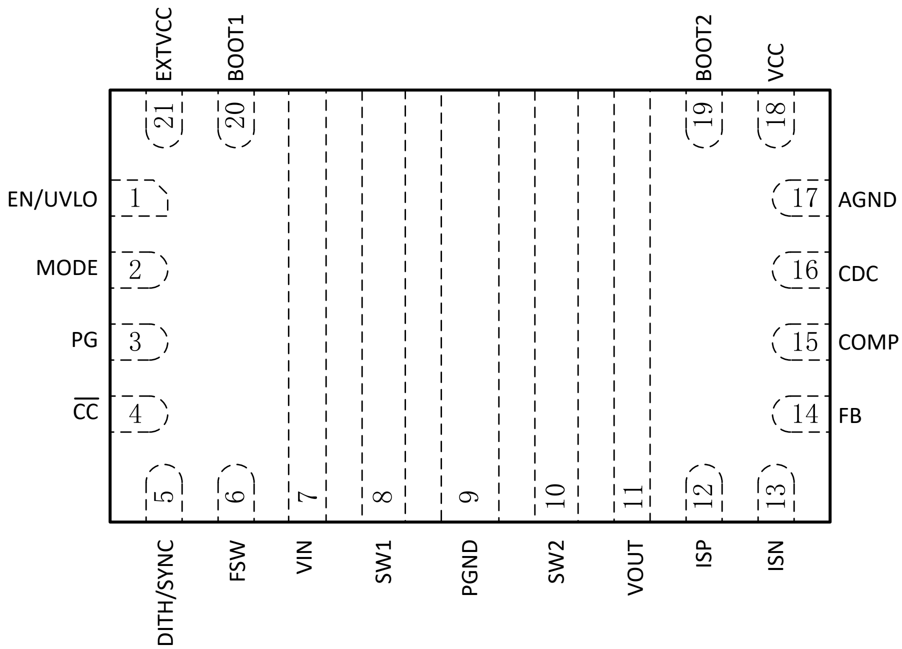


図 5-1. 21-pin VQFN-HR, RYQ Package (Transparent Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN/UVLO	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at the EN/UVLO pin is above the logic high voltage of 1.15 V, this pin acts as programmable UVLO input with 1.23-V internal reference.
2	MODE	I	Mode selection pin in light load condition. When it is connected to logic high voltage, the device works in forced PWM mode. When it is connected to logic low voltage, the device works in auto PFM mode. This pin can not be float in application.
3	PG	O	Power good indication open drain output. When the output voltage is above 95% of the setting output voltage, this pin outputs high impedance. When the output voltage is below 90% of the setting output voltage, this pin outputs low level
4	$\overline{CC}$	O	Constant current output indication open drain output. When output current limit is triggered, this pin outputs low level.
5	DITH/SYNC	I	Dithering frequency setting and synchronous clock input. Use a capacitor between this pin and ground to set the dithering frequency. When this pin is short to ground or pulled above 1.2 V, there is no dithering function. An external clock can be applied at this pin to synchronize the switching frequency.
6	FSW	I	The switching frequency is programmed by a resistor between this pin and the AGND pin.
7	VIN	PWR	Input of the buck-boost converter.
8	SW1	PWR	The switching node pin of the buck side. It is connected to the drain of the internal buck low-side power MOSFET and the source of internal buck high-side power MOSFET.
9	PGND	PWR	Power ground of the IC.
10	SW2	PWR	The switching node pin of the boost side. It is connected to the drain of the internal boost low-side power MOSFET and the source of internal boost high-side power MOSFET.
11	VOUT	PWR	Output of the buck-boost converter.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
12	ISP	I	Positive input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function.
13	ISN	I	Negative input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function.
14	FB	I	Connect to the center of a resistor divider to program the output voltage
15	COMP	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
16	CDC	O	Voltage output proportional to the sensed voltage between the ISP pin and the ISN pin. Use a resistor between this pin and AGND to increase the output voltage to compensate voltage droop across the cable caused by the cable resistance.
17	AGND	-	Signal ground of the IC.
18	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 4.7 µF is required between this pin and the AGND pin.
19	BOOT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 µF must be connected between this pin and the SW2 pin.
20	BOOT1	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 µF must be connected between this pin and the SW1 pin.
21	EXTVCC	I	Select the internal LDO or external 5V for VCC. When it is connected to logic high voltage or is left floating, select the internal LDO. When it is connected to logic low voltage, select the external 5V for VCC.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage range at terminals [(2)]	VIN, SW1	–0.3	42	V
	BOOT1	SW1–0.3	SW1+6	V
	VCC, PG, $\overline{CC}$, FSW, COMP, FB, MODE, CDC, DITH/SYNC, EXTVCC	–0.3	6	V
	VOUT, SW2, ISP, ISN	–0.3	25	V
	EN	-0.3	20	V
	BOOT2	SW2–0.3	SW2+6	V
	PG, $\overline{CC}$, FSW, COMP, FB, MODE, CDC, DITH/SYNC, EXTVCC	–0.3	VCC+0.3	V
T_J	Operating Junction, T_J [(3)]	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins[(2)]	±500	
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins[(2)]	±750	V

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	3.0		36	V
V_{OUT}	Output voltage range	0.8		22	V
L	Effective inductance range	1	4.7	10	µH
C_{IN}	Effective input capacitance range	4.7	22		µF
C_{OUT}	Effective output capacitance range	10	100	1000	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		RYQ (VQFN)	RYQ (VQFN)	UNIT
		21 PINS	21 PINS	
		Standard	EVM [(2)]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	27.5	°C/W

THERMAL METRIC[1]		RYQ (VQFN) 21 PINS Standard	RYQ (VQFN) 21 PINS EVM [2]	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.3	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.4	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.2	11.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS552892EVM-111, 4-layer, 2-oz/1-oz/1-oz/2-oz copper 91-mmx66-mm PCB.

6.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		3.0		36	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} rising	2.8	2.9	3.0	V
		V_{IN} falling	2.6	2.65	2.7	V
I_Q	Quiescent current into VIN pin	IC enabled, no load, no switching. V_{IN} = 3.0V to 24V, V_{OUT} = 0.8V, V_{FB} = V_{REF} + 0.1V, R_{FSW}=100kΩ, Tj up to 125°C		760	860	µA
	Quiescent current into VOUT pin	IC enabled, no load, no switching, V_{IN} = 3.0V, V_{OUT} = 3V to 20V, V_{FB} = V_{REF} + 0.1V, R_{FSW}=100kΩ, Tj up to 125°C		760	860	µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 3.0V to 14V, Tj up to 125°C, EXTVCC pin floating		0.8	3	µA
V_{CC}	Internal regulator output	I_{VCC} = 50mA, V_{IN} = 8V, V_{OUT} = 20V	5.05	5.2	5.45	V
EN/UVLO						
V_{EN_H}	EN Logic high threshold	V_{CC} = 3.0V to 5.5V			1.15	V
V_{EN_L}	EN Logic low threshold	V_{CC} = 3.0V to 5.5V	0.4			V
V_{EN_HYS}	Enable threshold hysteresis	V_{CC} = 3.0V to 5.5V	0.04			V
V_{UVLO}	UVLO rising threshold at the EN/UVLO pin	V_{CC} = 3.0V to 5.5V	1.20	1.23	1.26	V
V_{UVLO_HYS}	UVLO threshold hysteresis	V_{CC} = 3.0V to 5.5V		10		mV
I_{UVLO}	Sourcing current at the EN/UVLO pin	V_{UVLO} = 1.3V	4.4	5	5.6	µA
OUTPUT						
V_{OUT}	Output voltage range		0.8		22	V
V_{OVP}	Output overvoltage protection threshold		22.5	23.5	24.5	V
V_{OVP_HYS}	Over voltage protection hysteresis			1		V
I_{FB_LKG}	Leakage current at FB pin	Tj up to 125°C			100	nA
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{OUT} = 20V, V_{SW2} = 0V, Tj up to 125°C		1	20	µA
REFERENCE VOLTAGE						
V_{REF}	Reference voltage at the FB pin		1.188	1.2	1.212	V
POWER SWITCH						

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Low-side MOSFET on resistance on buck side	V_{OUT} = 20V, V_{CC}=5.2V		22		mΩ
	High-side MOSFET on resistance on buck side	V_{OUT} = 20V, V_{CC}=5.2V		14		mΩ
	Low-side MOSFET on resistance on boost side	V_{OUT} = 20V, V_{CC}=5.2V		11		mΩ
	High-side MOSFET on resistance on boost side	V_{OUT} = 20V, V_{CC}=5.2V		11		mΩ
INTERNAL CLOCK						
f_{SW}	Switching frequency	R_{FSW} =100k	180	200	220	kHz
		R_{FSW} =8.4k	2000	2200	2400	kHz
t_{OFF_min}	Min. off time	Boost mode		90	145	ns
t_{ON_min}	Min. on time	Buck mode		90	130	ns
V_{FSW}	Voltage at FSW pin			1		V
CURRENT LIMIT						
I_{LIM_AVG}	Average inductor current limit	TPS552892-Q1, V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz, V_{CC} = 5.2V	7	8	9	A
$I_{LIM\_PK\_H}$	Peak inductor current limit at high side	TPS552892-Q1, V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz		13		A
$I_{LIM\_PK\_L}$	Peak inductor current limit at low side	TPS552892-Q1, V_{IN} = 8V, V_{OUT} = 20V, F_{SW} = 400kHz		12		A
V_{SNS}	Current loop regulation voltage between ISP and ISN pin		48	50	52	mV
CABLE VOLTAGE DROP COMPENSATION						
V_{CDC}	Voltage at the CDC pin	R_{CDC} = 20kΩ or floating, $V_{ISP} – V_{ISN}$ = 50mV	0.95	1	1.05	V
		R_{CDC} = 20kΩ or floating, $V_{ISP} – V_{ISN}$ = 2mV		40	75	mV
I_{FB_CDC}	FB pin sinking current	External output feedback, R_{CDC} = 20kΩ, $V_{ISP} – V_{ISN}$ = 50mV	7.23	7.5	7.87	µA
		External output feedback, R_{CDC} = 20kΩ, $V_{ISP} – V_{ISN}$ = 0mV		0	0.3	µA
		External output feedback, R_{CDC} = floating, $V_{ISP} – V_{ISN}$ = 50mV		0	0.3	µA
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 400mV, V_{COMP}=1.5V, V_{CC}=5V		20		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 400mV, V_{COMP}=1.5V, V_{CC}=5V		60		µA
V_{CCLPH}	High clamp voltage at the COMP pin	FPWM mode, V_{OUT} = 1.8V to 22V		1.3		V
V_{CCLPL}	Low clamp voltage at the COMP pin	FPWM mode		0.7		V
G_{EA}	Error amplifier transconductance			190		µA/V
SOFT START						
t_{SS}	Soft-start time		2.5	3.6	5	ms
SPREAD SPECTRUM						
I_{DITH_CHG}	Dithering charge current	$V_{DITH/SYNC}$ = 1.0V; R_{FSW}=49.9kΩ; voltage rising from 0.9V		2		µA
I_{DITH_DIS}	Dithering discharge current	$V_{DITH/SYNC}$ = 1.0V; R_{FSW}=49.9kΩ; voltage falling from 1.1V		2		µA
V_{DITH_H}	Dither high threshold			1.07		V

T_J = -40°C to 125°C, V_{IN} = 12 V and V_{OUT} = 20 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DITH_L}	Dither low threshold			0.93		V
SYNCHRONOUS CLOCK						
V_{SNYC_H}	Sync clock high voltage threshold				1.2	V
V_{SYNC_L}	Sync clock low voltage threshold		0.4			V
t_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
HICCUP						
t_{HICCUP}	Hiccup off time			76		ms
MODE						
V_{MODE}	MODE logic high threshold	V_{CC} = 3V to 5.5V			1.2	V
V_{MODE}	MODE logic low threshold	V_{CC} = 3V to 5.5V	0.4			V
EXTVCC						
V_{EXTVCC}	EXTVCC Logic high threshold	V_{CC} = 3V to 5.5V			1.2	V
V_{EXTVCC}	EXTVCC Logic Low threshold	V_{CC} = 3V to 5.5V	0.4			V
Power Good						
I_{PG_H}	Leakage current into PG pin when outputting high impedance	V_{PG} = 5V			100	nA
V_{PG_L}	Output low voltage range of the PG pin	Sinking 4mA current		0.1	0.2	V
Current Limit Indication						
$I_{\overline{CC}\_H}$	Leakage current into $\overline{CC}$ pin when outputting high impedance	$V_{\overline{CC}}$ = 5 V			100	nA
$V_{\overline{CC}\_L}$	Output low voltage range of the $\overline{CC}$ pin	Sinking 4-mA current		0.1	0.2	V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below Tsd		20		°C

6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C, f_{SW} = 400 kHz, unless otherwise noted.

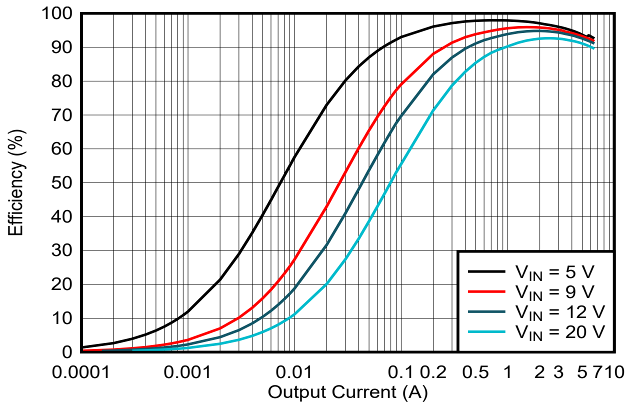


図 6-1. Efficiency vs Output Current, V_{OUT} = 5 V, FPWM

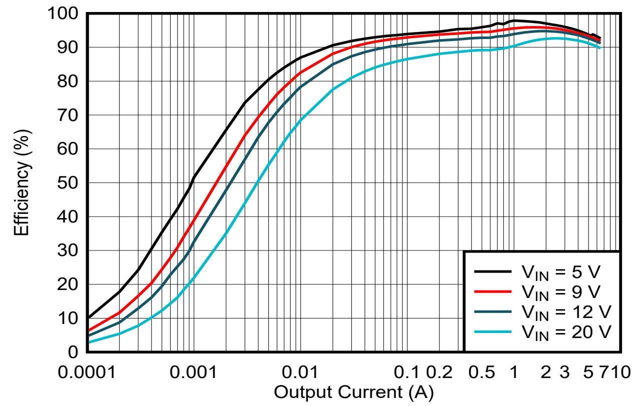


図 6-2. Efficiency vs Output Current, V_{OUT} = 5 V, PFM

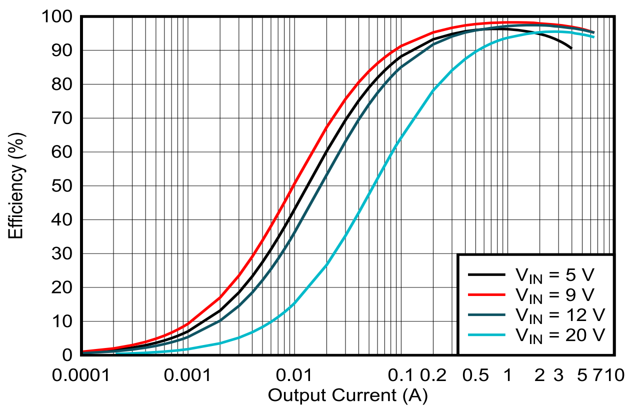


図 6-3. Efficiency vs Output Current, V_{OUT} = 9 V, FPWM

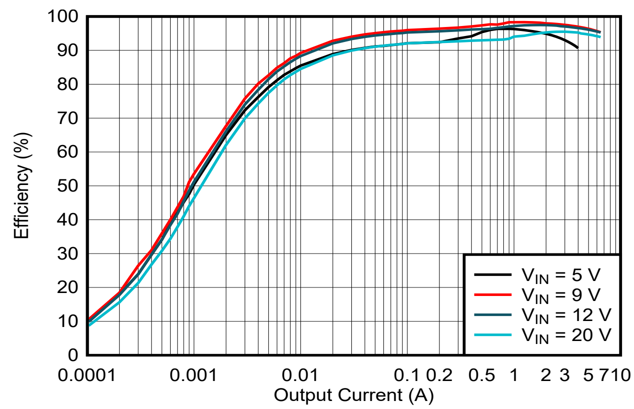


図 6-4. Efficiency vs Output Current, V_{OUT} = 9 V, PFM

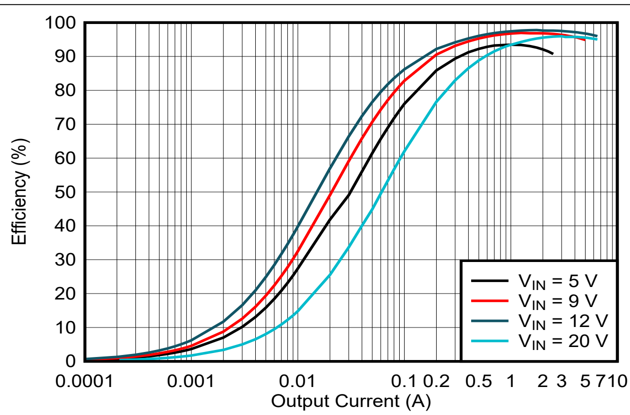


図 6-5. Efficiency vs Output Current, V_{OUT} = 12 V, FPWM

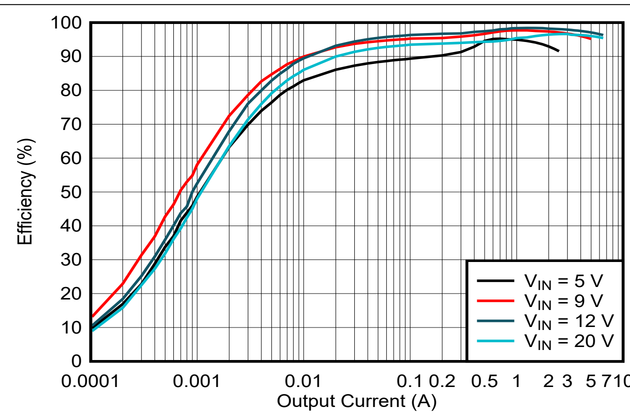


図 6-6. Efficiency vs Output Current, V_{OUT} = 12 V, PFM

6.6 Typical Characteristics (continued)

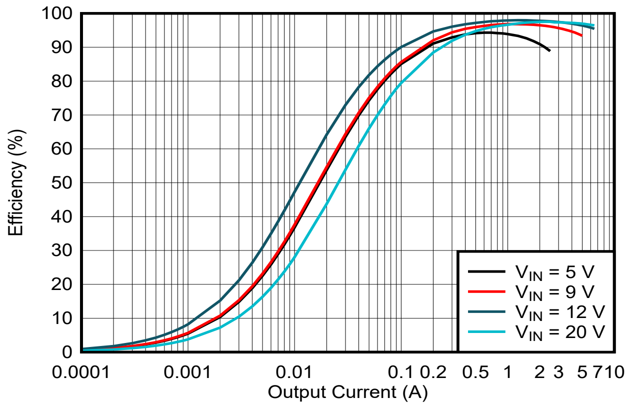


図 6-7. Efficiency vs Output Current, V_{OUT} = 15 V, FPWM

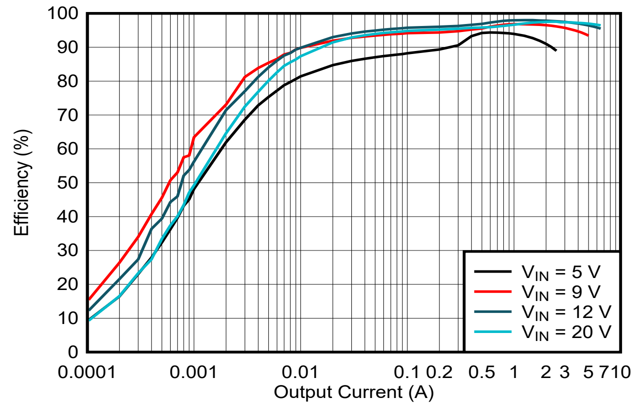


図 6-8. Efficiency vs Output Current, V_{OUT} = 15 V, PFM

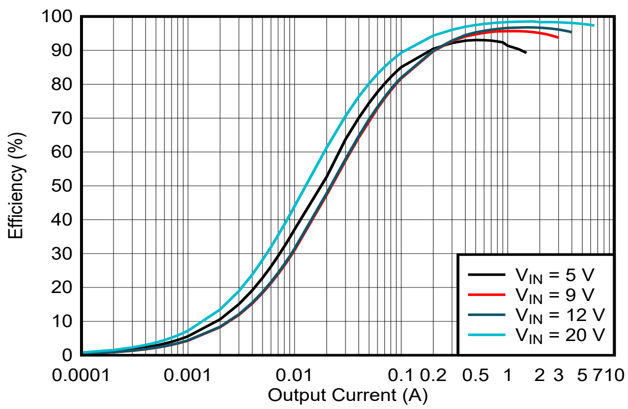


図 6-9. Efficiency vs Output Current, V_{OUT} = 20 V, FPWM

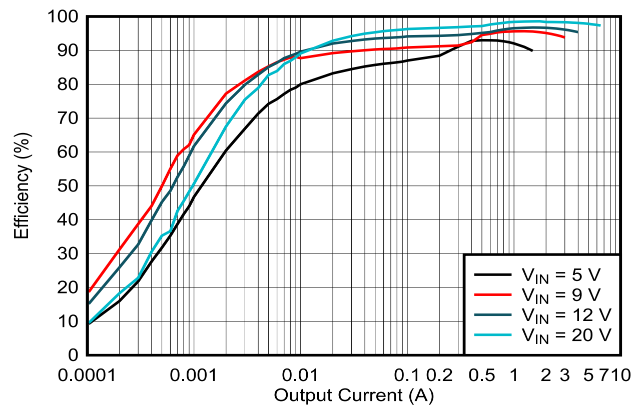


図 6-10. Efficiency vs Output Current, V_{OUT} = 20 V, PFM

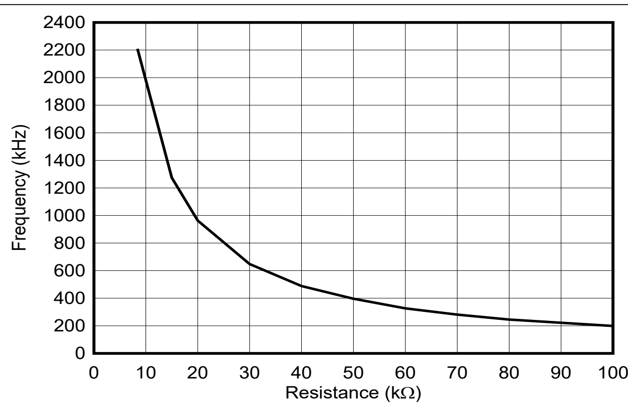


図 6-11. Switching Frequency vs Setting Resistance

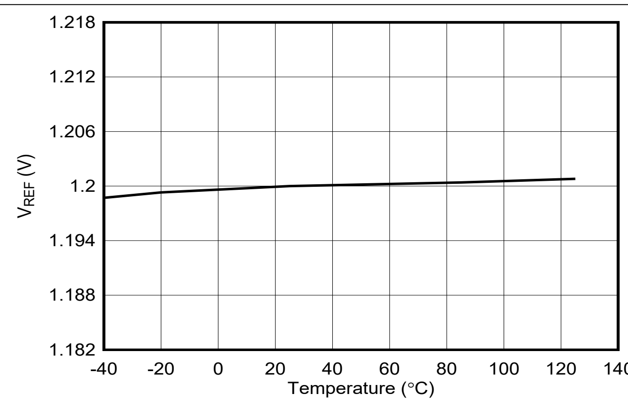


図 6-12. Reference Voltage vs Temperature (V_{REF} = 1.2 V)

6.6 Typical Characteristics (continued)

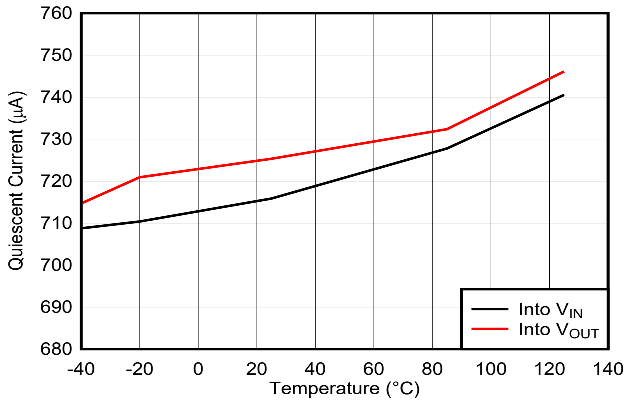


図 6-13. Quiescent Current vs Temperature

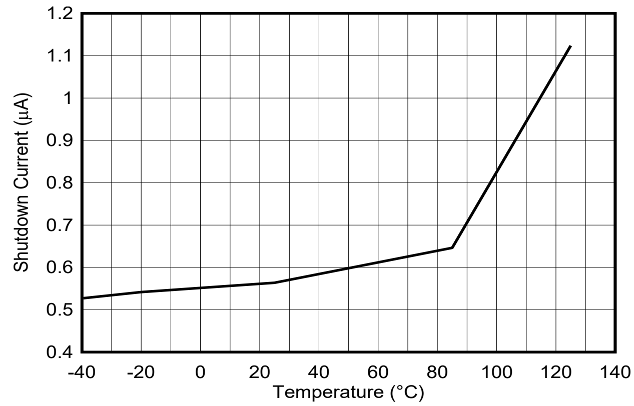


図 6-14. Shutdown Current vs Temperature

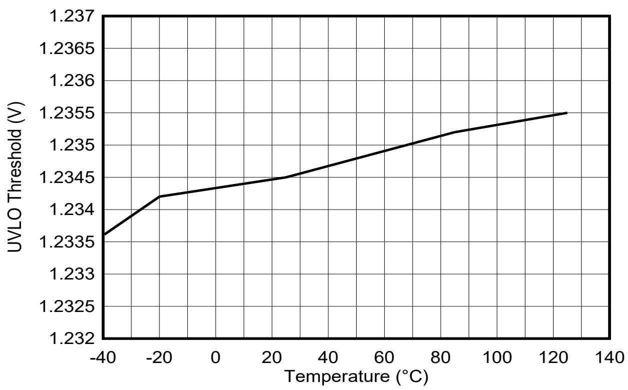


図 6-15. ENABLE/UVLO Rising Threshold vs Temperature

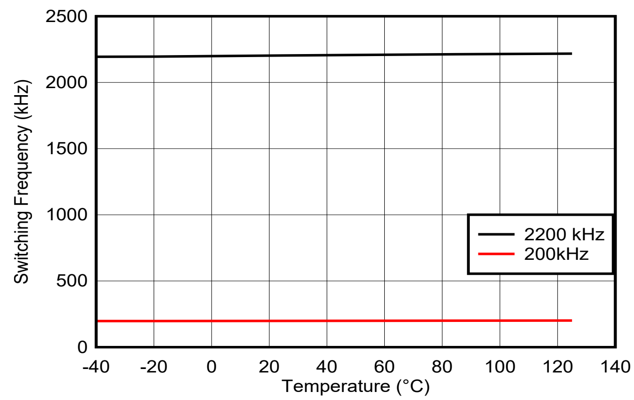


図 6-16. Switching Frequency vs Temperature

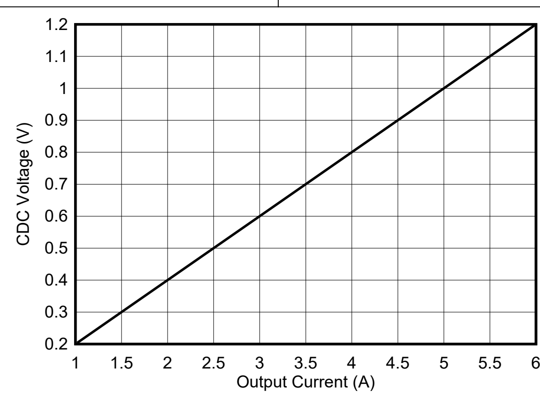


図 6-17. CDC Voltage vs Output Current with R_{SENSE} = 10 mΩ

7 Detailed Description

7.1 Overview

The TPS552892-Q1 is an 8-A buck-boost DC-to-DC converter with the four MOSFETs integrated. The TPS552892-Q1 can operate over a wide range of 3.0-V to 36-V input voltage and an output voltage of 0.8 V to 22 V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the set output voltage. The TPS552892-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS552892-Q1 operates in one-cycle buck and one-cycle boost mode alternately.

The TPS552892-Q1 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

An internal oscillator can be configured to operate over a wide range of frequency from 200 kHz to 2.2 MHz. The internal oscillator can also synchronize to an external clock applied to the DITH/SYNC pin. To minimize EMI, the TPS552892-Q1 can dither the switching frequency at ±7% of the set frequency.

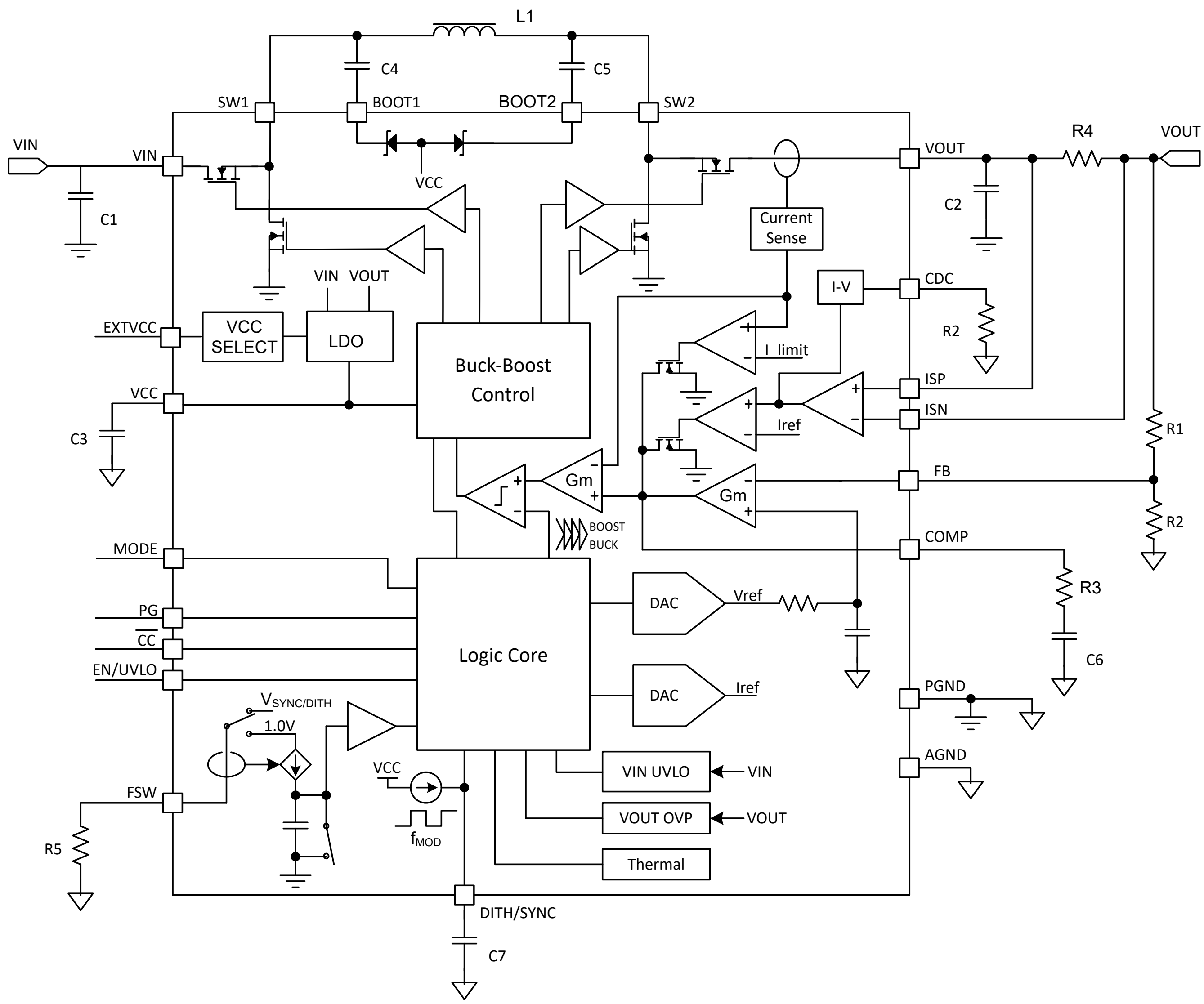
The TPS552892-Q1 works in fixed-frequency PWM mode at moderate to heavy load currents. In light load condition, the TPS552892-Q1 can be configured to automatically transition to PFM mode or be forced in PWM mode.

The TPS552892-Q1 provides average inductor current limit of 8 A typically. In addition, it provides cycle-by-cycle peak inductor current limit during transient to protect the device against overcurrent condition beyond the capability of the device.

A precision voltage threshold of 1.23 V with 5-μA sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side FETs to prevent damage to the devices powered by the TPS552892-Q1.

The device provides hiccup mode option to reduce the heating in the power components when output short circuit happens. The TPS552892-Q1 turns off for 76 ms and restarts at soft start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC Power Supply

An internal LDO to supply the TPS552892-Q1 outputs regulated 5.2-V voltage at the VCC pin. When V_{IN} is less than V_{OUT}, the internal LDO selects the power supply source by comparing V_{IN} to a rising threshold of 6.2 V with 0.3-V hysteresis. When V_{IN} is higher than 6.2 V, the supply for LDO is V_{IN}. When V_{IN} is lower than 5.9 V, the supply for LDO is V_{OUT}. When V_{OUT} is less than V_{IN}, the internal LDO selects the power supply source by comparing V_{OUT} to a rising threshold of 6.2 V with 0.3-V hysteresis. When V_{OUT} is higher than 6.2 V, the supply for LDO is V_{OUT}. When V_{OUT} is lower than 5.9 V, the supply for LDO is V_{IN}. 表 7-1 shows the supply source selection for the internal LDO.

表 7-1. V_{CC} Power Supply Logic

V_{IN}	V_{OUT}	INPUT for V_{CC} LDO
V_{IN} > 6.2 V	$V_{OUT} > V_{IN}$	V_{IN}
V_{IN} < 5.9 V	$V_{OUT} > V_{IN}$	V_{OUT}
$V_{IN} > V_{OUT}$	V_{OUT} > 6.2 V	V_{OUT}

表 7-1. V_{CC} Power Supply Logic (continued)

V_{IN}	V_{OUT}	INPUT for V_{CC} LDO
$V_{IN} > V_{OUT}$	$V_{OUT} < 5.9$ V	V_{IN}

7.3.2 EXTVCC Power Supply

To minimize the power dissipation of the internal LDO when both input voltage and output voltage are high, an external 5-V power source can be applied at the VCC pin to supply the TPS552892-Q1. The external 5-V power supply must have at least 100-mA output current capability and must be within the 4.75-V to 5.5-V regulation range. When the EXTVCC pin is connected to logic low, the device selects the external power supply to supply the device through VCC pin. When the EXTVCC pin is connected to logic high or is left floating, the device selects internal LDO.

7.3.3 Input Undervoltage Lockout

When the input voltage is below 2.6 V, the TPS552892-Q1 is disabled. When the input voltage is above 3 V, the TPS552892-Q1 can be enabled by pulling the EN pin to a high voltage above 1.3 V.

7.3.4 Enable and Programmable UVLO

The TPS552892-Q1 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3 V and the EN/UVLO pin is pulled above 1.15 V but less than the enable UVLO threshold of 1.23 V, the TPS552892-Q1 is enabled but still in standby mode. The TPS552892-Q1 starts to detect the MODE pin logic status.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23 V, the TPS552892-Q1 is enabled for switching operation. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in 図 7-1, the turnon threshold is calculated using 式 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times (1 + \frac{R1}{R2}) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 1.23 V at the EN/UVLO pin

The hysteresis between the UVLO turnon threshold and turnoff threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by the Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

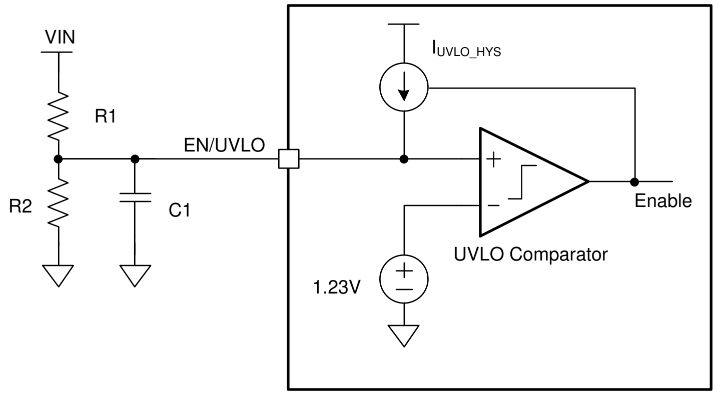


図 7-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in 図 7-2. The EN logic high level must be greater than enable threshold plus the V_{th} of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.

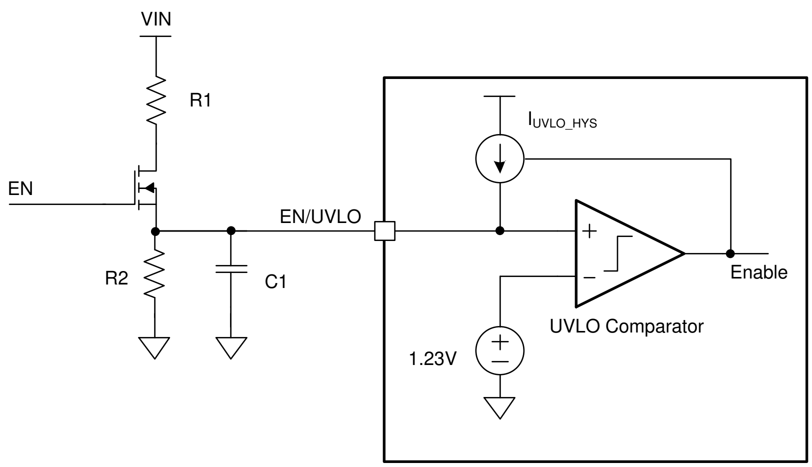


図 7-2. Logic Enable and Programmable UVLO

7.3.5 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPS552892-Q1 starts to ramp up the output voltage by ramping an internal reference voltage from 0 V to 1.2V within typical 3.6 ms.

7.3.6 Shutdown

When the EN/UVLO pin voltage is pulled below 0.4 V, the TPS552892-Q1 is in shutdown mode, and all functions are disabled.

7.3.7 Switching Frequency

The TPS552892-Q1 uses a fixed frequency average current control scheme. The switching frequency is between 200 kHz and 2.2 MHz set by placing a resistor at the FSW pin. An internal amplifier holds this pin at a fixed voltage of 1 V. The setting resistance is between maximum of 100 kΩ and minimum of 8.4 kΩ. Use Equation 3 to calculate the resistance by a given switching frequency.

$$f_{SW} = \frac{1000}{0.05 \times R_{FSW} + 35} \text{ (MHz)} \tag{3}$$

where

- R_{FSW} is the resistance at the FSW pin (Ω)

For noise-sensitive applications, the TPS552892-Q1 can be synchronized to an external clock signal applied to the DITH/SYNC pin. The duty cycle of the external clock is recommended in the range of 30% to 70%. A resistor also must be connected to the FSW pin when the TPS552892-Q1 is switching by the external clock. The external clock frequency at the DITH/SYNC pin must have lower than 0.4-V low level voltage and must be within ±30% of the corresponding frequency set by the resistor. 図 7-3 is a recommended configuration.

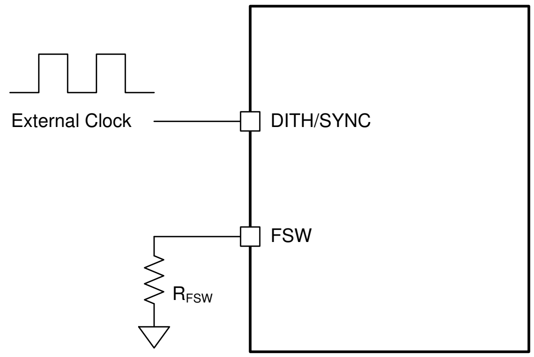


図 7-3. External Clock Configuration

7.3.8 Switching Frequency Dithering

The TPS552892-Q1 provides an optional switching frequency dithering that is enabled by connecting a capacitor from the DITH/SYNC pin to ground. 図 7-4 illustrates the dithering circuit. By charging and discharging the capacitor, a triangular waveform centered at 1 V is generated at the DITH/SYNC pin. The triangular waveform modulates the oscillator frequency by ±7% of the nominal frequency set by the resistance at the FSW pin. The capacitance at the DITH/SYNC pin sets the modulation frequency. A small capacitance modulates the oscillator frequency at a fast rate than a large capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate normally is below 1 kHz. Equation 4 calculates the capacitance required to set the modulation frequency, F_{MOD}.

$$C_{DITH} = \frac{1}{2.8 \times R_{FSW} \times F_{MOD}} \ (F) \tag{4}$$

where

- R_{FSW} is the switching frequency setting resistance (Ω) at the FSW pin
- F_{MOD} is the modulation frequency (Hz) of the dithering

Connecting the DITH/SYNC pin below 0.4 V or above 1.2 V disables switching frequency dithering. The dithering function also is disabled when an external synchronous clock is used.

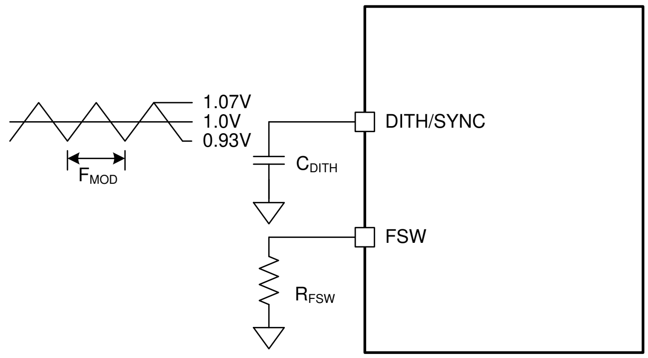


図 7-4. Switching Frequency Dithering

7.3.9 Inductor Current Limit

The TPS552892-Q1 implements both peak current and average inductor current limit. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 8 A (typical).

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against over current condition beyond the capability of the device.

7.3.10 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by V_{CC} through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPS552892-Q1 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to V_{CC} so that the high-side MOSFET remains on.

7.3.11 Output Voltage Setting

TPS552892-Q1 output voltage is configured with feedback resistors as shown in 図 7-5, use 式 5 to calculate the output voltage with the reference voltage at the FB pin.

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}) \tag{5}$$

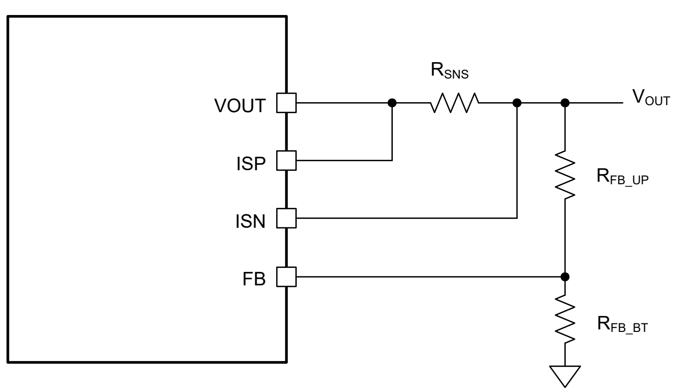


図 7-5. Output Voltage Setting

TI recommends using 100 kΩ for the up resistor R_{FB_UP}. The reference voltage V_{REF} is 1.2 V.

7.3.12 Output Current Monitoring and Cable Voltage Droop Compensation

The TPS552892-Q1 outputs a voltage at the CDC pin proportional to the sensed voltage across a output current sensing resistor between the ISP pin and the ISN pin. 式 6 shows the exact voltage at the CDC pin related to the sensed output current.

$$V_{CDC} = 20 \times (V_{ISP} - V_{ISN}) \tag{6}$$

To compensate the voltage droop across a cable from the output of the USB port to its powered device, the TPS552892-Q1 can lift its output voltage in proportion to the load current by placing a resistor between the CDC pin and AGND pin.

The output voltage rises in proportion to the current sourcing from the CDC pin through the resistor at the CDC pin. It is recommended to use 100-kΩ resistance for the up resistor of the feedback resistor divider. 式 7 shows the output voltage rise related to the sensed output current, the resistance at the CDC pin, and the up resistor of the output voltage feedback resistor divider.

$$V_{OUT\_CDC} = 3 \times R_{FB\_UP} \times (\frac{V_{ISP} - V_{ISN}}{R_{CDC}}) \tag{7}$$

where

- R_{FB_UP} is the up resistor of the resistor divider between the output and the FB pin
- R_{CDC} is the resistor at the CDC pin

When RFB_UP is 100 kΩ, the output voltage rise versus the sensed output current and the resistor at the CDC pin is shown in 図 7-6.

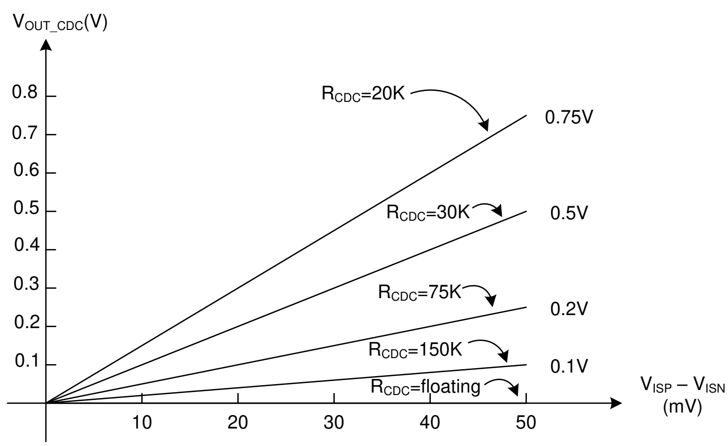


図 7-6. Output Voltage Rise versus Output Current

7.3.13 Output Current Limit

The output current limit is programmable by placing a current sensing resistor between the ISP pin and ISN pin. The voltage limit between the ISP pin and the ISN pin is set to 50 mV. Thus a smaller resistance gets higher current limit and a bigger resistance gets lower current limit.

Connecting the ISP and the ISN pin together to the VOUT pin disables the output current limit because the sensed voltage is always zero.

7.3.14 Overvoltage Protection

The TPS552892-Q1 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 23.5 V typically, the TPS552892-Q1 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.3.15 Output Short Circuit Protection

In addition to the average inductor current limit, the TPS55292-Q1 implements the output short-circuit protection by entering hiccup mode. After soft start-up time of 3.6 ms, the TPS552892-Q1 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current hitting the set limit and the output voltage below 0.8 V for 2 ms, the TPS552892-Q1 shuts down the switching for 76 ms (typical) and then repeats the soft start for 3.6 ms. The hiccup mode helps reduce the total power dissipation on the TPS552892-Q1 in the output short-circuit or overcurrent condition.

7.3.16 Power Good

The TPS552892-Q1 integrates a power-good function. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply like VCC. The PG pin goes high after VOUT reaches 95% of the target output voltage. When the output voltage drops below 90% of the target output voltage, the PG pin goes low.

7.3.17 Constant Current Output Indication

The TPS552892-Q1 integrates a constant current output indication function. It consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply like VCC. The $\overline{CC}$ pin goes low with a 128us delay time after the voltage between the ISP pin and the ISN pin reaches to 50mV.

7.3.18 Thermal Shutdown

The TPS552892-Q1 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

7.4 Device Functional Modes

In light load condition, the TPS552892-Q1 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss thus it gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency but the efficiency becomes lower than that of PFM mode.

7.4.1 PWM Mode

When the MODE pin is connected to logic high, the TPS552892-Q1 works in FPWM mode and the switching frequency is unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that might be caused by low switching frequency in light load condition.

7.4.2 Power Save Mode

The TPS552892-Q1 improves the efficiency at light load condition with PFM mode. When the MODE pin is connected to logic low, the TPS552892-Q1 can work in PFM mode at light load condition. When the TPS552892-Q1 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the switch-off time. When the TPS552892-Q1 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPS552892-Q1 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPS552892-Q1 resumes switching until the output voltage drops. Thus PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

8 Application and Implementation

注

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8.1 Application Information

The TPS552892-Q1 can operate over a wide range of 3.0 V to 36 V input voltage and output 0.8 V to 22 V. It can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPS552892-Q1 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPS552892-Q1 operates in one-cycle buck and one-cycle boost mode alternately. The switching frequency is set by an external resistor. To reduce the switching power loss in high power conditions, it is recommended to set the switching frequency below 500 kHz. If a system requires higher switching frequency above 500 kHz, it is recommended to set the lower switch current limit for better thermal performance.

8.2 Typical Application

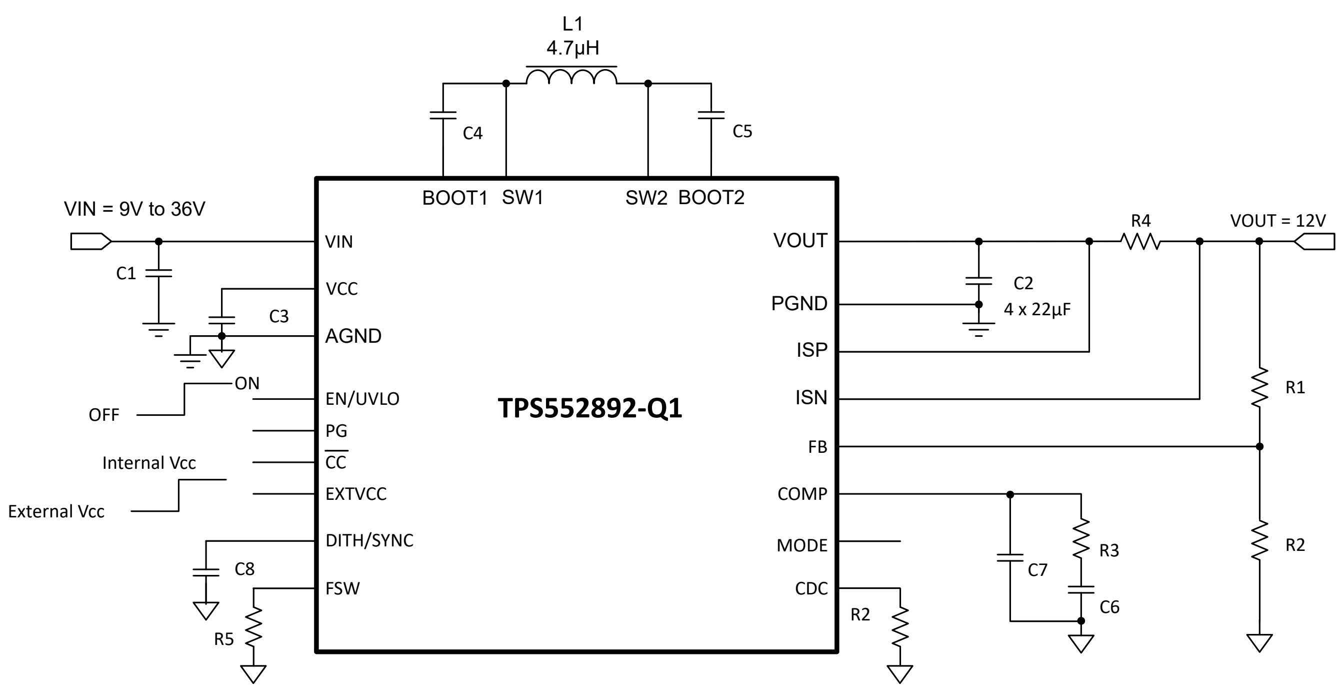

図 8-1. 12-V Power Supply With 9-V to 36-V Input Voltage

8.2.1 Design Requirements

The design parameters are listed in 表 8-1:

表 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	9 V to 36 V
Output voltage	12 V
Output current limit	3 A
Output voltage ripple	±50 mV
Operating mode at light load	FPWM

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The switching frequency of the TPS552892-Q1 is set by a resistor at the FSW pin. Use Equation 3 to calculate the resistance for the desired frequency. To reduce the switching power loss with such a high current application, a 1% standard resistor of 49.9 kΩ is selected for 400-kHz switching frequency for this application.

8.2.2.2 Output Voltage Setting

The output voltage is set by an external resistor divider (R1, R2 in the 図 8-1 circuit diagram). When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. The value of R2 is then calculated as 式 8:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)} \tag{8}$$

8.2.2.3 Inductor Selection

Since the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductance, saturation current, and DC resistance.

The TPS552892-Q1 is designed to work with inductor values between 1 µH and 10 µH. The inductor selection is based on consideration of both buck and boost modes of operation.

For buck mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum input voltage. In CCM, Equation 9 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \times V_{OUT}}{\Delta I_{L(P-P)} \times f_{SW} \times V_{IN(MAX)}} \tag{9}$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- V_{OUT} is the output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when VOUT equals half of the maximum input voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple to the maximum inductor current at the maximum output voltage. In CCM, Equation 10 shows the relationship between the inductance and the inductor ripple current.

$$L = \frac{V_{IN} \times (V_{OUT(MAX)} - V_{IN})}{\Delta I_{L(P-P)} \times f_{SW} \times V_{OUT(MAX)}} \quad (10)$$

where

- V_{IN} is the input voltage
- $V_{OUT(MAX)}$ is the maximum output voltage
- $\Delta I_{L(P-P)}$ is the peak to peak ripple current of the inductor
- f_{SW} is the switching frequency

For a certain inductor, the inductor ripple current achieves maximum value when V_{IN} equals to the half of the maximum output voltage. Choosing higher inductance gets smaller inductor current ripple while smaller inductance gets larger inductor current ripple.

For this application example, a 4.7-µH inductor is selected, which produces approximate maximum inductor current ripple of 50% of the highest average inductor current in buck mode and 50% of the highest average inductor current in boost mode.

In buck mode, the inductor DC current equals to the output current. In boost mode, the inductor DC current can be calculated with Equation 11.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (11)$$

where

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the power conversion efficiency

For a given maximum output current of the buck-boost converter TPS552892-Q1, the maximum inductor DC current happens at the minimum input voltage and maximum output voltage. Set the inductor current limit of the TPS552892-Q1 higher than the calculated maximum inductor DC current to make sure the TPS552892-Q1 has the desired output current capability.

In boost mode, the inductor ripple current is calculated with Equation 12.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (12)$$

where

- $\Delta I_{L(P-P)}$ is the inductor ripple current
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the inductor peak current is calculated with Equation 13.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (13)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI, but in the same way, load transient response time is increased. The selected inductor must have higher saturation current than the calculated peak current.

The conversion efficiency is dependent on the resistance of its current path. The switching loss associated with the switching MOSFETs, and the inductor core loss. Therefore, the overall efficiency is affected by the inductor DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. 表 8-2 lists recommended inductors for the TPS552892-Q1. In this application example, the Coilcraft inductor XAL7070-472 is selected for its small size, high saturation current, and small DCR.

表 8-2. Recommended Inductors

PART NUMBER	L (µH)	DCR (MAXIMUM) (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE (L x W x H mm)	VENDOR(1)
XAL7070-472ME	4.7	14.3	15.2/10.5	7.5 × 7.2 × 7.0	Coilcraft
VCHA085D-4R7MS6	4.7	15.6	16.0/8.8	8.7 × 8.2 × 5.2	Cyntec
IHLP4040DZER4R7M01	4.7	16.5	17/9.5	10.2 × 10.2 × 4.0	Vishay

(1) See the *Third-party Products* disclaimer.

8.2.2.4 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by Equation 14.

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \tag{14}$$

where

- $I_{CIN(RMS)}$ is the RMS current through the input capacitor
- I_{OUT} is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives $I_{CIN(RMS)} = I_{OUT}$ / 2. Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20 µF effective capacitance is a good starting point for this application. Add a 0.1-µF/0402 package ceramic capacitor and place it close to VIN pin and GND pin to suppress high frequency noise.

8.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 15, where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \tag{15}$$

where

- $I_{COUT(RMS)}$ is the RMS current through the output capacitor
- I_{OUT} is the output current

In this example, the maximum output ripple RMS current is 1.7 A.

The ESR of the output capacitor causes an output voltage ripple given by Equation 16 in boost mode.

$$V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times R_{COUT} \tag{16}$$

where

- R_{COUT} is the ESR of the output capacitance

The capacitance also causes a capacitive output voltage ripple given by Equation 17 in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{RIPPLE(CAP)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \tag{17}$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use Equation 16 and Equation 17 to calculate the minimum required effective capacitance of the C_{OUT}.

Add a 0.1-µF/0402 package ceramic capacitor and place it close to VOUT pin and GND pin to suppress high frequency noise.

8.2.2.6 Output Current Limit

The output current limit is implemented by putting a current sense resistor between the ISP and ISN pins. The value of the limit voltage between the ISP and ISN pins is 50 mV. The current sense resistor between the ISP and ISN pins should be selected to ensure that the output current limit is set high enough for output. The output current limit setting resistor is given by Equation 18.

$$R_{SNS} = \frac{V_{SNS}}{I_{OUT\_LIMIT}} \tag{18}$$

where

- V_{SNS} is the current limit setting voltage between the ISP and ISN pins
- I_{OUT_LIMIT} is the desired output current limit

Because the power dissipation is large, make sure the current sense resistor has enough power dissipation capability with large package.

8.2.2.7 Loop Stability

The TPS552892-Q1 uses average current control scheme. The inner current loop uses internal compensation and requires the inductor value must be larger than $1.2/f_{SW}$. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPS552892-Q1 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by Equation 19.

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \tag{19}$$

where

- R_{LOAD} is the output load resistance
- D is the switching duty cycle in boost mode
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.055 Ω

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use 式 20 to Equation 22 to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \tag{20}$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \tag{21}$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1\text{-}D)^2}{2\pi \times L} \tag{22}$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by Equation 23.

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \tag{23}$$

where

- G_{EA} is the transconductance of the error amplifier
- R_{EA} is the output resistance of the error amplifier
- V_{REF} is the reference voltage input to the error amplifier
- V_{OUT} is the output voltage
- f_{COMP1} and f_{COMP2} are the pole's frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The total open-loop gain is the product of $G_{PS}(s)$ and $G_C(s)$. The next step is to choose the loop crossover frequency, f_C, at which the total open-loop gain is 1, namely 0 dB. The higher in frequency that the loop gain stays above 0 dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0 dB at the frequency no higher than the lower of either 1/10 of the switching frequency, f_{SW} or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then, set the value of R_C, C_C, and C_P by Equation 24 to Equation 26.

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1\text{-}D) \times V_{REF} \times G_{EA}} \tag{24}$$

where

- f_C is the selected crossover frequency

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \tag{25}$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \tag{26}$$

If the calculated C_P is less than 10 pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

8.2.3 Application Curves

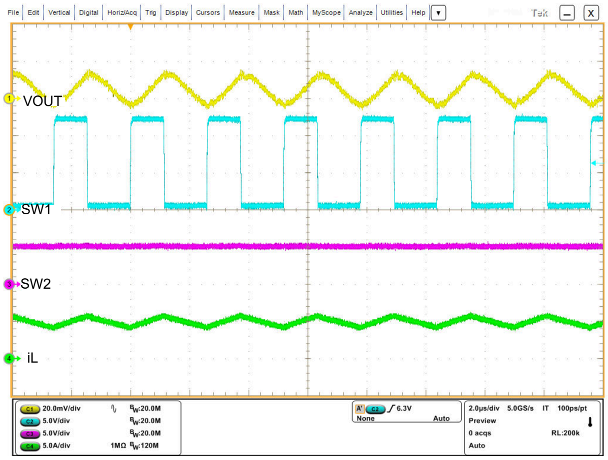

図 8-2. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 5 A, FPWM

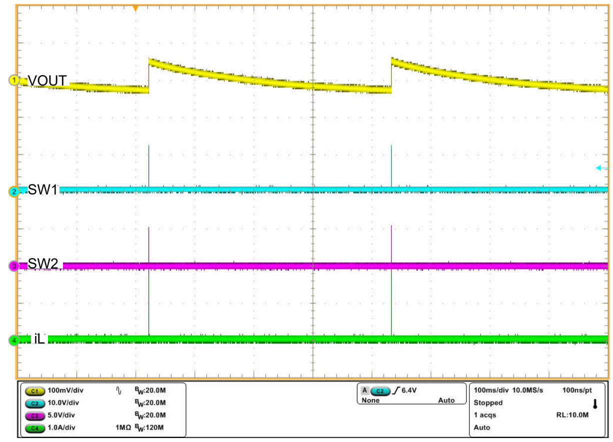

図 8-3. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 0 A, PFM

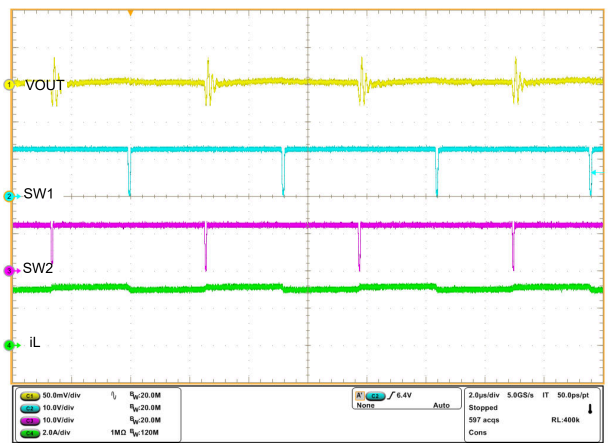

図 8-4. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 12 V, I_O = 3 A, FPWM

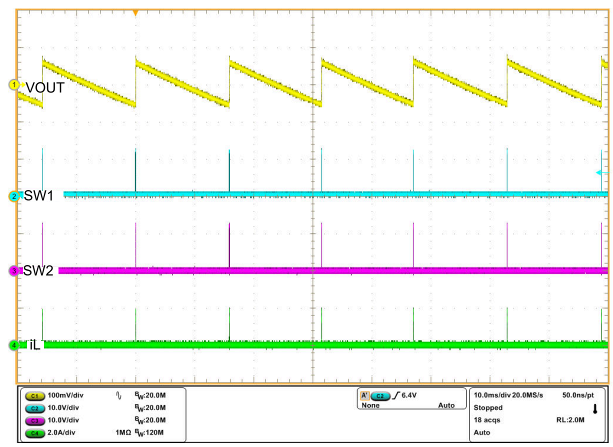

図 8-5. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 12 V, I_O = 0 A, PFM

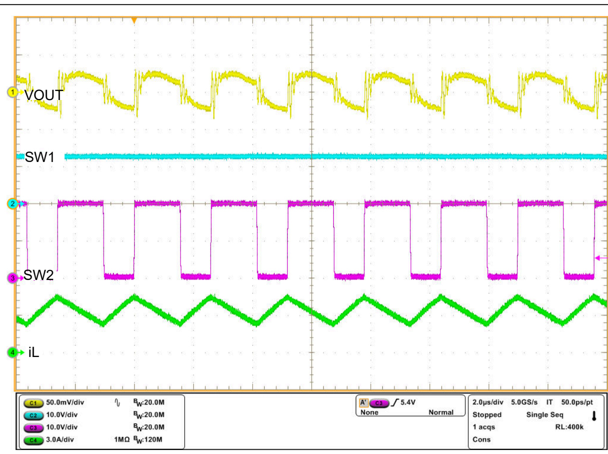

図 8-6. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 20 V, I_O = 2 A, FPWM

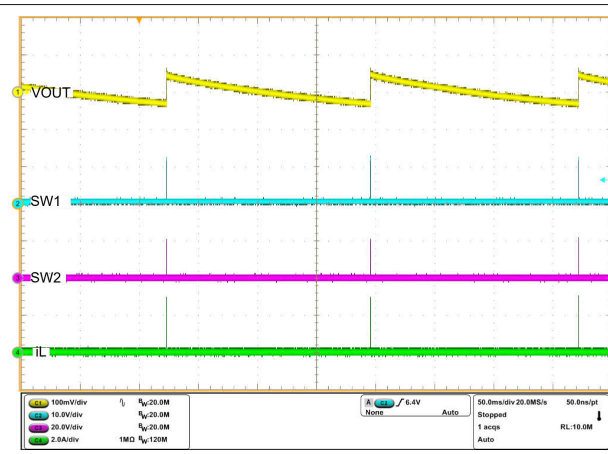

図 8-7. Switching Waveforms in V_{IN} = 12 V, V_{OUT} = 20 V, I_O = 0 A, PFM

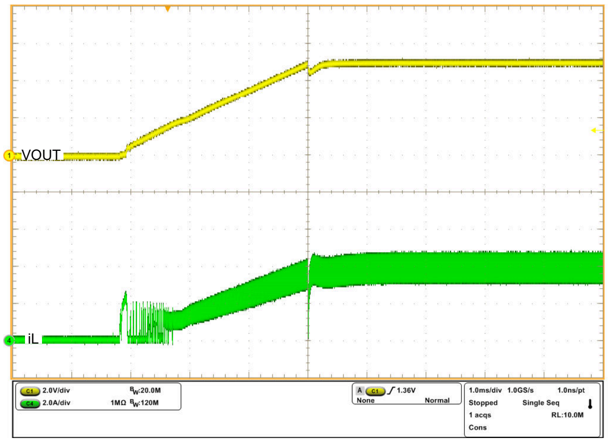

図 8-8. Start-up Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, R_{LOAD} = 1.2 Ω, FPWM

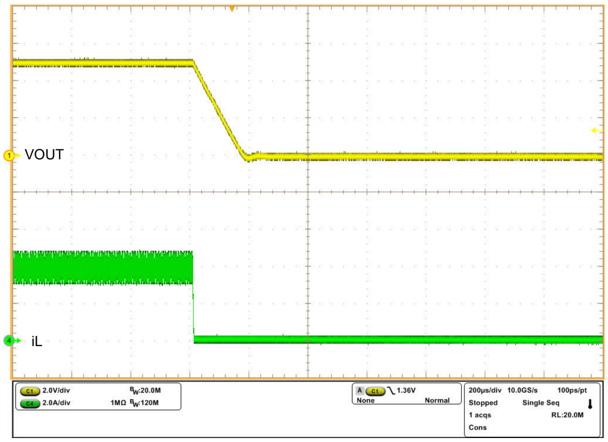

図 8-9. Shutdown Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, R_{LOAD} = 1.2 Ω, FPWM

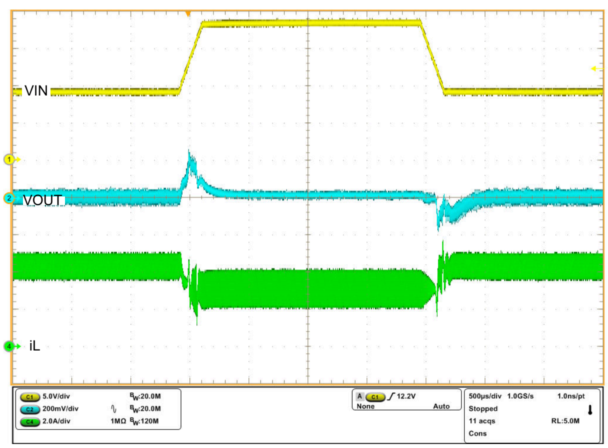

図 8-10. Line Transient Waveforms in V_{IN} = 9 V to 20 V, V_{OUT} = 12 V, I_O = 3 A with 200-µs Slew Rate, FPWM

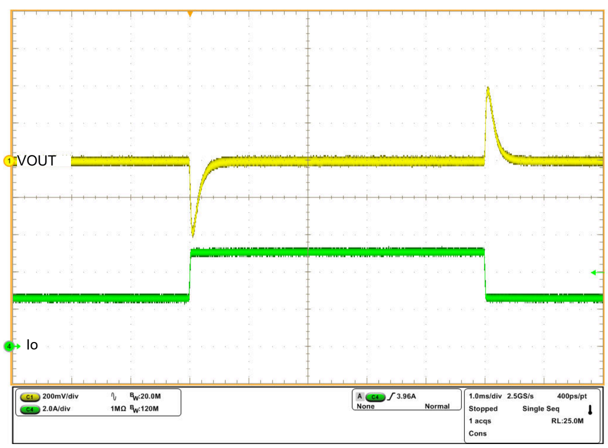

図 8-11. Load Transient Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, I_O = 2.5 A to 5 A with 20-µs Slew Rate, FPWM

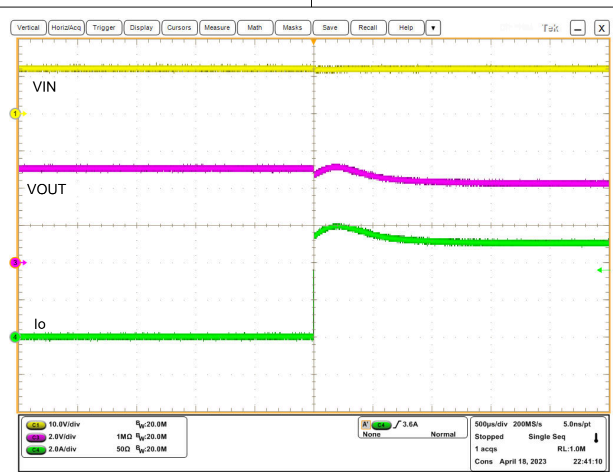

図 8-12. Output Current Limit Waveforms in V_{IN} = 12 V, V_{OUT} = 5 V, R_{LOAD} = 0.8 Ω, R_{SNS} = 10 mΩ, FPWM

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0 V to 36 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100 µF.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

1. Place the 0.1-µF small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops. This improves the radiation of high-frequency noise (EMI) and efficiency.
2. Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane. This also improves thermal performance.
3. Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
4. Use Kelvin connections to RSENSE for the current sense signals ISP and ISN and run lines in parallel from the RSENSE terminals to the IC pins. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
5. Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 and SW2 pins.
6. Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor should be directly connected with PGND plane through three to four vias.
7. Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
8. Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components, switching nodes SW1 and SW2, and high-current trace to prevent noise coupling into the analog signals.
9. To improve thermal performance, it is recommended to use thermal vias beneath the TPS552892-Q1 connecting the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

8.4.2 Layout Example

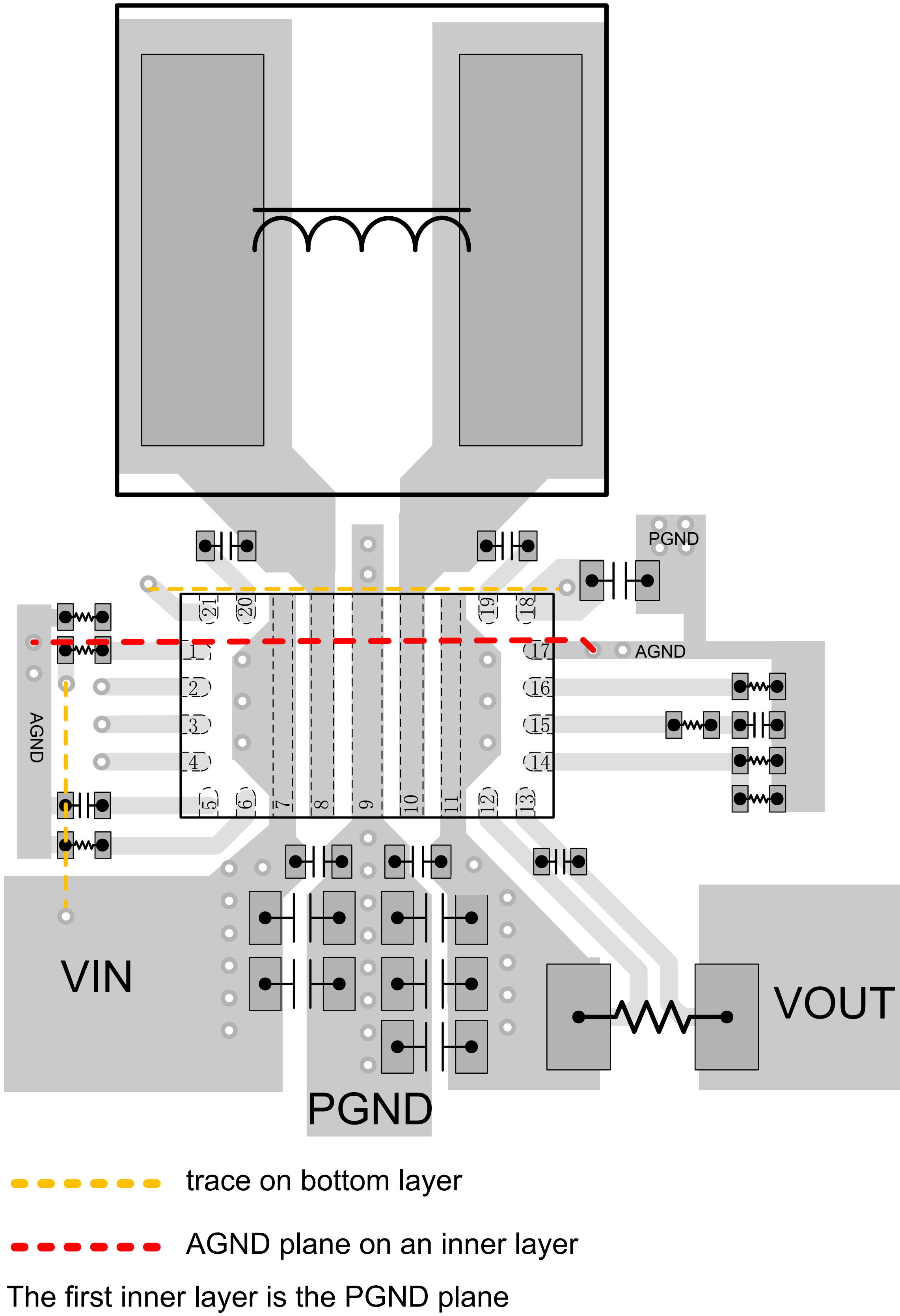

図 8-13. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS552892QWRYQRQ1	Active	Production	VQFN-HR (RYQ) | 21	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	52892Q
TPS552892QWRYQRQ1.A	Active	Production	VQFN-HR (RYQ) | 21	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	52892Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS552892-Q1 :

- Catalog : TPS552892

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

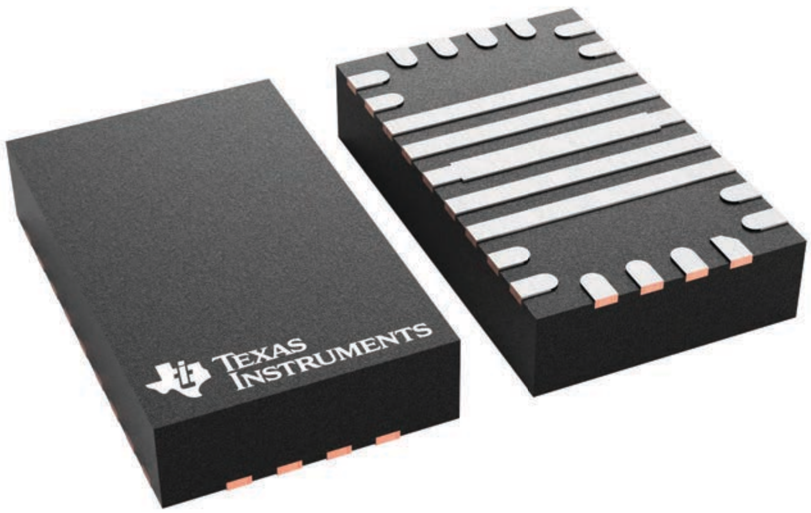
RYQ 21

VQFN - 1 mm max height

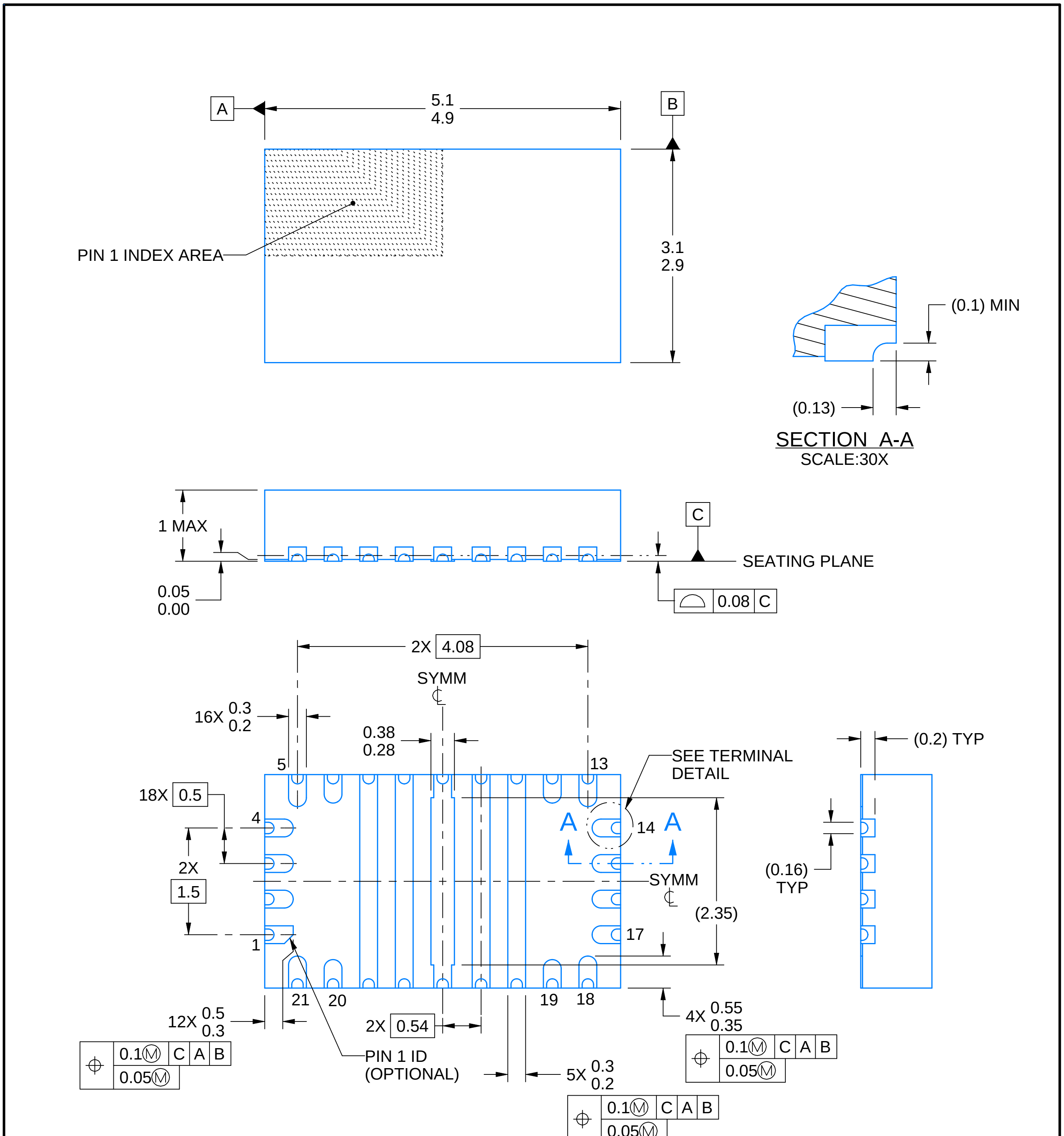
5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



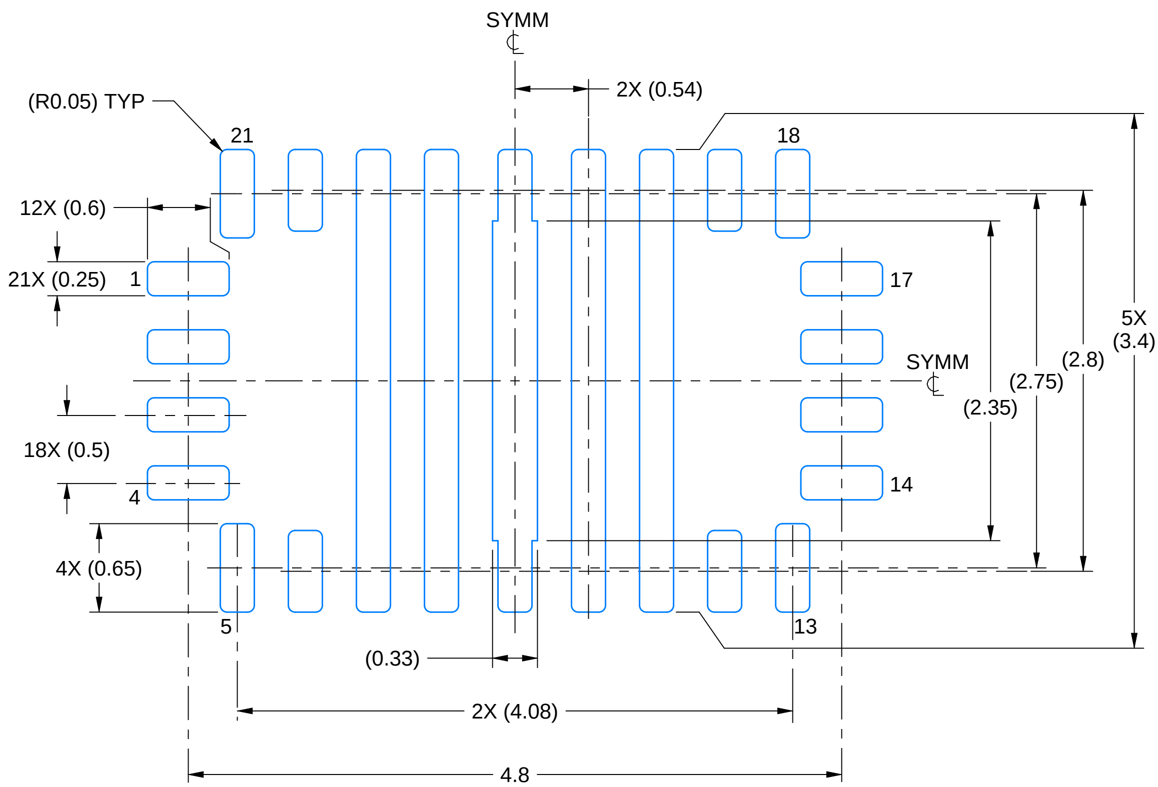
4228970/A



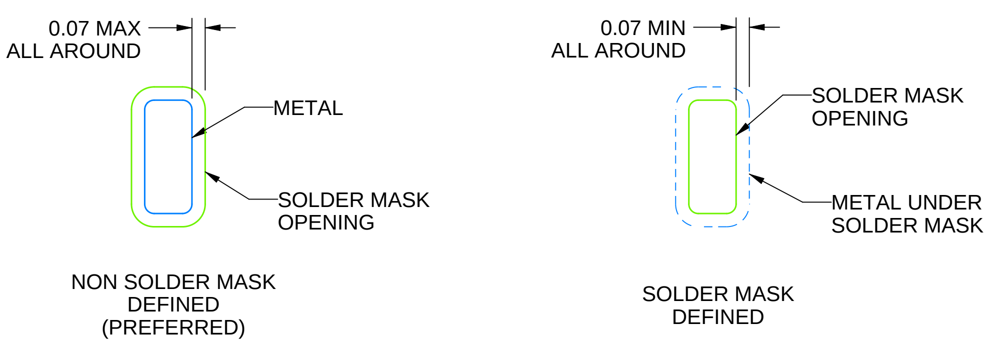
4228792/A 07/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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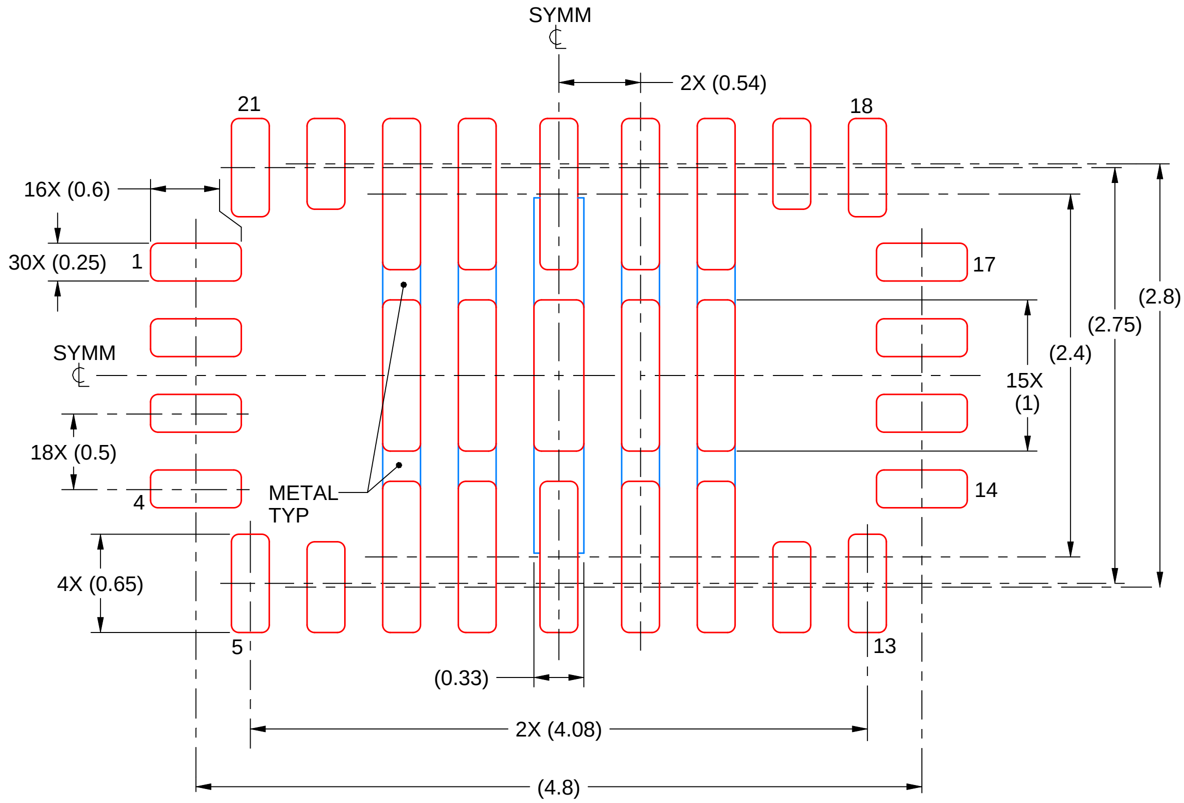
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PIN 7,8, 10 & 11 SOLDER COVERAGE = 88%
PIN 9 SOLDER COVERAGE = 64%
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.