TPS54325-Q1 4.5V～20V 3A 出力、同期整流 SWIFT 降圧スイッチャ、FET 内蔵

1 特長

- 車載アプリケーション認定済み
- 高速過渡応答を可能にする D-CAP2™ モード
- 低出力リップルで、出力セラミック・コンデンサが使用可能
- 4.5V～18V の広い V_{CC} 入力電圧範囲
- 2.0V～18V の広い V_{IN} 入力電圧範囲
- 0.76V～5.5V の出力電圧範囲
- 低デューティ・サイクルのアプリケーションに対して最適化された、高効率の内蔵 FET –120mΩ (ハイサイド) および 70mΩ (ローサイド)
- 高効率、シャットダウン時 10µA 未満
- 高い初期バンドギャップ・リファレンス精度
- 調整可能なソフトスタート
- プリバイアス付きのソフト・スタート
- スイッチング周波数 (f_{SW}):700kHz
- サイクルごとの過電流制限
- パワー・グッド出力
- WEBENCH® Power Designer により TPS54325-Q1 を使用するカスタム設計が可能

2 アプリケーション

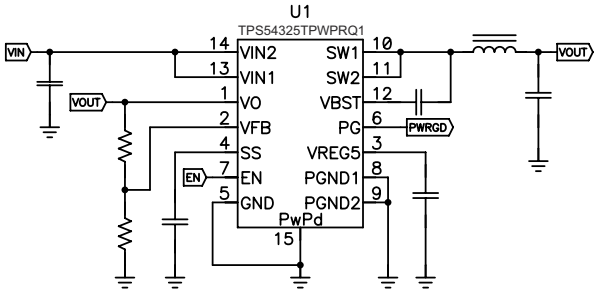
- 幅広い範囲の低電圧システム用アプリケーション
  - デジタル・テレビ用電源
  - 高精細 Blu-ray Disc™ プレーヤー
  - ネットワーク・ホーム・ターミナル
  - デジタル・セットトップ・ボックス (STB)

3 概要

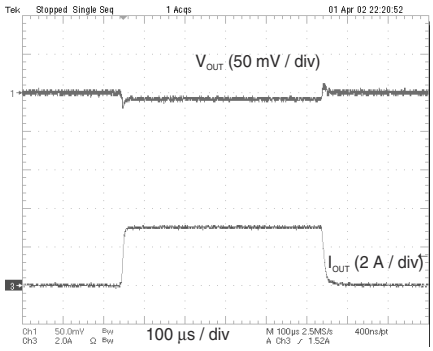
TPS54325-Q1 は、適応型オン時間 D-CAP2 モードに対応した同期整流降圧コンバータです。TPS54325-Q1 を採用することで、各種機器の電源バス・レギュレータに対して、コスト効果が高く、部品数の少ない、低スタンバイ電流のソリューションを実現できます。TPS54325-Q1 の主制御ループは、外部補償部品なしで非常に高速な過渡応答が得られる D-CAP2 モード制御を使用しています。また、低 ESR (等価直列抵抗) の出力コンデンサ (たとえば、POSCAP または SP-CAP) と超低 ESR セラミック・コンデンサの両方をサポートできる独自の回路も備えています。このデバイスは、4.5V～18V の VCC 入力、および 2.0V～18V の V_{IN} 入力電源電圧で動作します。出力電圧は、0.76V～5.5V の範囲でプログラミングできます。また、調整可能なスロー・スタート時間とパワー・グッド機能も備えています。TPS54325-Q1 は、14 ピンの HTSSOP パッケージで供給され、–40°C～105°C の温度範囲で動作するよう設計されています。

製品情報

型番	パッケージ	本体サイズ (公称)
TPS54325-Q1	HTSSOP	5.00mm × 4.40mm



概略回路図



負荷過渡応答

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2011) to Revision A (July 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• *ESD 定格、ピン構成および機能、詳細説明、機能ブロック図、機能説明、デバイスの機能モード、アプリケーションと実装、アプリケーション情報、代表的なアプリケーション、設計要件、詳細な設計手順、アプリケーション曲線、電源に関する推奨事項、レイアウト、レイアウトのガイドライン、レイアウト例、デバイスおよびドキュメントのサポート、メカニカル、パッケージ、および注文情報*を追加	1
• Corrected thermal information	5

5 Pin Configuration and Functions

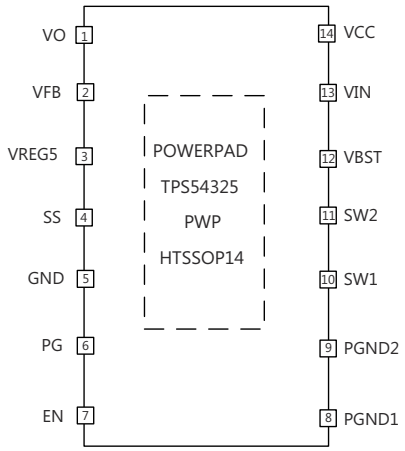


図 5-1. 14-Pin PWP HTSSOP Pinout

表 5-1. Pin Functions

Pin		Description
Name	NO.	
VO	1	Connect this pin to the output of the converter. This pin is used for on-time adjustment.
VFB	2	Converter feedback input. Connect this pin with a feedback resistor divider.
VREG5	3	5.5-V power supply output. Connect a capacitor (typically 1μF) to GND.
SS	4	Soft-start control. Connect an external capacitor to GND.
GND	5	Signal ground pin
PG	6	Open-drain power-good output
EN	7	Enable control input
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. These ground returns also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	Switch node connections between the high-side NFET and low-side NFET. These connections also serve as inputs to current comparators.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect a capacitor from this pin to respective SW1 and SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	Power input and connected to high-side NFET drain
VCC	14	Supply input for the 5-V internal linear regulator for the control circuitry
PowerPAD	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Connect to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage range	V_{IN}, V_{CC}, EN	–0.3	20	V
		V_{BST}	–0.3	26	
		V_{BST} (vs SW1, SW2)	–0.3	6.5	
		V_{FB}, V_O, SS, PG	–0.3	6.5	
		SW1, SW2	–2	20	
		SW1, SW2 (10-ns transient)	–3	20	
V_O	Output voltage range	V_{REG5}	–0.3	6.5	V
		P_{GND1}, P_{GND2}	–0.3	0.3	
V_{diff}	Voltage from GND to POWERPAD		–0.2	0.2	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions is not implied. Exposure to absolute maximum rated condition for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range, VCC, V_{IN} = 12 V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply input voltage range		4.5	18	V
V_{IN}	Power input voltage range		2	18	V
V_I	Input voltage range	V_{BST}	–0.1	24	V
		V_{BST}, (vs SW1, SW2)	–0.1	6	
		SS, PG	–0.1	6	
		EN	–0.1	18	
		V_O, V_{FB}	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10-ns transient)	–3	18	
		P_{GND1}, P_{GND2}	–0.1	0.1	
V_O	Output voltage range	V_{REG5}	–0.1	6	V
I_O	Output current range	I_{VREG5}	0	10	mA
T_A	Operating free-air temperature		–40	105	°C
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		PWP	UNIT
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating – nonswitching supply current	V_{CC} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		850	1300	µA
I_{CCSDN}	Shutdown supply current	V_{CC} current, T_A = 25°C, EN = 0 V			10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	2			V
V_{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V	757	765	775	mV
		T_A = 0°C to 105°C, V_O = 1.05 V	753		777	
		T_A = –40°C to 105°C, V_O = 1.05 V	750		780	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
R_{Dischg}	V_O discharge resistance	EN = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{CC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6.0 V < V_{CC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{REG5}	Output current	V_{CC} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C		70		mA
MOSFET						
R_{dsonh}	High-side switch resistance	25°C, V_{BST} – SW1, SW2 = 5.5 V		120		mΩ
R_{dsonl}	Low-side switch resistance	25°C		70		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	T_A = 25°C to 105°C	3.5	4.1		A
		T_A = –40°C	3.25	3.5		
THERMAL SHUTDOWN						
t_{SDN}	Thermal shutdown threshold	Shutdown temperature		150		°C
		Hysteresis		25		
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		145		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260		ns
SOFT START						

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SSC}	SS charge current	V_{SS} = 0 V	1.4	2.0	2.6	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (good)	85%	90%	95%	
		V_{FB} falling (fault)		85%		
I_{PG}	PG sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115%	120%	125%	
T_{OVPDEL}	Output OVP prop delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis		10%		
t_{UVPDEL}	Output UVP delay			0.25		ms
t_{UVPEN}	Output OVP enable delay	Relative to soft-start time		× 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake-up V_{REG5} voltage	3.45	3.70	3.95	V
		Hysteresis V_{REG5} voltage	0.15	0.25	0.35	

6.6 Typical Characteristics

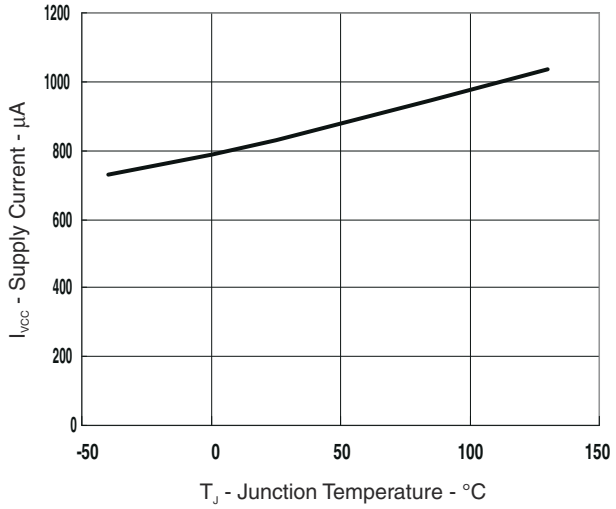


図 6-1. V_{CC} Temperature vs Junction Temperature

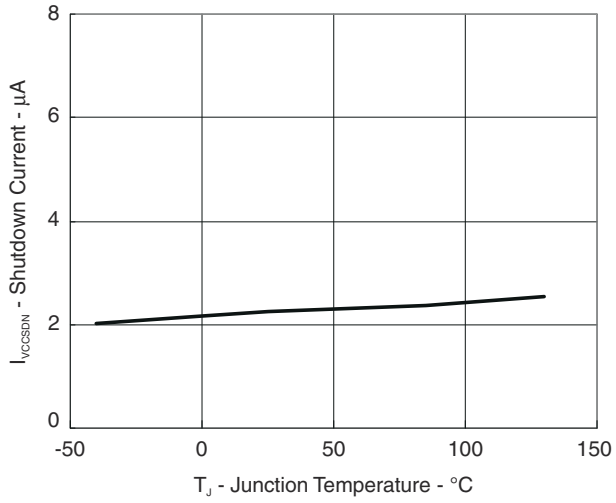


図 6-2. V_{CC} Shutdown Current vs Junction Temperature

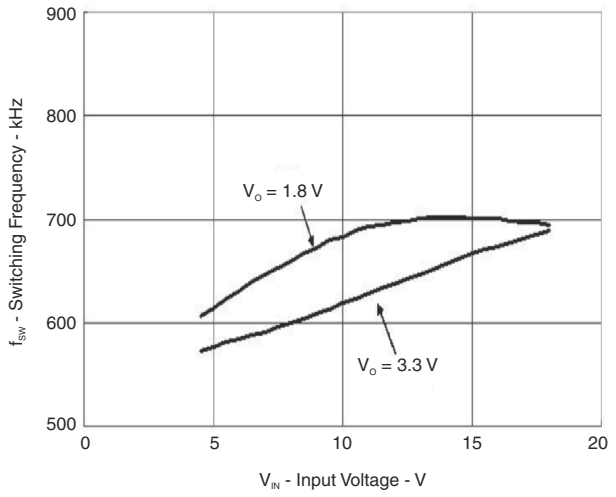


図 6-3. Switching Frequency vs Input Voltage (I_O = 1 A)

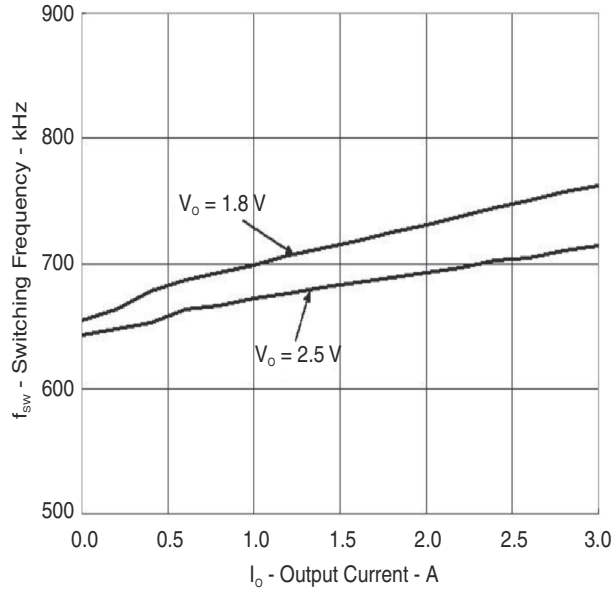


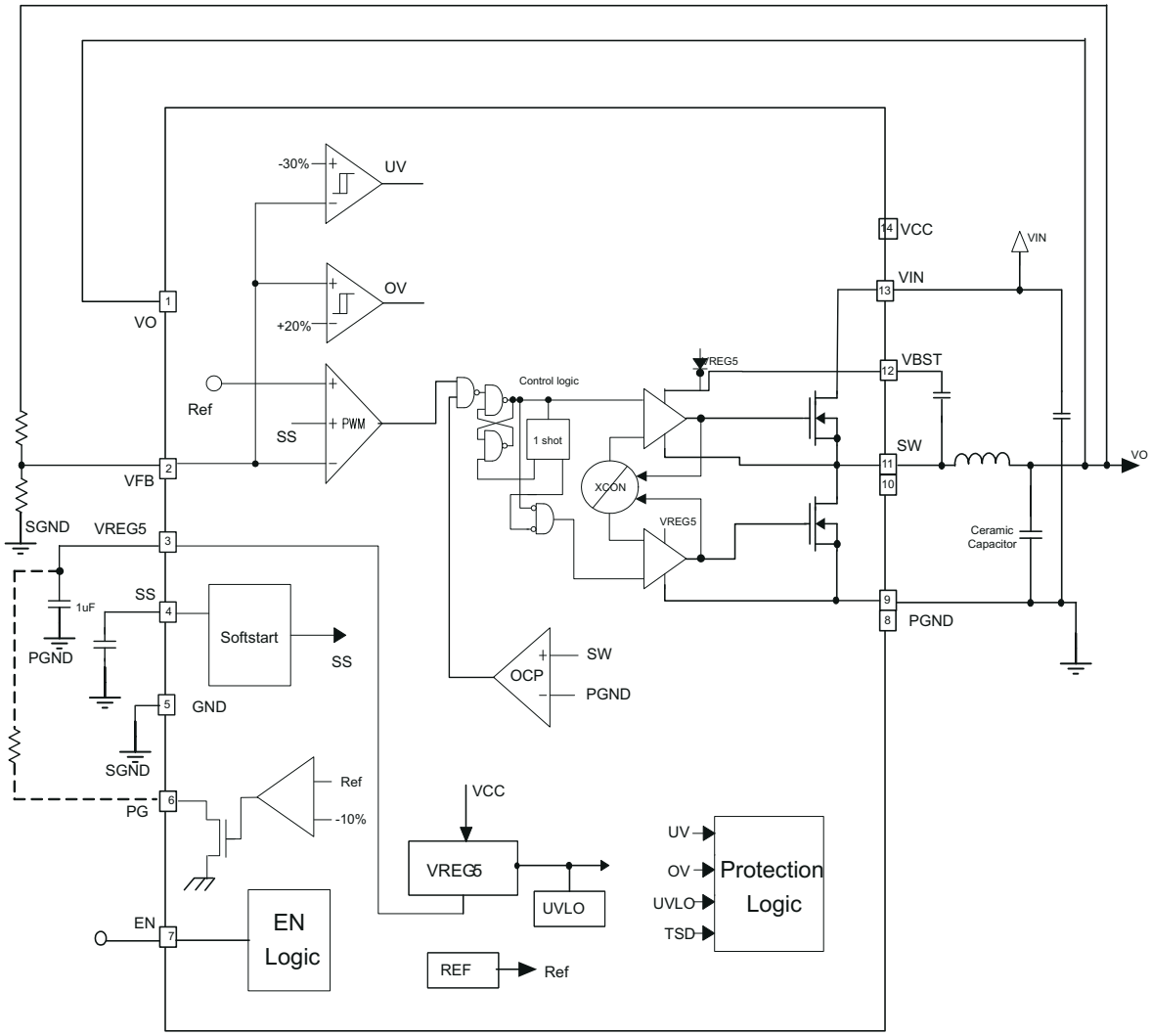
図 6-4. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS54325-Q1 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. The device operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start and Pre-Biased Soft Start

The TPS54325-Q1 has an adjustable soft start. When the EN pin becomes high, 2.0-µA current begins charging the capacitor, which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start-up. Use the following equation to find the slow-start time. VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$T_{SS}(ms) = \frac{C6(nF) \times V_{REF}}{I_{SS}(\mu A)} = \frac{C6(nF) \times 0.765}{2} \quad (1)$$

The TPS54325-Q1 contains a unique circuit to prevent current from being pulled from the output during start-up in the condition the output is prebiased. When the soft start commands a voltage higher than the prebias level (internal soft start becomes greater than feedback voltage (V_{FB})), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on time. The device then increments that on time on a cycle-by-cycle basis until it coincides with the time dictated by (1 – D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensures that the out voltage (V_O) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

7.3.2 Power Good

The TPS54325-Q1 has a power-good output. The power-good function is activated after soft start has finished. If the output voltage becomes within –10% of the target value, internal comparators detect a power-good state and the power-good signal becomes high. During start-up, power good start after 1.7 times the soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes under 15% of the target value, the power-good signal becomes low after a 10-µs internal delay.

7.3.3 Output Discharge Control

The TPS54325-Q1 discharges the output when EN is low or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges outputs using an internal 50-Ω M,OSFET which is connected to VO and PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.4 Current Protection

The TPS54325-Q1 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the off state and the controller keeps the off state when the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, the device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

The inductor current is monitored by the voltage between PGND pin and SW1 and SW2 pins. In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall off. Eventually, the output voltage ends up crossing the undervoltage protection threshold and shutdown.

7.3.5 Overvoltage and Undervoltage Protection

The TPS54325-Q1 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 µs, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 × soft-start time.

7.3.6 UVLO Protection

The TPS54325-Q1 has undervoltage lockout protection (UVLO) that monitors the voltage of VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54325-Q1 is shut off. This is non-latch protection.

7.3.7 Thermal Shutdown

The TPS54325-Q1 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 PWM Operation

The main control loop of the TPS54325-Q1 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an

internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. This mode is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal the one shot timer expires. This one shot timer is set by the converter input voltage ,V_{IN}, and the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR-induced output ripple from D-CAP2 mode control.

7.4.2 PWM Frequency and Adaptive On-Time Control

The TPS54325-Q1 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The TPS54325-Q1 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is V_{OUT} / V_{IN}, the frequency is constant

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS54325-Q1 device is typically used as a step-down converter, which converts a voltage in the range of 4.5 V to 18 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits

8.2 Typical Application

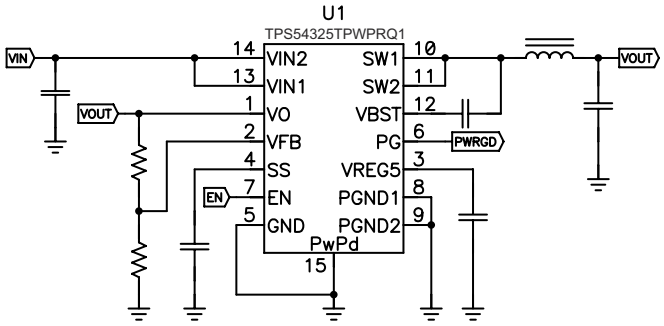


図 8-1. Schematic Diagram for Design Example

8.2.1 Design Requirements

表 8-1. Design Parameters

Parameter	Conditions	MIN	TYP	MAX	Unit
Input voltage		5			V
Output voltage			1.05		V
Operating frequency	V_I = 12 V, I_O = 1 A		700		kHz
Output current		0		3	A
Output ripple voltage	V_I = 12 V, I_O = 3 A		9		mVpp
Efficiency	V_I = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1.2 A		91%		

8.2.2 Detailed Design Procedure

To begin the design process, define these parameters for the application:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54325-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Inductor Selection

The inductance value is selected to provide approximately 30% peak-to-peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improves S/N ratio, and contributes to stable operation. Smaller ripple currents result in lower output voltage ripple. When using low-ESR output capacitors, output ripple voltage is usually low, so larger ripple currents are acceptable. The coefficient Kind represents the percentage of ripple current. The value of Kind must not be greater than 0.4. Use 0.3 when using low-ESR output capacitors. 式 2 can be used to calculate L1. Use 700 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 式 4 and the RMS current of 式 5.

$$L_O = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{I_{OUT} \times f_{SW} \times Kind} \tag{2}$$

$$Ilp - p = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{3}$$

$$I_{lpeak} = I_O + \frac{Ilp - p}{2} \tag{4}$$

$$I_{Lo(RMS)} = \sqrt{I_0^2 + \frac{1}{12} Ilp - p^2} \tag{5}$$

8.2.2.3 Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple. TI recommends using ceramic output capacitor. Using the following equations, an initial estimate for the capacitor value, ESR, and RMS current can be calculated. If the load transients are significant, consider using the load step, instead of ripple current to calculate the maximum ESR. Minimum C_O must be over 20 µF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{O(ripple)}}{I_{ripple}} - R_{ESR}\right)} \tag{6}$$

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{l(ripple)}} \tag{7}$$

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{8}$$

8.2.2.4 Input Capacitor Selection

The TPS54325-Q1 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage. In case of separate VCC and VIN, then a ceramic capacitor over 10 µF is recommended for the VIN and also placing ceramic capacitor over 0.1 µF for the VCC is recommended.

8.2.2.5 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends using a ceramic capacitor.

8.2.2.6 VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. TI recommends using a ceramic capacitor.

8.2.2.7 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using the following equations to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current is more noticeable

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (9)$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \times V_{OUT}) \times \left(1 + \frac{R1}{R2}\right) \quad (10)$$

8.2.3 Application Performance Plots

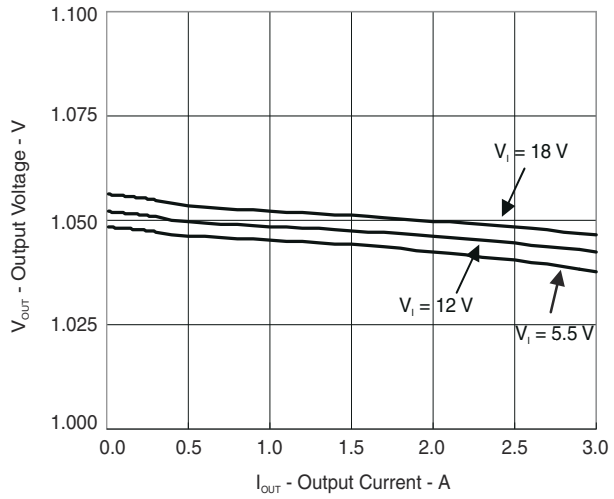


図 8-2. 1.05-V Output Voltage vs Output Current

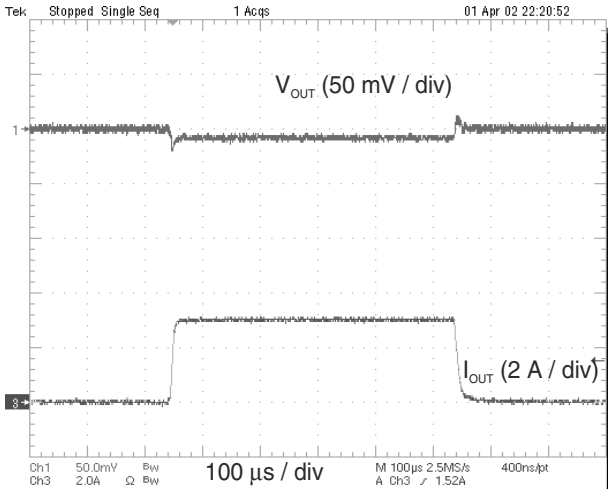


図 8-3. 1.05-V, 0-A to 3-A Load Transient Response

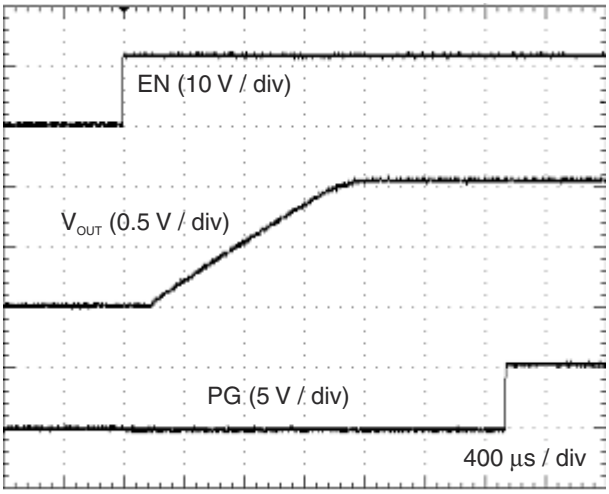


図 8-4. Start-Up Waveform

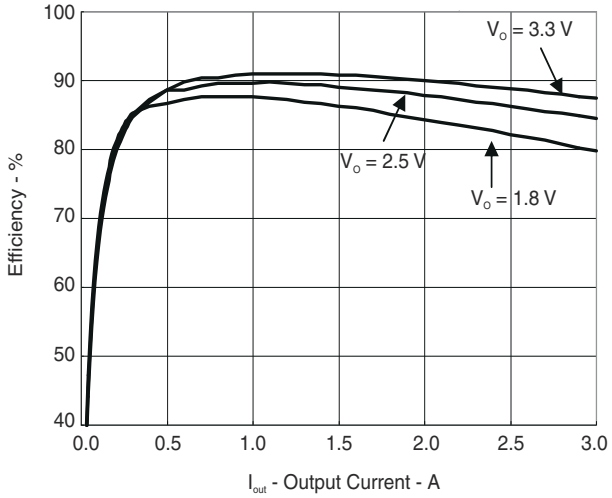


図 8-5. Efficiency vs Output Current (V_{IN} = 12 V)

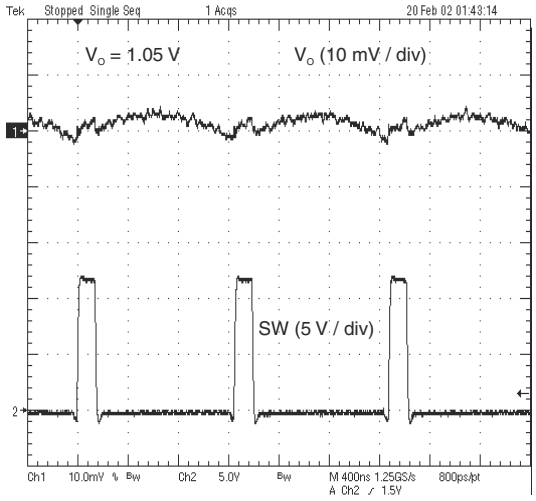


図 8-6. Voltage Ripple at Output

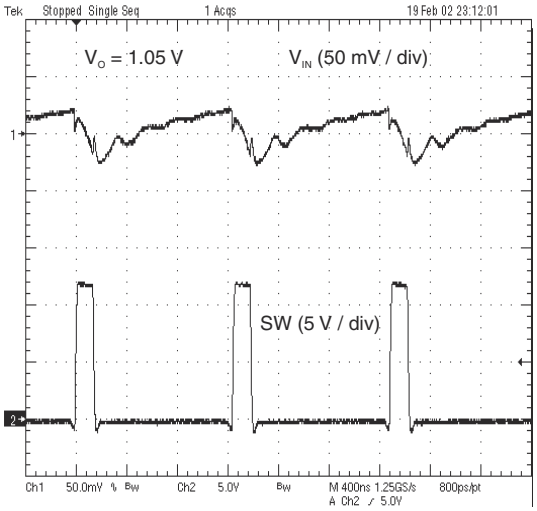


図 8-7. Voltage Ripple at Input

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4.5 V and 18 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- Keep the pattern lines for VIN and PGND broad.
- Exposed pad of device must be connected to PGND with solder.
- VREG5 capacitor must be placed near the device and connected PGND.
- Output capacitor must be connected to a broad pattern of the PGND.
- Voltage feedback loop must be as short as possible, and preferably with ground shield.
- Lower resistor of the voltage divider, which is connected to the VFB pin must be tied to SGND.
- Providing sufficient via is preferable for VIN, SW, and PGND connection.
- PCB pattern for VIN, SW, and PGND must be as broad as possible.
- If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
- Place the V_{IN} capacitor as close as possible to the device.

10.2 Layout Example

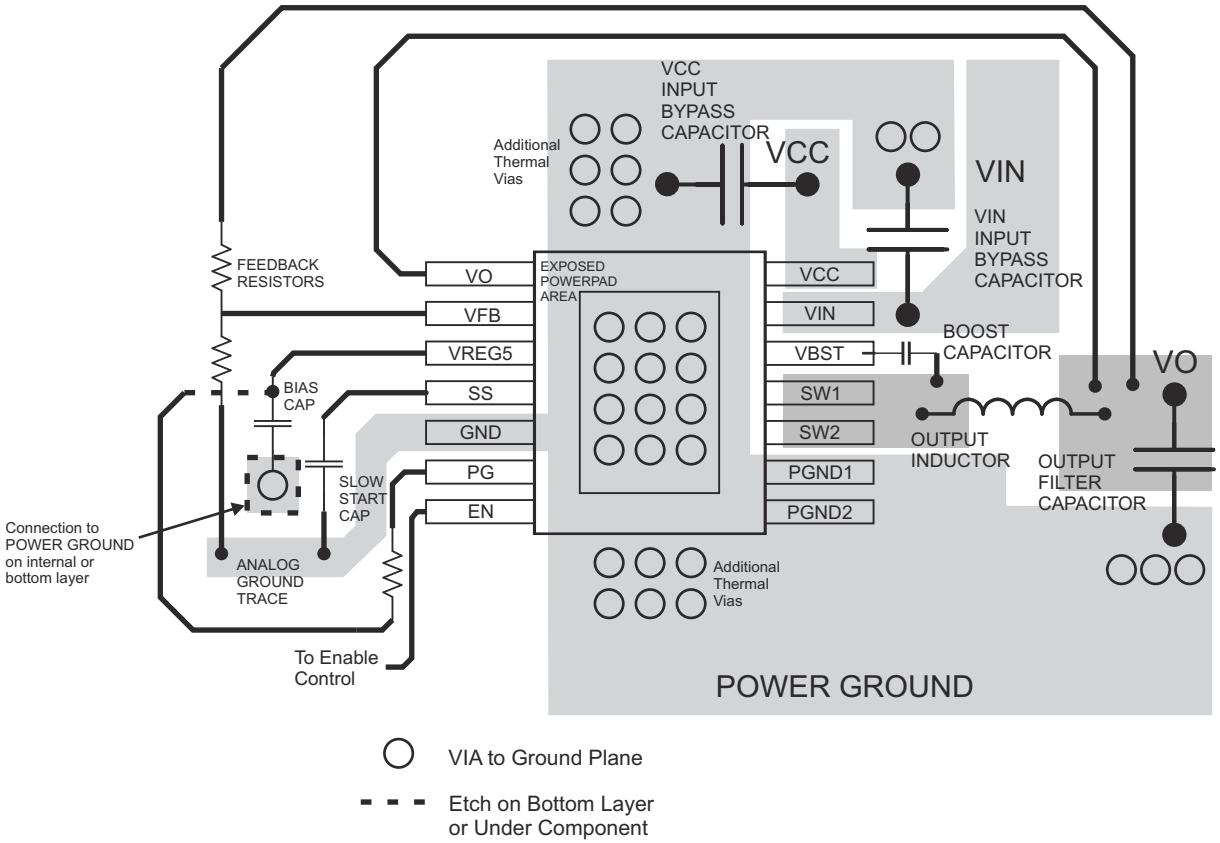


図 10-1. PCB Layout

10.3 Thermal Information

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be

used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to the *PowerPAD™ Thermally Enhanced Package* and *PowerPAD Made Easy* application notes.

The exposed thermal pad dimensions for this package are shown in the following illustration.

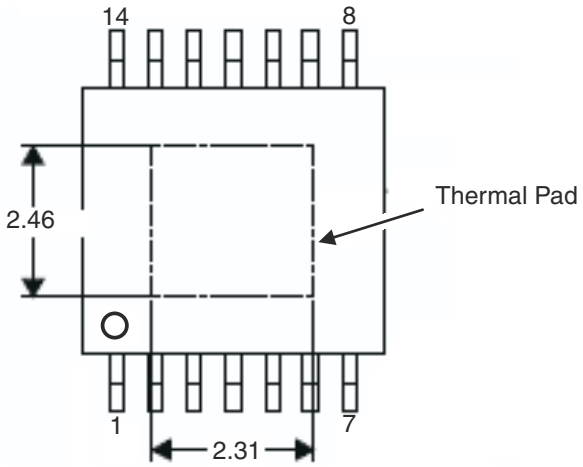


図 10-2. Thermal Pad Dimensions

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54325-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get the information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.5 Trademarks

D-CAP2™ and TI E2E™ are trademarks of Texas Instruments.
Blu-ray Disc™ is a trademark of Blu-ray Disc.
WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54325TPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	54325Q1
TPS54325TPWPRQ1.B	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	54325Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS54325-Q1 :

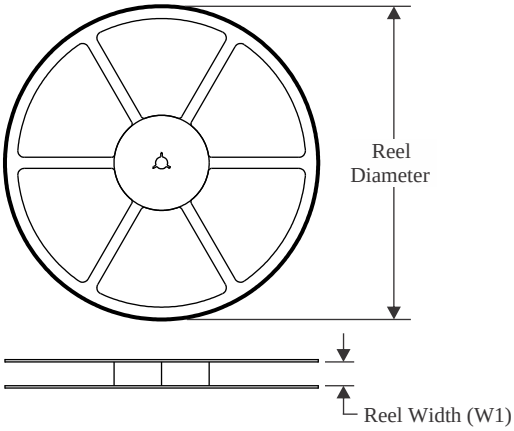
- Catalog : TPS54325

NOTE: Qualified Version Definitions:

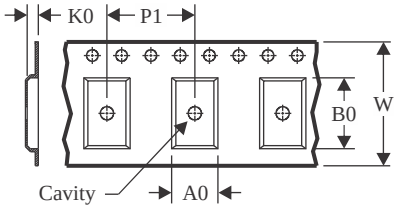
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

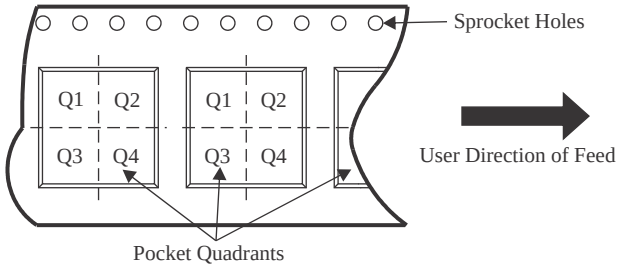


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

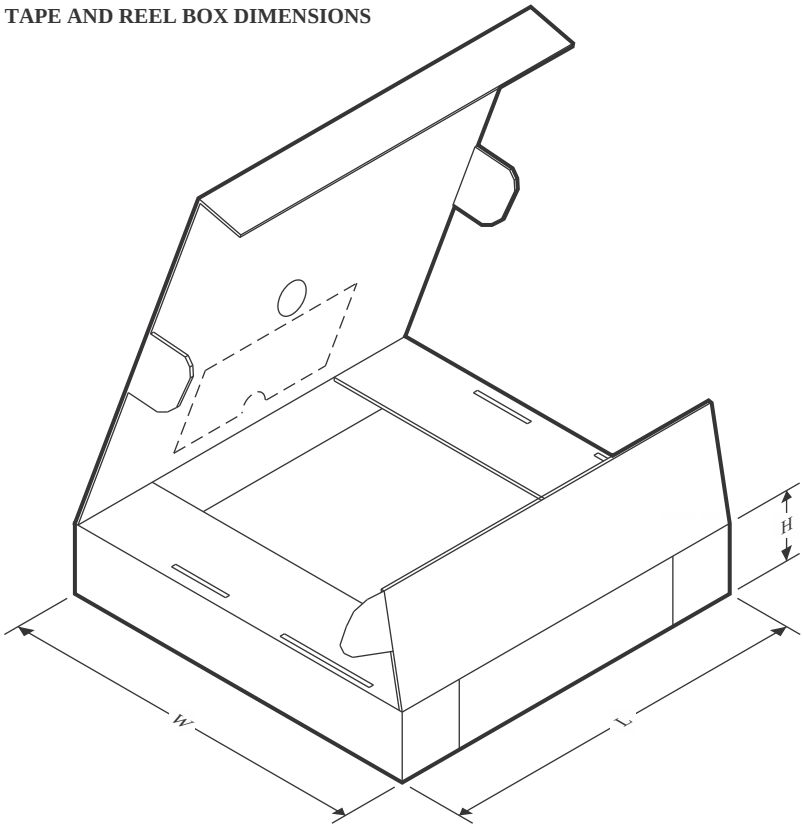
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54325TPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54325TPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

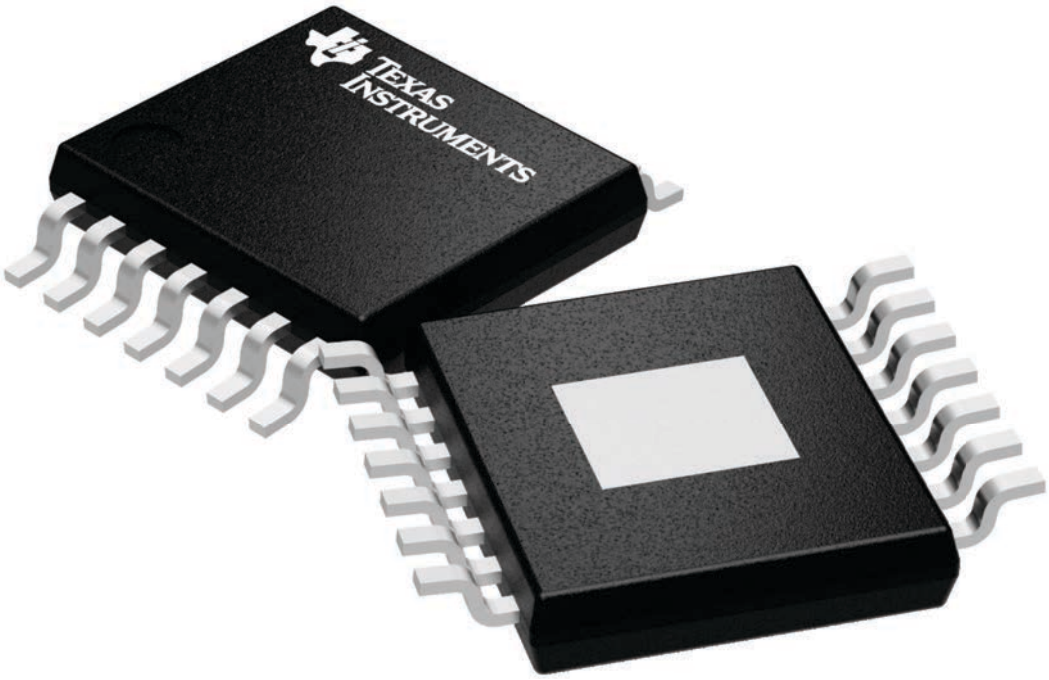
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



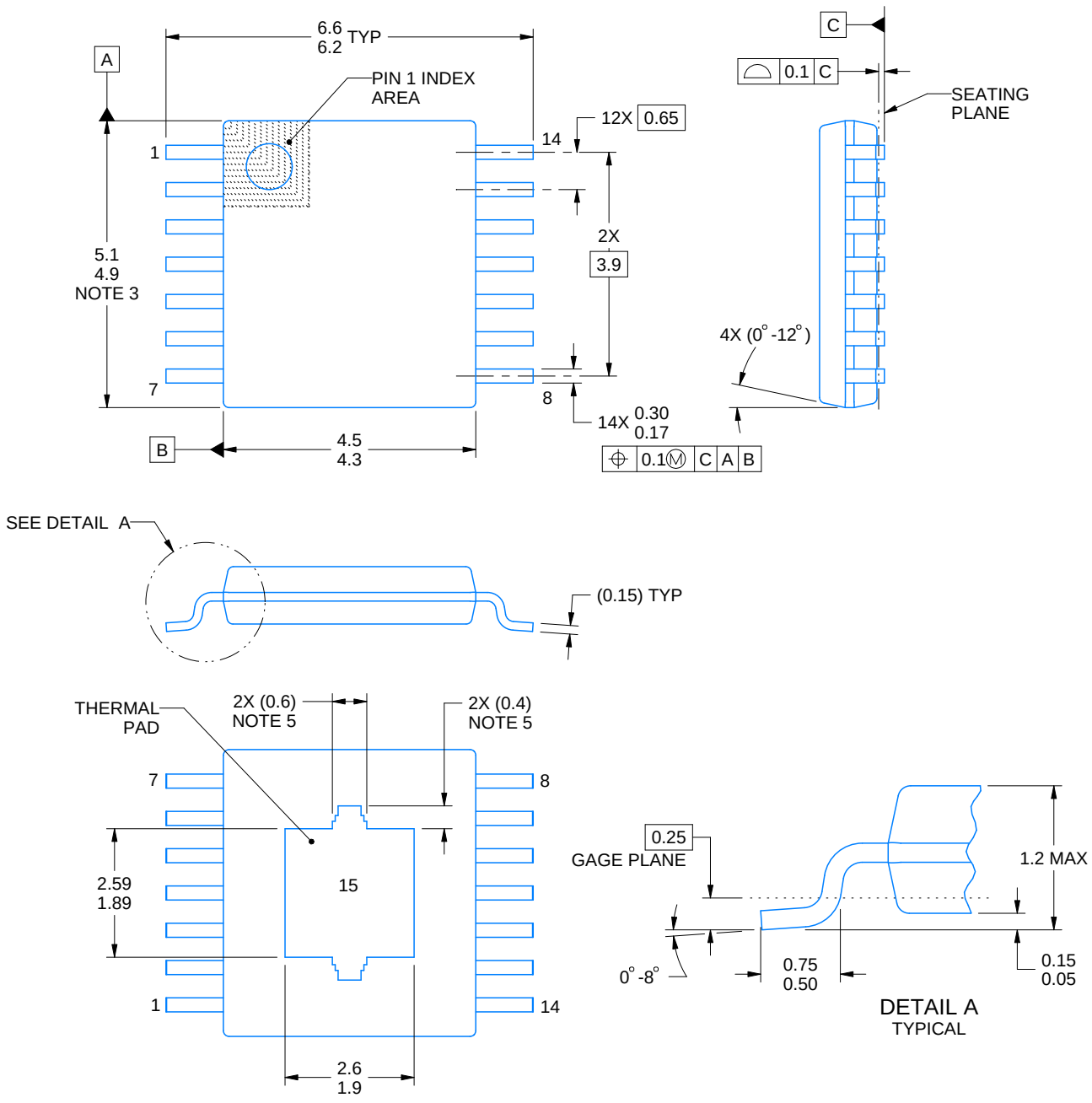
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

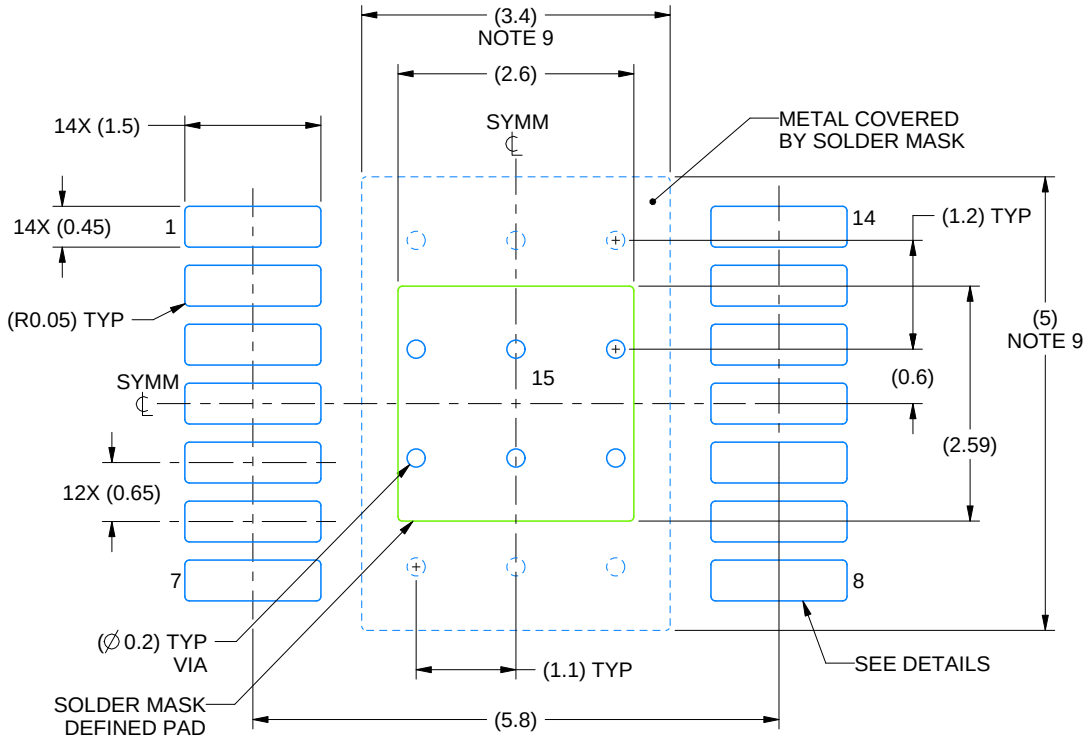
SMALL OUTLINE PACKAGE



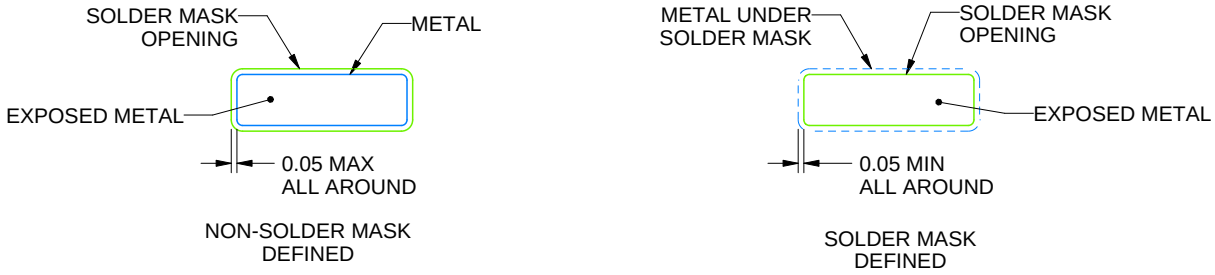
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

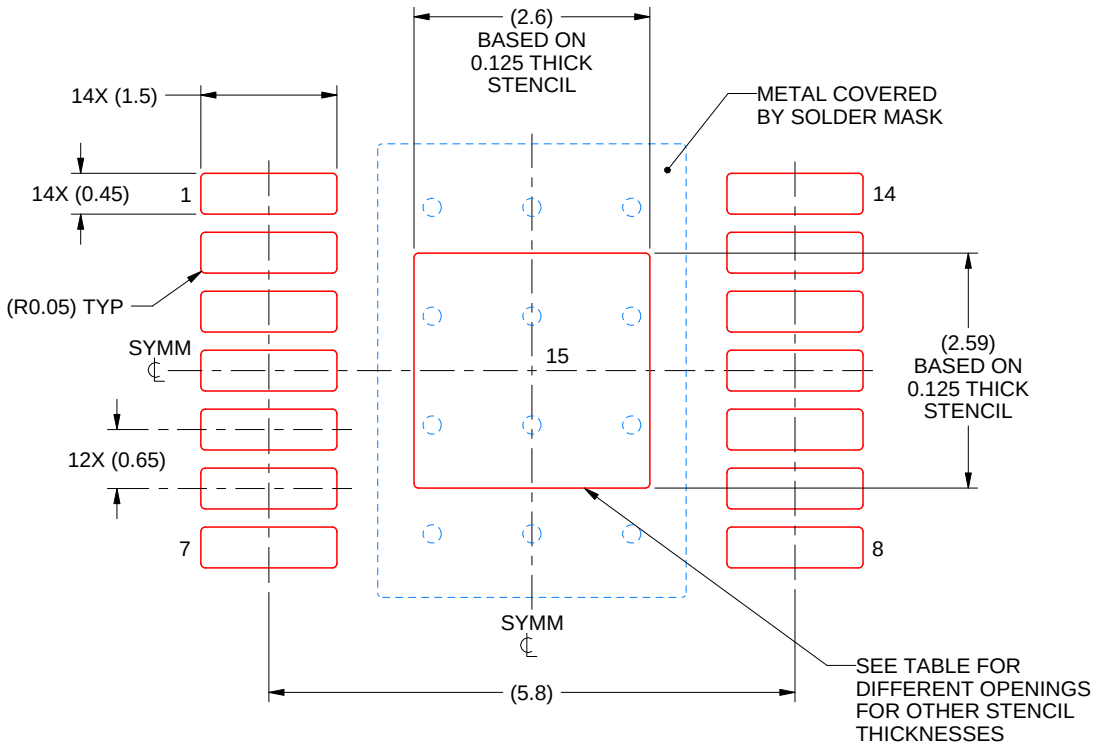


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月