TPA3110D2 15W、フィルタフリー、ステレオ、Class-Dオーディオ・パワー・アンプ、Speakerguard™付き

1 特長

- 16V電源から8Ω負荷へ、10% THD+Nで15W/ch
- 13V電源から8Ω負荷へ、10% THD+Nで10W/ch
- 16V電源から4Ωモノラル負荷へ、10% THD+Nで30W
- 効率90%のClass-D動作によりヒートシンクが不要
- 広い電源電圧範囲: 8V～26Vで動作可能
- フィルタフリー動作
- SpeakerGuard™スピーカー保護機能として可変の電力リミッタとDC保護を搭載
- フロースルーのピン配置により基板のレイアウトを簡単に作成可能
- 自動復帰オプション付きの堅牢なピン間の短絡保護および過熱保護回路
- 非常に優れたTHD+Nおよびポップフリー性能
- 4つの選択可能な固定ゲイン設定
- 差動入力

2 アプリケーション

- TV
- 消費者向けオーディオ機器

3 概要

TPA3110D2デバイスは、ブリッジ結合スピーカーを駆動するための、(1チャネル当たり) 15Wで高効率のClass-Dオーディオ・パワー・アンプです。高度なEMI抑制テクノロジにより、出力に安価なフェライト・ビーズ・フィルタを使用して、EMC要件を満たすことができます。SpeakerGuard™スピーカー保護回路には、可変の電力リミッタと、DC検出回路が内蔵されています。可変の電力リミッタにより、チップの電源よりも低い仮想電圧レールを設定して、スピーカーを流れる電流量を制限できます。DC検出回路は、PWM信号の周波数と振幅を測定し、入力コンデンサが損傷した場合や入力に短絡がある場合に出力段をシャットオフします。

TPA3110D2は、最低4Ωのステレオ・スピーカーを駆動できます。TPA3110D2は90%と高い効率を持つため、音楽の再生時に外部ヒートシンクが不要です。

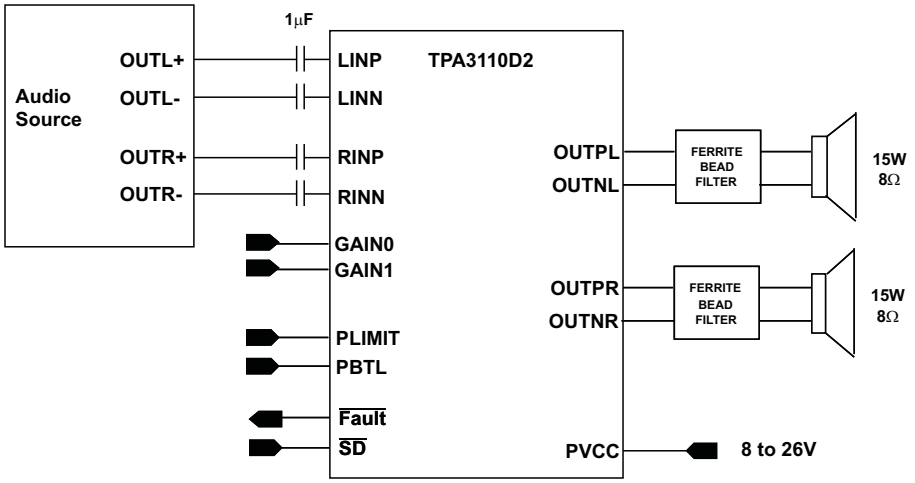
また、出力はGNDやVCCとの短絡や、出力-出力間の短絡に対しても完全に保護されています。この短絡保護と過熱保護回路には、自動復帰機能があります 。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPA3110D2	HTSSOP (28)	9.70mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

TPA3110D2簡易アプリケーション回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (November 2015) から **Revision F** に変更 **Page**

- Added Measurement note added to characterization graphs ... 10
- Added New Output Power vs Supply Voltage Characterization graph ... 10
- Added footnote for heatsink and EVM ... 14

Revision D (July 2012) から **Revision E** に変更 **Page**

- 「*ピン構成および機能* 」セクション、「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

Revision C (August 2010) から **Revision D** に変更 **Page**

- Added < 10 V/ms to V_I in the Absolute Maximum Ratings table, added Note 2 ... 5
- Changed the PBTL Select section. Added text - "The voltage slew.....series with the terminals." ... 19
- Added a 100kΩ resistor to AVCC Pin 14 and Note 1 to Figure 46 ... 24

Revision B (July 2010) から **Revision C** に変更 **Page**

- Replaced the Dissipations Ratings table with the Thermal Information table ... 6

Revision A (July 2009) から **Revision B** に変更 **Page**

- Added slew rate adjustment information ... 17
- Added AVCC to Pin 7 of Figure 46 ... 24

2009年7月発行のものから更新 **Page**

- Changed Changed the Stereo Class-D Amplifier with BTL Output and Single-Ended Input illustration Figure 42 - Corrected the pin names. 21
- Changed Changed the Stereo Class-D Amplifier with PBTL Output and Single-Ended Input illustration Figure 46 - Corrected the pin names. 24

5 Device Comparison Table

DEVICE NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	ADDITIONAL FEATURES
TPA3110D2	Stereo	Class D	15	Power limiter
TPA3130D1	Stereo	Class D	15	
TPA3118D2	Stereo	Class D	30	Power limiter
TPA3116D1	Stereo	Class D	50	Power limiter

6 Pin Configuration and F unctions

PWP Package
28-Pin HTSSOP With PowerPAD™
Top View

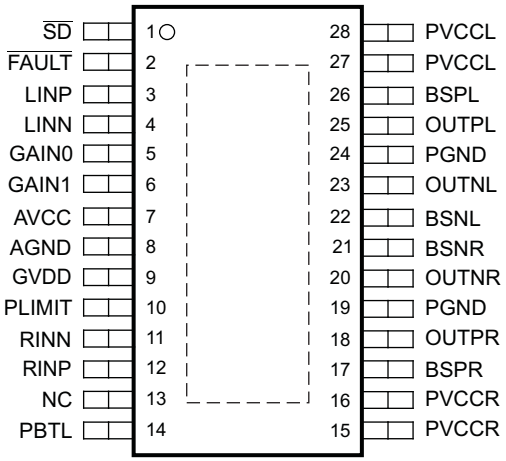


Table 1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
2	$\overline{FAULT}$	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
3	LINP	I	Positive audio input for left channel. Biased at 3 V.
4	LINN	I	Negative audio input for left channel. Biased at 3 V.
5	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
6	GAIN1	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
7	AVCC	P	Analog supply
8	AGND	—	Analog signal ground. Connect to the thermal pad.
9	GVDD	O	High-side FET gate drive supply. Nominal voltage is 7V. Also should be used as supply for PLIMIT function.
10	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
11	RINN	I	Negative audio input for right channel. Biased at 3 V.
12	RINP	I	Positive audio input for right channel. Biased at 3 V.
13	NC	—	Not connected
14	PBTL	I	Parallel BTL mode switch

Table 1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
15	PVCCR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
16	PVCCR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
17	BSPR	I	Bootstrap I/O for right channel, positive high-side FET.
18	OUTPR	O	Class-D H-bridge positive output for right channel.
19	PGND	—	Power ground for the H-bridges.
20	OUTNR	O	Class-D H-bridge negative output for right channel.
21	BSNR	I	Bootstrap I/O for right channel, negative high-side FET.
22	BSNL	I	Bootstrap I/O for left channel, negative high-side FET.
23	OUTNL	O	Class-D H-bridge negative output for left channel.
24	PGND	—	Power ground for the H-bridges.
25	OUTPL	O	Class-D H-bridge positive output for left channel.
26	BSPL	I	Bootstrap I/O for left channel, positive high-side FET.
27	PVCCL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
28	PVCCL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3 V	30 V	V
V_I	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$ (2)	–0.3 V	V_{CC} + 0.3 V	V
				< 10 V/ms	
		PLIMIT	–0.3	GVDD + 0.3	V
		RINN, RINP, LINN, LINP	–0.3	6.3	V
	Continuous total power dissipation		See *Thermal Information*		
R_L	Minimum Load Resistance	BTL: PVCC > 15 V		4.8	
		BTL: PVCC ≤ 15 V		3.2	
		PBTL		3.2	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature range(3)		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100-kΩ resister in series with the pins.
(3) The TPA3110D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$= 100 k, V_{CC}= 26 V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 2 V, V_{CC} = 18 V		50	μA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, PBTL, V_I = 0.8 V, V_{CC} = 18 V		5	μA
T_A	Operating free-air temperature		–40	85	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPA3110D2 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Characteristics: 24 V

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 24 V			32	50	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 24 V			250	400	μA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{on}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		μs
GVDD	Gate Drive Supply	I_{GVDD} = 100 μA		6.4	6.9	7.4	V
t_{DCDET}	DC Detect time	$V_{(RINN)}$ = 6 V, VRINP = 0 V			420		ms

7.6 DC Characteristics: 12 V

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PV_{CC} = 12V			20	35	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PV_{CC} = 12V			200		µA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High Side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2 mA		6.4	6.9	7.4	V
V_O	Output Voltage maximum under PLIMIT control	$V_{(PLIMIT)}$ = 2 V; V_I = 1 V rms		6.75	7.90	8.75	V

7.7 AC Characteristics: 24 V

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, V_{CC} = 16 V		15		W
THD+N	Total harmonic distortion + noise	V_{CC} = 16 V, f = 1 kHz, P_O = 7.5 W (half-power)		0.1%		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

7.8 AC Characteristics: 12 V

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz; V_{CC} = 13 V		10		W
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half-power)		0.06%		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

7.9 Typical Characteristics

All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110D2 EVM which is available at www.ti.com.

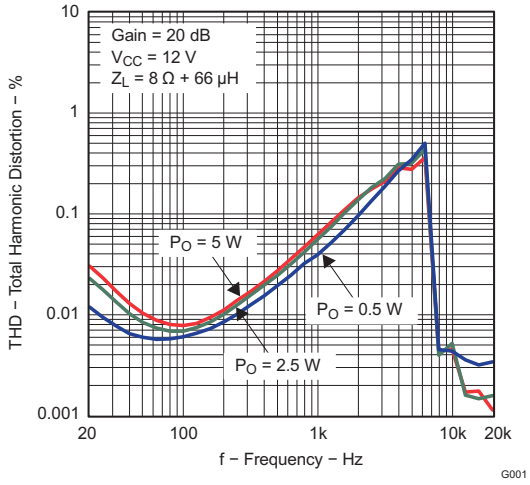


Figure 1. Total Harmonic Distortion vs Frequency (BTL)

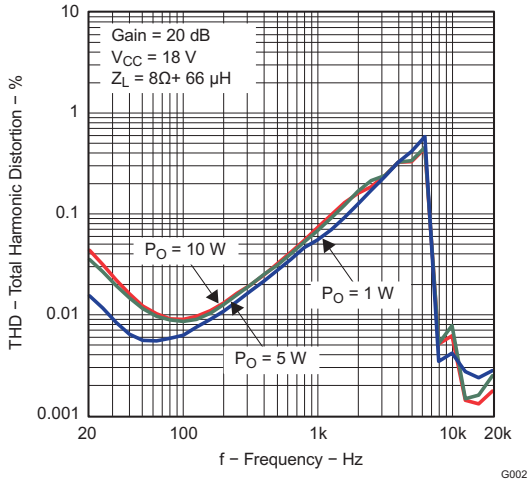


Figure 2. Total Harmonic Distortion vs Frequency (BTL)

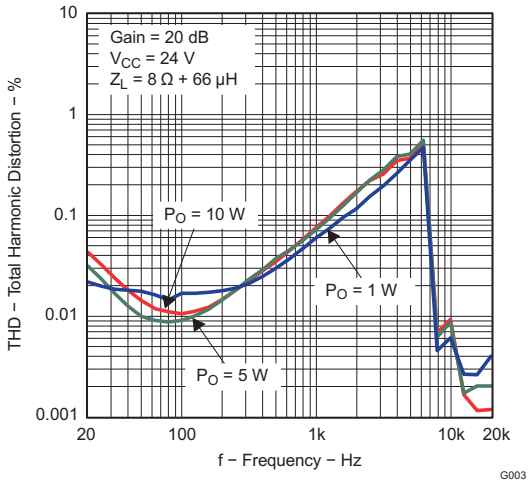


Figure 3. Total Harmonic Distortion vs Frequency (BTL)

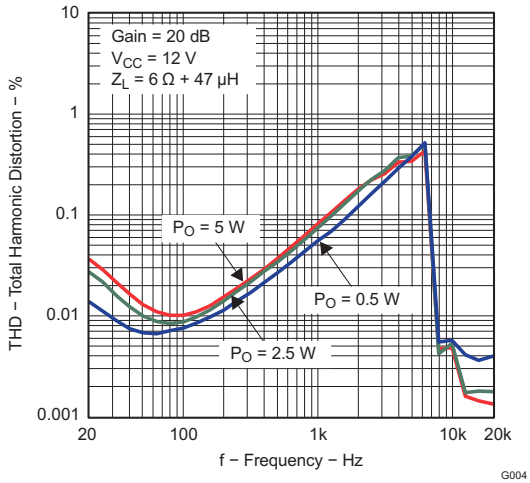


Figure 4. Total Harmonic Distortion vs Frequency (BTL)

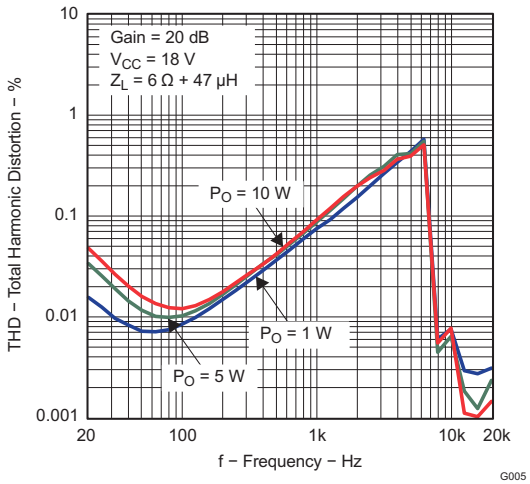


Figure 5. Total Harmonic Distortion vs Frequency (BTL)

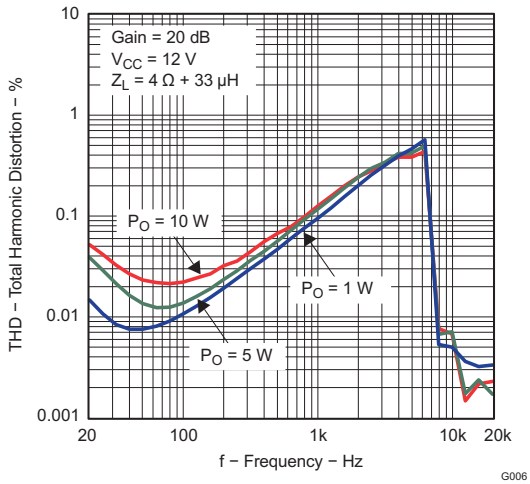


Figure 6. Total Harmonic Distortion vs Frequency (BTL)

Typical Characteristics (continued)

All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110D2 EVM which is available at www.ti.com.

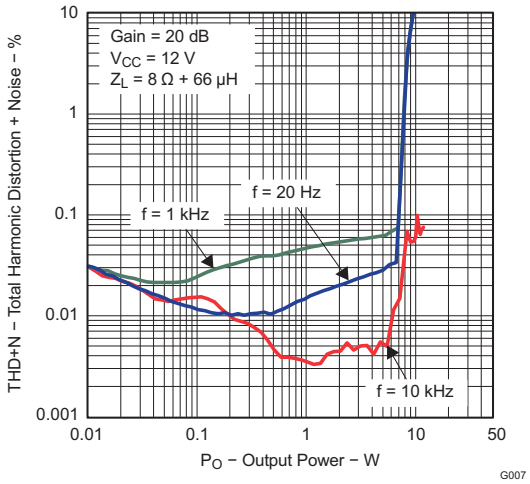


Figure 7. Total Harmonic Distortion + Noise vs Output Power (BTL)

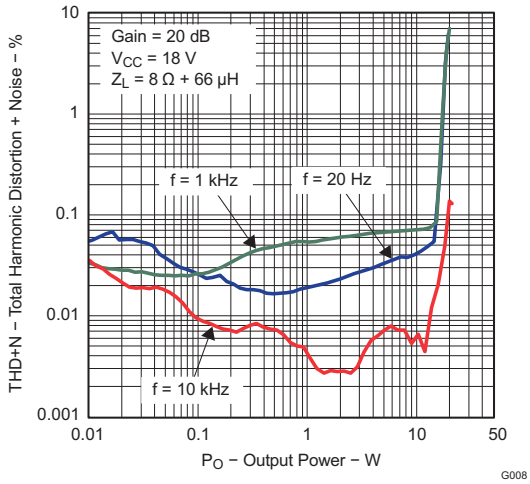


Figure 8. Total Harmonic Distortion + Noise vs Output Power (BTL)

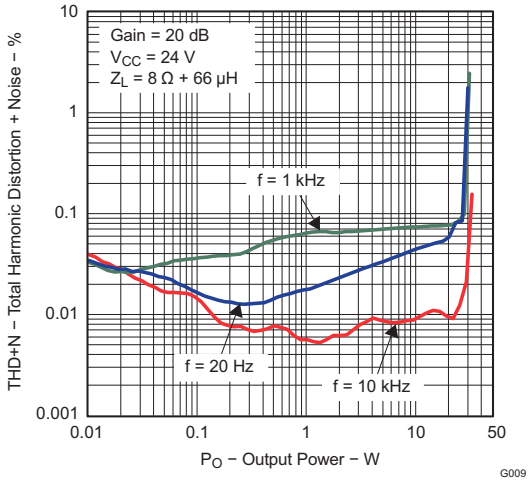


Figure 9. Total Harmonic Distortion + Noise vs Output Power (BTL)

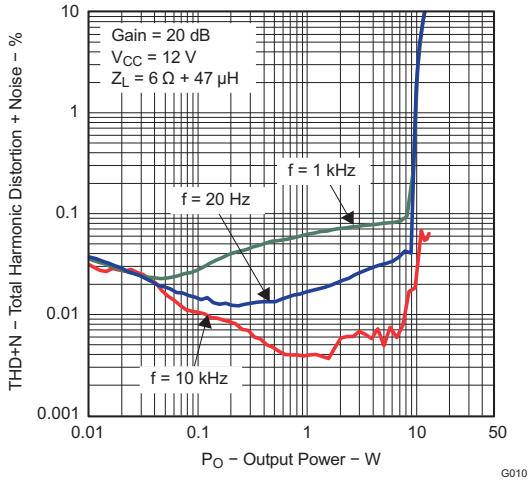


Figure 10. Total Harmonic Distortion + Noise vs Output Power (BTL)

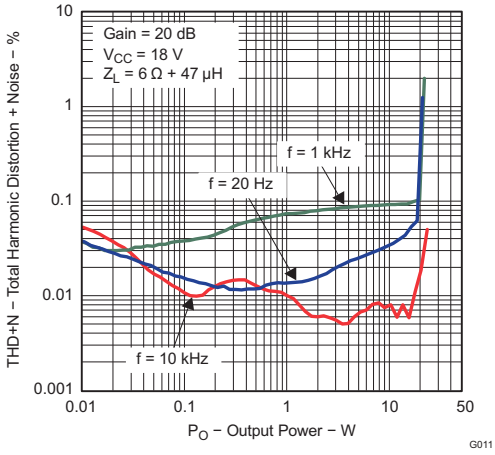


Figure 11. Total Harmonic Distortion + Noise vs Output Power (BTL)

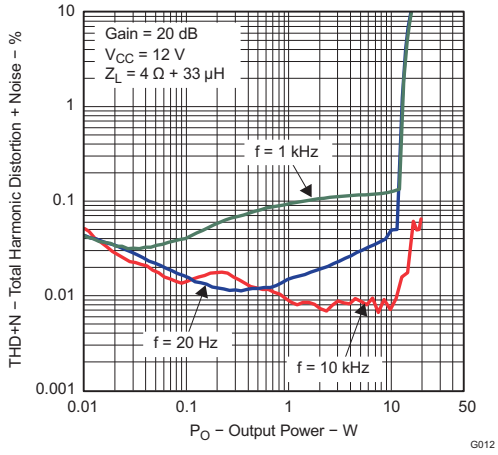


Figure 12. Total Harmonic Distortion + Noise vs Output Power (BTL)

Typical Characteristics (continued)

All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110D2 EVM which is available at www.ti.com.

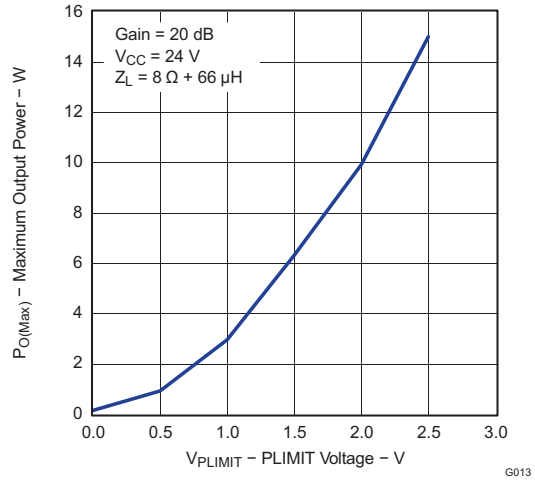
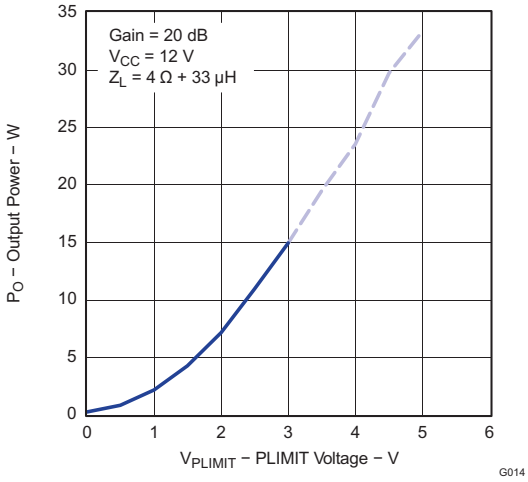


Figure 13. Maximum Output Power vs PLIMIT Voltage (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 14. Output Power vs PLIMIT Voltage (BTL)

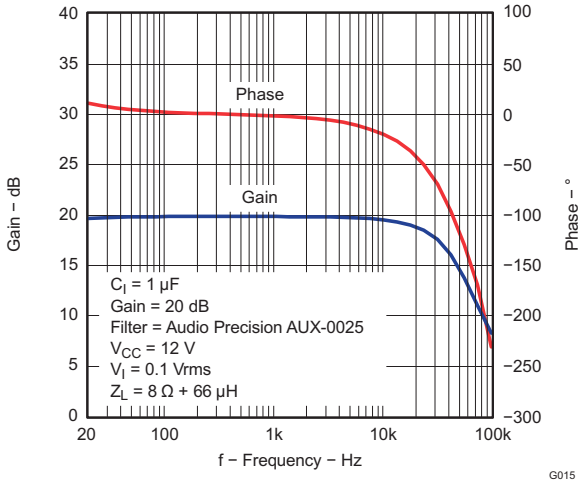
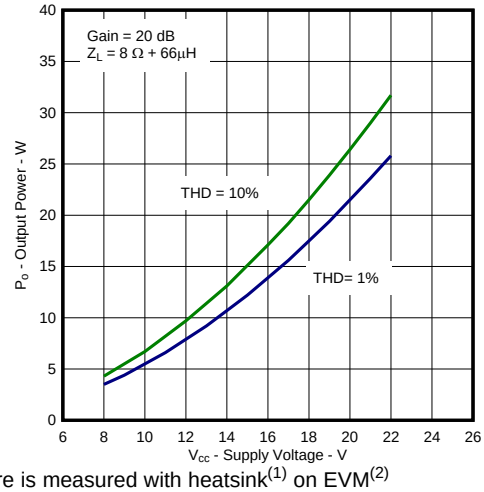
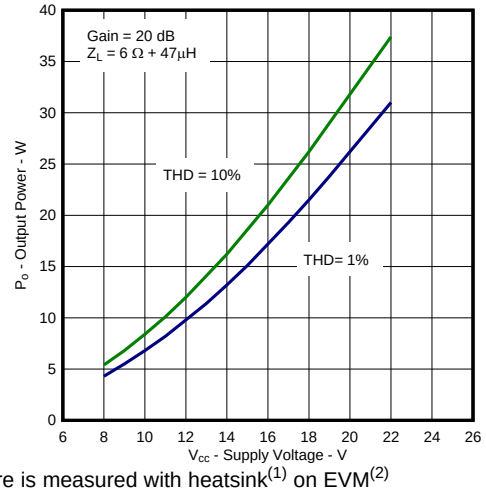


Figure 15. Gain and Phase vs Frequency (BTL)



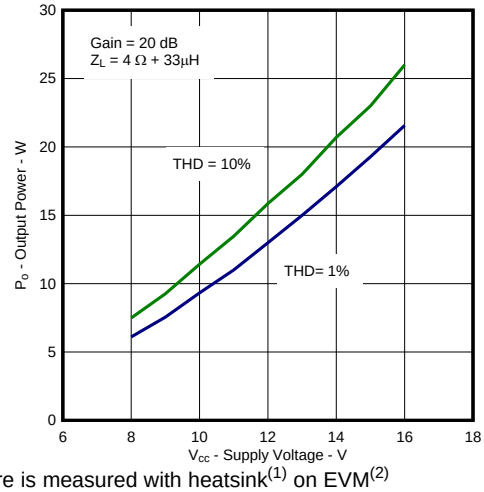
The figure is measured with heatsink(1) on EVM(2)

Figure 16. Output Power vs Supply Voltage (BTL)



The figure is measured with heatsink(1) on EVM(2)

Figure 17. Output Power vs Supply Voltage (BTL)

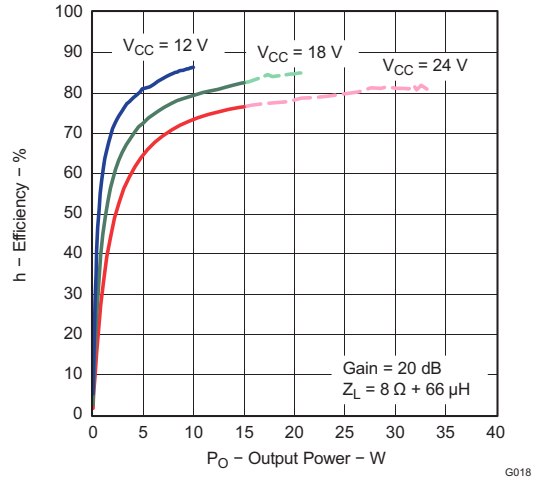


The figure is measured with heatsink(1) on EVM(2)

Figure 18. Output Power vs Supply Voltage (BTL)

Typical Characteristics (continued)

All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110D2 EVM which is available at www.ti.com.



Note: Dashed Lines represent thermally limited regions.

Figure 19. Efficiency vs Output Power (BTL)

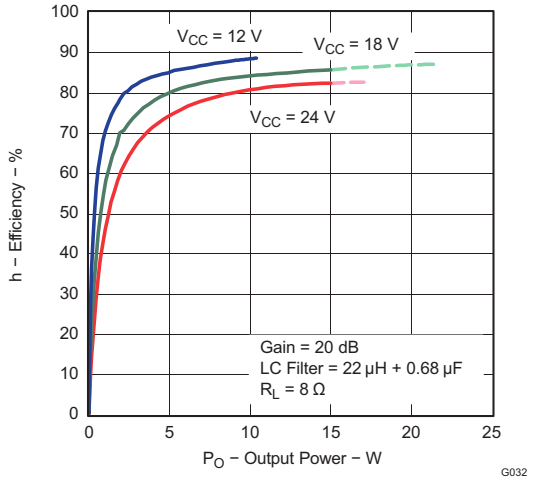
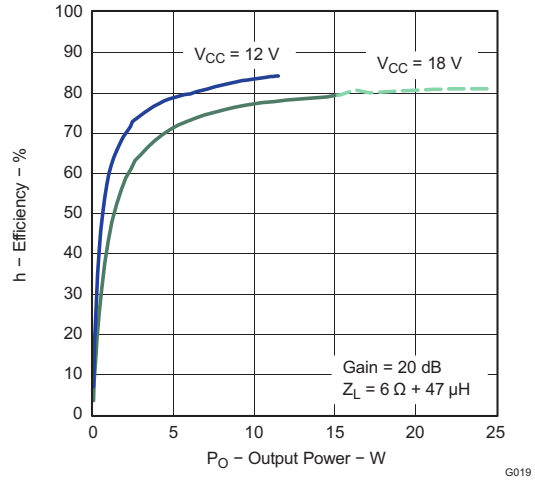


Figure 20. Efficiency vs Output Power (BTL With LC Filter)



Note: Dashed Lines represent thermally limited regions.

Figure 21. Efficiency vs Output Power (BTL)

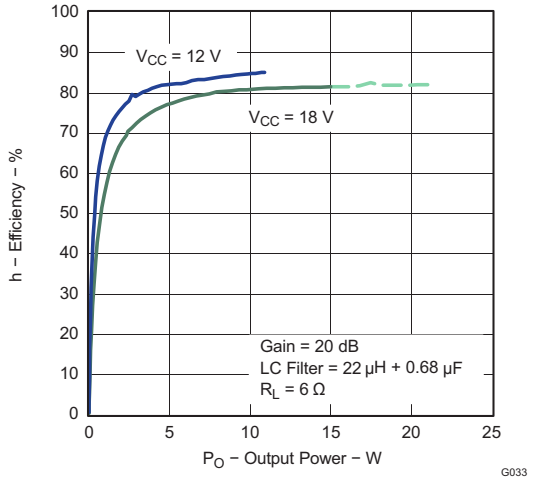


Figure 22. Efficiency vs Output Power (BTL With LC Filter)

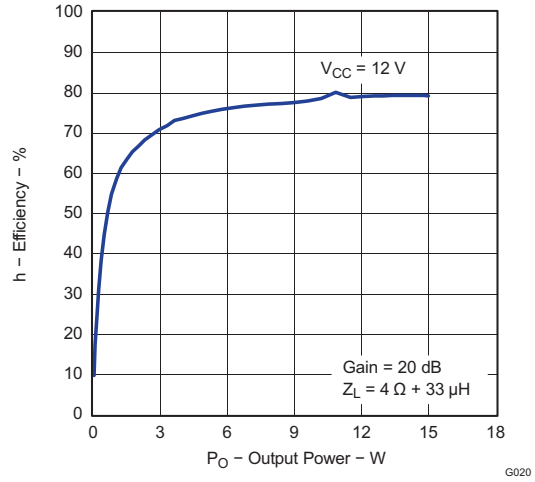


Figure 23. Efficiency vs Output Power (BTL)

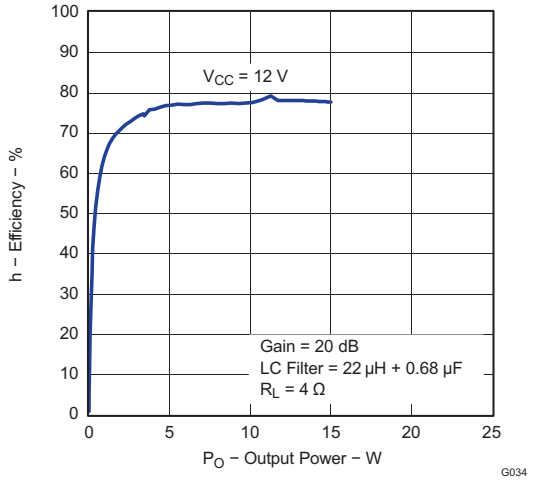
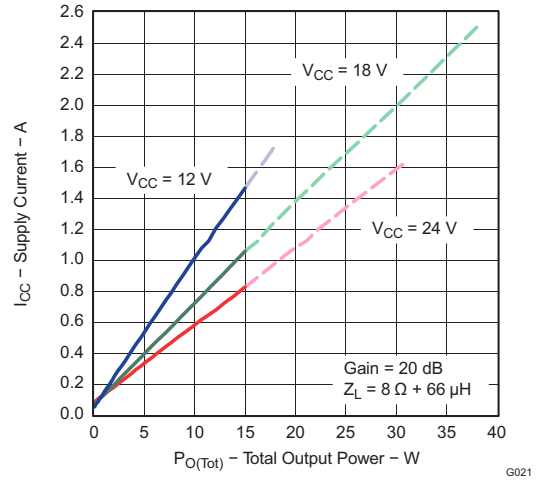


Figure 24. Efficiency vs Output Power (BTL With LC Filter)

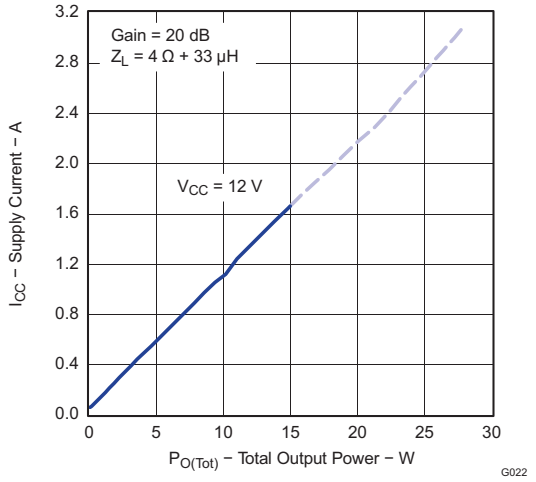
Typical Characteristics (continued)

All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110D2 EVM which is available at www.ti.com.



Note: Dashed Lines represent thermally limited regions.

Figure 25. Supply Current vs Total Output Power (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 26. Supply Current vs Total Output Power (BTL)

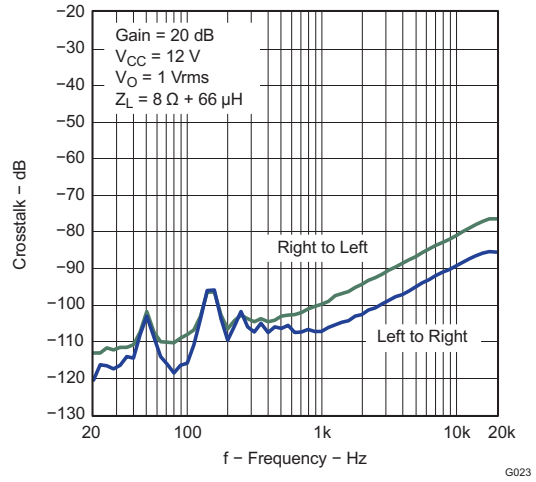


Figure 27. Crosstalk vs Frequency (BTL)

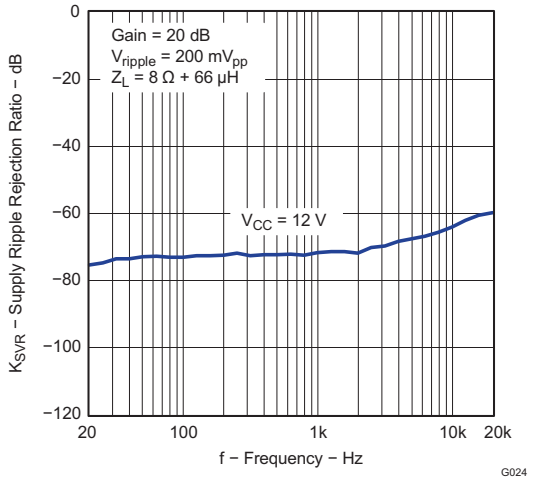


Figure 28. Supply Ripple Rejection Ratio vs Frequency (BTL)

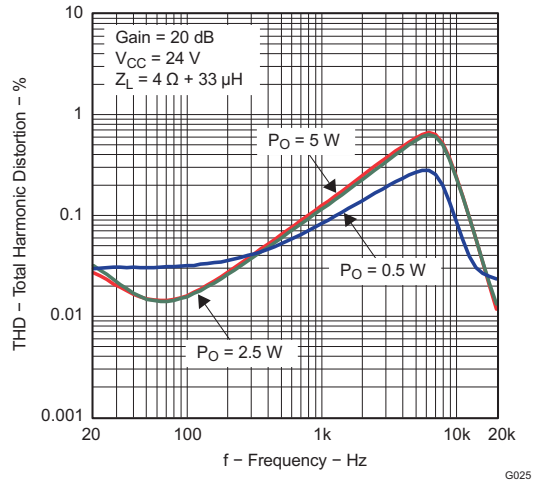


Figure 29. Total Harmonic Distortion vs Frequency (PBTL)

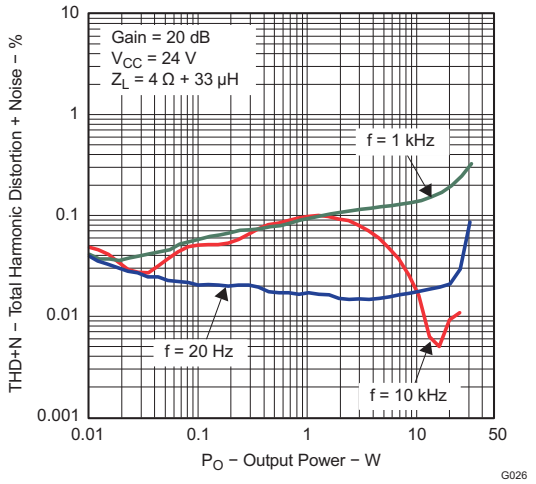


Figure 30. Total Harmonic Distortion + Noise vs Output Power (PBTL)

Typical Characteristics (continued)

All Measurements taken at 1 kHz, unless otherwise noted. Measurements were made using the TPA3110D2 EVM which is available at www.ti.com.

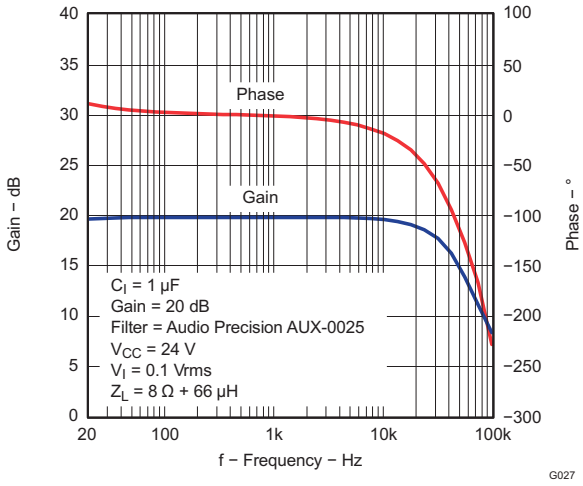
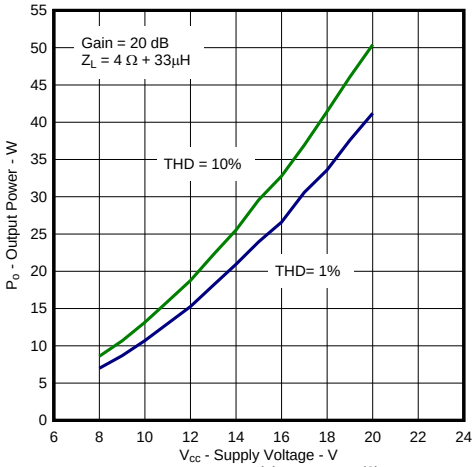


Figure 31. Gain and Phase vs Frequency (PBTL)



The figure is measured with heatsink(1) on EVM(2)

Figure 32. Output Power vs Supply Voltage (PBTL)

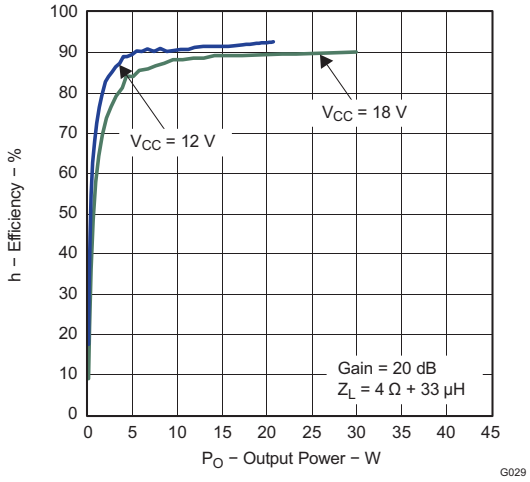


Figure 33. Efficiency vs Output Power (PBTL)

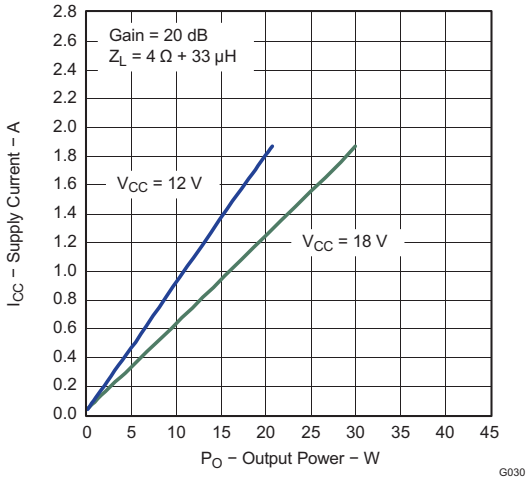


Figure 34. Supply Current vs Output Power (PBTL)

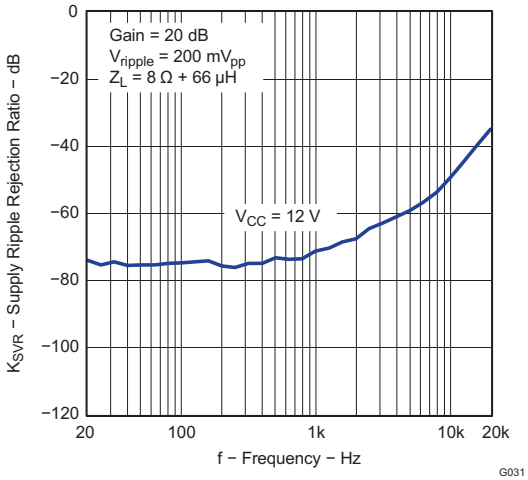


Figure 35. Supply Ripple Rejection Ratio vs Frequency (PBTL)

(1) Detailed parameters of heatsink: please refer to datasheet heatsink with part number ATS-TI10P-521-C1-R1.
(2) Related parameters of the two-layer EVM: copper thickness of top layer and bottom layer are both 0.03556mm.

8 Parameter Measurement Information

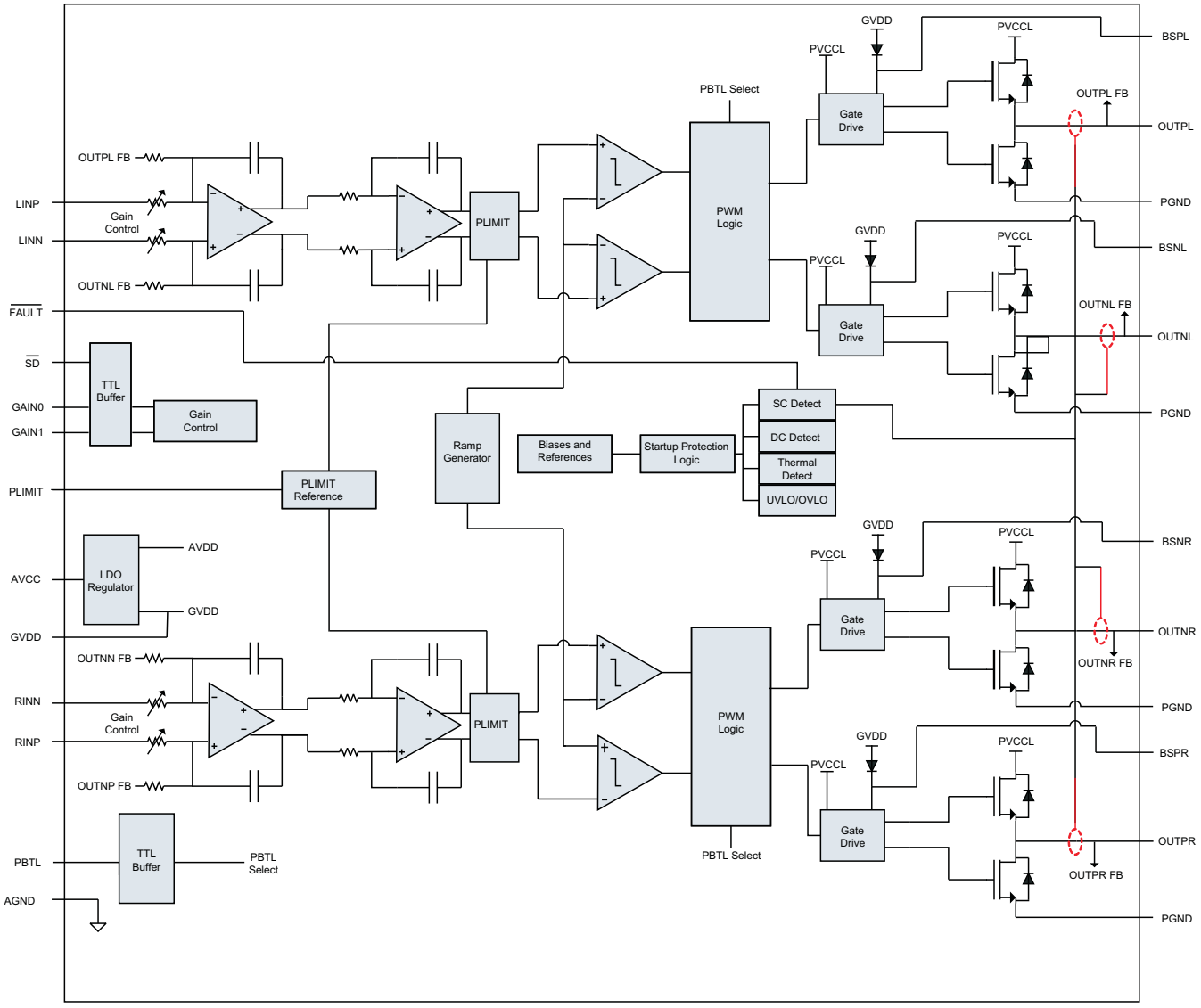
All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

The TPA3110D2 is a 15-W Class-D audio power amplifier. It is designed to drive BTL stereo speakers. This device is able to use inexpensive ferrite bead filters at the outputs while meeting EMC requirements. The TPA3110D2 can drive stereo speakers as low as 4 Ω and its high efficiency eliminates the need for an external heat sink. The device is fully protected against shorts to GND, VCC and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 TPA3110D2 Modulation Scheme

The TPA3110D2 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

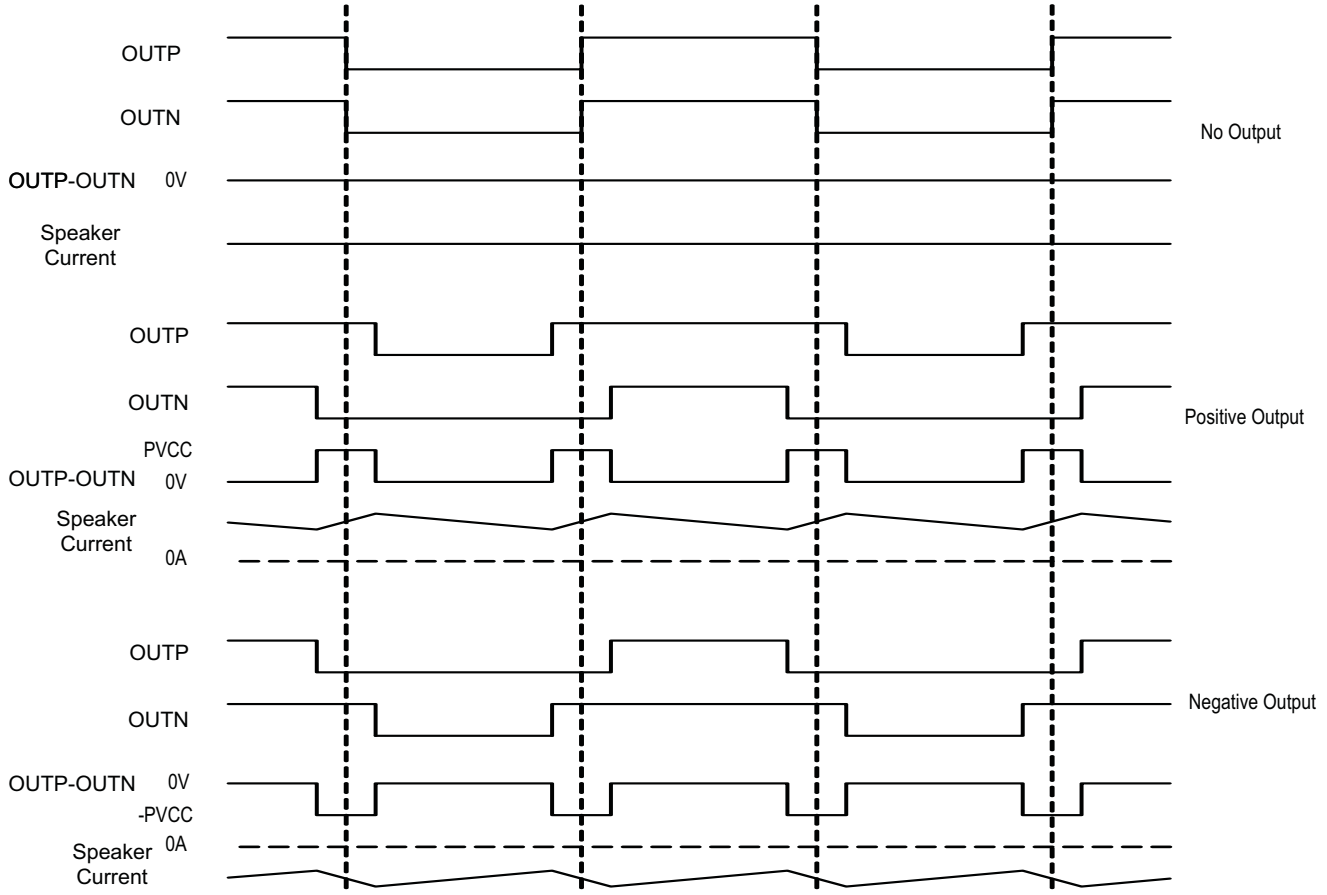


Figure 36. The TPA3110D2 Output Voltage And Current Waveforms Into An Inductive Load

9.3.1.1 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3110D2 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Feature Description (continued)

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3110D2 include 28L0138-80R-10 and HI1812V101R-10 from Steward and the 742792510 from Wurth Electronics.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPAD™ beneath the chip.

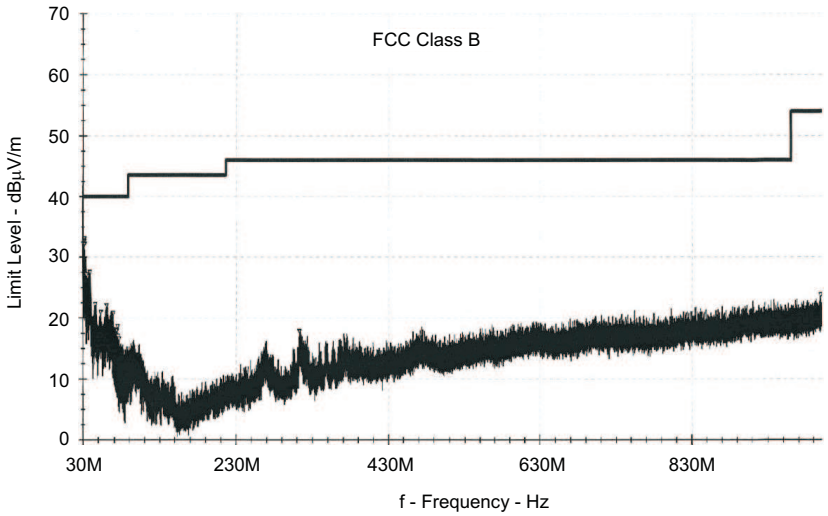


Figure 37. TPA3110D2 EMC Spectrum With FCC Class B Limits

9.3.1.2 Efficiency: LC Filter Required With The Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3110D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

Feature Description (continued)

9.3.1.3 When to Use an Output Filter for EMI Suppression

The TPA3110D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3110D2 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

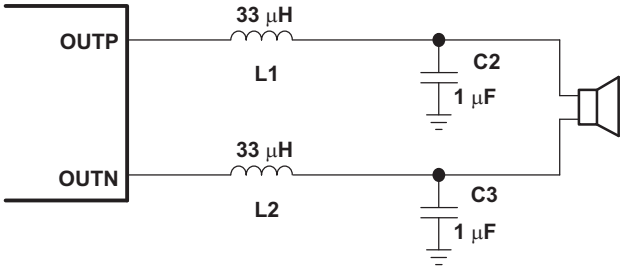


Figure 38. Typical LC Output Filter, Cutoff Frequency of 27 Khz, Speaker Impedance = 8 Ω

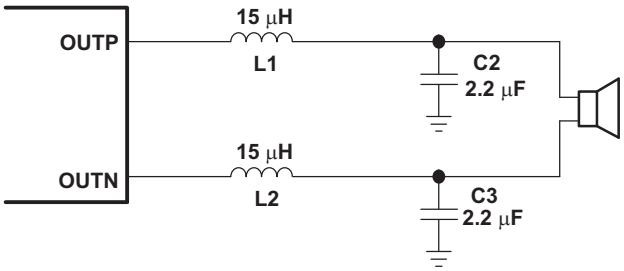


Figure 39. Typical Lc Output Filter, Cutoff Frequency Of 27 Khz, Speaker Impedance = 4 Ω

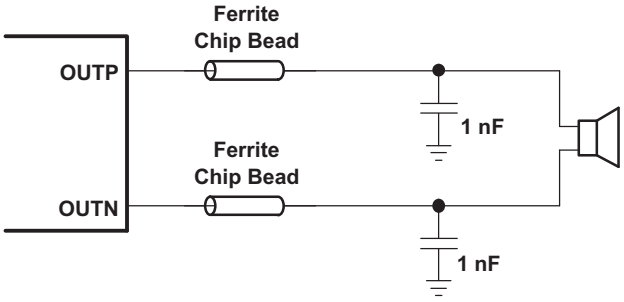


Figure 40. Typical Ferrite Chip Bead Filter (Chip Bead Example)

9.3.2 Gain Setting Via GAIN0 And GAIN1 Inputs

The gain of the TPA3110D2 is set by two input terminals, GAIN0 and GAIN1. The voltage slew rate of these gain terminals, along with terminals 1 and 14, must be restricted to no more than 10V/ms. For higher slew rates, use a 100kΩ resistor in series with the terminals.

Feature Description (continued)

The gains listed in Table 2 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the TPA3110D2. At the lower gain settings, the input impedance could increase as high as 72 kΩ

Table 2. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

9.3.3 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3110D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3110D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

9.3.4 PLIMIT

The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1μF capacitor from pin 10 to ground.

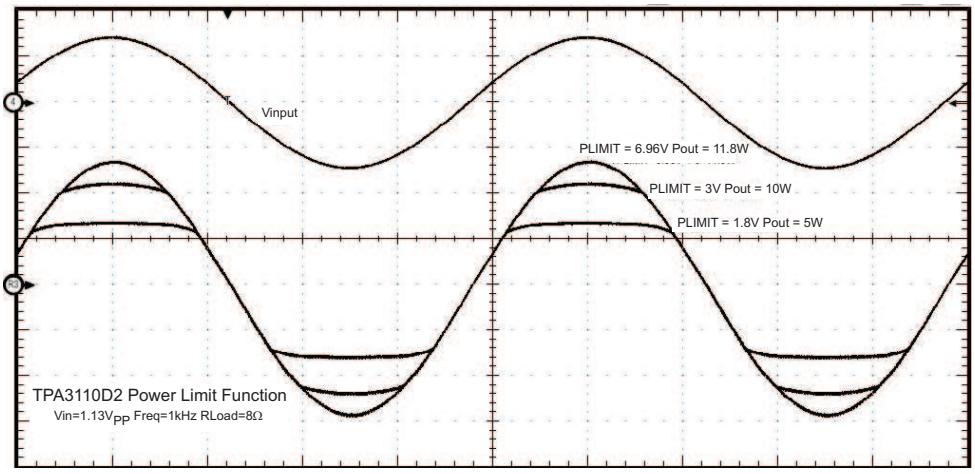


Figure 41. PLIMIT Circuit Operation

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a *virtual* voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

Where:

- R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.
- R_L is the load resistance.
- V_P is the peak amplitude of the output possible within the supply rail.
- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped) (1)

Table 3. PLIMIT Typical Operation

TEST CONDITIONS	PLIMIT VOLTAGE	OUTPUT POWER (W)	OUTPUT VOLTAGE AMPLITUDE (V_{P-P})
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	6.97	36.1 (thermally limited)	43
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	2.94	15	25.2
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	2.34	10	20
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	1.62	5	14
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	6.97	12.1	27.7
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	3.00	10	23
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.86	5	14.8
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	6.97	10.55	23.5
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.76	5	15

9.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1-μF capacitor to ground at this pin.

9.3.6 PBTL Select

TPA3110D2 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. The voltage slew rate of the PBTL pin must be restricted to no more than 10V/ms. For higher slew rates, use a 100kΩ resistor in series with the terminals. For an example of the PBTL connection, see the schematic in the APPLICATION INFORMATION section.

For normal BTL operation, connect the PBTL pin to local ground.

9.3.7 Thermal Protection

Thermal protection on the TPA3110D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ terminal.

9.3.8 DC Detect

TPA3110D2 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the $\overline{\text{FAULT}}$ pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling $\overline{\text{SD}}$ will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, +57%, -43%) for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the $\overline{\text{SD}}$ pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum differential input voltages required to trigger the DC detect are show in table 2. The inputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 4. DC Detect Threshold

AV(dB)	Vin (mV, differential)
20	112
26	56
32	28
36	17

9.3.9 Short-Circuit Protection and Automatic Recovery Feature

TPA3110D2 has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the short-circuit protection latch.

9.4 Device Functional Modes

9.4.1 $\overline{\text{SD}}$ Operation

The TPA3110D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SD}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SD}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SD}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section describes a stereo BTL application and a mono PBTL application. In the stereo application the Power Limiter is implemented, however in the mono application this limiter is not used.

10.2 Typical Applications

10.2.1 Stereo Class-D Amplifier With BTL Output and Single-Ended Inputs With Power Limiting

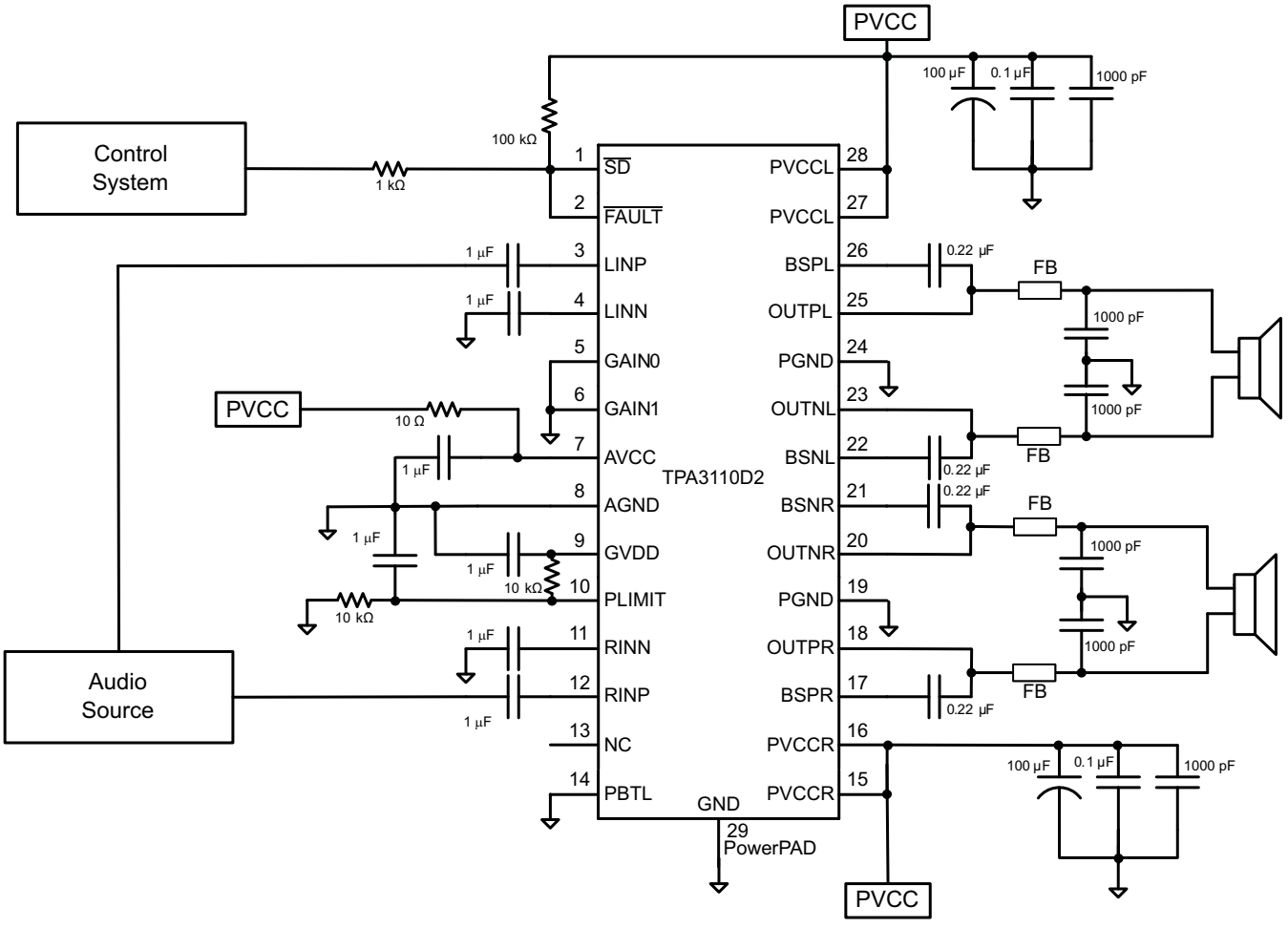


Figure 42. Typical Application Schematic With BTL Output and Single-Ended Inputs With Power Limiting

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 5.

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power supply	8 V to 26 V
Shutdown, gain, and PBTL controls	High > 2 V
	Low < 0.8 V
Speaker impedance BTL	4 to 8 Ω
Speaker impedance PBTL	2 to 8 Ω

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency may change when changing gain steps.

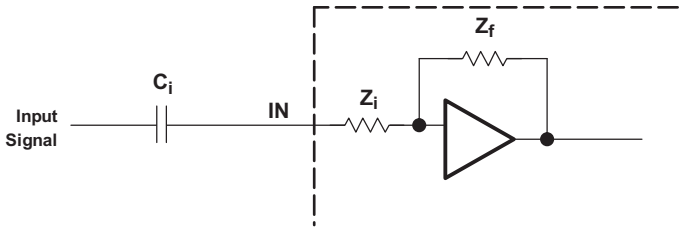


Figure 43. Input Impedance of the TPA3110D2

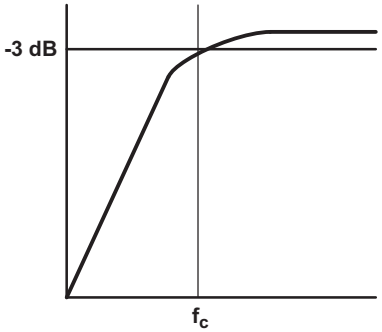
The –3-dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 2.

$$f = \frac{1}{2\pi Z_i C_i} \tag{2}$$

10.2.1.2.2 Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \tag{3}$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{4}$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 2 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

10.2.1.2.3 BSN and BSP Capacitors

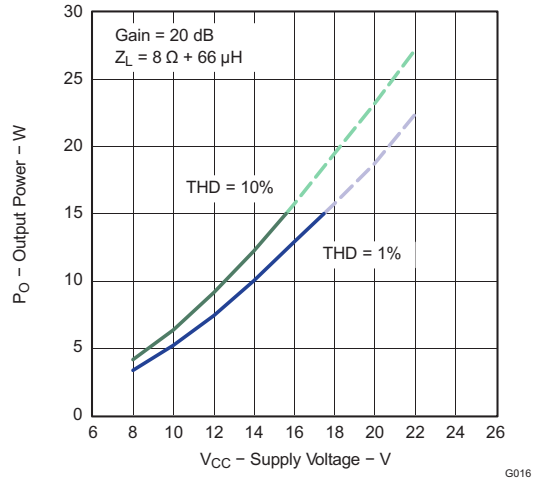
The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22 µF capacitor must be connected from OUTPx to BSPx, and one 0.22 µF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 42.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

10.2.1.2.4 Using Low-ESR Capacitors

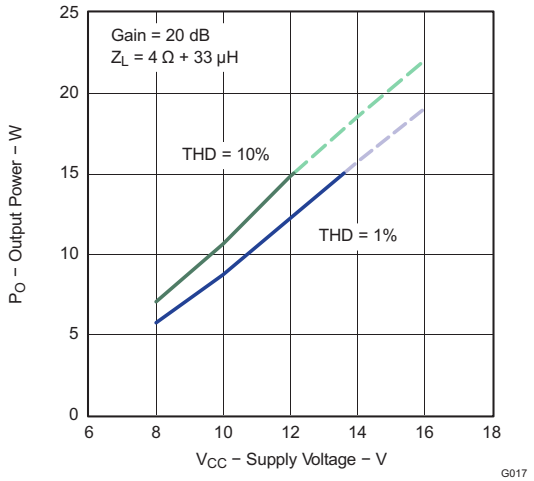
Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

10.2.1.3 Application Curves



Note: Dashed Lines represent thermally limited regions.

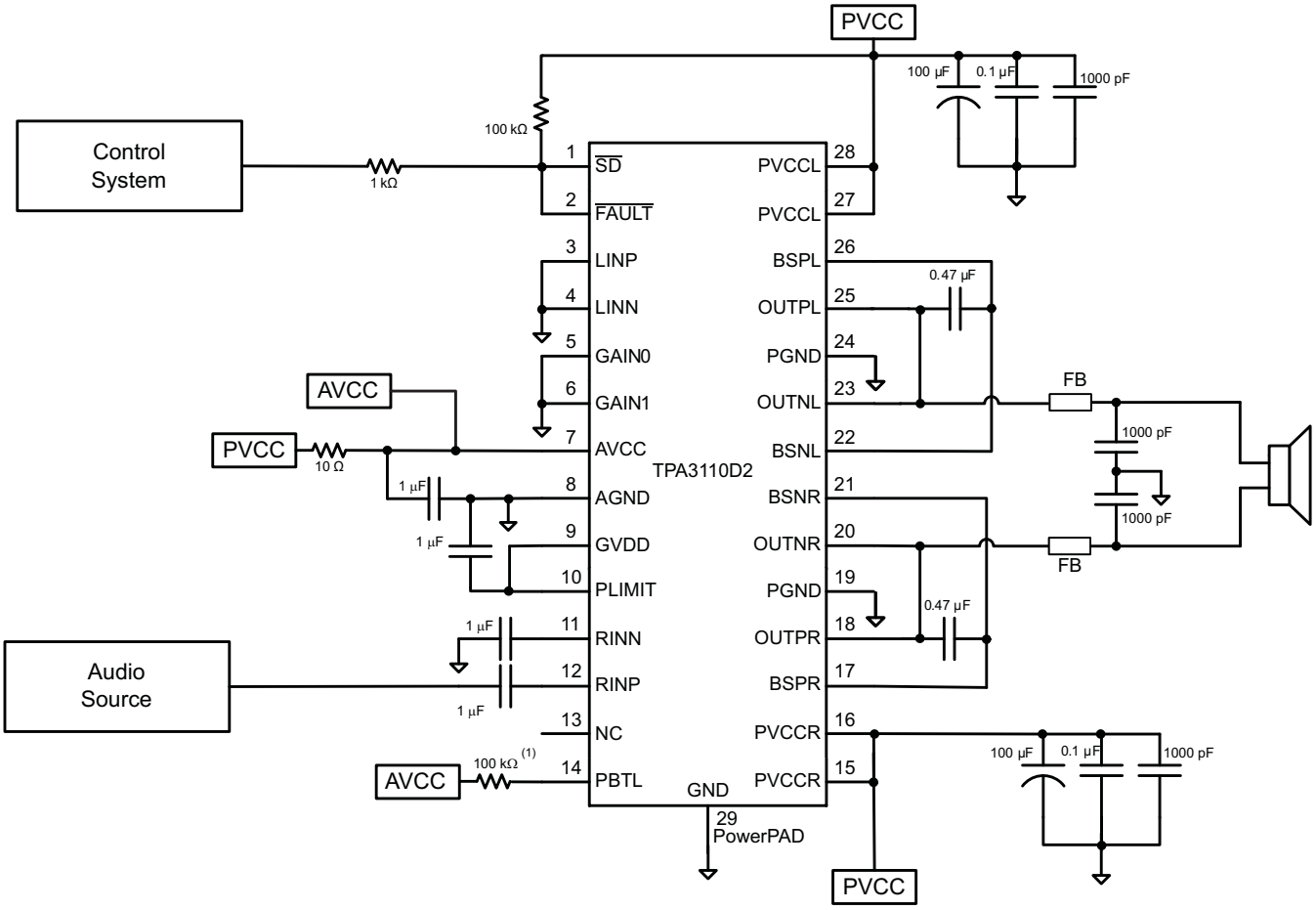
Figure 44. Output Power vs Supply Voltage (BTL)



Note: Dashed Lines represent thermally limited regions.

Figure 45. Output Power vs Supply Voltage (BTL)

10.2.2 Stereo Class-D Amplifier With PBTL Output and Single-Ended Input



(1) 100 kΩ resistor is needed if the PVCC slew rate is more than 10 V/ms.

Figure 46. Typical Application Schematic With PBTL Output and Single-Ended Input

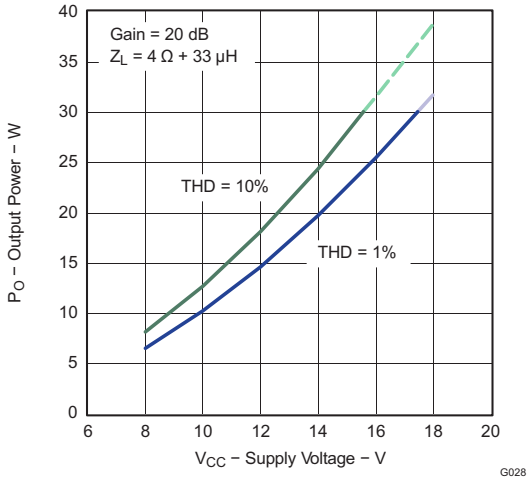
10.2.2.1 Design Requirements

Refer to Table 5 for the *Stereo Class-D Amplifier With PBTL Output and Single-Ended Input* Application Design Requirements.

10.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the *Stereo Class-D Amplifier With PBTL Output and Single-Ended Input* Application Detailed Design Procedure.

10.2.2.3 Application Curve



Note: Dashed Lines represent thermally limited regions.

Figure 47. Output Power vs Supply Voltage (PBTL)

11 Power Supply Recommendations

The TPA3110D2 is designed to operate form an input voltage supply range between 8-V and 26-V. Therefore, the output voltage range of power supply should be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling, C_S

The TPA3110D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPAD™) as possible.

For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 µF to 1 µF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 µF or greater placed near the audio power amplifier is recommended.

The 220-µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 µF or larger capacitor should be placed on each PVCC terminal. A 10-µF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

12 Layout

12.1 Layout Guidelines

The TPA3110D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3110D2 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR

Layout Guidelines (continued)

ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1μF and 1μF also of good quality to the PVCC connections at each end of the chip.

- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 7) decoupling capacitor should be grounded to analog ground (AGND). The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3110D2.
- Output filter—The ferrite EMI filter (Figure 40) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 38 and Figure 39) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46mm by 2.35mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3110D2 Evaluation Module (TPA3110D2EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at www.ti.com.

12.2 Layout Example

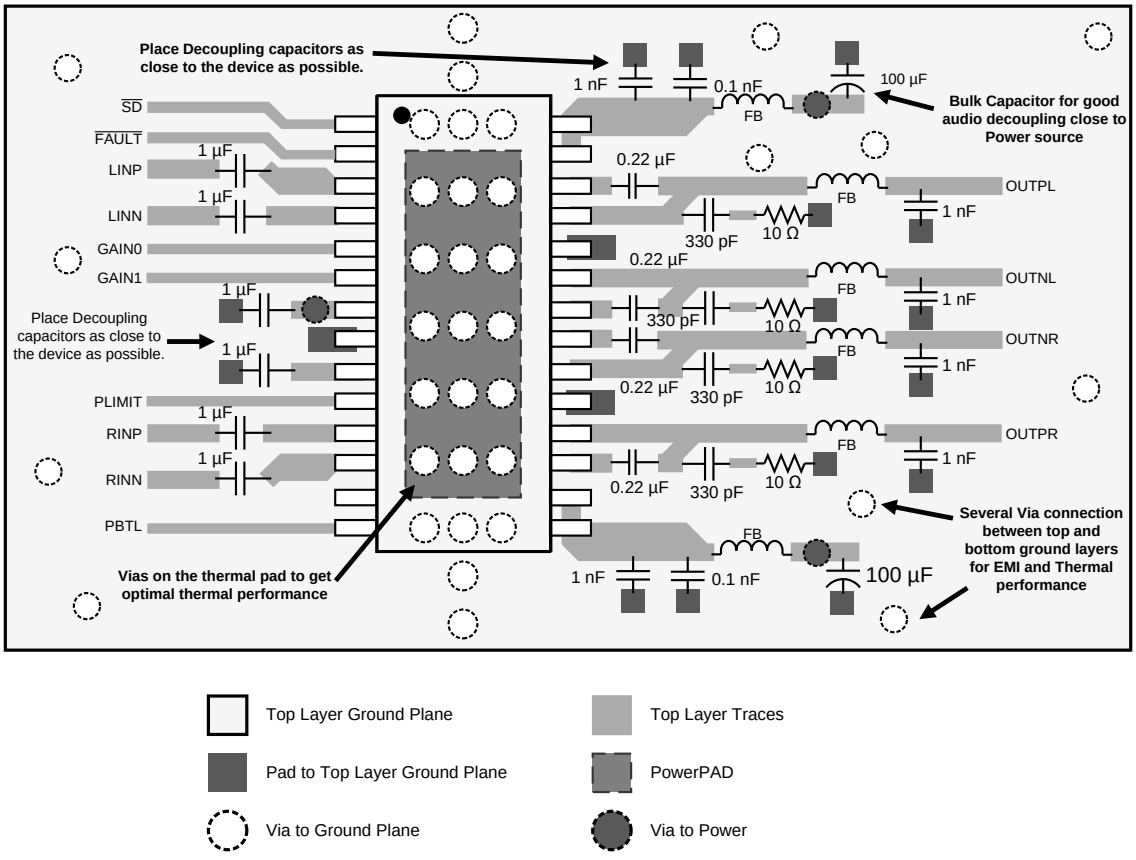


Figure 48. TPA3110D2 PCB Layout

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 開発サポート

TPA3110D2 TINA-TIリファレンス・デザインについては、SLAM052を参照してください。

TPA3110D2 TINA-TIのSpiceモデルについては、SLAM053を参照してください。

13.2 ドキュメントのサポート

13.2.1 関連資料

関連資料については、以下を参照してください。

- アプリケーション・レポート、*『放熱特性の優れたPowerPAD™パッケージ』*、SLMA002
- アプリケーション・レポート、*『アナログ部品のための熱量計算ツールの使用』*、SLUA566
- アプリケーション・レポート、*『AN-1737 Class Dオーディオ・アプリケーションにおけるEMIの管理』*、SNAA050
- アプリケーション・レポート、*『AN-1849 オーディオ・アンプ電源設計』*、SNAA057
- アプリケーション・レポート、*『オーディオ・パワー・アンプ性能測定のガイドライン』* SLOA068
- ユーザーズ・ガイド、*『TPA3110D2 EVMオーディオ・アンプ評価ボード』*、SLOU263

13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.4 商標

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3110D2PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWP.B	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWPRG4	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWPRG4.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2
TPA3110D2PWPRG4.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3110D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPA3110D2 :

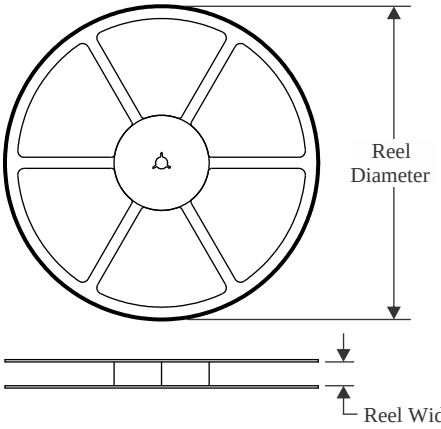
- Automotive : TPA3110D2-Q1

NOTE: Qualified Version Definitions:

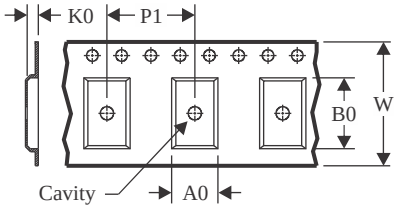
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

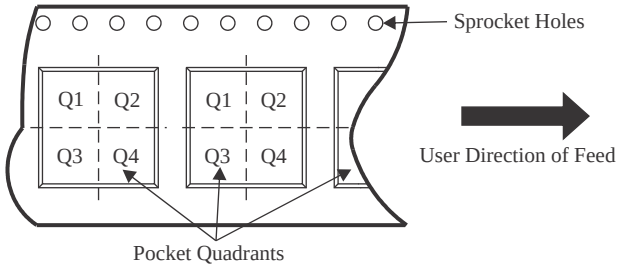


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

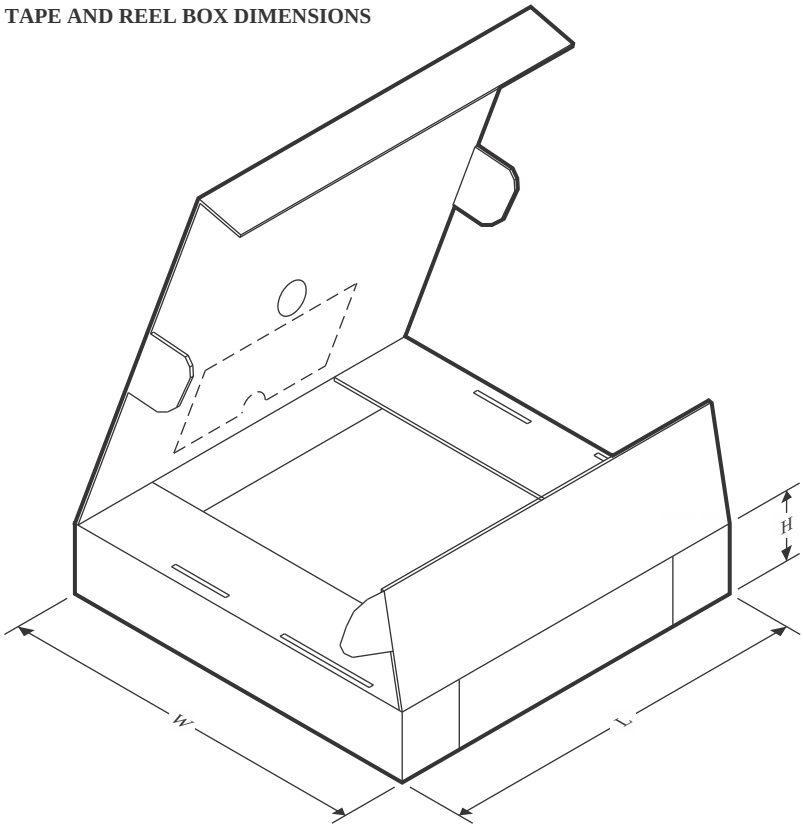
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3110D2PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPA3110D2PWPRG4	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

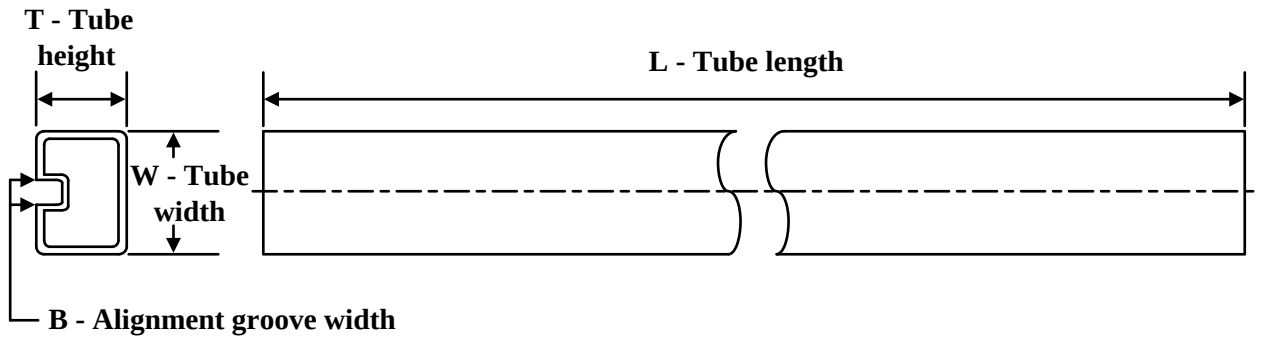
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3110D2PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPA3110D2PWPRG4	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3110D2PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA3110D2PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA3110D2PWP.B	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

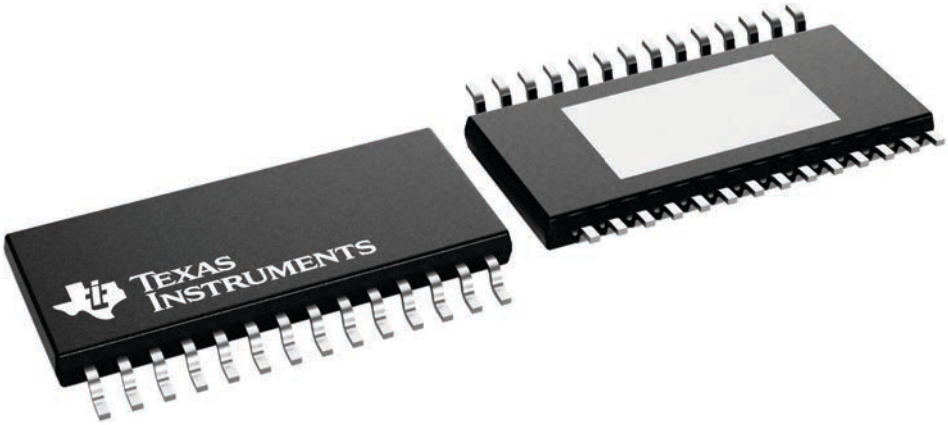
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

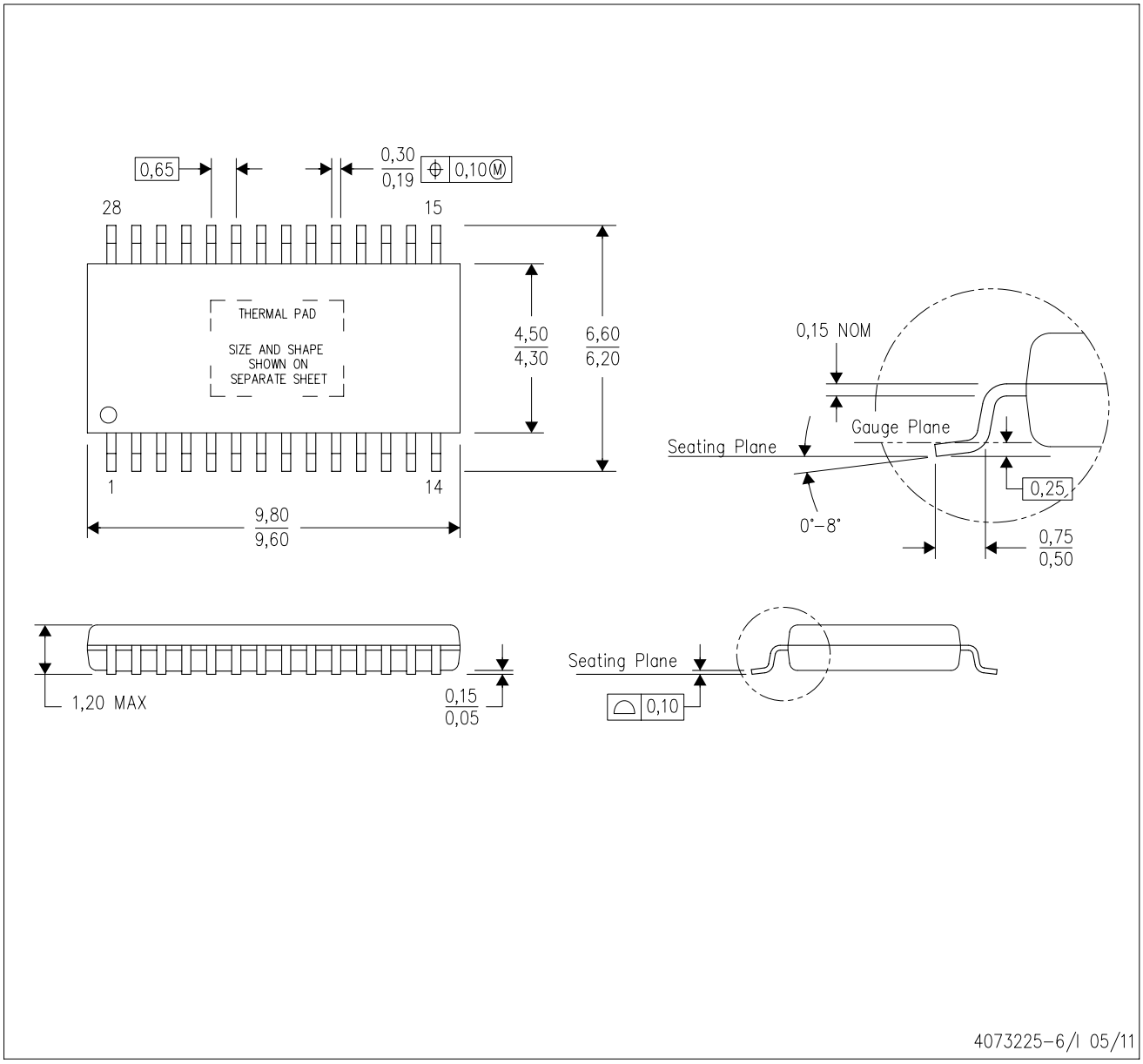
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

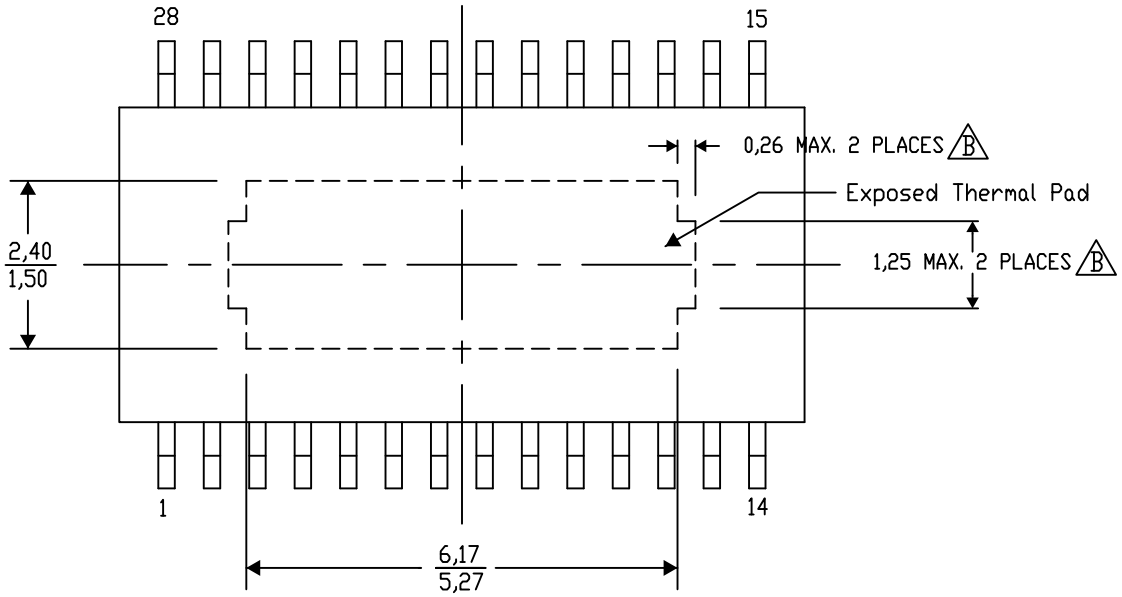
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

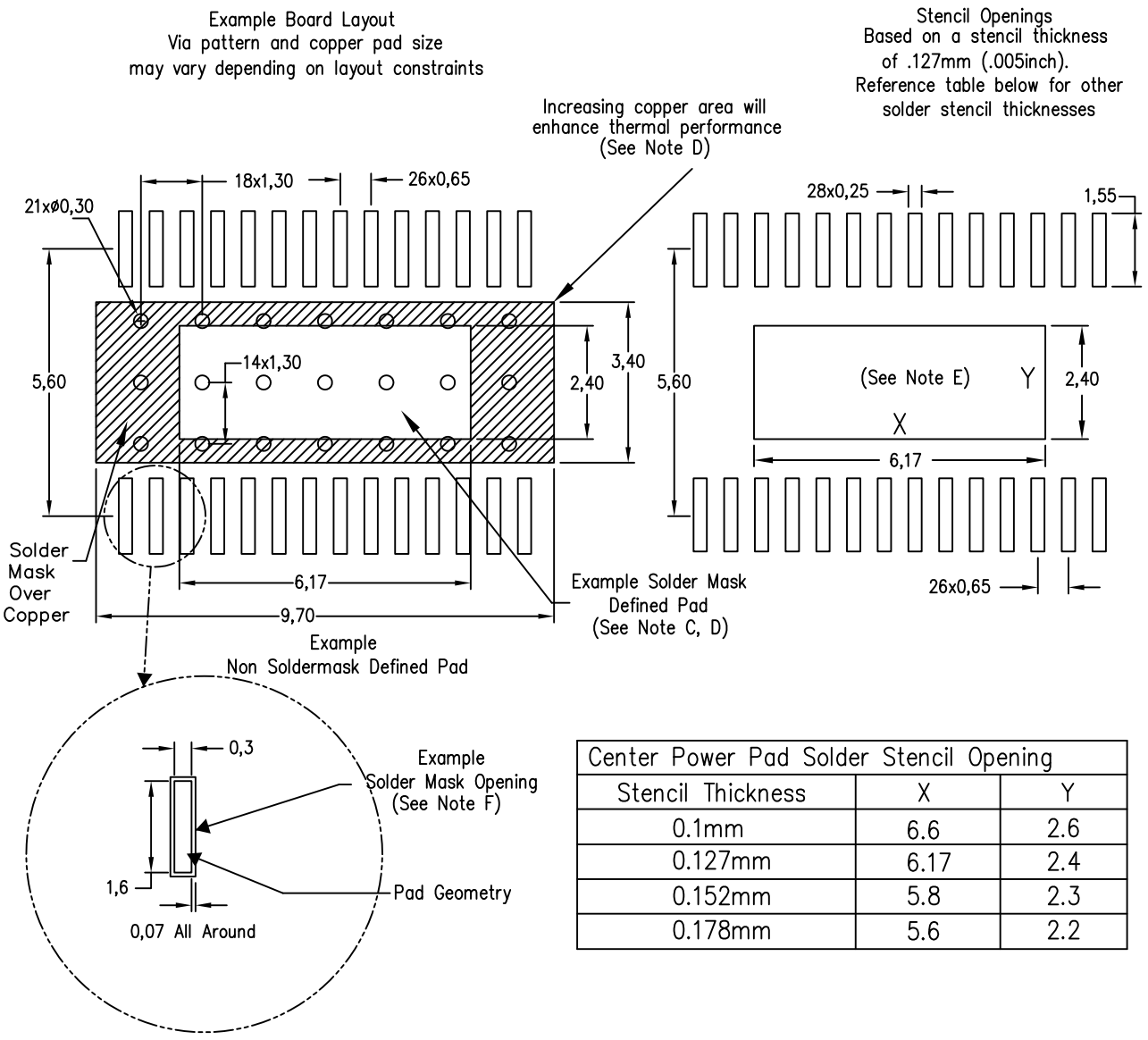
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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最終更新日：2025 年 10 月