TEXAS INSTRUMENTS
TDP2004
JAJSSB8 – NOVEMBER 2023

TDP2004 4 チャネル 20Gbps DisplayPort 2.1 リニア リドライバ

1 特長

- 最大 20Gbps の DisplayPort 2.1 をサポート - RBR、HBRx、UHBRx
- 最大 20Gbps までのほとんどの AC 結合インターフェイスをサポートする、プロトコルに依存しないリニア イコライザ
- 20Gbps (10Ghz ナイキスト) での優れた電気的性能:
  - 19dB のイコライゼーション
  - 1.8V DC の直線性、1.08V AC の直線性
  - -15/-16dB Rx/Tx リターン ロス
  - -60dB の NEXT、-43dB の FEXT クロストーク
  - PRBS データによる 70fs の低付加 RJ
- DisplayPort 1.4 および 2.1 リンク トレーニングに対して透過的
- 3.3V 単一電源、低アクティブ電力:160mW/チャネル
- 内部電圧レギュレータにより電源ノイズへの耐性を実現
- 高い直線性により DP コンプライアンス テストが容易
- 高いチャネル BW による優れたリニア EQ カーブ
- ピンストラップ、I^2C または EEPROM プログラミング
  - 18 個の EQ ブースト設定
  - 5 個のフラット ゲイン設定
- TDP2004:0～70℃の商業用温度範囲
- TDP2004I:-40～85℃の工業用温度範囲
- 4mm × 6.0mm、40 ピン WQFN パッケージ

2 アプリケーション

- デスクトップ PC またはマザーボード
- PC、ノート PC、およびタブレット
- ドッキング・ステーション
- TV、ゲーム、ホーム シアター、およびエンターテインメント
- 業務用オーディオ、ビデオ、サイネージ
- 試験 / 測定機器
- 医療用
- フラット パネル モニタ

3 概要

TDP2004 は、4 チャネルの低消費電力高性能リニア リピータまたはリドライバで、最大 20Gbps の DisplayPort 2.1 をサポートするよう設計されています。

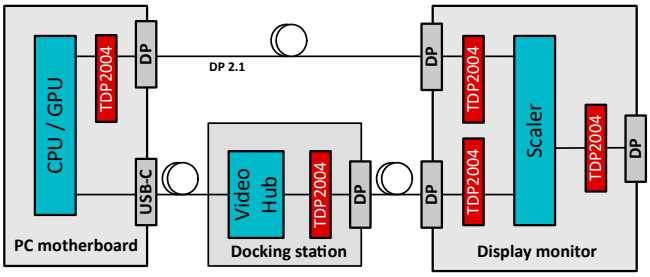
TDP2004 のレシーバは、連続時間リニア・イコライザ (CTLE) を搭載し、プログラマブルな高周波数での昇圧を実現しています。イコライザは、相互接続媒体 (例:PCB 配線) に起因する符号間干渉 (ISI) によって完全に閉じた入力アイを開くことができます。CTLE レシーバにはリニア出力ドライバが接続されています。TDP2004 のリニアなデータパスは、送信プリセット信号特性を保持します。高帯域幅で、チャネル間クロストークが少なく、付加ジッタが小さく、反射損失特性が非常に優れた本デバイスは、便利なイコライゼーション機能を備えていることを除いて、リンク内でほとんど受動素子のように振舞います。DisplayPort リンクのトレーニングは、ソース Tx とシンク Rx の間でパッシブ チャネルの一部となるリニア リドライバを使用して効果的に行われます。このリンク・トレーニング・プロトコルの透過性は、最良の電気的リンクと考えられる最短のレイテンシをもたらします。本デバイスのデータ・パスは、基板上のすべての電源ノイズに対して高い耐性を示す内部的に安定化された電源レールを使用しています。

また、このデバイスは AC および DC ゲインの変動が小さいため、大容量プラットフォームを展開する際の一貫したイコライゼーションにも対応しています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
TDP2004	RNQ (WQFN、40)	4mm × 6mm
TDP2004I		

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション

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4 Pin Configuration and Functions

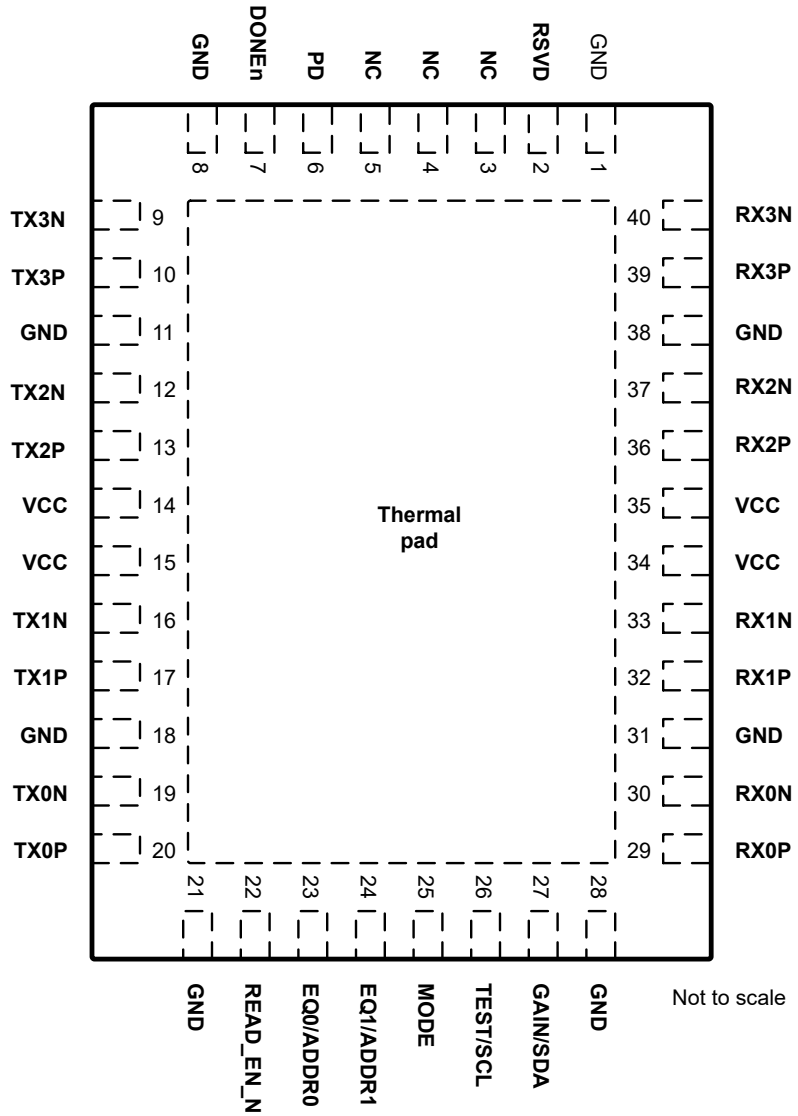


図 4-1. RNQ Package, 40-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DONEn	7	O, 3.3 V open drain	In **SMBus/I²C Primary mode**: Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7 kΩ required for operation. High: External EEPROM load failed or incomplete Low: External EEPROM load successful and complete In **SMBus/I²C Secondary/Pin mode**: This output is High-Z. The pin can be left floating.

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
MODE	25	I, 5-level	Sets device control configuration modes. 5-level IO pin as provided in 表 6-3. The pin can be exercised at device power up or in normal operation mode. L0: **Pin mode** – device control configuration is done solely by strap pins. L1: **SMBus/I²C Primary mode** – device control configuration is read from external EEPROM. When the TDP2004 has finished reading from the EEPROM successfully, it will drive the DONEn pin LOW. SMBus/I²C secondary operation is available in this mode before, during or after EEPROM reading. Note: during EEPROM reading if the external SMBus/I²C primary wants to access TDP2004 registers it must support arbitration. L2: **SMBus/I²C Secondary mode** – device control configuration is done by an external controller with SMBus/I²C primary. L3 and L4 (Float): RESERVED – TI internal test modes.
EQ0 / ADDR0	23	I, 5-level	In **Pin mode:** Sets receiver linear equalization (CTLE) boost for channels 0-3 as provided in 表 6-1. These pins are sampled at device power-up only. In **SMBus/I²C mode:** Sets SMBus / I²C secondary address as provided in 表 6-4. These pins are sampled at device power-up only.
EQ1 / ADDR1	24	I, 5-level	
GAIN / SDA	27	I, 5-level / I/O, 3.3 V LVCMOS, open drain	In **Pin mode:** Flat gain (DC and AC) from the input to the output of the device for channels 0-3. The pin is sampled at device power-up only. In **SMBus/I²C mode:** 3.3 V SMBus/I²C data. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I²C interface standard.
GND	1, 8, 11, 18, 21, 28, 31, 38, EP	P	Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
PD	6	I, 3.3 V LVCMOS	2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1-MΩ weak pull-down resistor. High: power down for channels 0-3 Low: power up, normal operation for channels 0-3
READ_EN_N	22	I, 3.3 V LVCMOS	In **SMBus/I²C Primary mode**: After device power up, when the pin is low, it initiates the SMBus / I²C Primary mode EEPROM read function. When EEPROM read is complete (indicated by assertion of DONEn low), this pin can be held low for normal device operation. During the EEPROM load process the device's signal path is disabled. In **SMBus/I²C Secondary and Pin modes:** In these modes the pin is not used. The pin can be left floating. The pin has internal 1-MΩ weak pull-down resistor.
RSVD	2	—	Reserved use for TI. The pin must be left floating (NC).
TEST / SCL	26	I, 5-level / I/O, 3.3 V LVCMOS, open drain	In **Pin mode:** TI test mode. External 1 kΩ pull down resistor must be installed. In **SMBus/I²C mode:** 3.3V SMBus/I²C clock. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I²C interface standard.
RX0N	30	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 0.
RX0P	29	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 0.
RX1N	33	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 1.
RX1P	32	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 1.
RX2N	37	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 2.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RX2P	36	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 2.
RX3N	40	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 3.
RX3P	39	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 3.
TX0N	19	O	Inverting pin for 100 Ω differential driver output. Channel 0.
TX0P	20	O	Non-inverting pin for 100 Ω differential driver output. Channel 0.
TX1N	16	O	Inverting pin for 100 Ω differential driver output. Channel 1.
TX1P	17	O	Non-inverting pin for 100 Ω differential driver output. Channel 1.
TX2N	12	O	Inverting pin for 100 Ω differential driver output. Channel 2.
TX2P	13	O	Non-inverting pin for 100 Ω differential driver output. Channel 2.
TX3N	9	O	Inverting pin for 100 Ω differential driver output. Channel 3.
TX3P	10	O	Non-inverting pin for 100 Ω differential driver output. Channel 3.
VCC	14, 15, 34, 35	P	Power supply pins. VCC = 3.3 V ±10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane. Install a decoupling capacitor to GND near each VCC pin.

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and open drain I/O voltage	–0.5	4.0	V
$VIO_{5LVL,ABSMAX}$	5-level input I/O voltage	–0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance	DC to <50 Hz, sinusoidal[1]			250	mVpp
		50 Hz to 500 kHz, sinusoidal[1]			100	mVpp
		500 kHz to 2.5 MHz, sinusoidal[1]			33	mVpp
		Supply noise, >2.5 MHz, sinusoidal[1]			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_A	Operating ambient temperature	TDP2004	0		70	°C
		TDP2004I	-40		85	°C
T_J	Operating junction temperature	TDP2004			105	°C
		TDP2004I			125	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD and READ_EN_N	200			µs
VCC_{SMBUS}	SMBus/I²C SDA and SCL open drain termination voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency	SMBus secondary mode	10		400	kHz
VID_{LAUNCH}	Source launch amplitude	Differential signaling			1200	mVpp
DR	Data rate		1		20	Gbps

5.4 Thermal Information

THERMAL METRIC[1]		TDP2004 RNQ, 40 Pins	UNIT
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	30.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

5.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{ACT}	Device active power	4 channels active, EQ = 0-2		0.57	0.71	W
		4 channels active, EQ = 5-19		0.69	0.85	W
P_{STBY}	Device power consumption in standby power mode	All channels disabled (PD = H)		17	25	mW
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PD, READ_EN_N pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD, READ_EN_N pins			1.08	V
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7 kΩ (SDA, SCL, DONEn pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = –4 mA (SDA, SCL, DONEn pins)			0.4	V
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD, READ_EN_N pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PD, READ_EN_N pins)	-10			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6 V, VCC = 0 V, (SCL, SDA, , PD, READ_EN_N pins)			200	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SDA, SCL, PD, READ_EN_N pins		1.6		pF
5 Level IOs (MODE, GAIN, EQ0, EQ1 pins)						
I_{IH_5L}	Input high leakage current, 5-level IOs	VIN = 2.5 V			10	µA
I_{IL_5L}	Input low leakage current for all 5-level IOs except MODE.	VIN = GND	-10			µA
$I_{IL\_5L,MODE}$	Input low leakage current for MODE pin	VIN = GND	-200			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC common vode voltage	Device is in active or standby state		1.4		V
$Z_{RX\text{-}DC}$	Rx DC single-ended impedance			50		Ω
Transmitter						
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential Tx impedance	Impedance of Tx during active signaling, VID,diff = 1 Vpp		100		Ω
$V_{TX\text{-}DC\text{-}CM}$	Tx DC common mode voltage			1.0		V
$I_{TX\text{-}SHORT}$	Tx short circuit current	Total current the Tx can supply when shorted to GND		70		mA

5.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	3 GHz		-19		dB
		4 GHz		-18		dB
		5 GHz		-18		dB
		6 GHz		-17		dB
		10 GHz		-15		dB
XT_{RX}	Receiver-side pair-to-pair isolation; Port A or Port B	Minimum over 10 MHz to 10 GHz range		-60		dB
Transmitter						
$RL_{TX-DIFF}$	Output differential return loss	3 GHz		-19		dB
$RL_{TX-DIFF}$	Output differential return loss	4.0 GHz		-18		dB
$RL_{TX-DIFF}$	Output differential return loss	5.0 GHz		-18		dB
$RL_{TX-DIFF}$	Output differential return loss	6.0 GHz		-17		dB
$RL_{TX-DIFF}$	Output differential return loss	10 GHz		-16		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum over 10 MHz to 10 GHz range		-60		dB
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either low-to-high or high-to-low transition.		100	130	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	Between any two lanes within a single transmitter.			20	ps
$T_{RJ-DATA}$	Additive random jitter with data	Jitter through redriver minus the calibration trace. 20Gbps PRBS15. 800 mVpp-diff input swing		70		fs
XT	Channel to channel xtalk (between adjacent active channels, FEXT	Minimum over 10 MHz to 10 GHz range, normalized to EQ gain of 0dB		-43		dB
FLAT-GAIN	Broadband DC and AC flat gain - input to output, measured at DC	Minimum EQ, GAIN = L0		-5.6		dB
		Minimum EQ, GAIN = L1		-3.8		dB
		Minimum EQ, GAIN = L2		-1.2		dB
		Minimum EQ, GAIN = L3		2.6		dB
		Minimum EQ, GAIN = L4 (Float)		0.6		dB
$EQ\text{-}MAX_{10G}$	EQ boost at max setting (EQ INDEX = 19)	AC gain at 10 GHz relative to gain at 100 MHz.		19		dB
LINEARITY-DC	Output DC linearity	at GAIN = L4		1750		mVpp
LINEARITY-AC	Output AC linearity	at 10Gbps, with GAIN = L4		1100		mVpp
		at 20Gbps, with GAIN = L4		1080		mVpp

5.7 SMBUS/I^{2}C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Secondary Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs

5.7 SMBUS/I²C Timing Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU-STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD-DAT}	Data hold time		0			µs
T_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		2		ns
t_{SU-STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs
C_b	Capacitive load for each bus line				400	pF
Primary Mode						
f_{SCL-M}	SCL clock frequency			303		kHz
t_{LOW-M}	SCL low period			1.90		µs
T_{HIGH-M}	SCL high period			1.40		µs
$t_{SU-STA-M}$	Set-up time for a repeated START condition			2		µs
$t_{HD-STA-M}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated			1.5		µs
$T_{SU-DAT-M}$	Data setup time			1.4		µs
$t_{HD-DAT-M}$	Data hold time			0.5		µs
t_{R-M}	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		120		ns
T_{F-M}	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		2		ns
$t_{SU-STO-M}$	Stop condition setup time			1.5		µs
EEPROM Timing						
T_{EEPROM}	EEPROM configuration load time	Time to assert DONEn after READ_EN_N has been asserted.		7.5		ms
T_{POR}	Time to first SMBus access	Power supply stable after initial ramp. Includes initial power-on reset time.		50		ms

5.8 Typical Characteristics

図 5-1 shows typical EQ gain curves versus frequency for different EQ settings. 図 5-2 shows typical differential return loss for Rx and Tx pins.

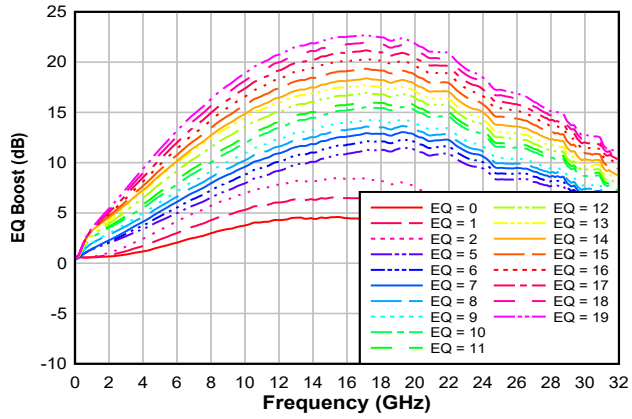


図 5-1. Typical EQ Boost vs Frequency

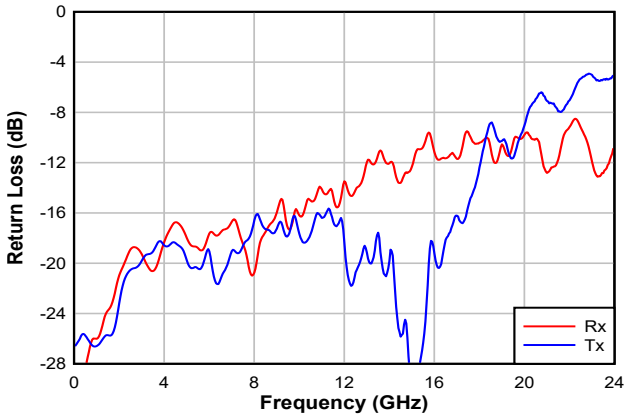


図 5-2. Typical Differential Return Loss

5.9 Typical Jitter Characteristics

図 5-3 and 図 5-4 show eye diagrams at 20Gbps that compare jitter through calibration traces (left), and jitter through TDP2004 (right) at TI evaluation boards with minimal channels. The eye diagrams illustrate that TDP2004 adds very little random jitter (RJ).

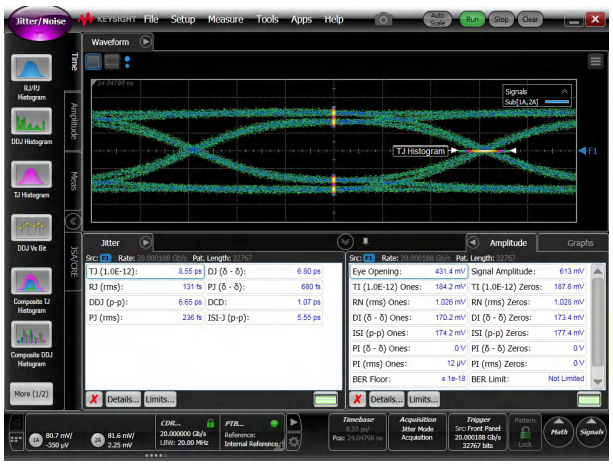


図 5-3. Through Baseline Calibration Trace Setup for 20Gbps

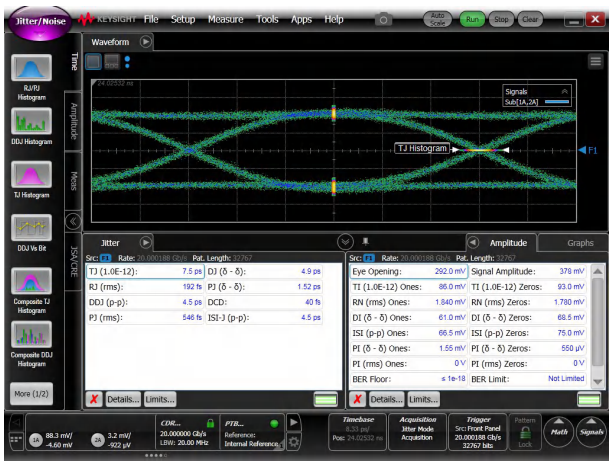


図 5-4. Through TDP2004 for 20Gbps

6 Detailed Description

6.1 Overview

The TDP2004 is a four-channel multi-rate linear repeater with integrated signal conditioning. The device's signal channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

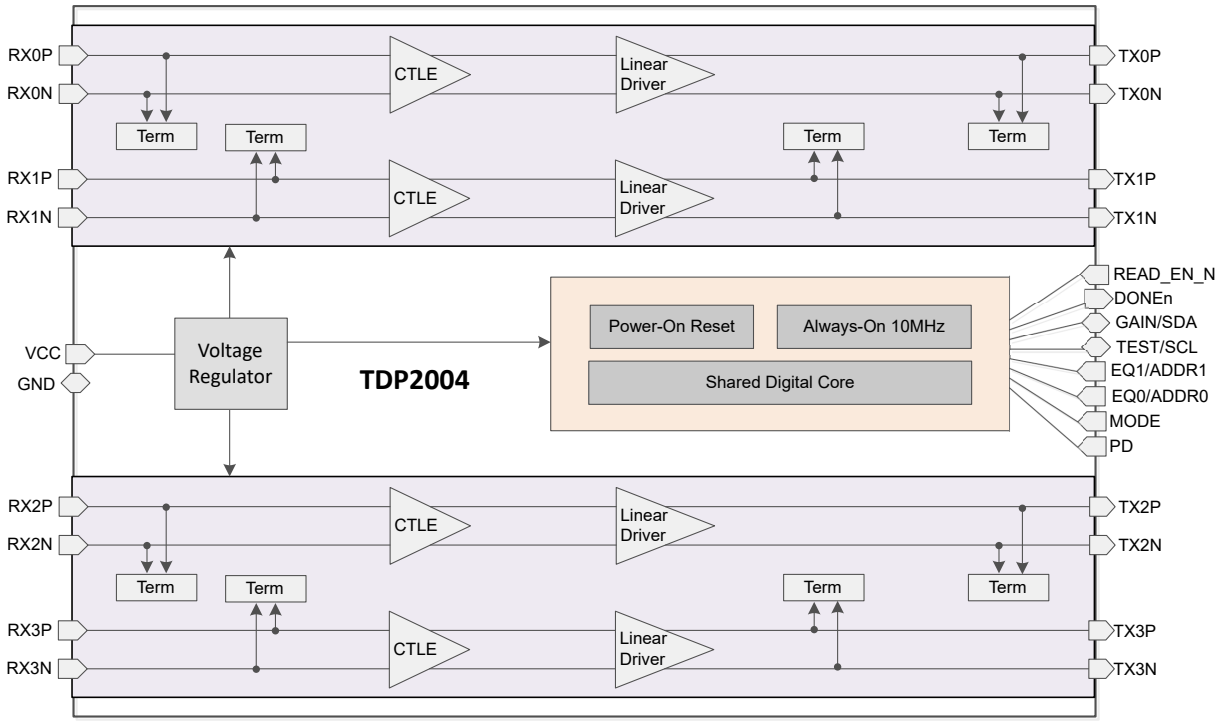
The TDP2004 can be configured three different ways:

Pin mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I^{2}C Primary mode – device control configuration is read from external EEPROM. When the TDP2004 has finished reading from the EEPROM successfully, it will drive the DONEn pin LOW. SMBus/I^{2}C secondary operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I^{2}C primary wants to access TDP2004 registers, then it must support arbitration. The mode is preferred when software implementation is not desired.

SMBus/I^{2}C Secondary mode – provides most flexibility. Requires a SMBus/I^{2}C primary device to configure TDP2004 though writing to its secondary address.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Linear Equalization

The TDP2004 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain

profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I^{2}C mode. In Pin mode the settings are optimized for FR4 traces.

表 6-1 provides available equalization boost at 20Gbps (10 GHz Nyquist frequency) through EQ control pins or SMBus/I^{2}C registers. In Pin Control mode EQ1 and EQ0 pins set equalization boost for channels 0-3. In I^{2}C mode individual channels can be independently programmed for EQ boost. If the TDP2004 is used for other data rates equalization gain can be extracted from 図 5-1.

表 6-1. Equalization Control Settings

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)
EQ INDEX	Pin mode		SMBus/I^{2}C Mode				at 10 GHz
	EQ1	EQ0	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass	
0	L0	L0	0	0	0	1	4.0
1	L0	L1	1	0	0	1	5.0
2	L0	L2	3	0	0	1	7.0
5	L1	L0	0	0	1	0	8.0
6	L1	L1	1	0	1	0	9.0
7	L1	L2	2	0	1	0	9.5
8	L1	L3	3	0	3	0	10.0
9	L1	L4	4	0	3	0	11.0
10	L2	L0	5	1	7	0	12.0
11	L2	L1	6	1	7	0	12.5
12	L2	L2	8	1	7	0	13.5
13	L2	L3	10	1	7	0	14.5
14	L2	L4	10	2	15	0	15.0
15	L3	L0	11	3	15	0	15.5
16	L3	L1	12	4	15	0	16.5
17	L3	L2	13	5	15	0	17.0
18	L3	L3	14	6	15	0	18.0
19	L3	L4	15	7	15	0	19.0

6.3.2 Flat-Gain

The GAIN pin can be used to set the overall data-path flat gain (DC and AC) of the TDP2004 when the device is in Pin mode. The pin GAIN sets the Flat-Gain for channels 0-3. In I^{2}C mode each channel can be independently set. 表 6-2 provides flat gain control configuration settings. In the default recommendation for most systems will be GAIN = L4 (float) that provides flat gain of 0 dB.

The flat-gain and equalization of the TDP2004 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

表 6-2. Flat Gain Configuration Settings

Pin mode GAIN	I^{2}C Modeflat_gain_2:0	Flat Gain
L0	0	-5.6 dB
L1	1	-3.8 dB
L2	3	-1.2 dB

表 6-2. Flat Gain Configuration Settings (続き)

Pin mode GAIN	I²C Modeflat_gain_2:0	Flat Gain
L4 (float)	5	0.6 dB (default recommendation)
L3	7	+2.6 dB

6.4 Device Functional Modes

6.4.1 Active Mode

The device is in normal operation. In this mode, the TDP2004 redrives and equalizes video mainlink signals to provide better signal integrity.

6.4.2 Standby Mode

The device is in standby mode invoked by PD = H. In this mode, the device is in standby mode conserving power.

6.5 Programming

6.5.1 Pin mode

The TDP2004 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 5-level pins for device control and signal integrity optimum settings.

6.5.1.1 Five-Level Control Inputs

The TDP2004 has four (EQ0, EQ1, GAIN, and MODE) 5-level input pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The 5-level pins except MODE are sampled at power-up only. The MODE pin can be exercised at device power up or in normal operation mode.

表 6-3. 5-level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	F (Float)

6.5.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus/I²C Secondary control mode), then the TDP2004 is configured through a standard I²C or SMBus interface that may operate up to 400 kHz. The secondary address of the TDP2004 is determined by the pin strap settings on the ADDR1 and ADDR0 pins. The sixteen possible secondary addresses for channels 0-3 are provided in 表 6-4. In SMBus/I²C modes the SCL and SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

表 6-4. SMBUS/I2C Secondary Address Settings

ADDR1	ADDR0	7-bit Secondary Address Channels 0-3
L0	L0	0x18
L0	L1	0x1A
L0	L2	0x1C
L0	L3	0x1E
L0	L4	Reserved
L1	L0	0x20

表 6-4. SMBUS/I2C Secondary Address Settings (続き)

ADDR1	ADDR0	7-bit Secondary Address Channels 0-3
L1	L1	0x22
L1	L2	0x24
L1	L3	0x26
L1	L4	Reserved
L2	L0	0x28
L2	L1	0x2A
L2	L2	0x2C
L2	L3	0x2E
L2	L4	Reserved
L3	L0	0x30
L3	L1	0x32
L3	L2	0x34
L3	L3	0x36
L3	L4	Reserved

The TDP2004 has two types of registers:

- **Shared Registers:** these registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers:** these registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group through broadcast writes to Channels 0-3

Channel Registers Base Address	Channel 0-3 Access
0x00	Channel 0 registers
0x20	Channel 1 registers
0x40	Channel 2 registers
0x60	Channel 3 registers
0x80	Broadcast write channel 0-3 registers, read channel 0 registers
0xA0	Broadcast write channel 0-1 registers, read channel 0 registers
0xC0	Broadcast write channel 2-3 registers, read channel 2 registers
0xE0	Channel 0-3 share registers

6.5.2.1 Shared Registers

表 6-5. General Registers (Offset = 0xE2)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device reset control: Reset all I^2C registers to default values (self-clearing).
5	rst_i2c_mas	R/W/SC	0x0	Reset I^2C Primary (self-clearing).
4-1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM configuration load.

表 6-6. EEPROM_Status Register (Offset = 0xE3)

Bit	Field	Type	Reset	Description
7	eecfg_cmplt	R	0x0	EEPROM load complete.

表 6-6. EEPROM_Status Register (Offset = 0xE3) (続き)

Bit	Field	Type	Reset	Description
6	eecfg_fail	R	0x0	EEPROM load failed.
5	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image.
4	eecfg_atmpt_0	R	0x0	see MSB
3	eecfg_cmplt	R	0x0	EEPROM load complete 2.
2	eecfg_fail	R	0x0	EEPROM load failed 2.
1	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image 2.
0	eecfg_atmpt_0	R	0x0	see MSB

表 6-7. DEVICE_ID0 Register (Offset = 0xF0)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011
2	device_id0_2	R	0x1	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

表 6-8. *DEVICE_ID1 Register (Offset = 0xF1)*

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1001: TDP2004
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x0	see MSB

6.5.2.2 Channel Registers

表 6-9. EQ Gain Control Register (Channel register base + Offset = 0x01)

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage1_3	R/W	0x0	EQBoost stage 1 control See 表 6-1 for details
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost stage 2 control See 表 6-1 for details
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

表 6-10. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

表 6-10. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03) (続き)

Bit	Field	Type	Reset	Description
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile See 表 6-1 for details
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat gain select: See 表 6-2 for details
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

表 6-11. TI Test Mode Control Register (Channel register base + Offset = 0x04)

Bit	Field	Type	Reset	Description
7-3, 1-0	RESERVED	R	0x0	Reserved
2	TI test mode	R/W	0x0	Set TI test mode: 0: test mode is enabled 1: test mode is disabled. Must be set to "1" for normal operation.

表 6-12. PD Override Register (Channel register base + Offset = 0x05)

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^{2}C 0: Manual override disabled 1: Manual override enabled
6-0	device_en	R/W	0x111111	Manual power down of redriver various blocks of a channel – gated by device_en_override = 1 111111: All blocks in the channel are enabled 000000: All blocks in the channel are disabled

表 6-13. Bias Register (Channel register base + Offset = 0x06)

Bit	Field	Type	Reset	Description
5-3	Bias current	R/W	0x100	Control bias current Set 001 for best performance
7,6,2-0	Reserved	R/W	0x00000	Reserved

6.5.3 SMBus/I^{2}C Primary Mode Configuration (EEPROM Self Load)

The TDP2004 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after the device's initial power-up. If the TDP2004 is configured for SMBus Primary mode, then it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, theTDP2004 becomes an SMBus primary and attempts to self-configure by reading the device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the TDP2004 has finished reading from the EEPROM successfully, it will drive the DONEn pin LOW. SMBus/I^{2}C secondary operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I^{2}C primary wants to access TDP2004 registers, then it must support arbitration.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2Kb (256 × 8-bit) is recommended.
- Set MODE = L1, configure for SMBus Primary mode.
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 3.3 V supply
- In SMBus/I^{2}C modes the SCL and SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Multiple TDP2004 can be cascaded to read from single EEPROM. Tie the READ_EN_N pin of the first device low (GND) to automatically initiate EEPROM read at power up. DONEn of the first device can be fed into READ_EN_N of the next device with 4.7k pull-up resistors. Leave the DONEn pin of the final device floating, or connect the pin to a micro-controller input to monitor the completion of the final EEPROM read.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TDP2004 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

7.2 Typical Applications

The TDP2004 is a linear redriver that can be used as DisplayPort mainlink signal conditioner. The device can be used in wide range of AC coupled interfaces including DisplayPort 1.4, 2.1 up to 20Gbps.

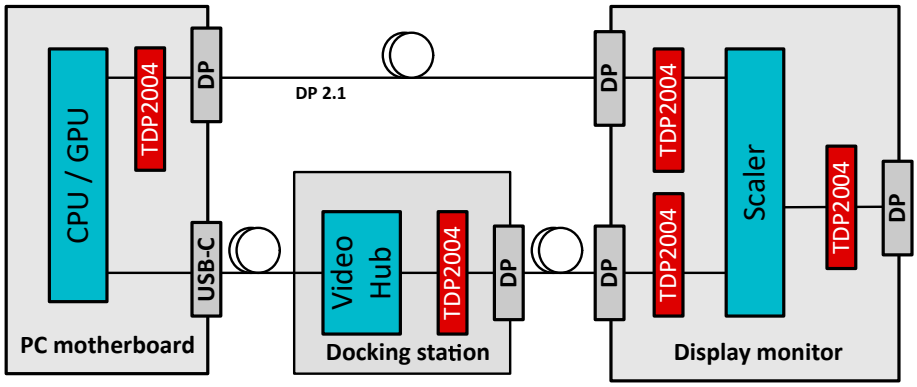


図 7-1. Typical Application

7.2.1 DP 2.1 Mainlink Signal Conditioning

The TDP2004 can be used in a PC motherboard or in a docking station or in a display monitor among other applications to boost DisplayPort mainlink signals to increase the reach of the source and sink channel. The following sections outline detailed procedures and design requirements for a typical DP 2.1 application. However, the design recommendations can be used in other use cases.

7.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near the receiver end of each channel segment to minimize reflections.
- AC-coupling capacitors of 220 nF are recommended. Set the maximum body size to 0402 and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Surface mount connector is recommended. For through hole connection, back-drill connector vias and signal vias to minimize stub length.
- Use ground reference plane vias for a low inductance path for the return current.

7.2.1.2 Detailed Design Procedure

The TDP2004 provides signal conditioning for four DP mainlink channels. The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device. The redriver becomes part of the electrical channel along with passive traces, cables, and other channel elements, resulting in optimum source and sink parameters for best electrical link. 図 7-2 shows a simplified schematic for DisplayPort application using TDP2004.

DisplayPort side band signals AUXp,n and HPD is bypassed. The link will still have successful link training through TDP2004. An inverted HPD signal can be used to control the device standby operation utilizing the PD pin; however appropriate filtering out of HPD interrupt signals must be provisioned.

In some applications where a micro-controller or other link monitoring device has DP link state information, it can exercise I^2C registers of TDP2004 for additional power management.

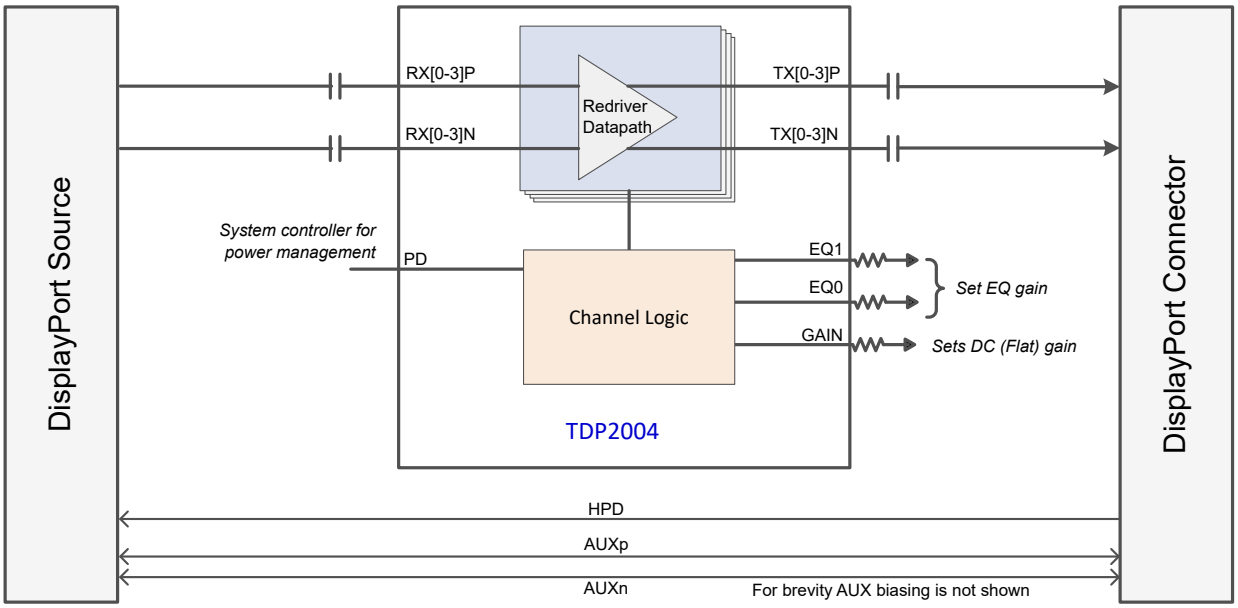


図 7-2. Simplified Schematic for DP 2.1 Signal Conditioning in a Source Application such as PC Motherboard in Pin Mode

7.2.1.3 Application Curves

The TDP2004 is a linear redriver that can be used to extend channel reach of a DP link. The redriver can help to pass compliance by removing ISI deterministic jitter at data rates up to 20Gbps (UHBR20). 図 7-3 - 図 7-6 shows a typical DP 2.1 Tx compliance channel setup along with compliance Eye Diagrams at TP3_EQ with or without redriver. The comparison of eye diagrams show that TDP2004 can provide signal conditioning by extending horizontal and vertical eye openings that makes a failing eye to pass.

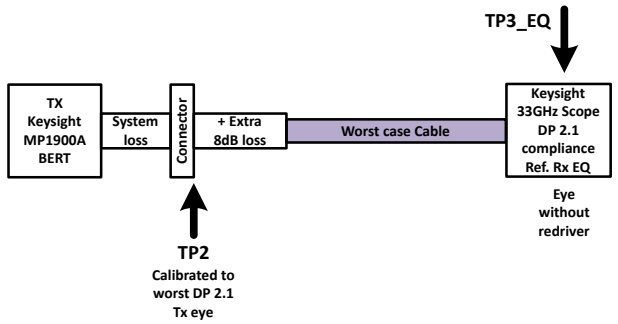


図 7-3. A Typical 20Gbps (UHBR20) DP 2.1 Tx Compliance Channel Setup with no Redriver

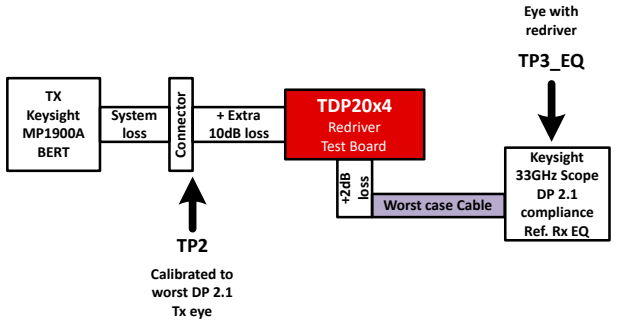


図 7-4. A Typical 20Gbps (UHBR20) DP 2.1 Tx Compliance Channel Setup with Redriver

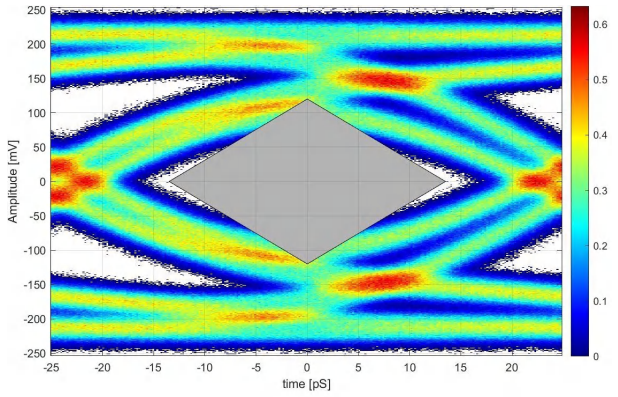


図 7-5. DP 2.1 Tx Compliance Eye Diagram at TP3_EQ with no Redriver

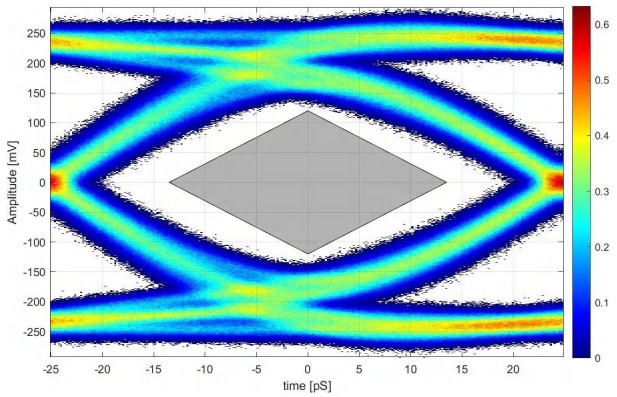


図 7-6. DP 2.1 Tx Compliance Eye Diagram at TP3_EQ with TDP2004 for Signal Conditioning

7.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The TDP2004 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 µF capacitor per VCC pin, one 1.0 µF bulk capacitor per device, and one 10 µF bulk capacitor per power bus that delivers power to one or more TDP2004 devices. The local decoupling (0.1 µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the TDP2004 ground pad.

7.4 Layout

7.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.
6. Please refer to land pattern example in the mechanical drawing section for the device thermal pad design recommendation.

7.4.2 Layout Example

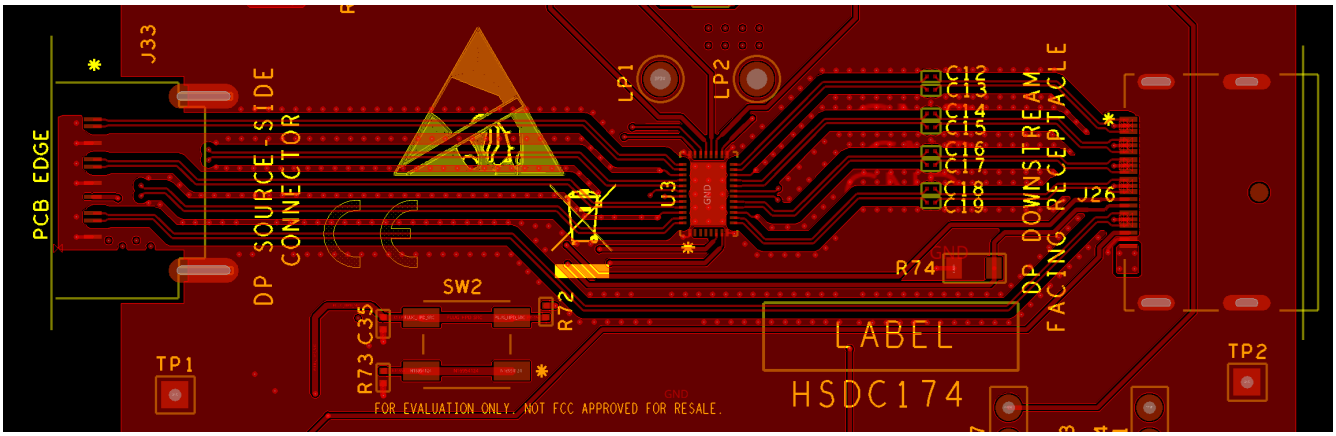


図 7-7. TDP2004 Layout Example – Sub-Section of TI evaluation board with DP connectors

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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8.3 Trademarks

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8.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

DATE	REVISION	NOTES
November 2023	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDP2004IRNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TDP2	Samples
TDP2004IRNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TDP2	Samples
TDP2004RNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TDP2	Samples
TDP2004RNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TDP2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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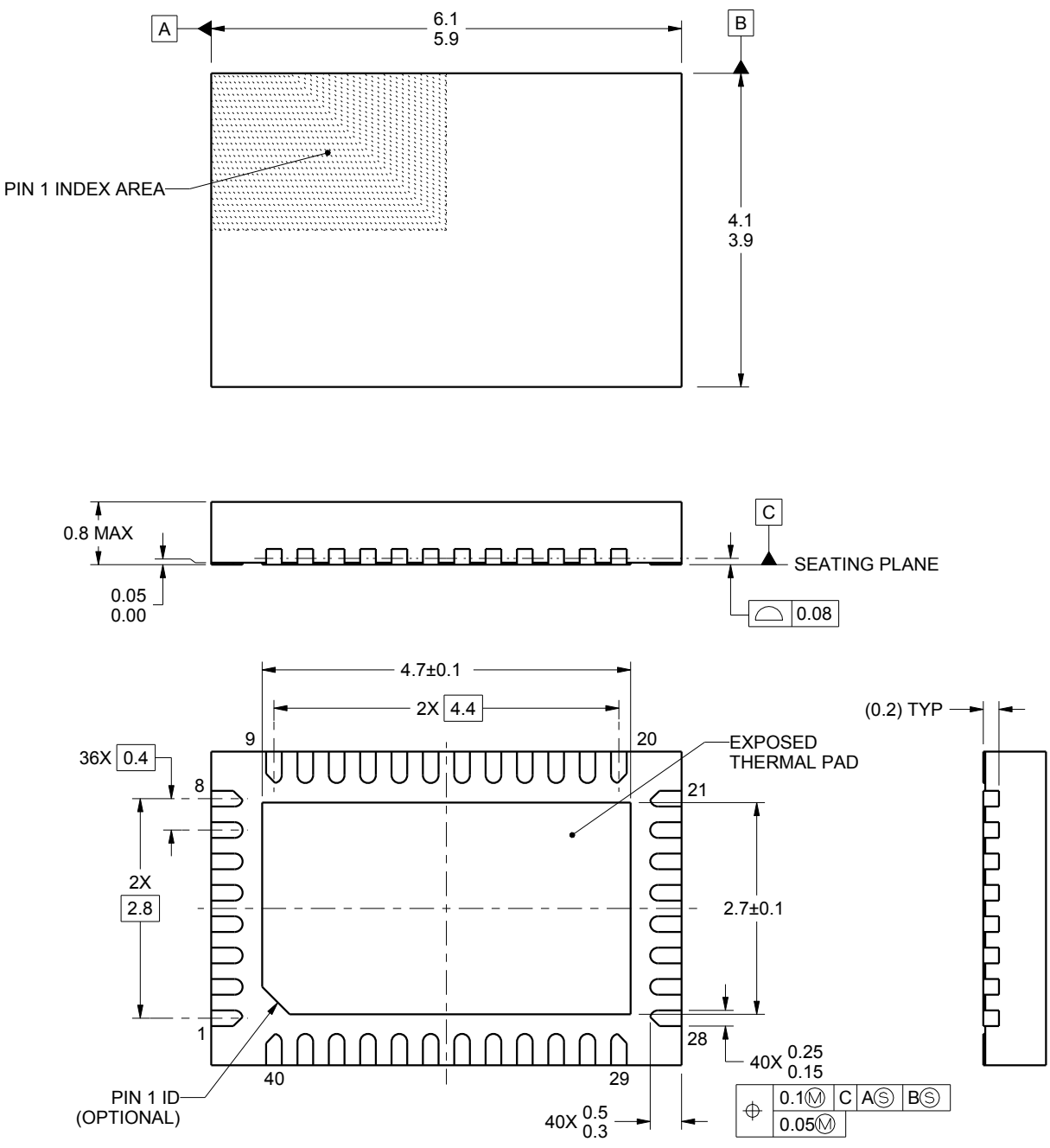
PACKAGE OUTLINE

RNQ0040A

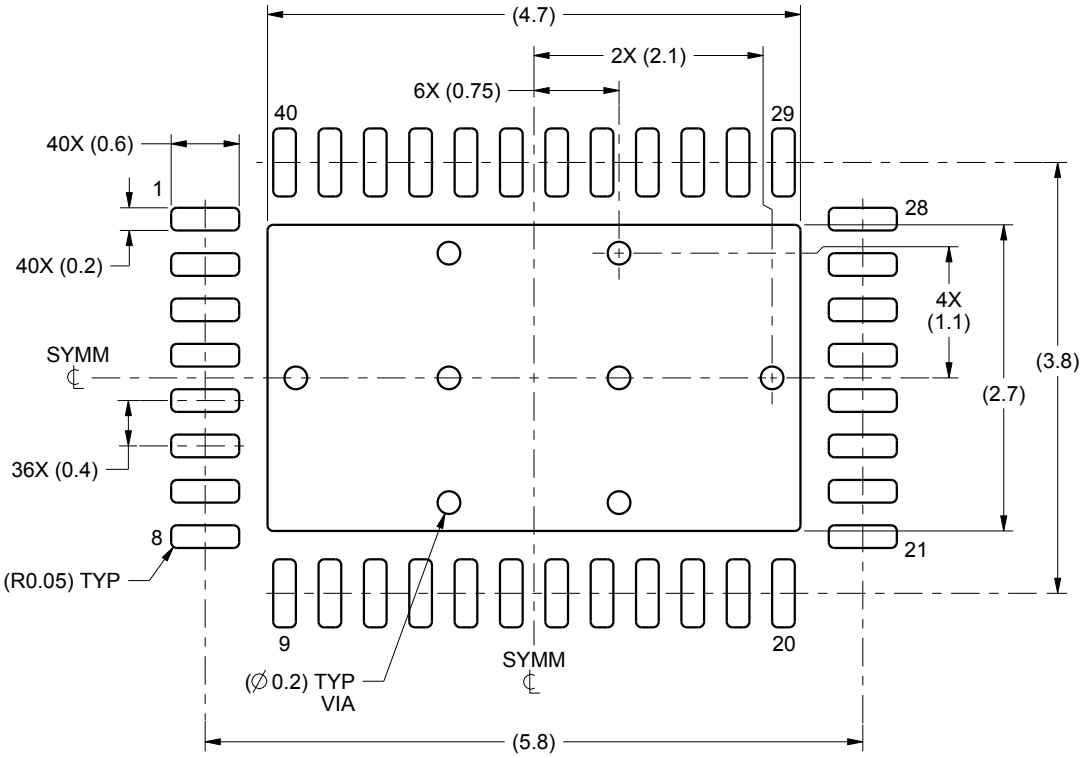
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

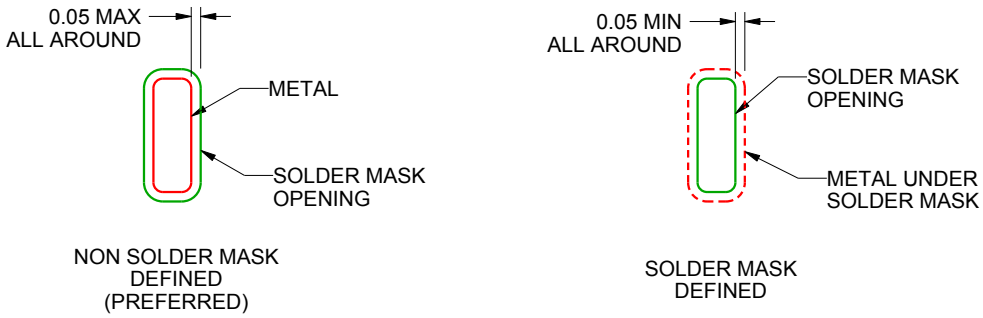


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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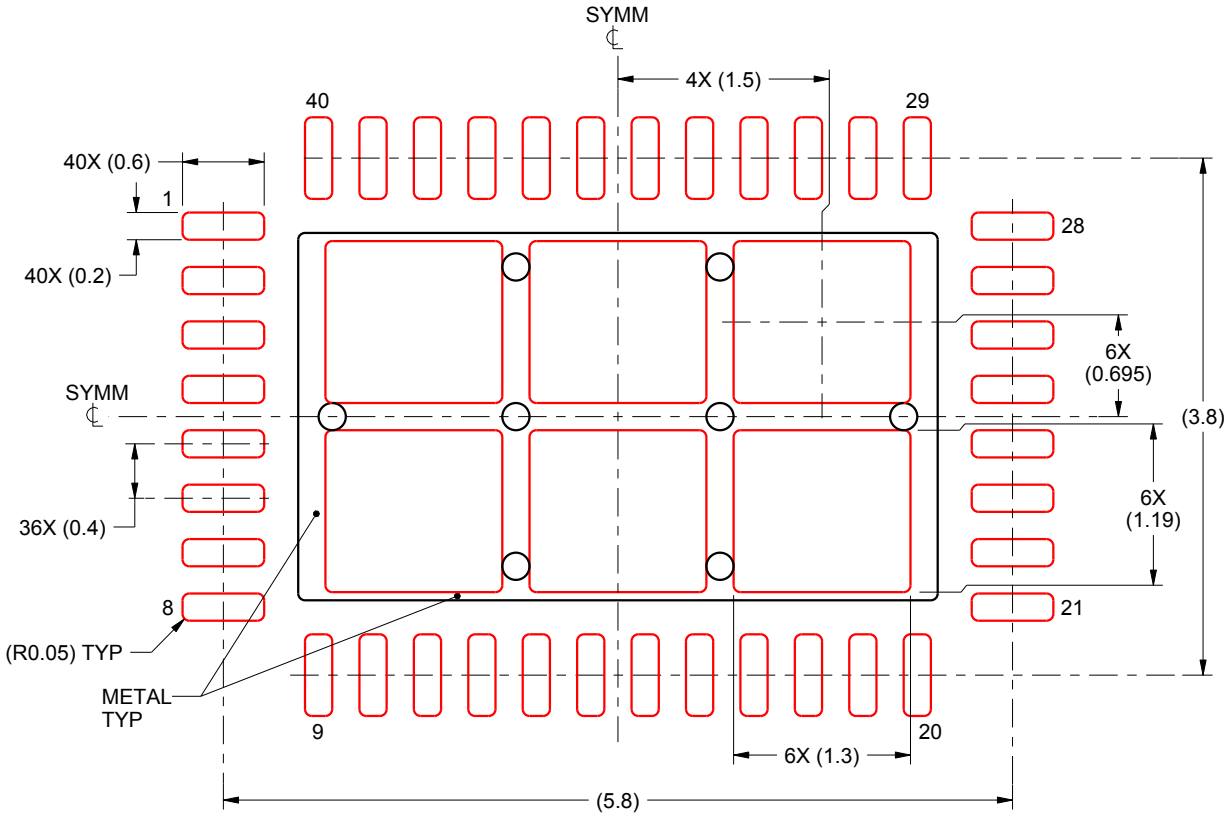
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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