SNx5LBC176 差動バス・トランシーバ

1 特長

- 双方向トランシーバ
- ANSI 規格 TIA/EIA-485-A と ISO 8482:1987(E) の要件を満たす、または上回る性能
- 高速、低消費電力の LinBiCMOS™ 回路
- シリアルとパラレルの両方のアプリケーションでの高速動作に対応
- 低スキュー
- ノイズの多い環境の長いバスラインでのマルチポイントの伝送用に設計
- 非常に小さいディスエーブル時消費電流 ... 200µA 以下
- 広い正および負の入力 / 出力バス電圧範囲
- サーマル・シャットダウン保護
- ドライバの正および負電流制限
- 開路フェイルセーフ・レシーバ設計
- レシーバ入力感度 ...±200mV 以内
- レシーバ入力ヒステリシス ...50mV (標準値)
- 5V 単一電源で動作
- グリッチ・フリーのパワーアップ / パワーダウン保護機能
- Q 温度仕様、車載用として提供 HighRel 車載用アプリケーション構成制御 / 印刷サポート車載規格に基づく認定

2 概要

SN55LBC176 、 SN65LBC176 、 SN65LBC176Q 、 SN75LBC176 差動バス・トランシーバは、マルチポイント・バス伝送ライン上での双方向データ通信を目的として設計されたモノリシック IC です。これらのデバイスは平衡伝送ライン用に設計されており、ANSI 規格 TIA/EIA-485-A (RS-485) および ISO 8482:1987(E) に適合しています。

SN55LBC176 、 SN65LBC176 、 SN65LBC176Q 、 SN75LBC176 は、3 ステート差動ライン・ドライバと差動入力ライン・レシーバを統合しており、どちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力は、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディスエーブルされている場合、または V_{CC} = 0 の場合、バスへの負荷を最小化するように設計されています。このポートは広い正負の同相電圧範囲を持っているため、本デバイスはパーティライン・アプリケーションに適しています。ドライバとレシーバをディスエーブルにすることにより、デバイスの消費電流を低減できます。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN55LBC176	LCCC (20)	8.89mm × 8.89mm
	CDIP (8)	9.60mm × 6.67mm
SN65LBC176	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm
SN75LBC176	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

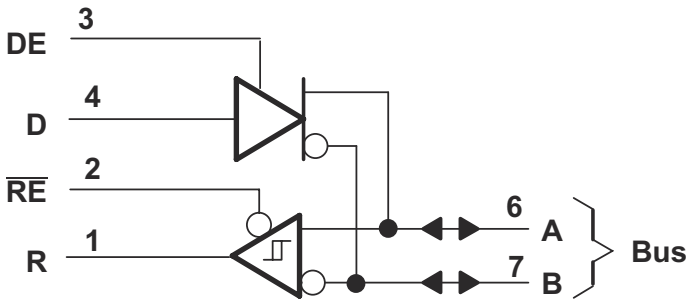

図 2-1. 論理図 (正論理)

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Table of Contents

1 特長 ... 1
2 概要 ... 1
3 Revision History ... 2
4 概要 (続き) ... 3
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Recommended Operating Conditions ... 4
6.3 Thermal Information: SN55LBC176 ... 4
6.4 Thermal Information: SN65LBC176, SN75LBC176 ... 5
6.5 Dissipation Ratings ... 5
6.6 Driver Electrical Characteristics ... 5
6.7 Driver Switching Characteristics ... 7
6.8 Receiver Electrical Characteristics ... 8
6.9 Receiver Switching Characteristics ... 8
7 Parameter Measurement Information ... 9
8 Detailed Description ... 12
8.1 Functional Block Diagram ... 12
8.2 Device Functional Modes ... 12
9 Device and Documentation Support ... 14
9.1 Device Support ... 14
9.2 Trademarks ... 14
9.3 Electrostatic Discharge Caution ... 15
9.4 Glossary ... 15
10 Mechanical, Packaging, and Orderable Information ... 15

3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (December 2010) to Revision I (October 2022)	Page
• 「ピン構成および機能」セクション、「熱に関する情報」表、「詳細説明」セクション、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

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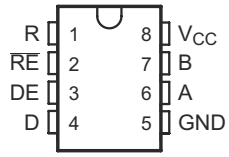
4 概要 (続き)

これらのトランシーバは、このデータシートの動作条件と特性のセクションに規定された範囲内で、ANSI 規格 TIA/EIA−485 (RS-485) および ISO 8482 アプリケーションに適しています。ミリタリー温度範囲全体では、TIA/EIA−485−A と ISO 8482:1987 (E) に含まれる一部の制限は満たされておらず、またはテストされていません。

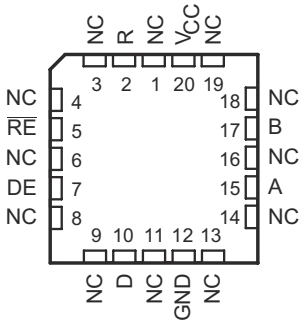
動作温度範囲は、SN55LBC176 が -55℃～125℃、SN65LBC176 が -40℃～85℃、SN65LBC176Q が -40℃～125℃、SN75LBC176 が 0℃～70℃です。

5 Pin Configuration and Functions

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC,PDIP, CDIP	LCCC		
R	1	2	O	Logic output RS485 data
$\overline{RE}$	2	5	I	Receiver enable/disable
DE	3	7	I	Driver enable/disable
D	4	10	I	Logic input RS485 data
GND	5	12	-	Ground
A	6	15	I/O	RS485 bus pin; Non-Inverting
B	7	17	I/O	RS485 bus pin; Inverted
V_{CC}	8	20	-	5V Supply Voltage
NC	-	1,2,3,6,8,9,11,13,14,16,18,19	-	No Internal Connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		7	V
Voltage range at any bus terminal	–10	15	V
Input voltage, V_I (D, DE, R, or $\overline{RE}$)	–0.3	V_{CC} + 0.5	V
Receiver output current, I_O	–10	10	mA
Continuous total power dissipation	See セクション 6.5		
Storage temperature range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		–7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, VIL	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (1)		–12		12	V
High-level output current, I_{OH}	Driver	–60			mA
	Receiver	–400			µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A	SN55LBC176	−55		125	°C
	SN65LBC176	–40		85	
	SN65LBC176Q	–40		125	
	SN75LBC176	0		70	

(1) Differential input /output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

6.3 Thermal Information: SN55LBC176

THERMAL METRIC(1)		FK	JG	UNIT
		20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	51.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	86.5	
Ψ_{JT}	Junction-to-top characterization parameter	31.0	23.7	
Ψ_{JB}	Junction-to-board characterization parameter	36.0	80.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	11.6	

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6.4 Thermal Information: SN65LBC176, SN75LBC176

THERMAL METRIC[1]		D	P	UNIT
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	54.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	42.1	
Ψ_{JT}	Junction-to-top characterization parameter	8.8	22.9	
Ψ_{JB}	Junction-to-board characterization parameter	62.6	41.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Dissipation Ratings

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 110°C POWER RATING
D	Low K[1]	526 mW	5.0 mW/°C	301 mW	226 mW	—
	High K[2]	882 mW	8.4 mW/°C	504 mW	378 mW	—
P		840 mW	8.0 mW/°C	480 mW	360 mW	—
JG		1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
FK		1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

6.6 Driver Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA			–1.5		V
V_O	Output voltage	I_O = 0			0	6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0			1.5	6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 54 Ω, See 図 7-1,		55LBC176, 65LBC176, 65LBC176Q	1.1		V
		See [2]		75LBC176	1.5	5	
$\lvert V_{OD3} \rvert$	Differential output voltage	V_{test} = – 7 V to 12 V, See Figure 2,		55LBC176, 65LBC176, 65LBC176Q	1.1		V
		See [2]		75LBC176	1.5	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage [1]	R_L = 54 Ω or 100 Ω, See 図 7-1			–0.2	0.2	V
V_{OC}	Common-mode output voltage				–1	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage[1]				–0.2	0.2	V
I_O	Output current	Output disabled, See [3]	V_O = 12 V			1	mA
			V_O = –7 V		–0.8		
I_{IH}	High-level input current	V_I = 2.4 V			–100		µA
I_{IL}	Low-level input current	V_I = 0.4 V			–100		µA

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6.6 Driver Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{OS}	Short circuit output current	V_O = −7 V			–250		mA
		V_O = 0			–150		
		V_O = V_{CC}				250	
		V_O = 12 V					
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled	55LBC176, 65LBC176Q		1.75	mA
				65LBC176, 75LBC176		1.5	
			Receiver and driver disabled	55LBC176, 65LBC176Q		0.25	
				65LBC176, 75LBC176		0.2	

(1) Δ| V_{OD} | | and Δ | V_{OC} | are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.
(2) This device meets the V_{OD} requirements of TIA/EIA−485−A above 0°C only.
(3) This applies for both power on and off; refer to TIA/EIA−485−A for exact conditions.

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6.7 Driver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		SN55LBC176 SN65LBC176Q			SN65LBC176 SN75LBC176			UNIT
				MIN	TYP	MAX	MIN	TYP(1)	MAX	
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, See 図 7-3	C_L = 50 pF,	8		31	8		25	ns
$t_{t(OD)}$	Differential output transition time				12			12		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)					6		0	6	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 図 7-4			65			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 図 7-5			65			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See 図 7-4			105			60	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See 図 7-5			105			35	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

表 6-1. Driver Symbol Equivalents

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD} \rvert$	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	None
I_O	I_{ia}, I_{ib}

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6.8 Receiver Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-}) (see 図 7-4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA			–1.5			V
V_{OH}	High level output voltage	V_{ID} = 200 mV, See 図 7-6	I_{OH} = –400 µA,		2.7			V
V_{OL}	Low level output voltage	V_{ID} = –200 mV, See 図 7-6	I_{OL} = 8 mA,				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V			–20		20	µA
I_I	Line input current	Other input = 0 V, See (3)	V_I = 12 V				1	mA
			V_I = –7 V		–0.8			
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V			–100			µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V			–100			µA
r_I	Input resistance				12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled	SN55LBC176, SN65LBC176, SN65LBC176Q			0.25	mA
				SN75LBC176			0.2	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.
(3) This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

6.9 Receiver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	SN55LBC176 SN65LBC176Q		SN65LBC176 SN75LBC176			UNIT
			MIN	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = –1.5 V to 1.5 V, See 図 7-7	11	37	11		33	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11	37	11		33	ns
$t_{sk(p)}$	Pulse skew (| t_{PLH} – t_{PHL} |)			10		3	6	ns
t_{PZH}	Output enable time to high level	See 図 7-8		35			35	ns
t_{PZL}	Output enable time to low level			35			30	ns
t_{PHZ}	Output disable time from high level	See 図 7-8		35			35	ns
t_{PLZ}	Output disable time from low level			35			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

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7 Parameter Measurement Information

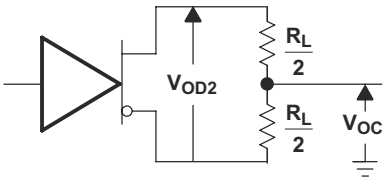

図 7-1. Driver V_{OD} and V_{OC}

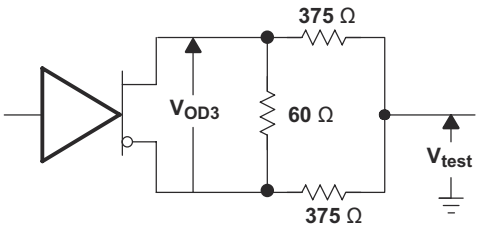

図 7-2. Driver V_{OD3}

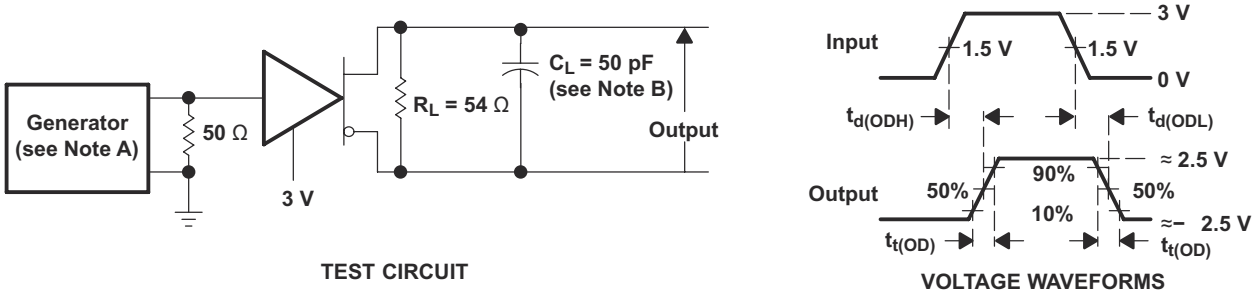

図 7-3. Driver Test Circuit and Voltage Waveforms

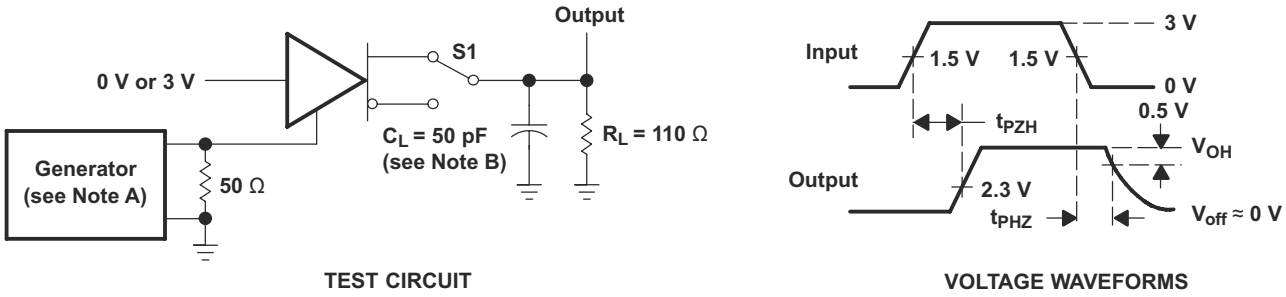

図 7-4. Driver Test Circuit and Voltage Waveforms

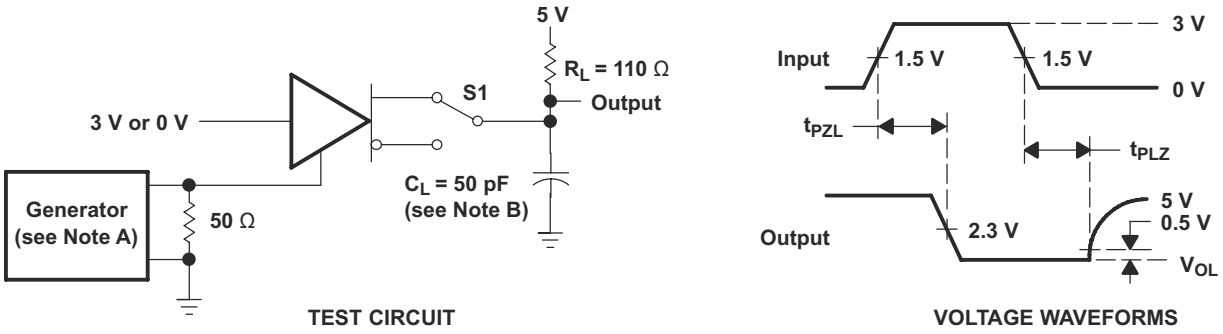

図 7-5. Driver Test Circuit and Voltage Waveforms

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
D. C_L includes probe and jig capacitance.

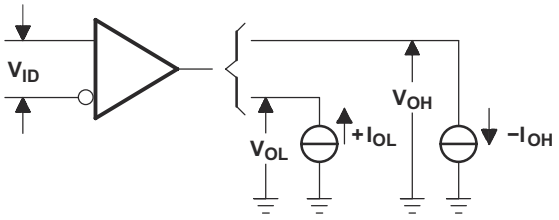

図 7-6. Receiver V_{OH} and V_{OL}

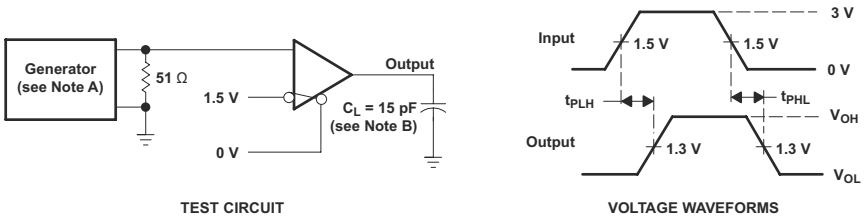

図 7-7. Receiver Test Circuit and Voltage Waveforms

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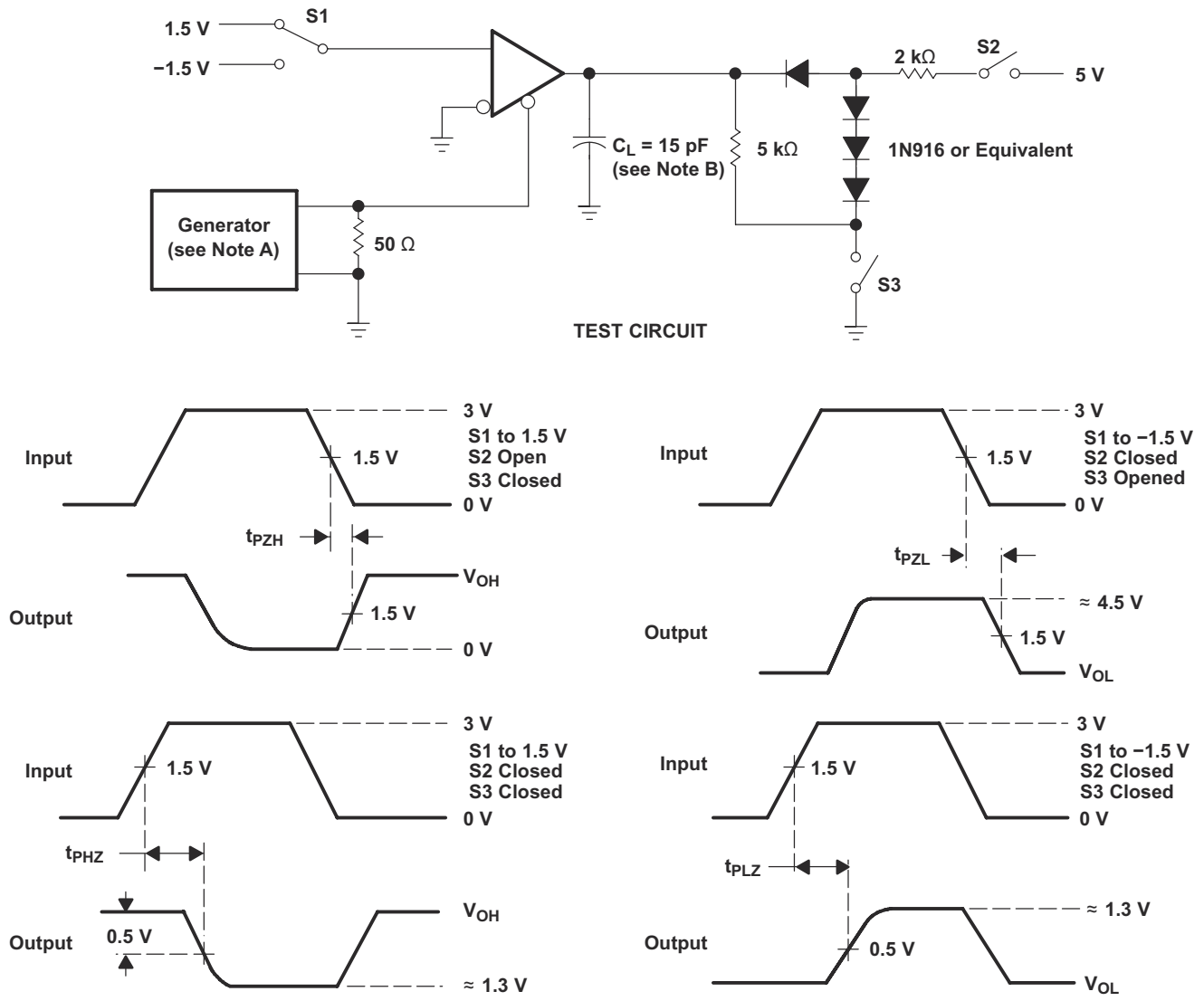


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

図 7-8. Receiver Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

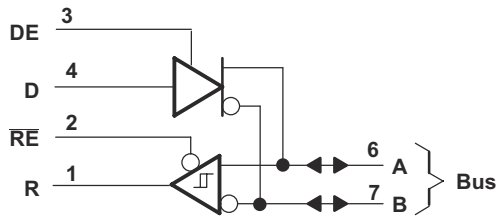
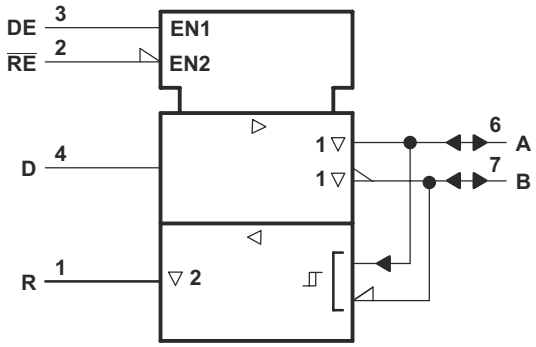


図 8-1. Logic Diagram (Positive Logic)



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

図 8-2. Logic Symbol(A)

8.2 Device Functional Modes

表 8-1. Driver Function Tables(1)

DRIVER			
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 8-2. Receiver Function Tables(1)

RECEIVER		
DIFFERENTIAL INPUTS $V_{ID} = V_{IA} - V_{IB}$	ENABLE $\overline{RE}$	OUTPUTS R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

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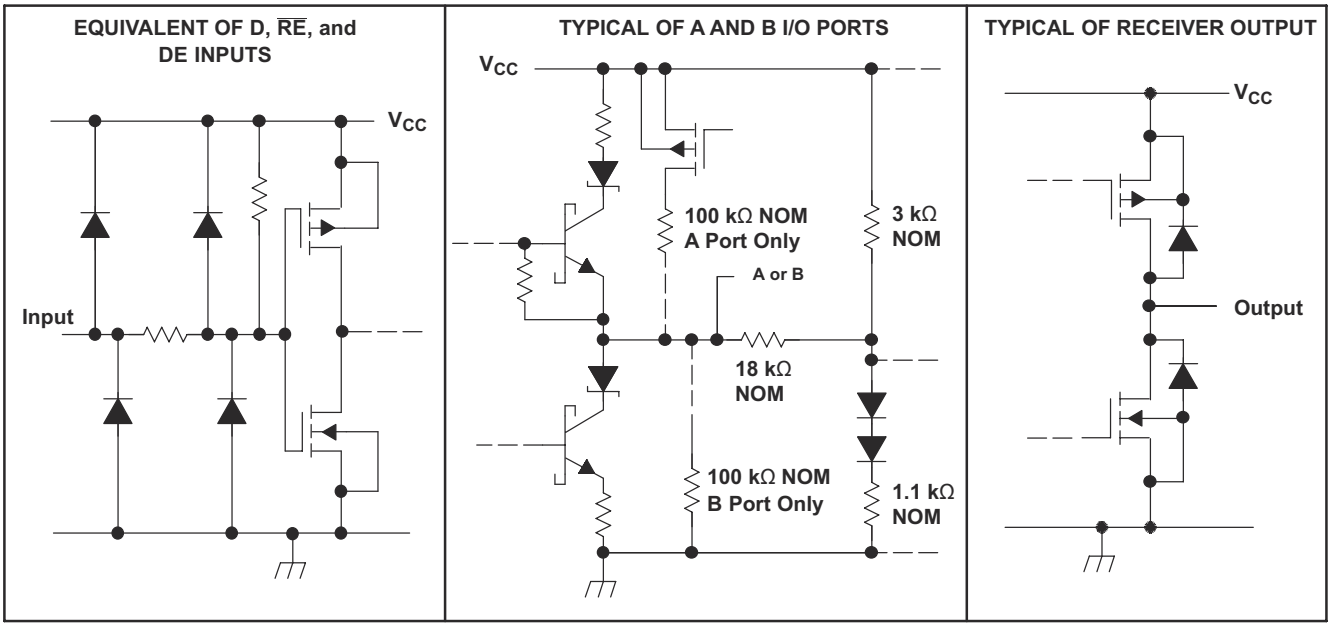

図 8-3. Schematics of Inputs and Outputs

9 Device and Documentation Support

9.1 Device Support

9.1.1 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see 図 9-1).

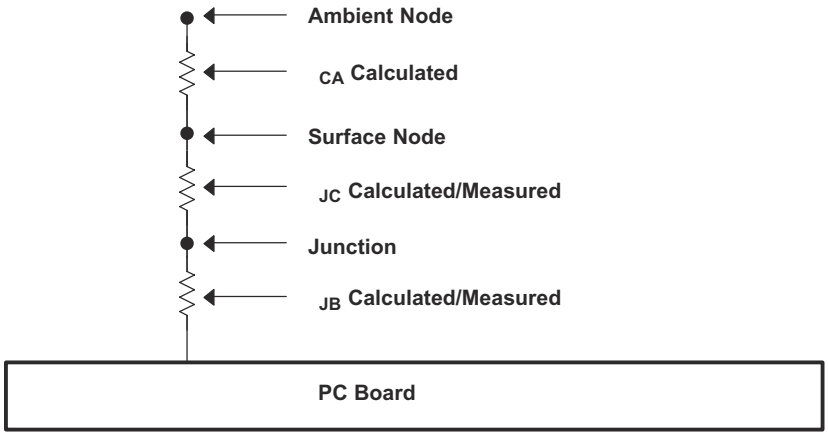

図 9-1. Thermal Resistance

9.2 Trademarks

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9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9318301Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55LBC176FK
5962-9318301QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176
SN65LBC176DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176
SN65LBC176DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176
SN65LBC176DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176
SN65LBC176P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC176
SN65LBC176P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC176
SN65LBC176QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB176Q
SN65LBC176QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB176Q
SN65LBC176QDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(J176Q1, LB176Q)
SN65LBC176QDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(J176Q1, LB176Q)
SN75LBC176D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	7LB176
SN75LBC176P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC176
SN75LBC176P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC176
SNJ55LBC176FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55LBC176FK
SNJ55LBC176FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55LBC176FK
SNJ55LBC176JG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176
SNJ55LBC176JG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55LBC176, SN65LBC176, SN75LBC176 :

- Catalog : SN75LBC176
- Automotive : SN65LBC176-Q1
- Military : SN55LBC176

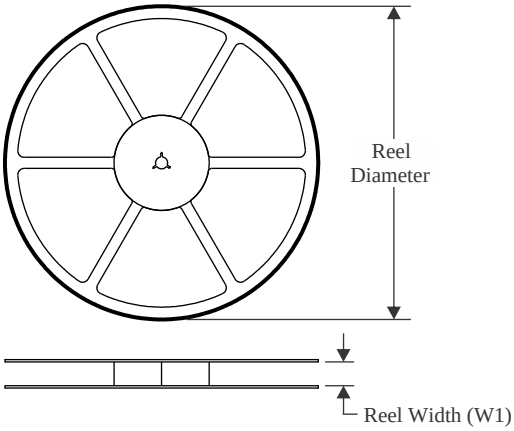
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

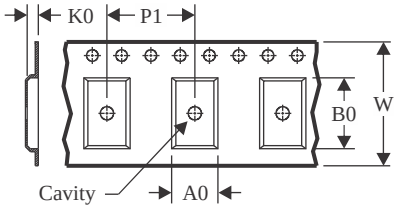
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

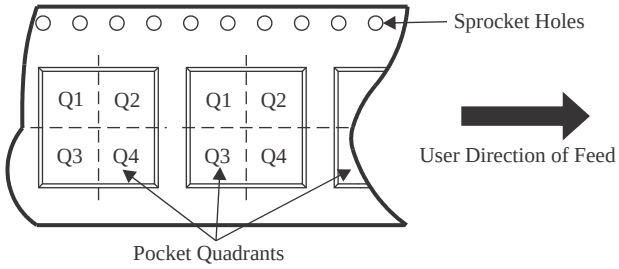


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

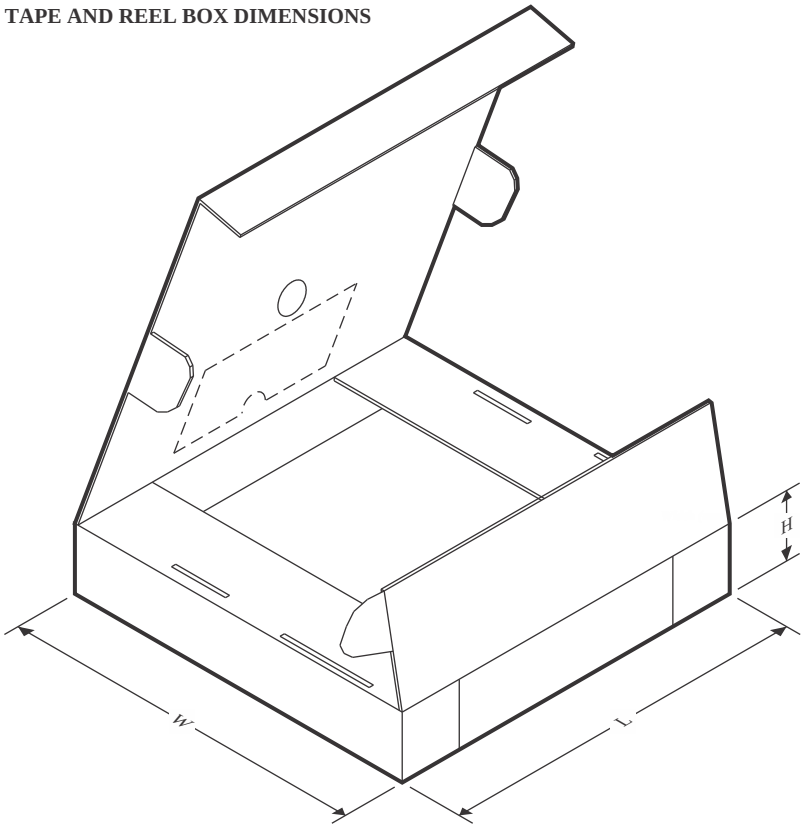
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

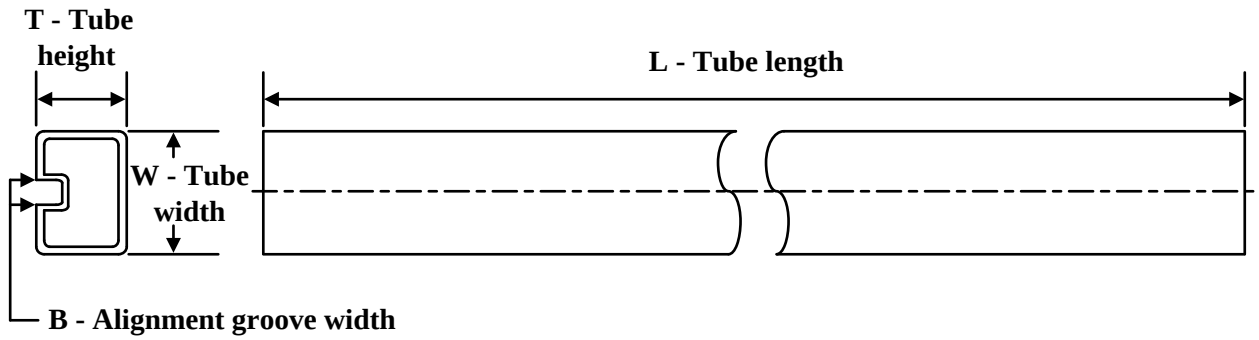
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9318301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN65LBC176P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC176P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC176P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC176P.A	P	PDIP	8	50	506	13.97	11230	4.32
SNJ55LBC176FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LBC176FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

GENERIC PACKAGE VIEW

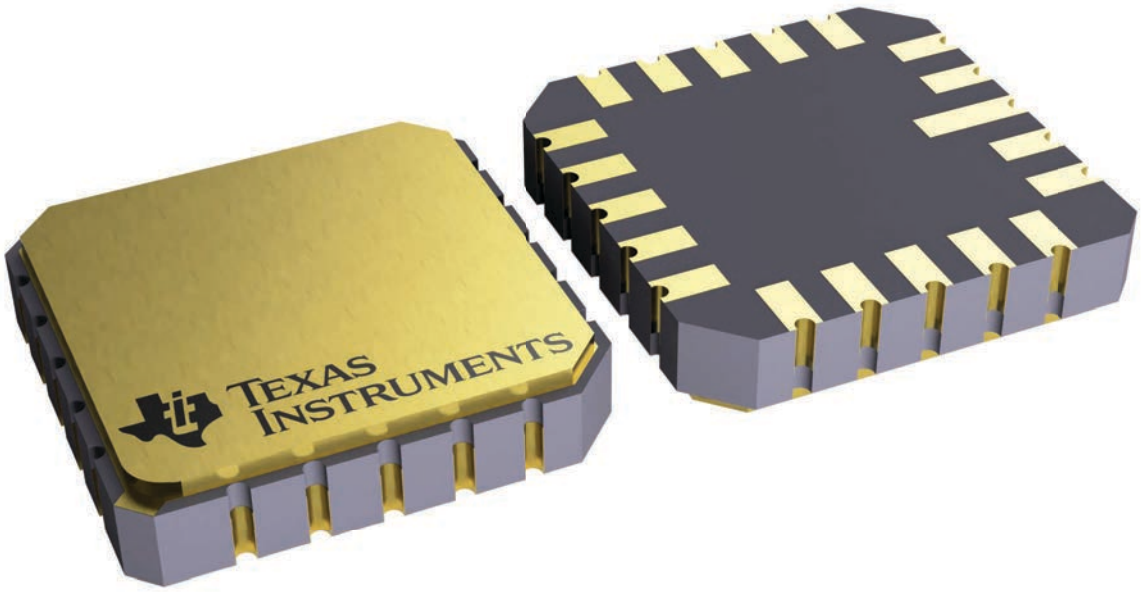
FK 20

LCCC - 2.03 mm max height

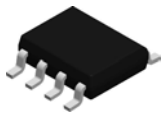
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

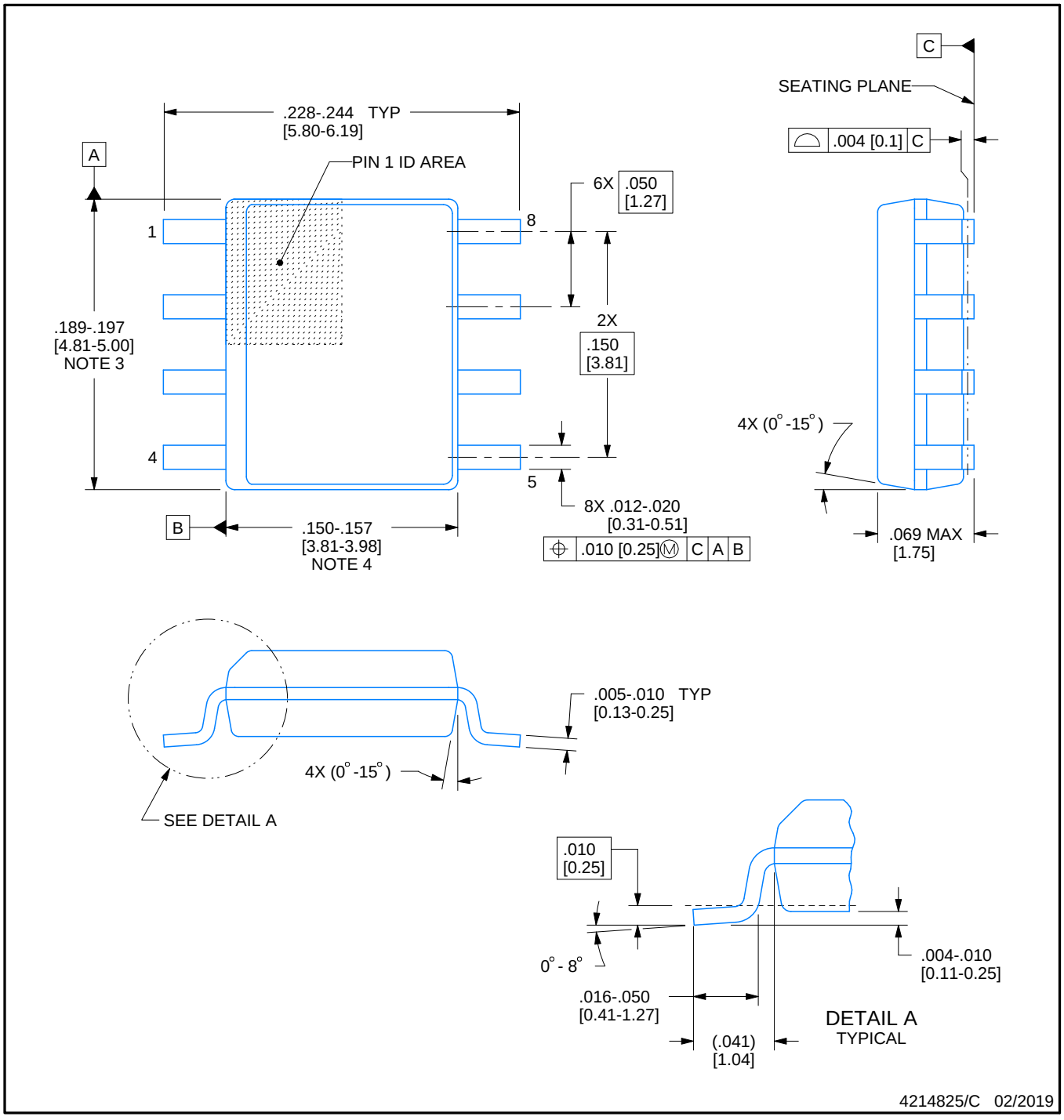


PACKAGE OUTLINE

D0008A

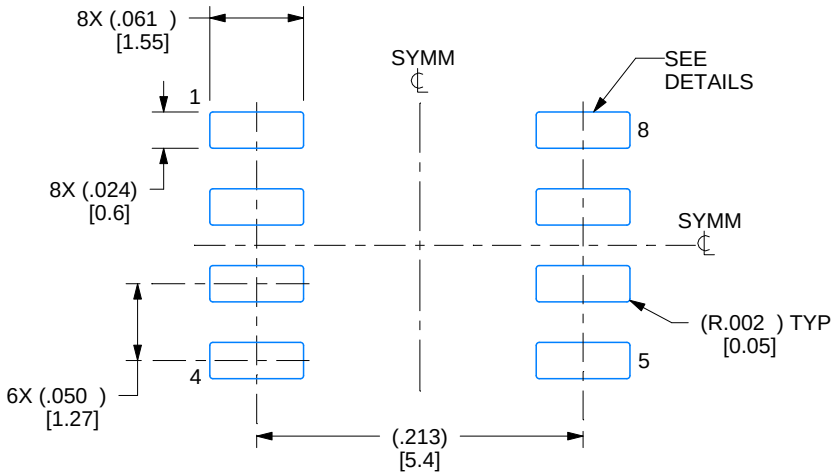
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

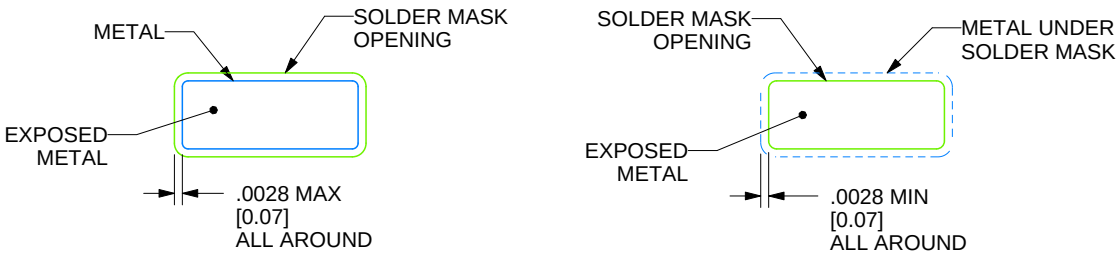


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

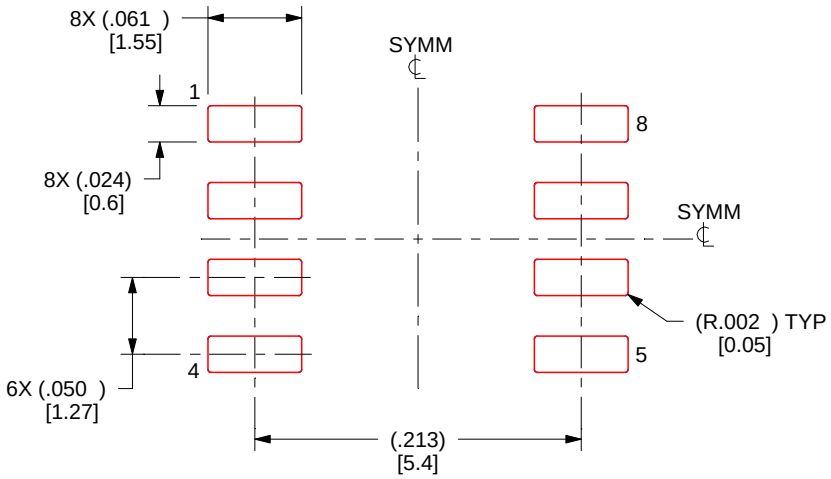
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



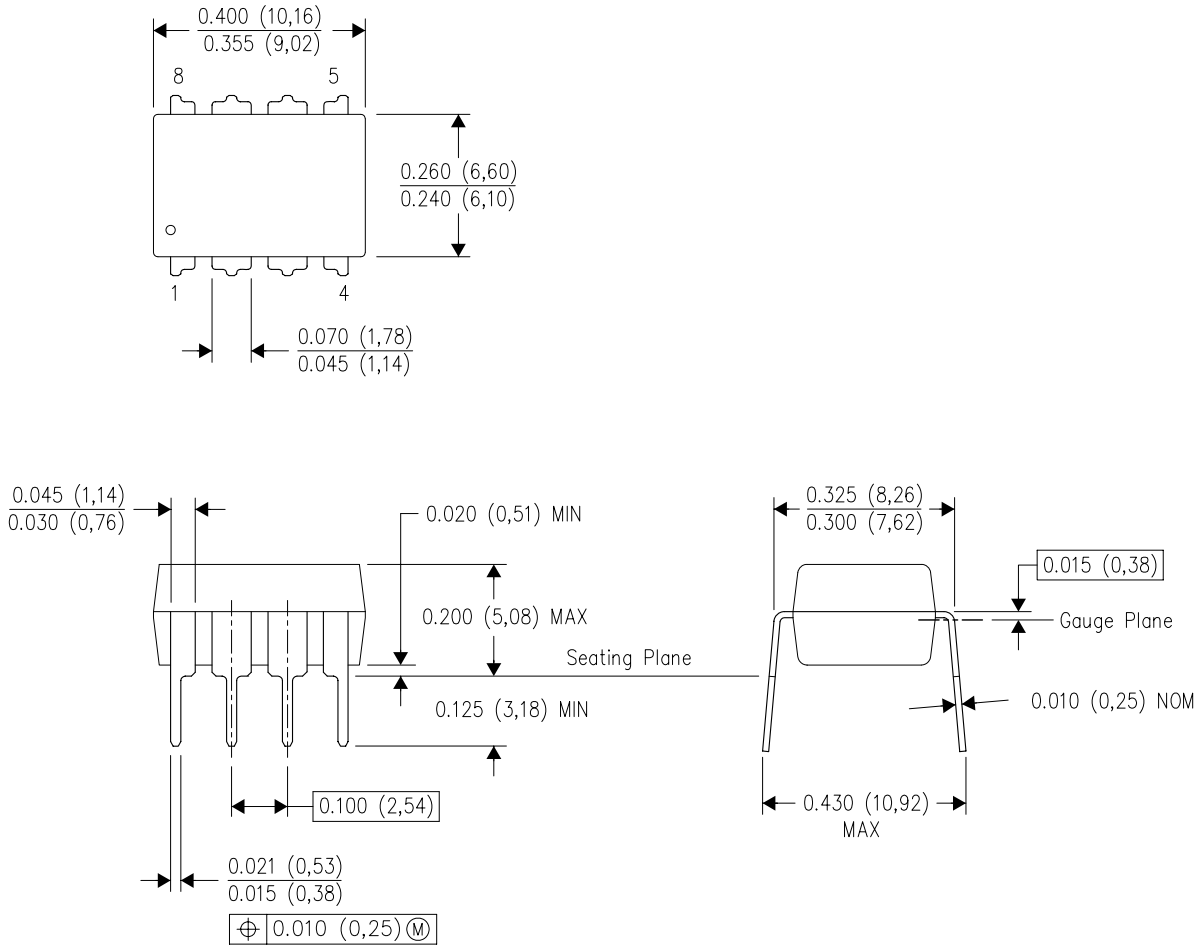
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



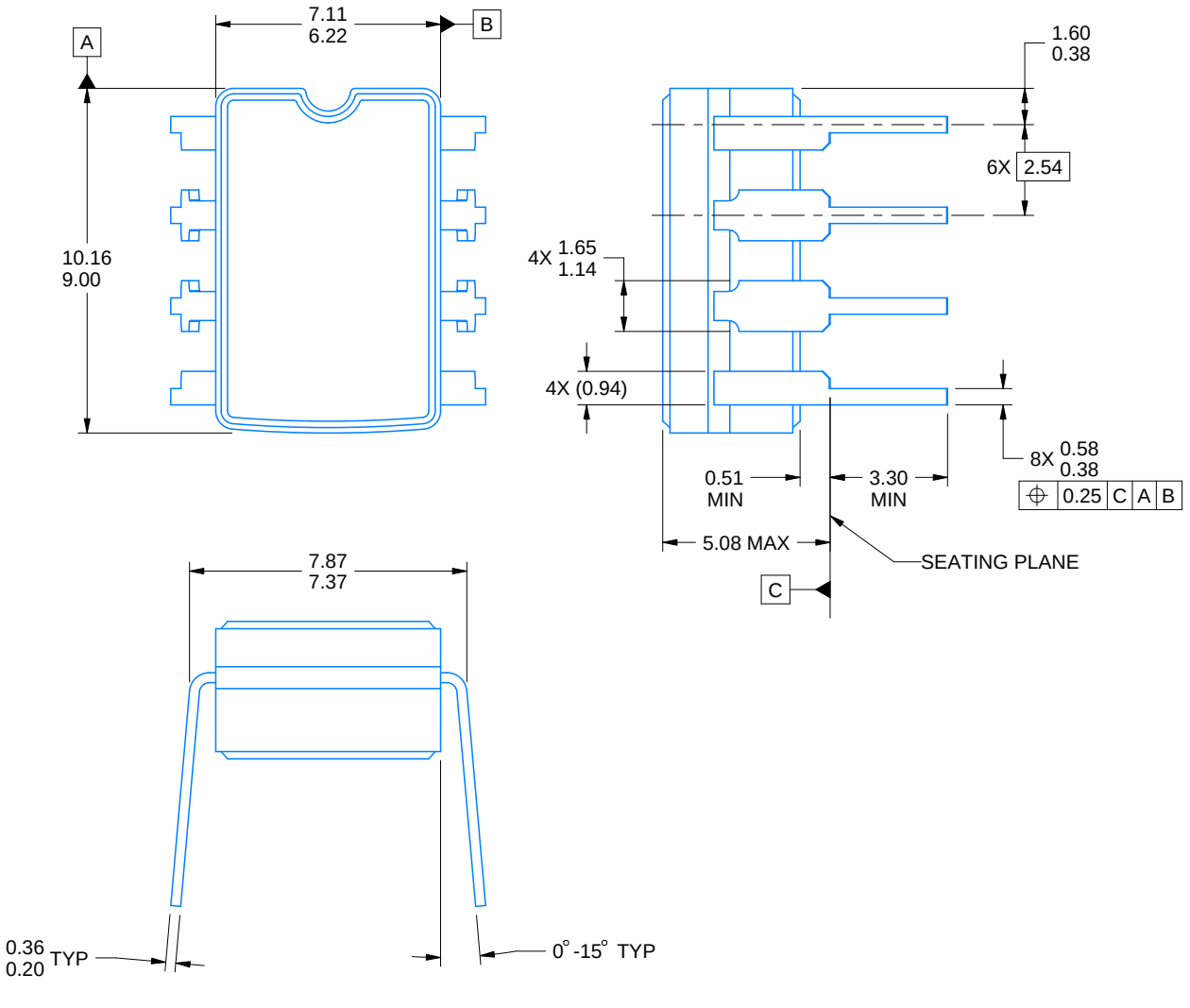
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

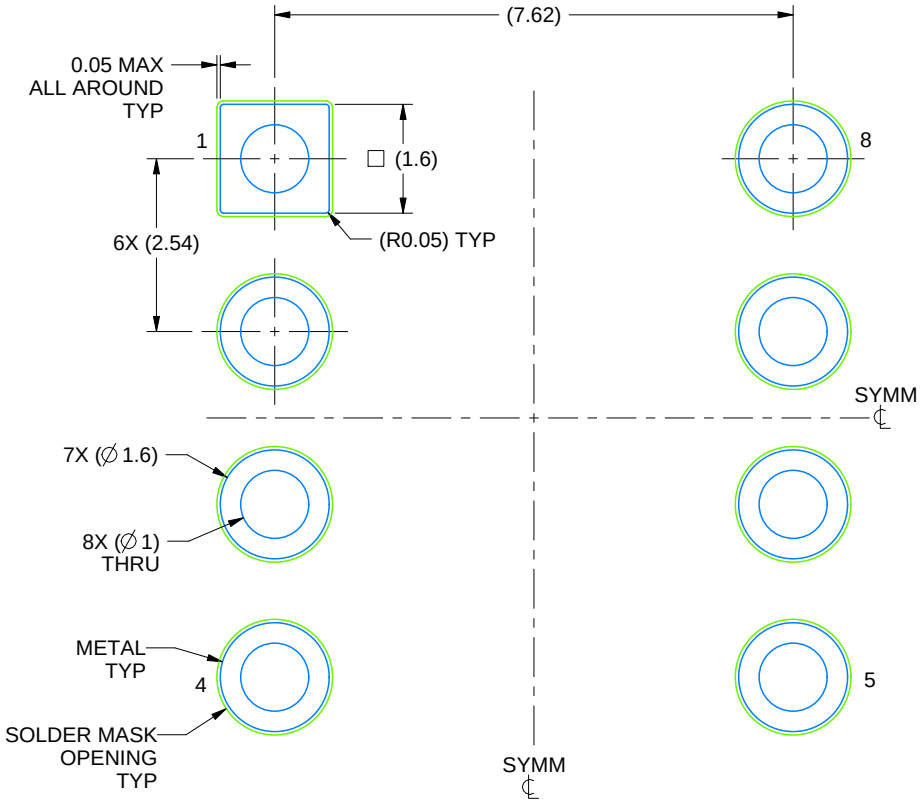
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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最終更新日：2025 年 10 月