TEXAS INSTRUMENTS
OPA333, OPA2333
JAJS010E – MARCH 2006 – REVISED DECEMBER 2015

OPAx333 1.8V、*micro*Power、CMOSゼロドリフト・シリーズ・オペアンプ

1 特長

- 低オフセット電圧：10μV (最大値)
- ゼロ·ドリフト：0.05μV/℃（最大値）
- 0.01Hz～10Hzのノイズ：1.1μV_{PP}
- 静止電流：17μA
- 単一電源動作
- 電源電圧：1.8V～5.5V
- レール・ツー・レール入出力
- *micro*Sizeパッケージ：SC70、SOT23

2 アプリケーション

- トランスデューサ
- 温度計測
- 電子計測器
- 医療用計測機器
- バッテリ駆動計測器
- ハンドヘルド・テスト機器

3 概要

CMOSオペアンプのOPAx333シリーズは、独自のオートキャリブレーション技術を使用して、非常に低いオフセット電圧（最大10μV）とゼロに限りなく近い時間および温度ドリフトを同時に提供します。これらの小型で高精度、低静止電流のオペアンプ·シリーズは、レールを100mV上回る同相範囲を持つ高インピーダンス入力と、レールの50mV以内でスイングするレール·ツー·レールの出力を提供します。さらに、+1.8V (±0.9V)の低電圧から最大+5.5V (±2.75V)までの単電源あるいは2電源で使用できます。このオペアンプ·シリーズは、低電圧の単電源動作に対して最適化されています。

OPAx333ファミリは、従来の相補入力段に起因するクロスオーバがない優れたCMRRを提供しています。この設計により、アナログ/デジタル·コンバータ(ADC)の微分直線性の低下がなく、優れたADC駆動性能が得られます。

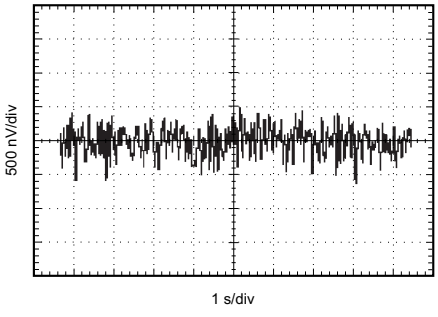
OPA333（シングル版）は5ピンSOT-23、SOT、および8ピンSOICパッケージで提供しています。OPA2333 (デュアル版)は8ピンVSON、SOIC、およびVSSOPパッケージで提供しています。これらはすべて−40℃～+125℃で動作を規定しています。

製品情報(1)

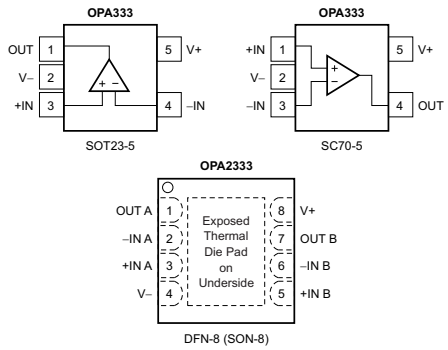
型番	パッケージ	本体サイズ(公称)
OPA333	SOT-23 (5)	2.90mm×1.60mm
	SOT (5)	2.00mm×1.25mm
	SOIC (8)	4.90mm×3.90mm
OPA2333	VSON (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.90mm
	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

0.1Hz～10Hzのノイズ



OPAx333ピン配置図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (November 2013) から **Revision E** に変更 **Page**

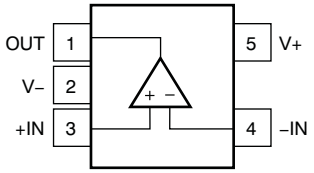
- *「ピン構成と機能」*セクション、*「ESD定格」*および*「熱に関する情報」*の表、*「機能概要」*セクション、*「デバイスの機能モード」*、*「アプリケーションと実装」*セクション、*「電源に関する推奨事項」*セクション、*「レイアウト」*セクション、*「デバイスおよびドキュメントのサポート」*セクション、*「メカニカル、パッケージ、および注文情報」*セクション 追加 ... 1

Revision C (May 2007) から **Revision D** に変更 **Page**

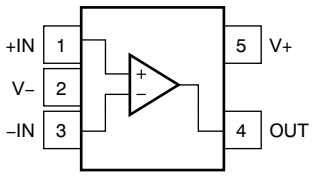
- データシートの形式を最新の標準的な外観に変更 ... 1
- OPA2333 DFN-8ピン配置を1ページ目に追加 ... 1
- Changed 2nd *signal input terminals* parameter in the Absolute Maximum Ratings from "voltage" to "current" (typo) ... 5
- Added Table 1 ... 8

5 Pin Configuration and Functions

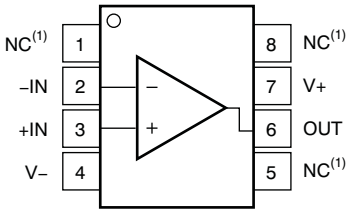
OPA333 DBV Package
5-Pin SOT
Top View



OPA333 DCK Package
5-Pin SC70
Top View



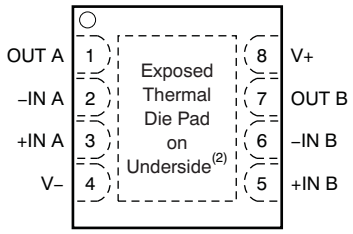
OPA333 D Package
8-Pin SOIC
Top View



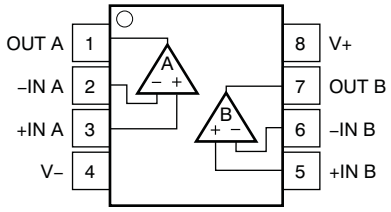
Pin Functions: OPA333

PIN				I/O	DESCRIPTION
NAME	SOIC	SOT	SC70		
+IN	3	3	1	I	Noninverting input
–IN	2	4	3	I	Inverting input
NC	1, 5, 8	—	—	—	No internal connection (can be left floating)
OUT	6	1	4	O	Output
V+	7	5	5	—	Positive (highest) power supply
V–	4	2	2	—	Negative (lowest) power supply

OPA2333 DRB Package
8-Pin VSON With Exposed Thermal Pad
Top View



OPA2333 D or DGK Package
8-Pin SOIC or VSSOP
Top View



Pin Functions: OPA2333

PIN			I/O	DESCRIPTION
NAME	VSON	SOIC, VSSOP		
+IN	—	—	I	Noninverting input
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
–IN	—	—	I	Inverting input
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
OUT	—	—	O	Output
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V+	8	8	—	Positive (highest) power supply
V–	4	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Voltage	Supply	7		V
	Signal input terminals(2)	–0.3	(V+) + 0.3	
Current	Signal input terminals(2)	–1	1	mA
	Output short-circuit(3)	Continuous		
Operating junction temperature, T_J			150	°C
Operating temperature, T_A		–40	150	
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage, V_S	1.8	5.5	V
Specified temperature	–40	125	°C

6.4 Thermal Information: OPA333

THERMAL METRIC(1)		OPA333			UNIT
		D (SOIC)	DBV (SOT)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.6	61.7	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2333

THERMAL METRIC(1)		OPA2333			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (VSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	180.3	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.0	2.4	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	22.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	10.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		2	10	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		0.02	0.05	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5.5 V, T_A = –40°C to 125°C		1	5	µV/V
	Long-term stability(1)			See note (1)		µV
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A= 25°C		±70	±200	pA
		T_A = –40°C to 125°C		±150		
I_{OS}	Input offset current			±140	±400	
NOISE						
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz		1.1		
i_n	Input current noise	f = 10 Hz		100		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to 125°C	106	130		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ, T_A = –40°C to 125°C	106	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = +1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	R_L = 10 kΩ		30	50	mV
		R_L = 10 kΩ, T_A = –40°C to 125°C			70	
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive			See *Typical Characteristics*		
	Open-loop output impedance	f = 350 kHz, I_O = 0 A		2		kΩ
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 A		17	25	µA
		T_A = –40°C to 125°C			28	
	Turn-on time	V_S = +5 V		100		µs
TEMPERATURE						
T_A	Specified range		–40		125	°C
	Operating range		–40		150	°C
T_{stg}	Storage range		–65		150	°C

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

6.7 Typical Characteristics

Table 1. List of Typical Characteristics

TITLE	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Production Distribution	Figure 2
Open-Loop Gain vs Frequency	Figure 3
Common-Mode Rejection Ratio vs Frequency	Figure 4
Power-Supply Rejection Ratio vs Frequency	Figure 5
Output Voltage Swing vs Output Current	Figure 6
Input Bias Current vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Quiescent Current vs Temperature	Figure 9
Large-Signal Step Response	Figure 10
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Positive Overvoltage Recovery	Figure 12
Negative Overvoltage Recovery	Figure 13
Settling Time vs Closed-Loop Gain	Figure 14
Small-Signal Overshoot vs Load Capacitance	Figure 15
0.1-Hz to 10-Hz Noise	Figure 16
Current and Voltage Noise Spectral Density vs Frequency	Figure 17

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

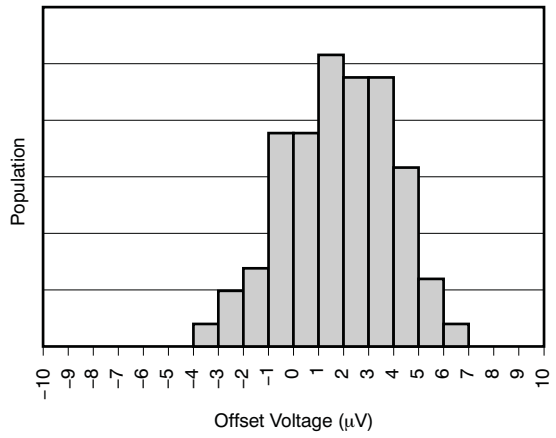


Figure 1. Offset Voltage Production Distribution

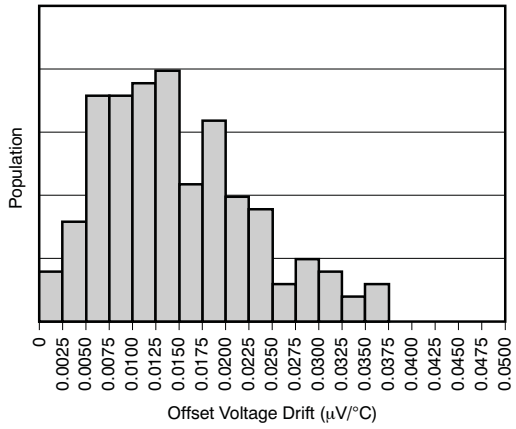


Figure 2. Offset Voltage Drift Production Distribution

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

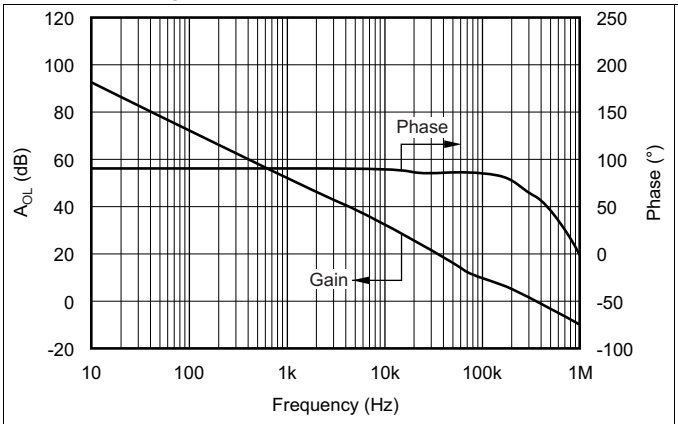


Figure 3. Open-Loop Gain and Phase vs Frequency

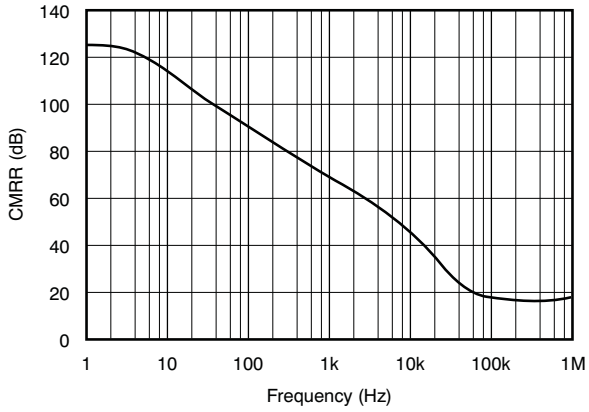


Figure 4. Common-Mode Rejection Ratio vs Frequency

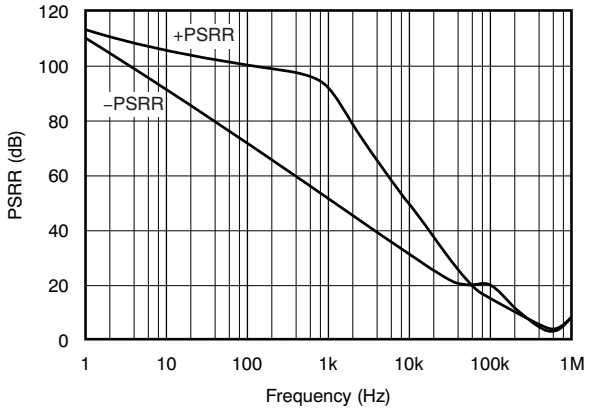


Figure 5. Power-Supply Rejection Ratio vs Frequency

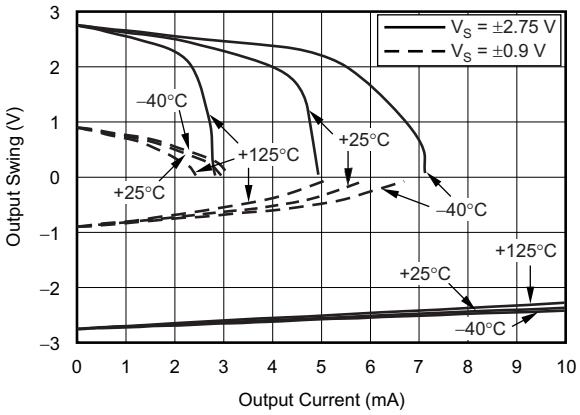


Figure 6. Output Voltage Swing vs Output Current

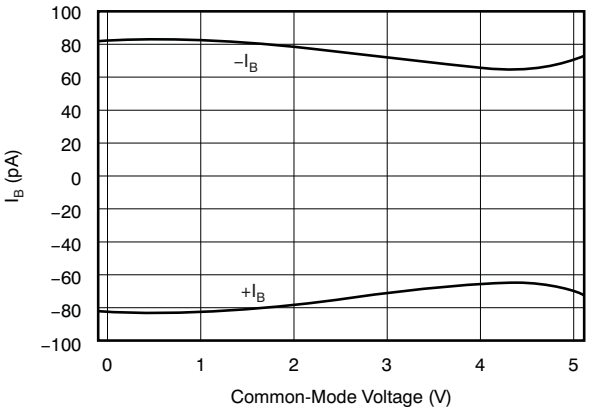


Figure 7. Input Bias Current vs Common-Mode Voltage

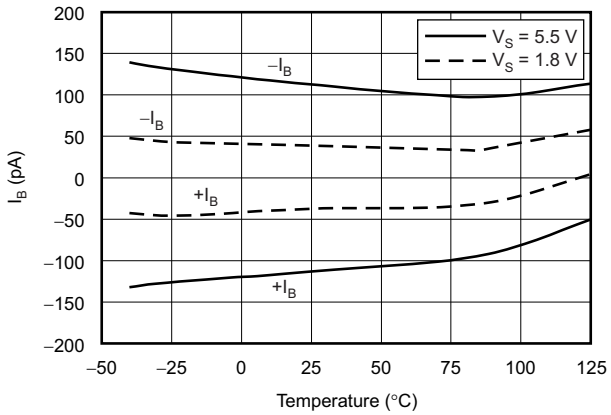


Figure 8. Input Bias Current vs Temperature

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

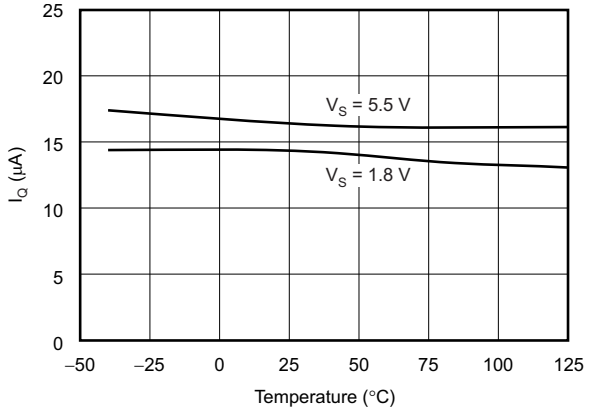


Figure 9. Quiescent Current vs Temperature

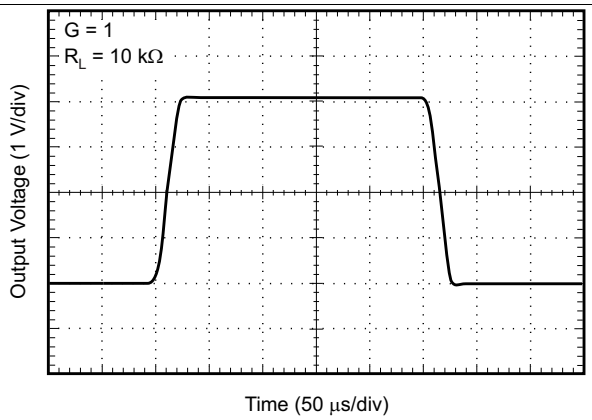


Figure 10. Large-Signal Step Response

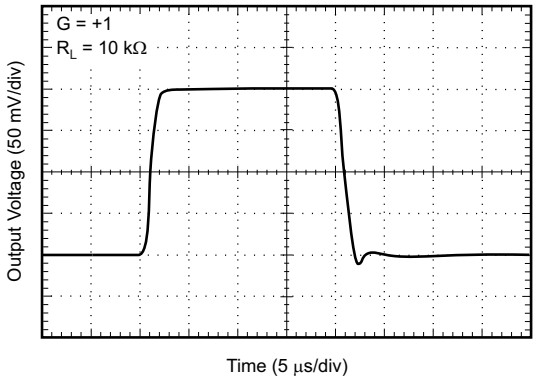


Figure 11. Small-Signal Step Response

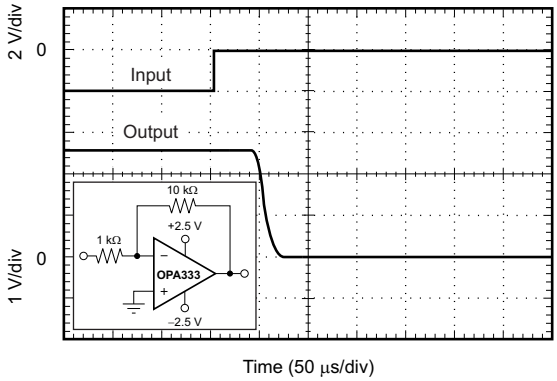


Figure 12. Positive Overvoltage Recovery

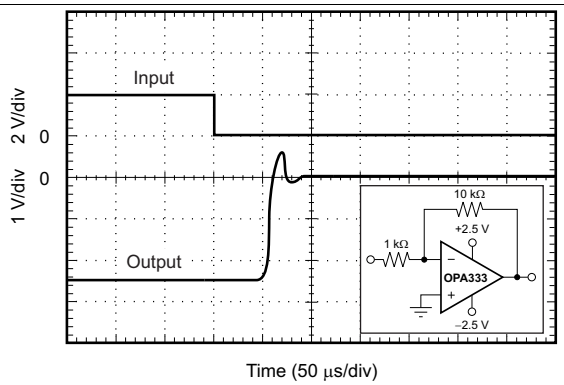


Figure 13. Negative Overvoltage Recovery

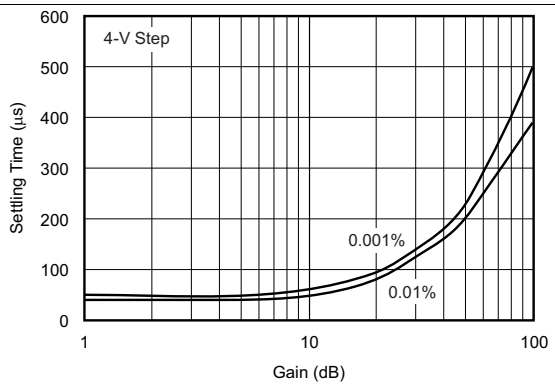


Figure 14. Settling Time vs Closed-Loop Gain

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

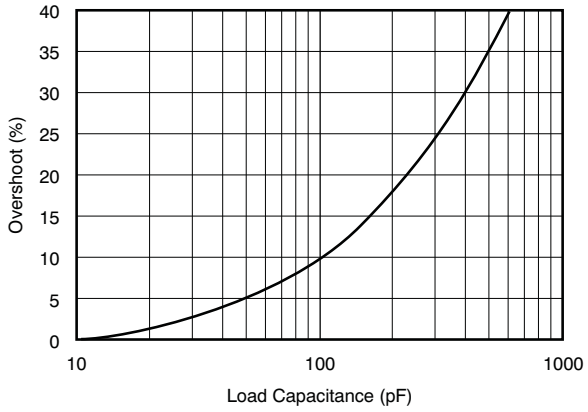


Figure 15. Small-Signal Overshoot vs Load Capacitance

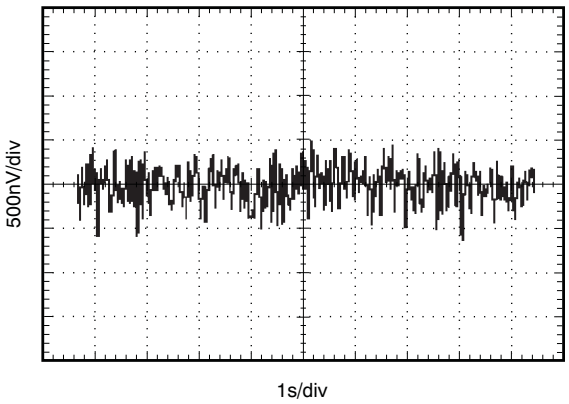


Figure 16. 0.1-Hz to 10-Hz Noise

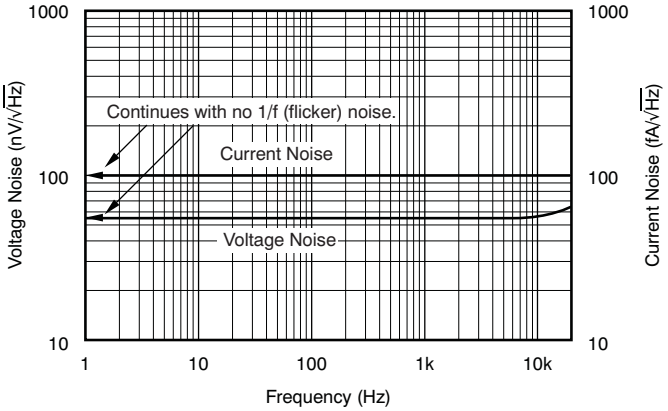


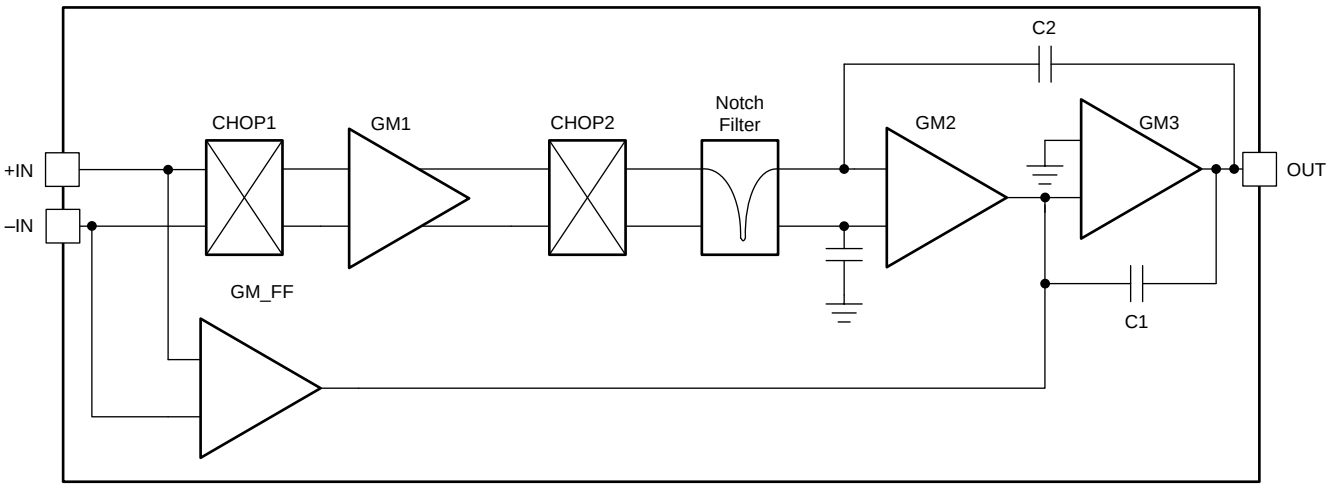
Figure 17. Current and Voltage Noise Spectral Density vs Frequency

7 Detailed Description

7.1 Overview

The OPAx333 is a family of Zero-Drift, low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The Zero-Drift architecture provides ultra low offset voltage and near-zero offset voltage drift.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA333 and OPA2333 are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

7.3.1 Operating Voltage

The OPA333 and OPA2333 operational amplifiers operate over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section.

CAUTION

Supply voltages higher than +7 V (absolute maximum) can permanently damage the device.

Feature Description (continued)

7.3.2 Input Voltage

The OPA333 and OPA2333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 70 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

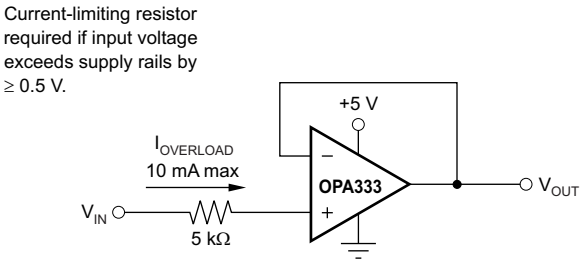


Figure 18. Input Current Protection

7.3.3 Internal Offset Correction

The OPA333 and OPA2333 operational amplifiers use an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.4 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good, single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA333 and OPA2333 can be made to swing to, or slightly below, ground on a single-supply power source. This swing is achieved with the use of the use of another resistor and an additional, more negative power supply than the operational amplifier negative supply. A pulldown resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 19.

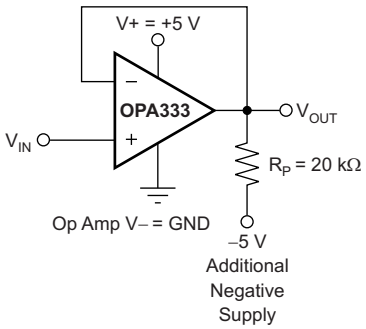


Figure 19. V_{OUT} Range to Ground

Feature Description (continued)

The OPA333 and OPA2333 have an output stage that allows the output voltage to be pulled to the negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333 and OPA2333 are characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ.

NOTE

This configuration increases the current consumption by several hundreds of microamps.

Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns after the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

7.3.5 DFN Package

The OPA2333 is offered in an DFN-8 package (also known as *SON*). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard PCB assembly techniques. See Application Reports SLUA271, *QFN/SON PCB Attachment* and SCBA017, *Quad Flatpack No-Lead Logic Packages*, both are available for download at www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the package should be connected to V– or left unconnected.

7.4 Device Functional Modes

The OPAx333 device has a single functional mode. The device is powered on as long as the power supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx333 family is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-μF capacitors are adequate.

8.2 Typical Applications

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 20 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 21 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333 facilitate excellent dc accuracy for the circuit.

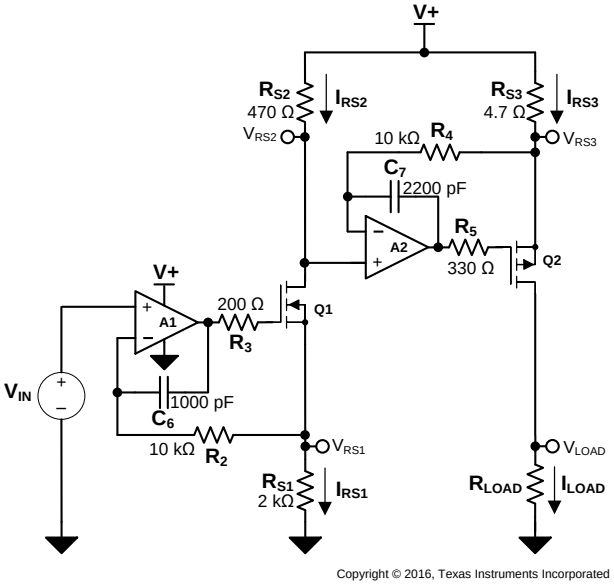


Figure 20. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

8.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2333 CMOS operational amplifier is a high-precision, 5-uV offset, 0.05-μV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2333 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2333 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in TIPD102.

8.2.1.3 Application Curve

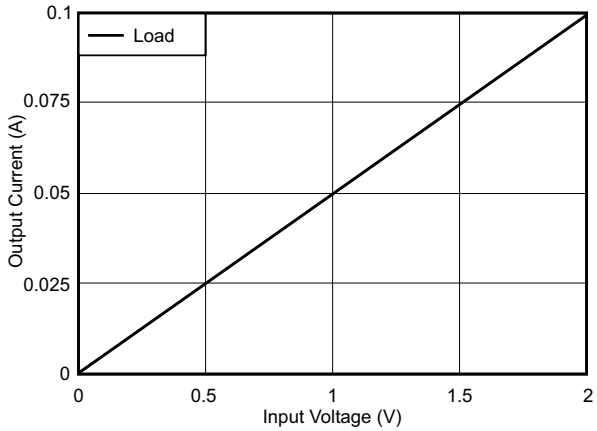


Figure 21. Measured Transfer Function for High-Side V-I Converter

Typical Applications (continued)

8.2.2 Precision, Low-Level Voltage-to-Current (V-I) Converter

The circuit shown in Figure 22 is a precision, low-level voltage-to-current (V-I) converter. The converter translates in input voltage of 0 V to 5 V and output current of 0 µA to 5 µA. Figure 23 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333 facilitate excellent dc accuracy for the circuit. Figure 24 shows the calibrated error for the entire range of the circuit.

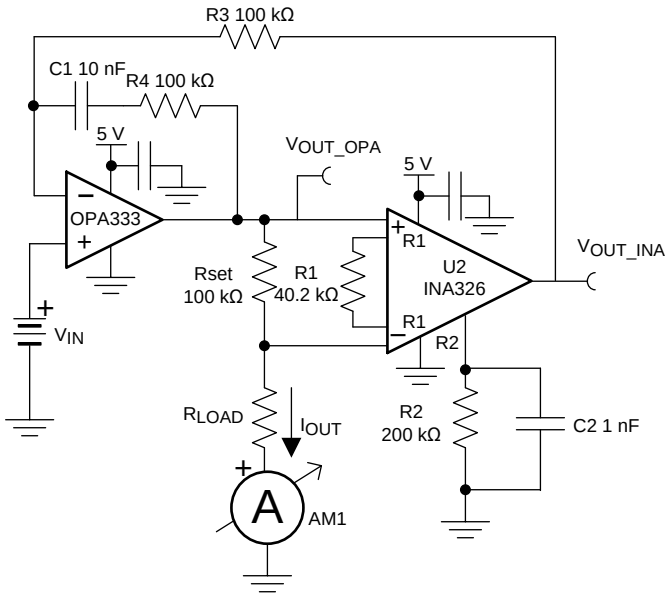


Figure 22. Low-Level, Precision V-I Converter

8.2.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 5 V DC
- Output: 0 µA to 5 µA DC

8.2.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, R_{SET}, and the instrumentation amplifier (INA) gain. During operation, the input voltage divided by the INA gain appears across the set resistor in Equation 1:

$$V_{SET} = V_{IN}/G_{INA} \quad (1)$$

The current through R_{SET} must flow through the load, so I_{OUT} is V_{SET} / R_{SET}. I_{OUT} remains a well-regulated current as long as the total voltage across R_{SET} and R_{LOAD} does not violate the output limits of the operational amplifier or the input common-mode limits of the INA. The voltage across the set resistor (V_{SET}) is the input voltage divided by the INA gain (that is, V_{SET} = 1 V / 10 = 0.1 V). The current is determined by V_{SET} and R_{SET} shown in Equation 2:

$$I_{OUT} = V_{SET} / R_{SET} = 0.1\ V / 100\ k\Omega = 1\ \mu A \quad (2)$$

A detailed error analysis, design procedure, and additional measured results are given in TIPD107.

Typical Applications (continued)

8.2.2.3 Application Curves

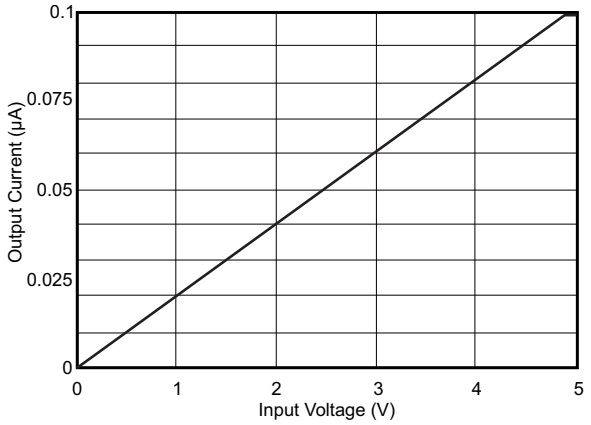


Figure 23. Measured Transfer Function for Low-Level Precision V-I

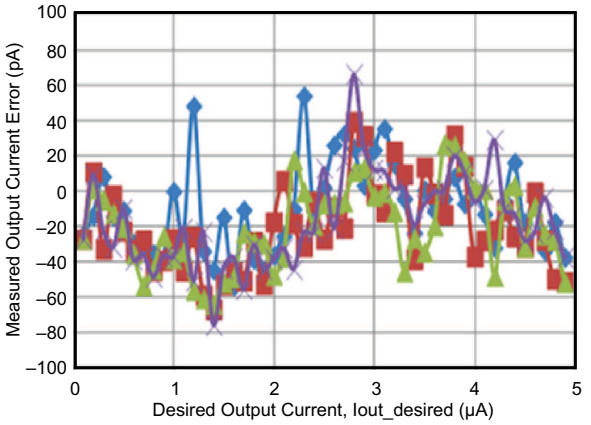


Figure 24. Calibrated Output Error for Low-Level V-I

8.2.3 Composite Amplifier

The circuit shown in Figure 25 is a composite amplifier used to drive the reference on the ADS8881. The OPA333 provides excellent dc accuracy, and the THS4281 allows the output of the circuit to respond quickly to the transient current requirements of a typical SAR data converter reference input. The ADS8881 system was optimized for THD and achieved a measured performance of –110 dB. The linearity of the ADC is shown Figure 26.

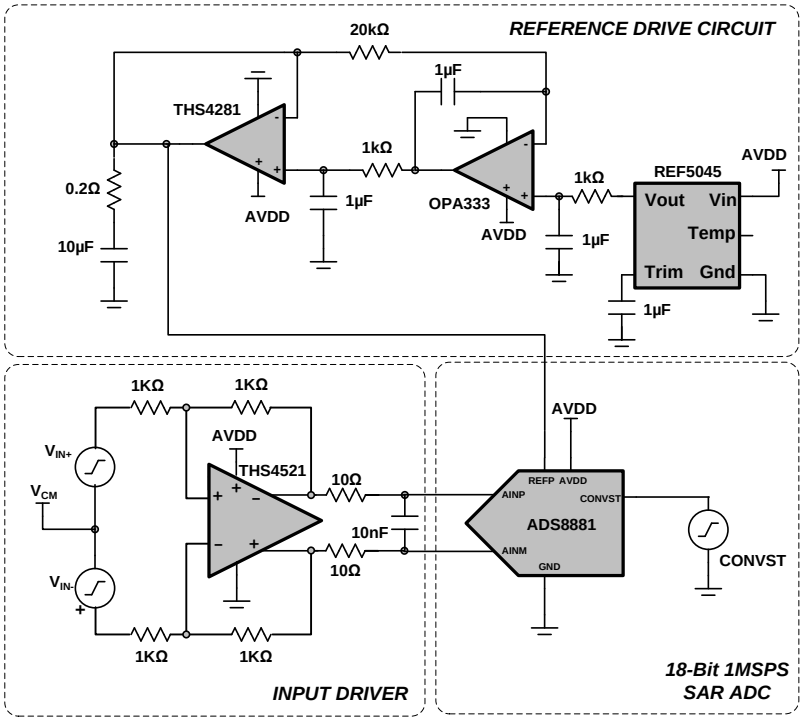


Figure 25. Composite Amplifier Reference Driver Circuit

Typical Applications (continued)

8.2.3.1 Design Requirements

The design requirements for this block design are:

- System Supply Voltage: 5 V DC
- ADC Supply Voltage: 3.3 V DC
- ADC Sampling Rate: 1 MSPS
- ADC Reference Voltage (VREF): 4.5 V DC
- ADC Input Signal: A differential input signal with amplitude of V_{pk} = 4.315 V (–0.4 dBFS to avoid clipping) and frequency, f_{IN} = 10 kHz are applied to each differential input of the ADC

8.2.3.2 Detailed Design Procedure

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver design. The circuit comprises the critical analog circuit blocks, the input driver, anti-aliasing filter, and the reference driver. Each analog circuit block should be carefully designed based on the ADC performance specifications in order to maximize the distortion and noise performance of the data acquisition system while consuming low power. The diagram includes the most important specifications for each individual analog block. This design systematically approaches the design of each analog circuit block to achieve a 16-bit, low-noise and low-distortion data acquisition system for a 10-kHz sinusoidal input signal. The first step in the design requires an understanding of the requirement of extremely low distortion input driver amplifier. This understanding helps in the decision of an appropriate input driver configuration and selection of an input amplifier to meet the system requirements. The next important step is the design of the anti-aliasing RC-filter to attenuate ADC kick-back noise while maintaining the amplifier stability. The final design challenge is to design a high-precision reference driver circuit, which would provide the required value VREF with low offset, drift, and noise contributions.

In designing a very low distortion data acquisition block, it is important to understand the sources of nonlinearity. Both the ADC and the input driver introduce nonlinearity in a data acquisition block. To achieve the lowest distortion, the input driver for a high-performance SAR ADC must have a distortion that is negligible against the ADC distortion. This parameter requires the input driver distortion to be 10 dB lower than the ADC THD. This stringent requirement ensures that overall THD of the system is not degraded by more than –0.5 dB.

$$THD_{AMP} < THD_{ADC} - 10\ dB \quad (3)$$

It is therefore important to choose an amplifier that meets the above criteria to avoid the system THD from being limited by the input driver. The amplifier nonlinearity in a feedback system depends on the available loop gain. A detailed error analysis, design procedure, and additional measured results are given in TIPD115.

8.2.3.3 Application Curve

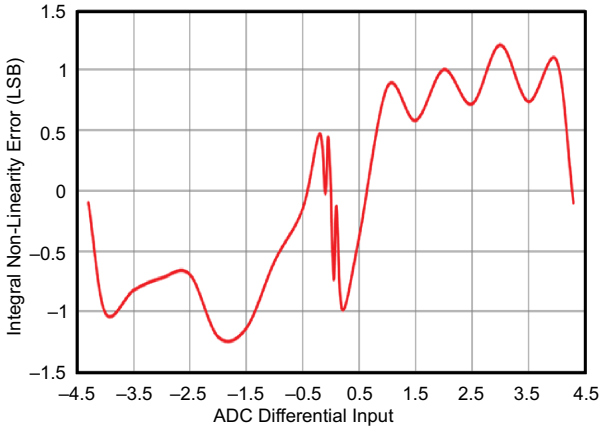


Figure 26. Linearity of the ADC8881 System

8.3 System Examples

8.3.1 Temperature Measurement Application

Figure 27 shows a temperature measurement application.

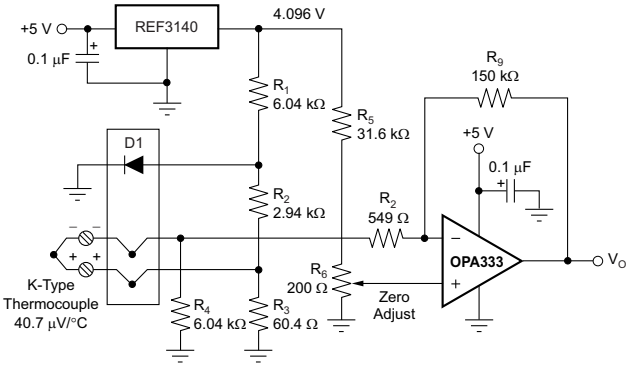


Figure 27. Temperature Measurementf

8.3.2 Single Operational Amplifier Bridge Amplifier Application

Figure 28 shows the basic configuration for a bridge amplifier.

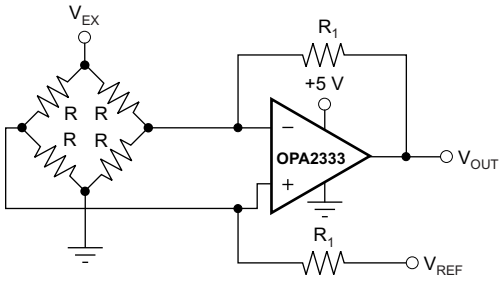
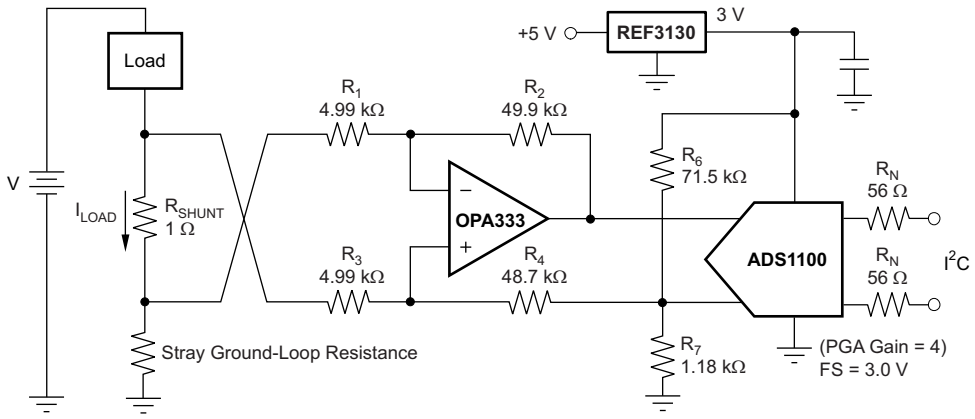


Figure 28. Single Operational Amplifier Bridge Amplifier

8.3.3 Low-Side Current Monitor Application

A low-side current shunt monitor is shown in Figure 29. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.

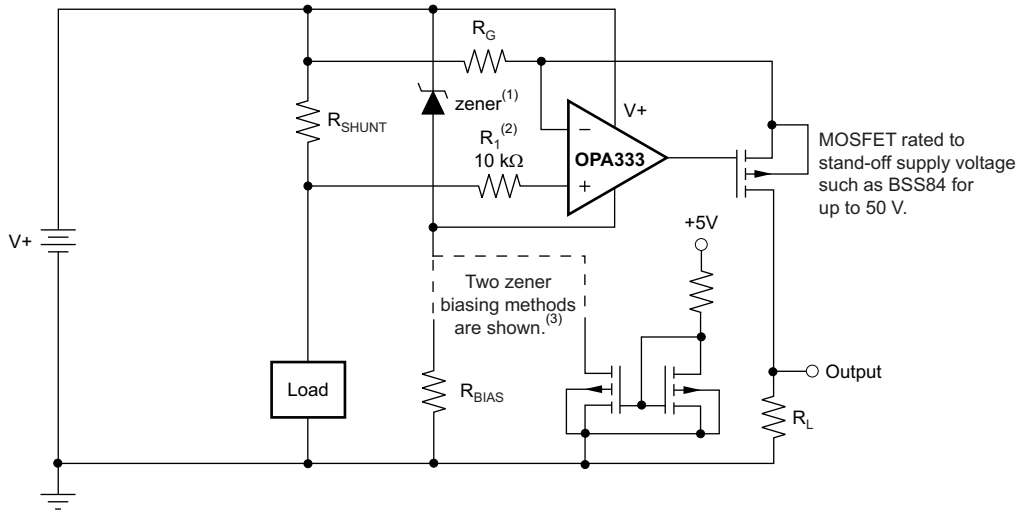


NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 29. Low-Side Current Monitor

8.3.4 Other Applications

Additional application ideas are shown in Figure 30 through Figure 33.



(1) Zener rated for op amp supply capability (that is, 5.1 V for OPA333).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual N-MOSFETs (FDG6301N, NTJD4001N, or Si1034).

Figure 30. High-Side Current Monitor

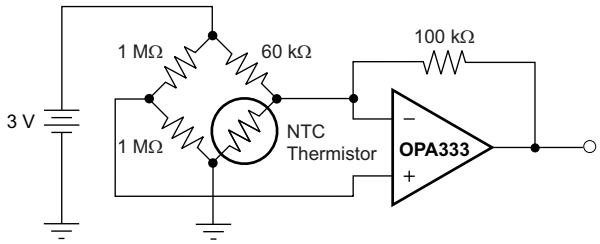


Figure 31. Thermistor Measurement

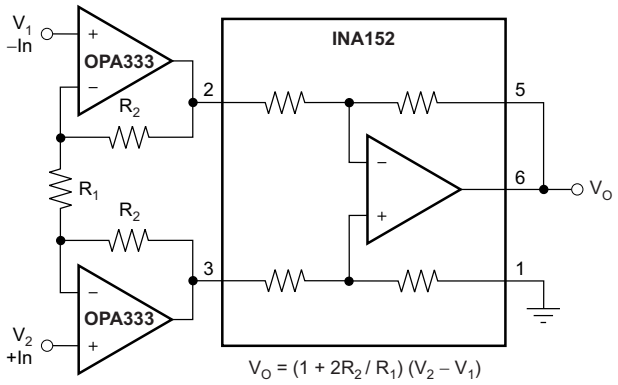
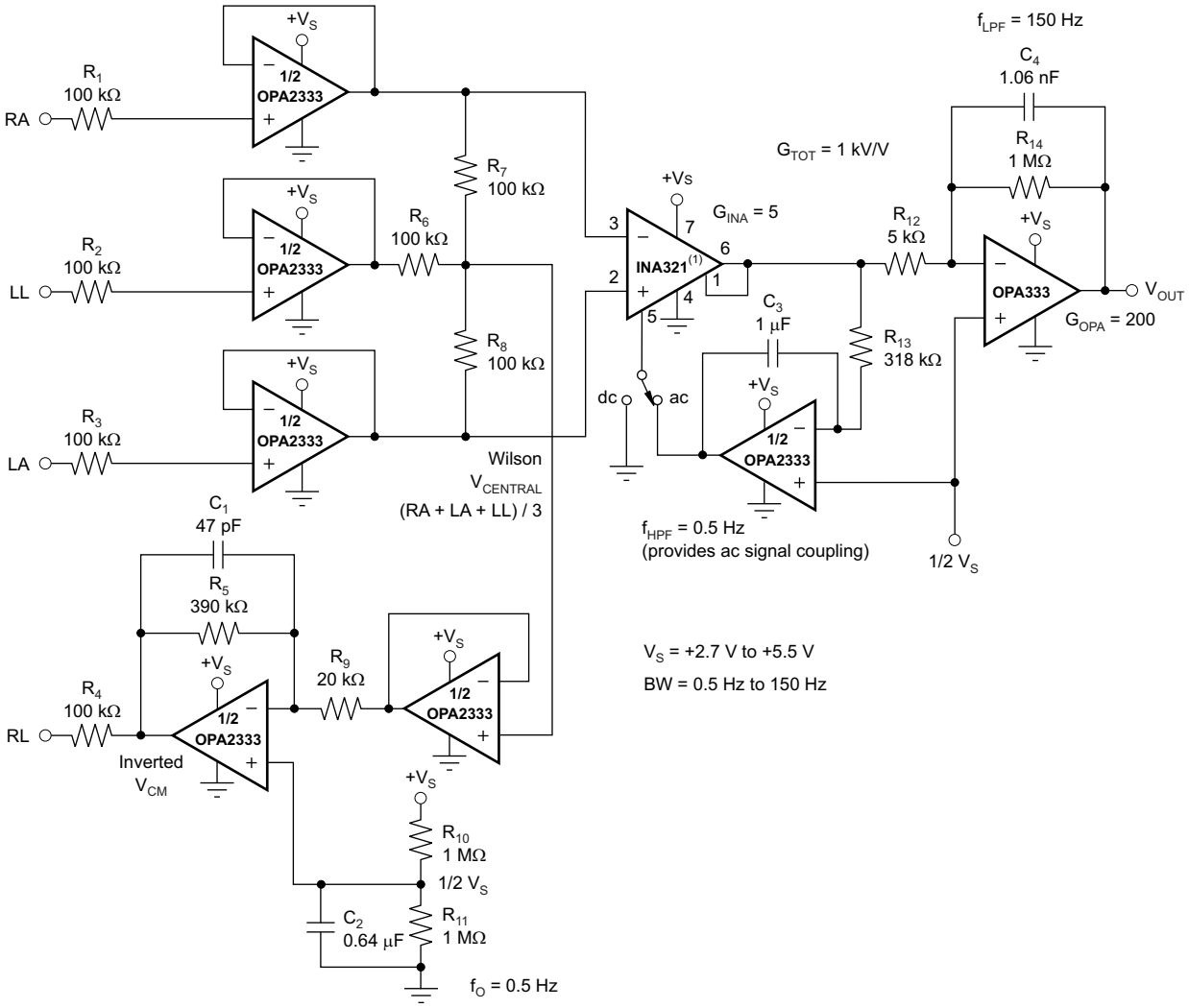


Figure 32. Precision Instrumentation Amplifier



(1) Other instrumentation amplifiers can be used, such as the INA326, which has lower noise, but higher quiescent current.

Figure 33. Single-Supply, Very Low Power, ECG Circuit

9 Power Supply Recommendations

The OPAx333 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

10 Layout

10.1 Layout Guidelines

10.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA333 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

10.1.2 DFN Layout Guidelines

Solder the exposed leadframe die pad on the DFN package to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

10.2 Layout Example

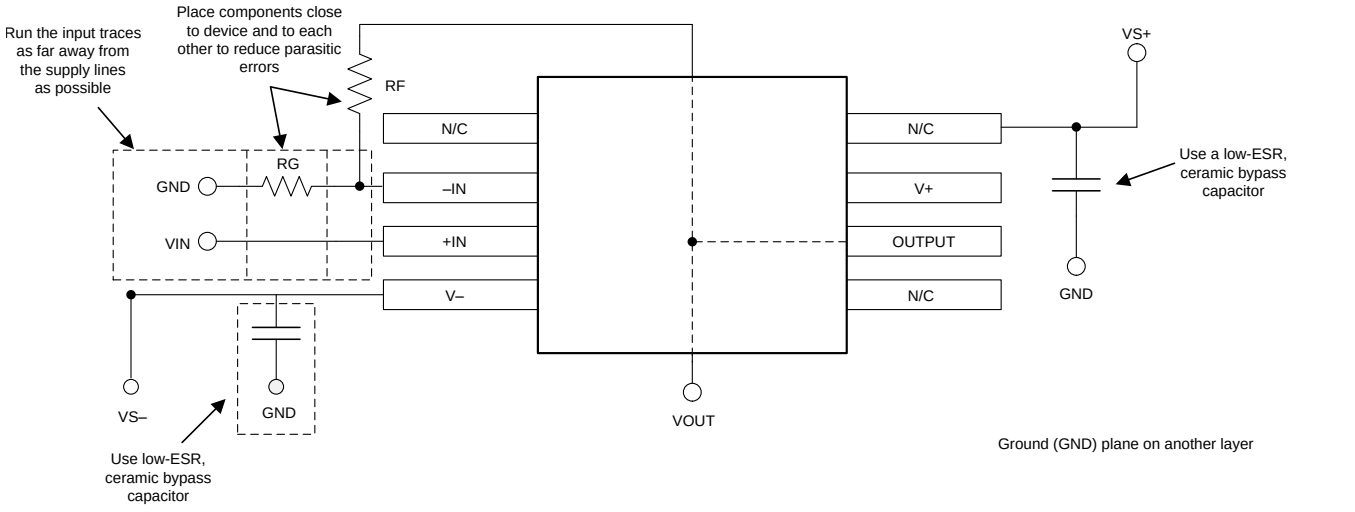


Figure 34. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

この製品の開発サポートについては、以下を参照してください。

- *ハイサイドV-Iコンバータ*、*0V～2V入力*、*0mA～100mA出力*、*1%フルスケール誤差*、TIPD102
- *低レベルV-Iコンバータ・リファレンス・デザイン*、*0V～5V入力*、*0μA～5μA出力*、TIPD107
- *18ビット*、*1MSPS*、*シリアル・インターフェイス*、*マイクロパワー*、*真の差動入力*、*SAR型ADC*、ADS8881
- *超低消費電力*、*高速*、*レール・ツー・レール入出力*、*電圧帰還オペアンプ*、THS4281
- *最小歪みと最小ノイズを実現するために最適化されたデータ・アクイジション*、*18ビット*、*1MSPSのリファレンス・デザイン*、TIPD115
- *セルフ・キャリブレーション*、*16ビットA/Dコンバータ*、ADS1100
- *最大20 ppm/℃*、*100uA*、*SOT23-3シリーズ基準電圧*、REF3130
- *高精度*、*低ドリフト*、*CMOS計装アンプ*、INA326

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『QFN/SON PCB Attachment』*、SLUA271
- *『クワッド・フラットパックの鉛フリー・ロジック・パッケージ』*、SCBA017

11.3 関連リンク

表 2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA333	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2333	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。***エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2333AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A
OPA2333AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A
OPA2333AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A
OPA2333AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDGKTG4.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBAQ
OPA2333AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A
OPA2333AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A
OPA2333AIDRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ
OPA2333AIDRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ
OPA2333AIDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ
OPA2333AIDRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ
OPA2333AIDRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ
OPA2333AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A
OPA333AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ
OPA333AIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ
OPA333AIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ
OPA333AIDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ
OPA333AIDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ
OPA333AIDBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA333AIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	BQY
OPA333AIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BQY
OPA333AIDCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BQY
OPA333AIDCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	BQY
OPA333AIDCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BQY
OPA333AIDCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	BQY
OPA333AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A
OPA333AIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA2333, OPA333 :

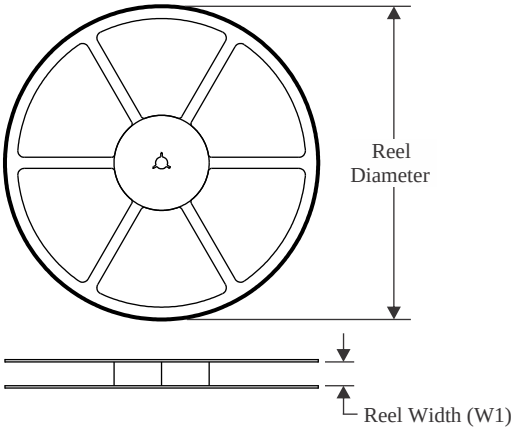
- Automotive : OPA2333-Q1, OPA333-Q1

NOTE: Qualified Version Definitions:

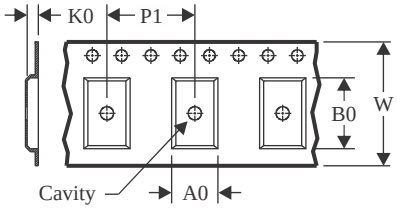
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

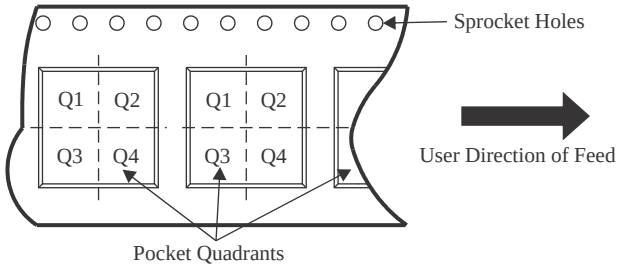


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

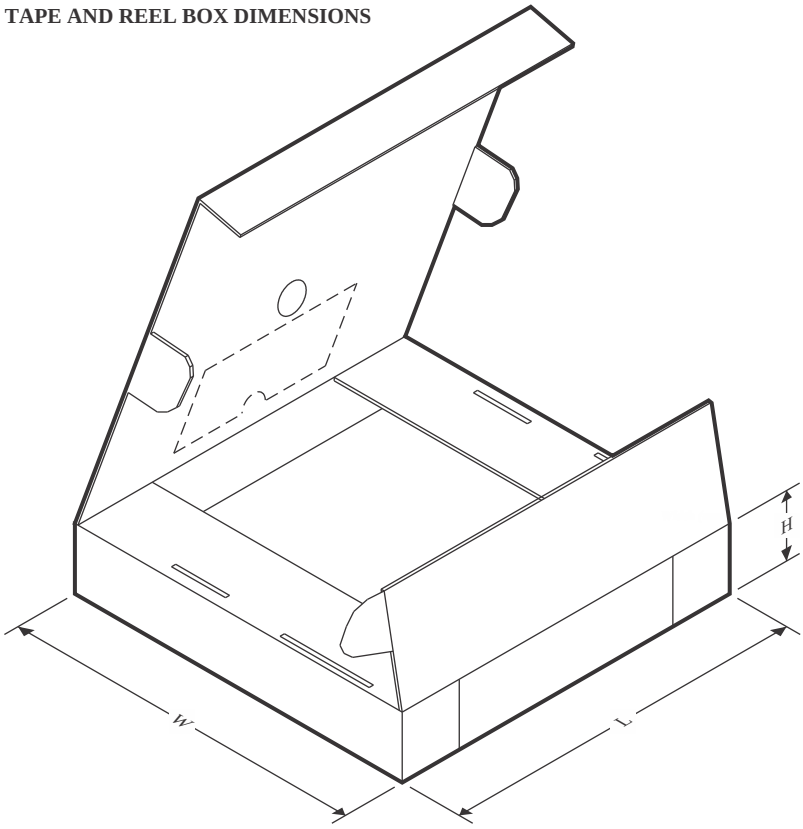


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2333AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2333AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA333AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA333AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA333AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
OPA333AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
OPA333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA333AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

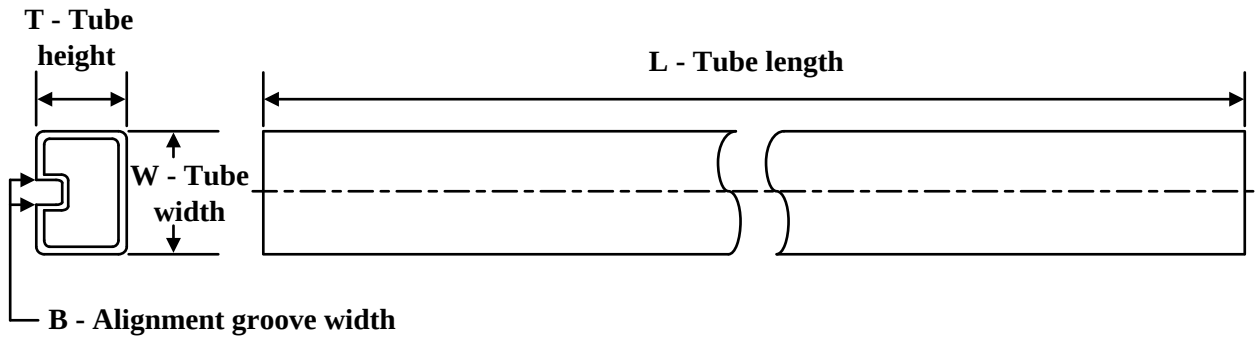
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2333AIDGKRG4	VSSOP	DGK	8	2500	364.0	364.0	27.0
OPA2333AIDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2333AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2333AIDGKTG4	VSSOP	DGK	8	250	364.0	364.0	27.0
OPA2333AIDGKTG4	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2333AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2333AIDRBR	SON	DRB	8	3000	353.0	353.0	32.0
OPA2333AIDRBT	SON	DRB	8	250	213.0	191.0	35.0
OPA333AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA333AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA333AIDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
OPA333AIDCKR	SC70	DCK	5	3000	200.0	183.0	25.0
OPA333AIDCKT	SC70	DCK	5	250	200.0	183.0	25.0
OPA333AIDCKT	SC70	DCK	5	250	210.0	185.0	35.0
OPA333AIDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA333AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

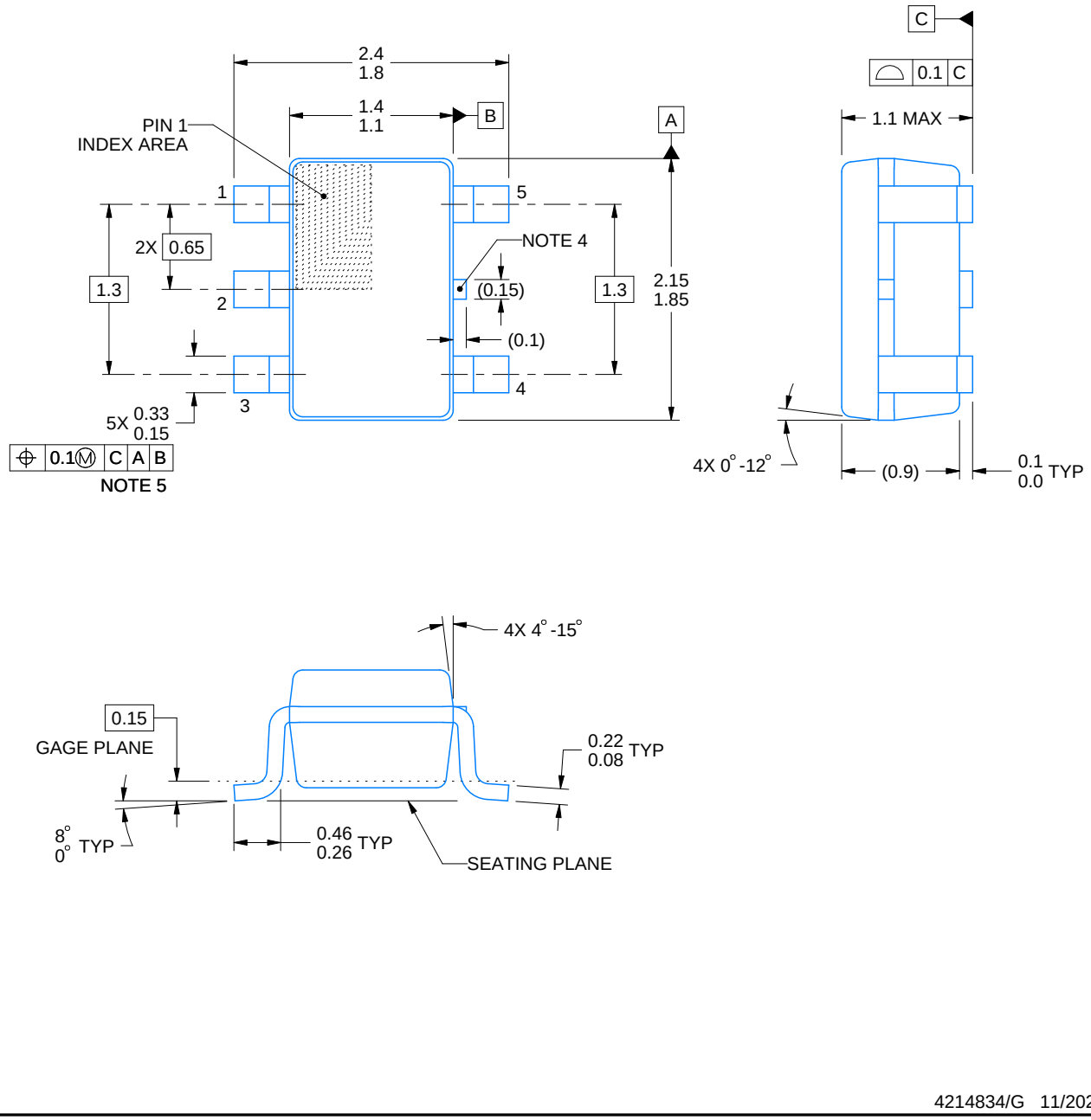
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2333AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2333AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2333AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA333AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA333AID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA333AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA333AIDG4	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

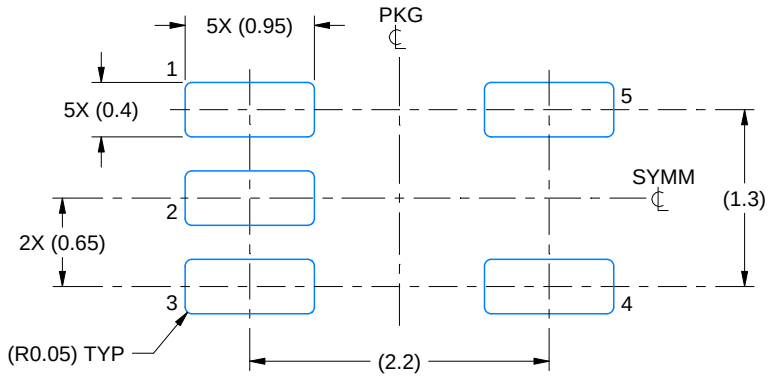
SMALL OUTLINE TRANSISTOR



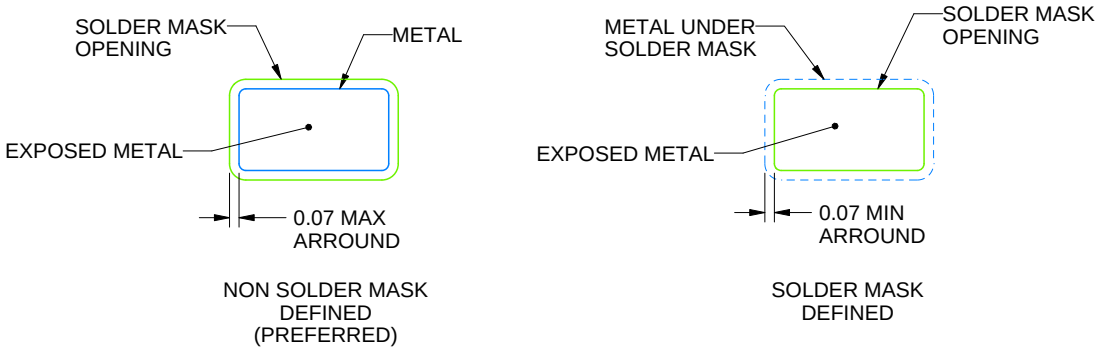
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

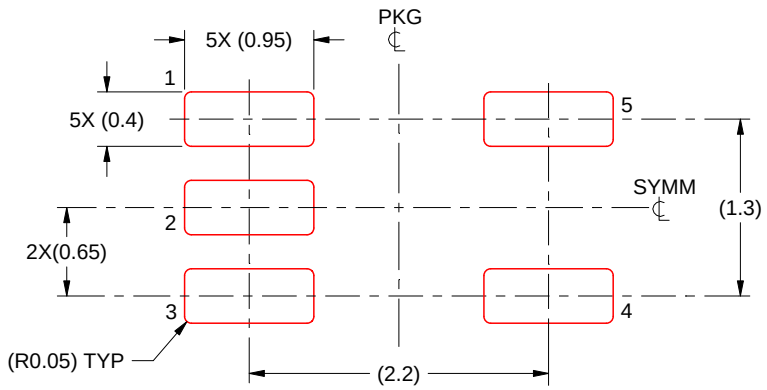


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

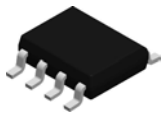


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

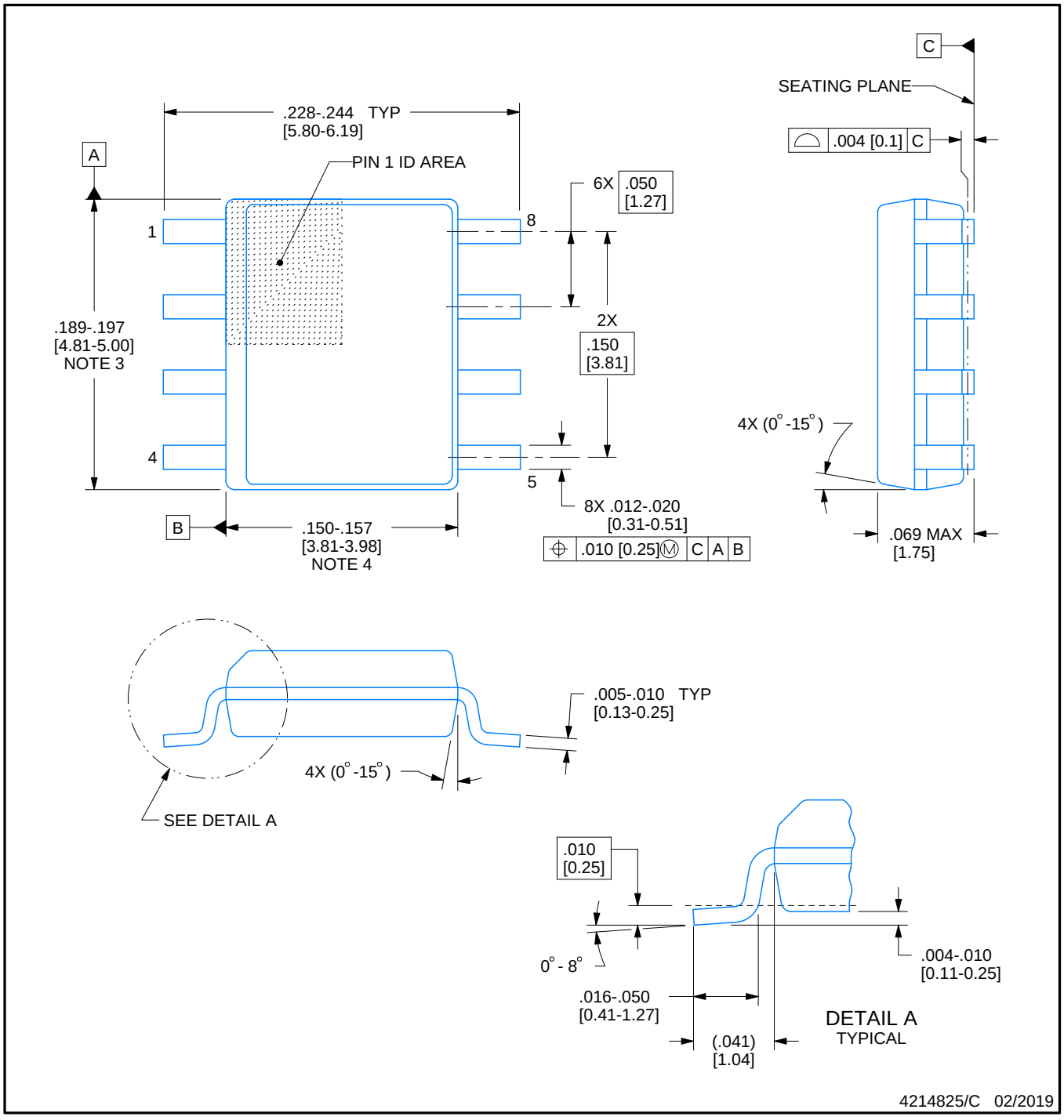


PACKAGE OUTLINE

D0008A

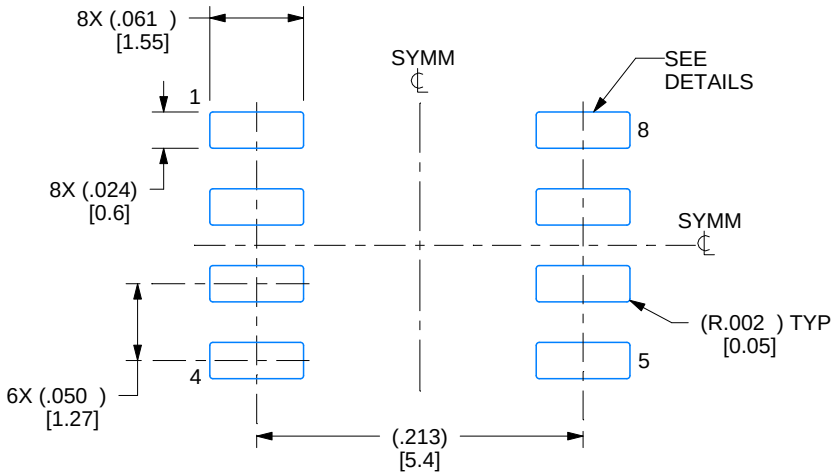
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

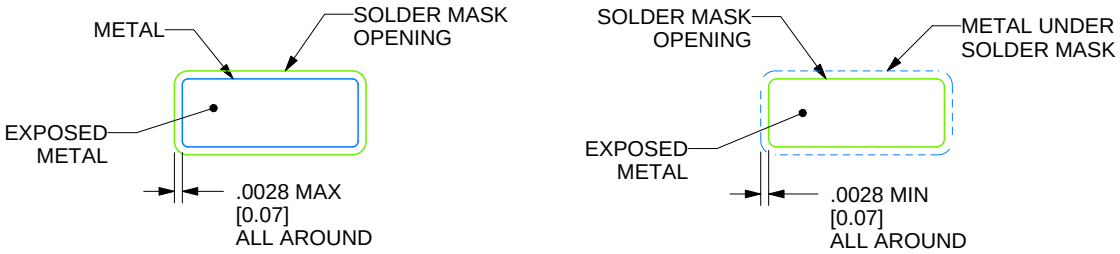


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

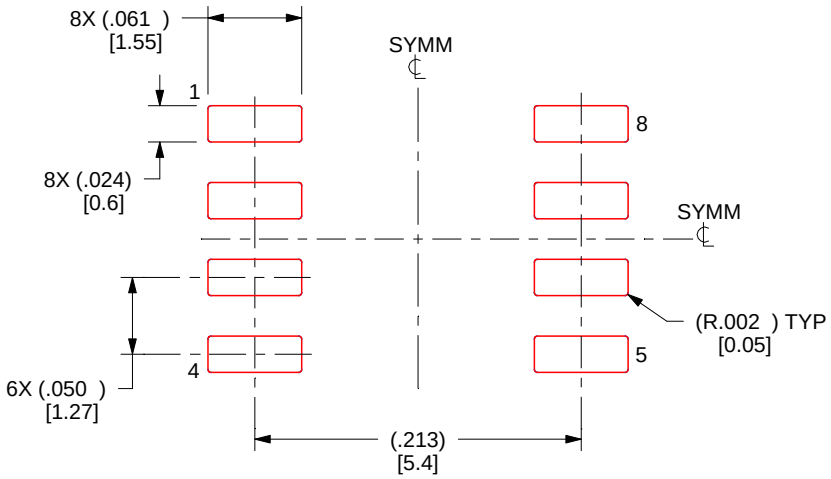
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

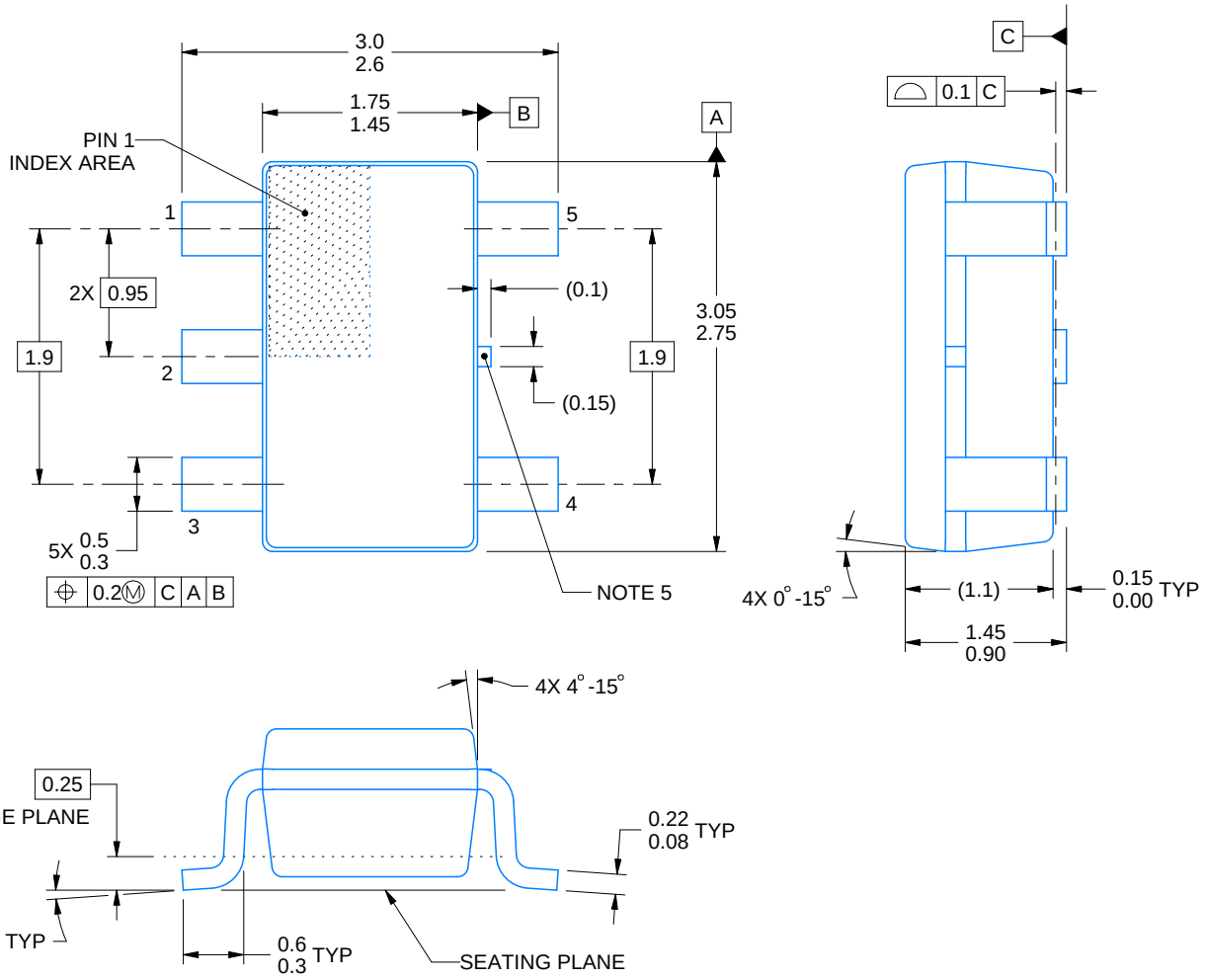
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

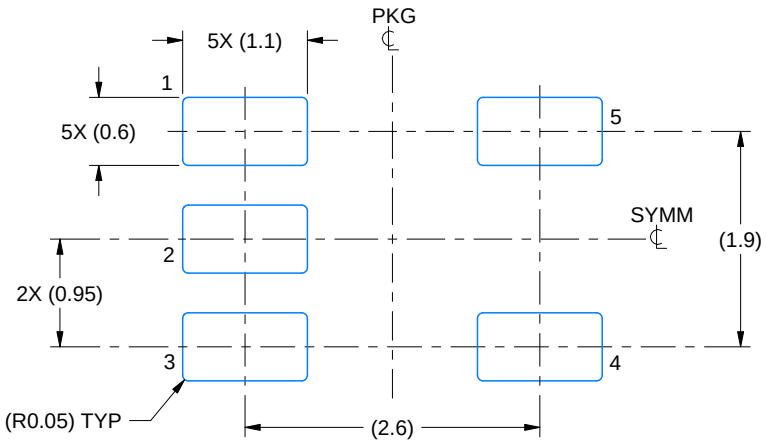
SMALL OUTLINE TRANSISTOR



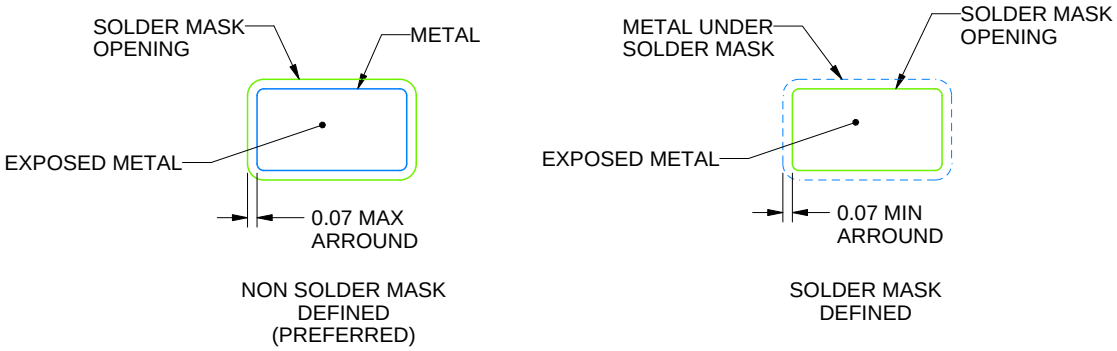
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

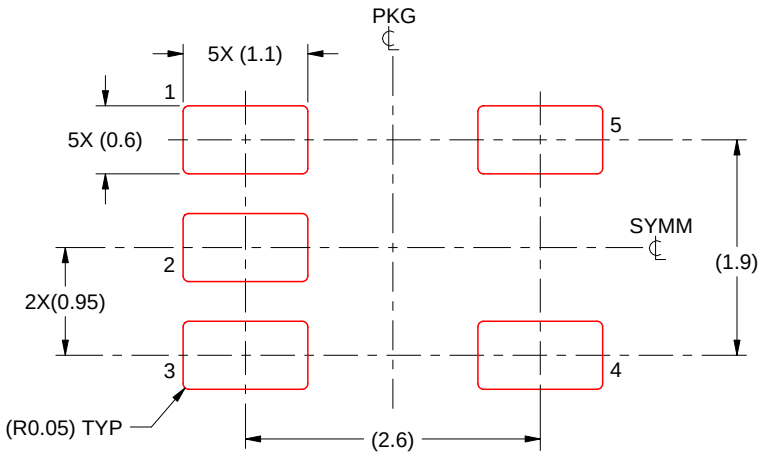


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

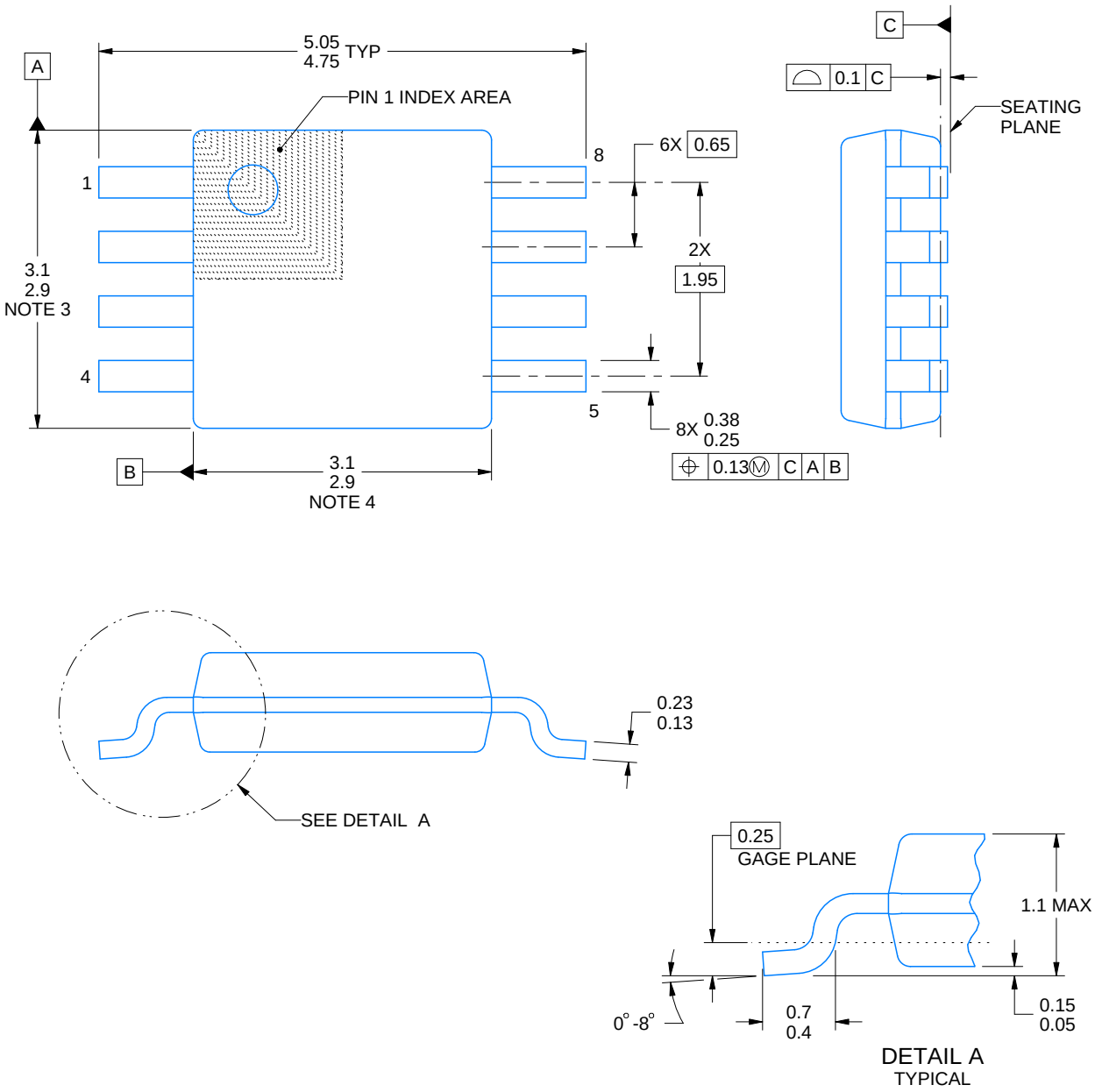
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

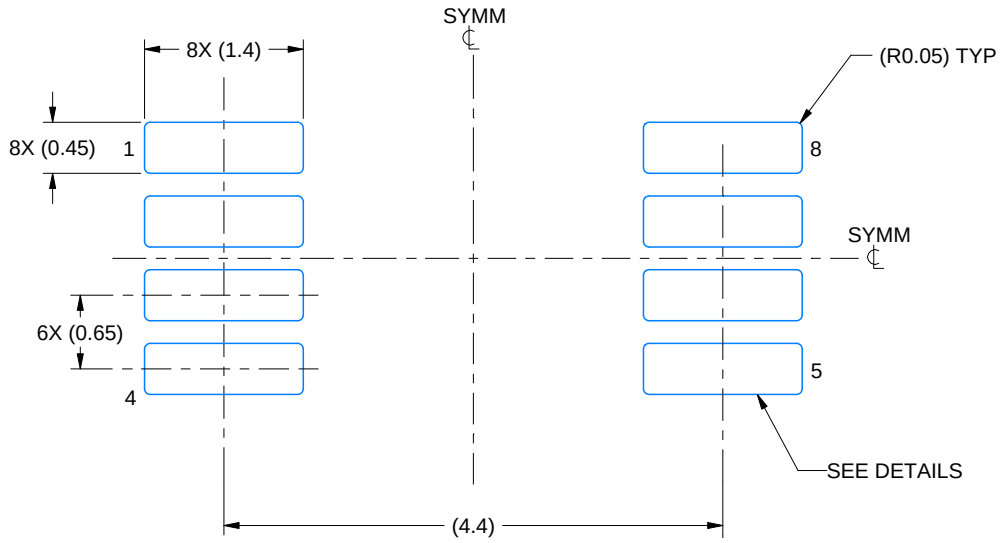
SMALL OUTLINE PACKAGE



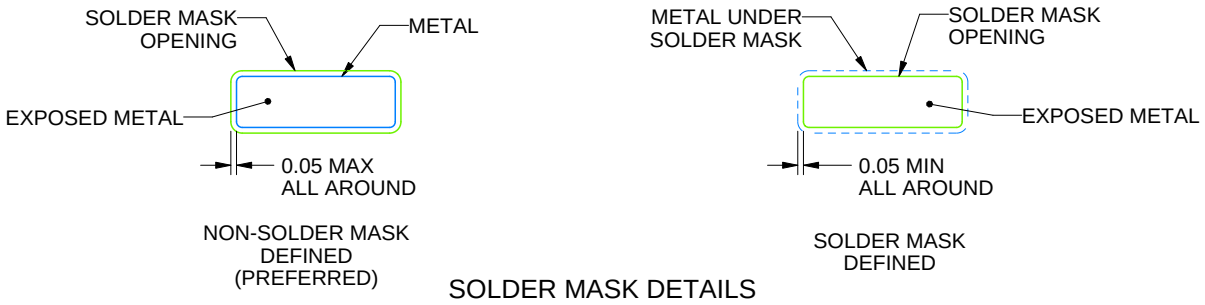
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

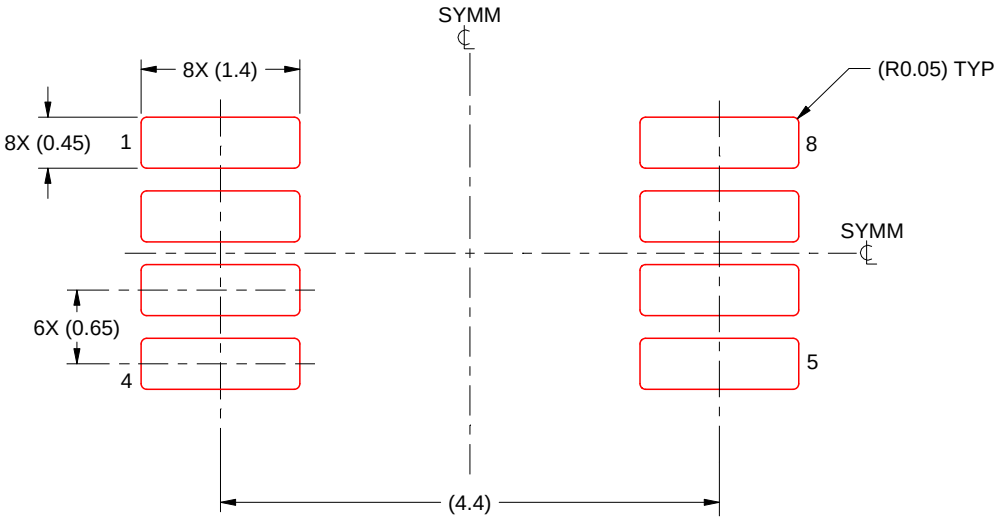


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

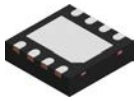
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

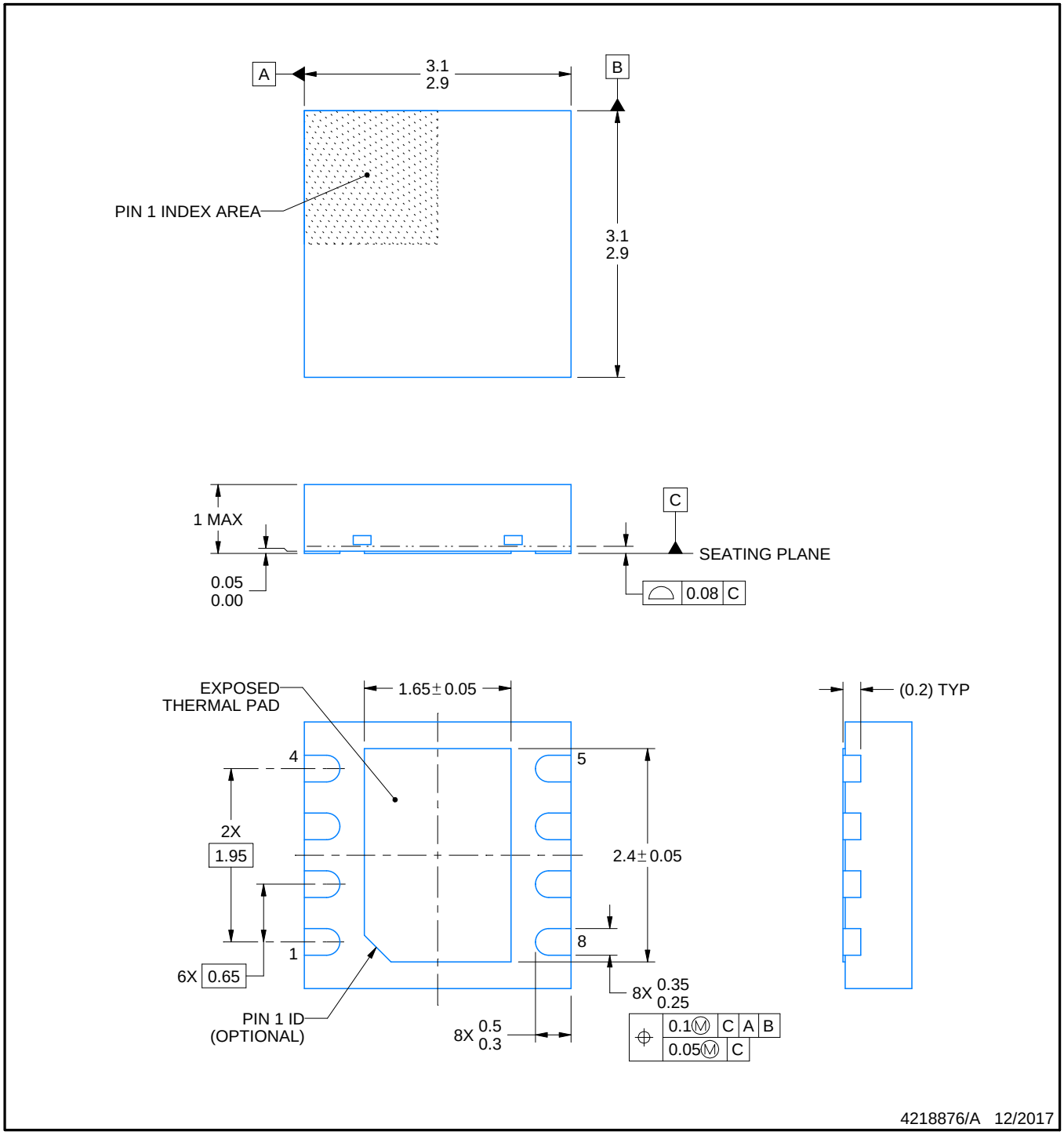
DRB0008B



PACKAGE OUTLINE

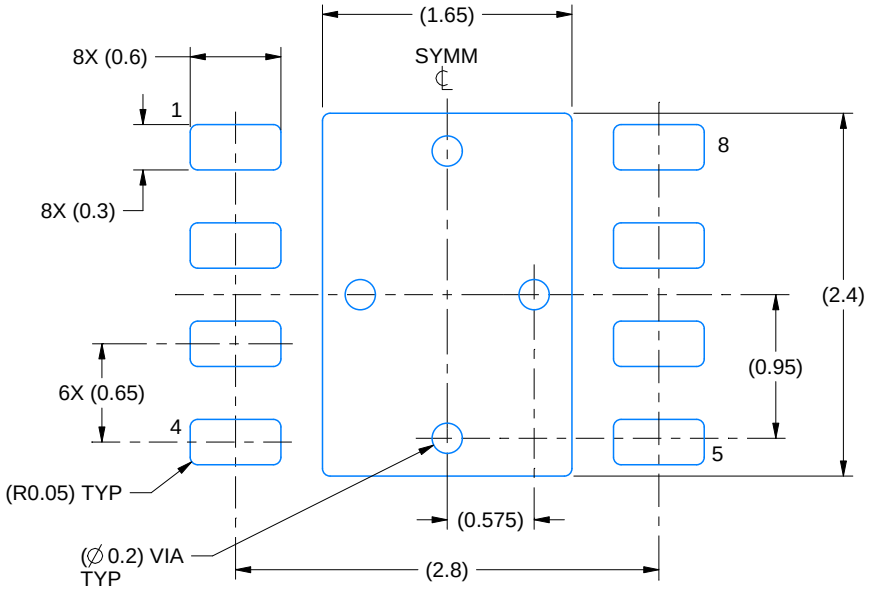
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

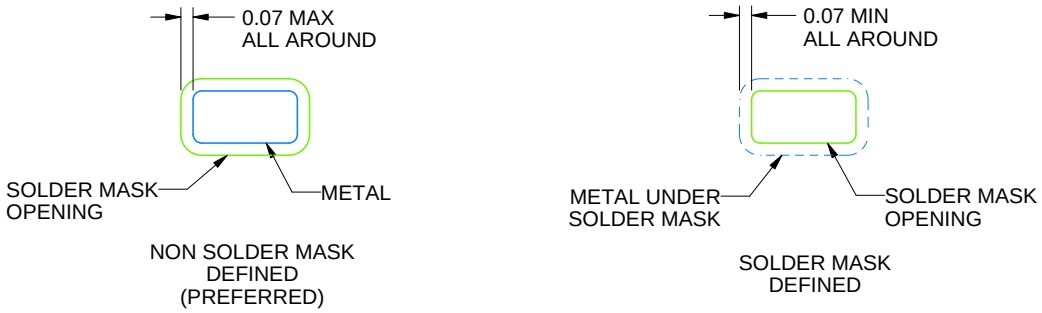


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

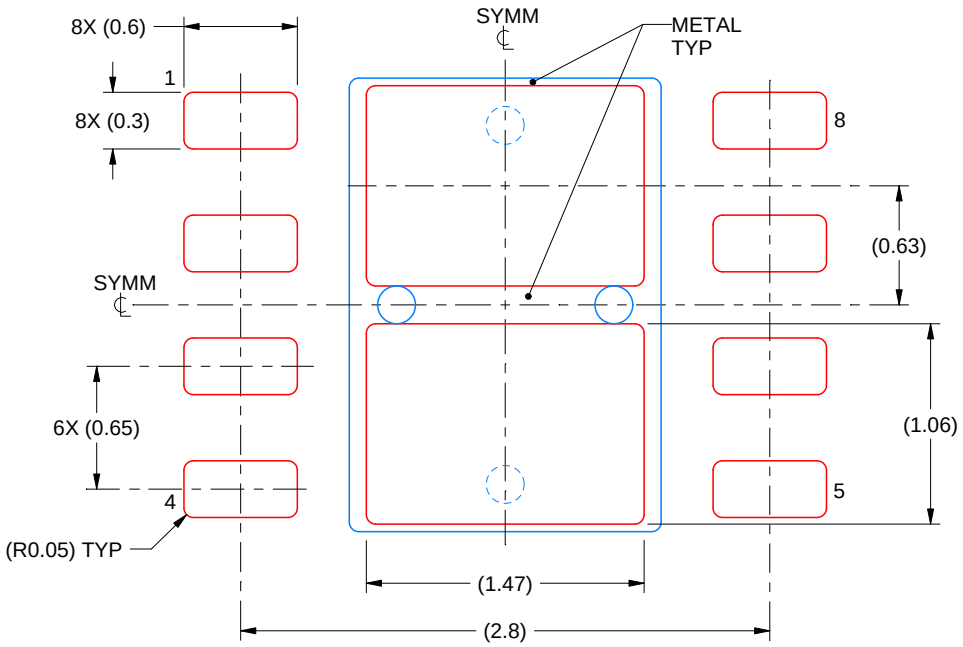


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月