ISO7710 高速、堅牢な EMC 強化型 1 チャネル・デジタル・アイソレータ

1 特長

- 100Mbps のデータ・レート
- 堅牢な絶縁バリア:
  - 1500 V_{RMS} の動作電圧で 100 年を超える予測寿命
  - 最高 5000V_{RMS} の絶縁定格
  - 最高 12.8kV のサージ耐量
  - CMTI:±100kV/µs (標準値)
- 広い電源電圧範囲:2.25V～5.5V
- 2.25V から 5.5V への電圧レベル変換
- デフォルト出力 HIGH (ISO7710) および LOW (ISO7710F) のオプション
- 広い温度範囲:–55℃～125℃
- 低消費電力:1.7mA (標準値、1Mbps 時)
- 小さい伝搬遅延時間:11ns (標準値、電源電圧 5V 時)
- 堅牢な電磁気互換性 (EMC)
  - システム・レベルの ESD、EFT、サージ耐性
  - 絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護
  - 低い放射
- パッケージはワイド SOIC (DW-16) およびナロー SOIC (D-8) を選択可能
- 車載用バージョンを利用可能:ISO7710-Q1
- 安全関連認証
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁
  - UL 1577 部品認定プログラム
  - IEC 62368-1、IEC 61010-1、IEC 60601-1、GB 4943.1 認定

2 アプリケーション

- 産業用オートメーション
- モーター制御
- 電源
- 太陽光インバータ
- 医療用機器

3 概要

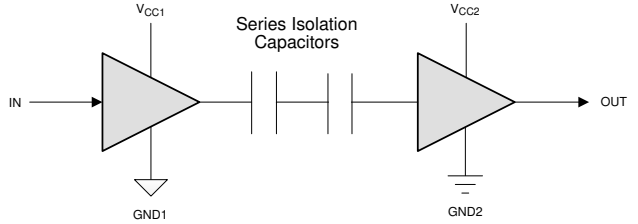
ISO7710 デバイスは、高性能の 1 チャネル・デジタル・アイソレータであり、UL 1577 準拠で 5000V_{RMS} (DW パッケージ) および 3000V_{RMS} (D パッケージ) の絶縁定格を備えています。デバイスは VDE、TUV、CSA、CQC 認定も取得しています。

ISO7710 デバイスは電磁気耐性が高く、エミッションが少なく、低消費電力を実現し、CMOS または LVCMOS デジタル I/O が絶縁されています。この絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素 (SiO_2) 絶縁バリアによって分離されています。入力電力または入力信号が失われた場合のデフォルト出力は、接尾辞 F のないデバイスでは HIGH、接尾辞 F のあるデバイスでは LOW です。詳細は「デバイスの機能モード」のセクションを参照してください。

このデバイスを絶縁電源と組み合わせて使用することで、RS-485、RS-232、CAN などのデータ・バスやその他の回路のノイズ電流がローカル・グランドに入り込む、あるいはノイズに敏感な回路に干渉するまたは損傷を与える、といったことを防止できます。革新的なチップ設計およびレイアウト技法により、ISO7710 デバイスは電磁気互換性が大幅に強化されているため、システム・レベルの ESD、EFT、サージ、および放射のコンプライアンスを容易に達成できます。ISO7710 デバイスには、ワイド・ボディ (DW) の 16 ピン SOIC パッケージのものと、ナロー・ボディ (D) の 8 ピン SOIC パッケージのものが用意されています。

製品情報

部品番号	パッケージ	本体サイズ (公称)
ISO7710	SOIC (D)	4.90mm×3.91mm
	SOIC (DW)	10.30mm × 7.50mm



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簡略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (April 2020) to Revision D (March 2023) **Page**

- 標準名を次のように変更：「DIN V VDE V 0884-11:2017-01」から「DIN EN IEC 60747-17 (VDE 0884-17)」(ドキュメント全体を通して) ... 1
- ドキュメント全体を通して、IEC/EN/CSA 60950-1 規格への参照を削除 ... 1
- ドキュメント全体を通して、すべての標準名から標準リビジョンおよび年への参照を削除 ... 1
- Added Maximum impulse voltage (V_{IMP}) specification per DIN EN IEC 60747-17 (VDE 0884-17) ... 9
- Changed test conditions and values of Maximum surge isolation voltage (V_{IOSM}) specification per DIN EN IEC 60747-17 (VDE 0884-17) ... 9
- Clarified method b test conditions of Apparent charge (q_{PD}) ... 9
- Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDB from: 135 years to: 169 years in per DIN EN IEC 60747-17 (VDE 0884-17) ... 25
- Changed 図 9-5 per DIN EN IEC 60747-17 (VDE 0884-17) ... 25

Changes from Revision B (March 2017) to Revision C (April 2020) **Page**

- ドキュメント全体を通して編集上および体裁上の変更 ... 1
- 次のように変更：「絶縁バリアの寿命：40 年以上」から「1500 V_{RMS} の動作電圧で 100 年を超える予測寿命」に変更 (セクション 1) ... 1
- セクション 1 に「最大 5000V_{RMS} の絶縁定格」を追加 ... 1
- セクション 1 に「最大 12.8kV のサージ能力」を追加 ... 1
- セクション 1 に「絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護」を追加 ... 1
- 「車載用バージョンを利用可能：ISO7710x-Q1」を追加 (セクション 1) ... 1
- 次のように変更：「DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 準拠の VDE 強化絶縁」から「DIN VDE V 0884-11:2017-01 準拠の VDE 強化絶縁」(セクション 1) ... 1

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- セクション 1 で CSA、CQC、TUV の箇条書き項目を、標準名による 1 つの箇条書き項目に統合 1
- セクション 1 で、「DW-16 パッケージの VDE、UL、CSA、TUV 認定は完了、他のすべての認定は計画中」項目を削除 1
- 「図 3-1」を、単一の絶縁コンデンサの代わりに、直列の 2 つの絶縁コンデンサを示すよう更新 1
- Added "Contact discarge per IEC 61000-4-2" specification of 8000V 6
- Changed "Signaling rate" to "Data rate" and added table note 7
- Updated DW-16 package V_{IORM} and V_{IOWM} values 9
- Added TDDB figure reference to V_{IOWM} 9
- Updated V_{IOSM}, V_{IOTM}, q_{pd} test conditions 9
- Corrected ground symbols for "Input (Devices with F suffix)" in セクション 8.4.1 22
- Fixed 図 9-2 INPUT wire connection 24
- Added セクション 9.2.3.1 sub-section under セクション 9.2.3 section 25
- Added '*How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*' to セクション 12.1 section 29

Changes from Revision A (December 2016) to Revision B (March 2017) **Page**

- Added D-8 values for TUV 11
- Changed the *Electrostatic Discharge Caution* statement 29

Changes from Revision * (November 2016) to Revision A (December 2016) **Page**

- 「特長」を次のように変更:「IEC 60950-1、IEC 60601-1、IEC 61010-1 最終機器標準」から「IEC 60950-1 および IEC 60601-1 最終機器標準」 1
- Added Climatic category 9
- Updated CSA column and changed DW package to (DW-16) 11
- Changed t_{ie} TYP value from 1.5 to 1 in Switching Characteristics tables throughout the document 16

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5 Pin Configuration and Functions

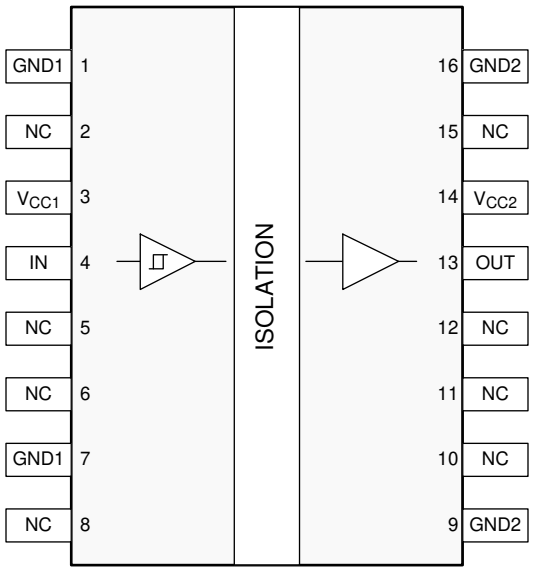

図 5-1. DW Package 16-Pin SOIC Top View

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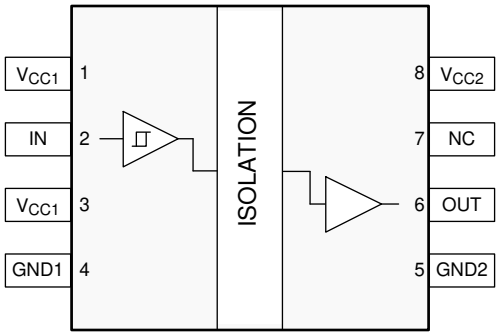

図 5-2. D Package 8-Pin SOIC Top View

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DW	D		
V_{CC1}	3	1, 3	—	Power supply, V_{CC1}
V_{CC2}	14	8	—	Power supply, V_{CC2}
GND1	1, 7	4	—	Ground connection for V_{CC1}
GND2	9, 16	5	—	Ground connection for V_{CC2}
IN	4	2	I	Input channel
OUT	13	6	O	Output channel
NC	2, 5, 6, 8, 10 ,11, 12, 15	7	—	Not connect pin; it has no internal connection

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6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply Voltage (2)	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	V_{CCX} + 0.5 (3)	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High level output current	V_{CC2} = 5 V	-4			mA
		V_{CC2} = 3.3 V	-2			
		V_{CC2} = 2.5 V	-1			
I_{OL}	Low level output current	V_{CC2} = 5 V			4	mA
		V_{CC2} = 3.3 V			2	
		V_{CC2} = 2.5 V			1	
V_{IH}	High level Input voltage		0.7 x V_{CC1}		V_{CC1}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CC1}	V
DR(1)	Data Rate		0		100	Mbps
T_A	Ambient temperature		-55	25	125	°C

(1) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

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6.4 Thermal Information

THERMAL METRIC [(1)]		ISO7710		UNIT
		DW (SOIC) (16-Pin)	D(SOIC) (8-Pin)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.4	146.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	63.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	80.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.0	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.8	79.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7710						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			50	mW
P_{D1}	Maximum power dissipation (side-1)				12.5	mW
P_{D2}	Maximum power dissipation (side-2)				37.5	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	D-8	
IEC 60664-1					
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	n/a	
DIN EN IEC 60747-17 (VDE 0884-17)(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test, see 図 9-5	1500	450	V_{RMS}
		DC voltage	2121	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	8000	4242	V_{PK}
V_{IMP}	Maximum impulse voltage((3))	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage((4))	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	10000	V_{PK}
q_{pd}	Apparent charge((5))	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$ (ISO7710), t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	~0.4	~0.4	pF
R_{IO}	Insulation resistance((6))	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	> 10^9	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

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(3) Testing is carried out in air to determine the surge immunity of the package
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

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6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW-16, Reinforced) and 637 V_{PK} (D-8); Maximum surge isolation voltage, 12800 V_{PK} (DW-16, Reinforced) and 10000 V_{PK} (D-8)	Reinforced insulation per CSA 62368-1 and IEC 62368-1, 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} (DW-16) max working voltage	DW-16: Single protection, 5000 V_{RMS}; D-8: Single protection, 3000 V_{RMS}	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage; D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage	5000 V_{RMS} (DW-16) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 61010-1 up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (D-8) 5000 V_{RMS} (DW-16) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 62368-1 up to working voltage of 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate numbers: CQC21001304083 (DW-16) CQC15001121656 (D-8)	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting((1)) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat
the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =94.4°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 6-1			241	mA
		$R_{\theta JA}$ = 94.4°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 6-1			368	
		$R_{\theta JA}$ = 94.4°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 6-1			482	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 94.4°C/W, T_J = 150°C, T_A = 25°C, see 図 6-2			1324	mW
T_S	Maximum safety temperature				150	°C
D-8 PACKAGE						
I_S	Safety input, output, or supply current (1)	$R_{\theta JA}$ =146.1°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 6-3			156	mA
		$R_{\theta JA}$ = 146.1°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 6-3			238	
		$R_{\theta JA}$ = 146.1°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 6-3			311	
P_S	Safety input, output, or total power (1)	$R_{\theta JA}$ = 146.1°C/W, T_J = 150°C, T_A = 25°C, see 図 6-4			856	mW
T_S	Maximum safety temperature (1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

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$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; see 図 7-1	V_{CC2} - 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 図 7-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CC1}	0.7 x V_{CC1}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CC1}	0.4 x V_{CC1}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CC1}	0.2 x V_{CC1}		V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1200 V; see 図 7-3	85	100		kV/µs
C_I	Input Capacitance (1)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V;		2		pF

(1) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7710							
Supply current - DC signal	V_I = V_{CC1}(ISO7710), V_I = 0 V (ISO7710 with F suffix)		I_{CC1}		0.5	0.8	mA
			I_{CC2}		0.6	1	
	V_I = 0V (ISO7710), V_I = V_{CC1} (ISO7710 with F suffix)		I_{CC1}		1.6	2.5	
			I_{CC2}		0.6	1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.6	1.1	
		10 Mbps	I_{CC1}		1.1	1.6	
			I_{CC2}		1.1	1.6	
		100 Mbps	I_{CC1}		1.4	2	
			I_{CC2}		5.9	7	

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6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA ; see 図 7-1	V_{CC2} - 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA ; see 図 7-1		0.1	0.3	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CC1}	0.7 x V_{CC1}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CC1}	0.4 x V_{CC1}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CC1}	0.2 x V_{CC1}		V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1200 V; see 図 7-3	85	100		kV/µs

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7710							
Supply current - DC signal	V_I = V_{CC1} (ISO7710), V_I = 0 V (ISO7710 with F suffix)		I_{CC1}		0.5	0.8	mA
			I_{CC2}		0.6	1	
	V_I = 0V (ISO7710), V_I = V_{CC1} (ISO7710 with F suffix)		I_{CC1}		1.6	2.5	
			I_{CC2}		0.6	1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.6	1	
		10 Mbps	I_{CC1}		1	1.6	
			I_{CC2}		1.1	1.4	
		100 Mbps	I_{CC1}		1.3	1.8	
			I_{CC2}		4.3	5.3	

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6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA ; see 図 7-1	V_{CC2} - 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA ; see 図 7-1		0.05	0.2	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CC1}	0.7 x V_{CC1}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CC1}	0.4 x V_{CC1}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CC1}	0.2 x V_{CC1}		V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1200 V; see 図 7-3	85	100		kV/µs

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7710							
Supply current - DC signal	V_I = V_{CC1} (ISO7710), V_I = 0 V (ISO7710 with F suffix)		I_{CC1}		0.5	0.8	mA
			I_{CC2}		0.6	1	
	V_I = 0V (ISO7710), V_I = V_{CC1} (ISO7710 with F suffix)		I_{CC1}		1.6	2.5	
			I_{CC2}		0.6	1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.6	1	
		10 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.9	1.4	
		100 Mbps	I_{CC1}		1.2	1.6	
			I_{CC2}		3.4	4.4	

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6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.9	ns
$t_{sk(pp)}$	Part-to-part skew time (2)				4.5	ns
t_r	Output signal rise time	See 図 7-1		1.8	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7V. See 図 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5	ns
$t_{sk(pp)}$	Part-to-part skew time (2)				4.5	ns
t_r	Output signal rise time	See 図 7-1		0.7	3	ns
t_f	Output signal fall time			0.7	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7V. See 図 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1	7.5	12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5.1	ns
$t_{sk(pp)}$	Part-to-part skew time((2))				4.6	ns
t_r	Output signal rise time	See 図 7-1		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7V. See 図 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

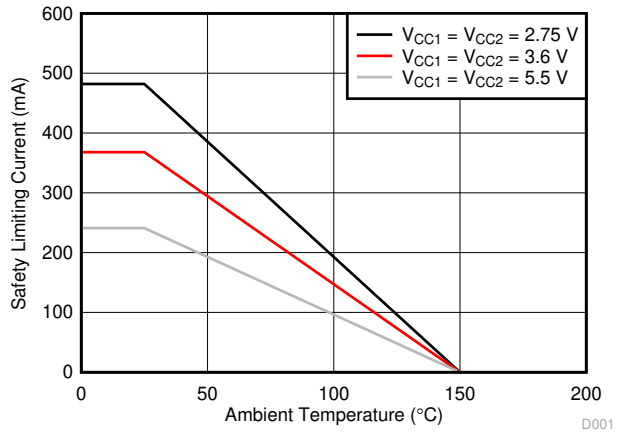

図 6-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

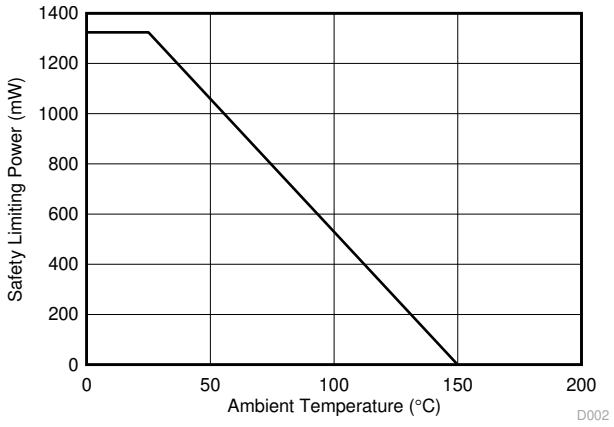

図 6-2. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

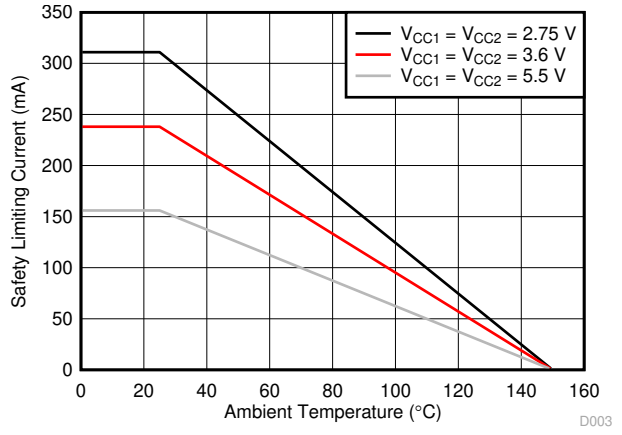

図 6-3. Thermal Derating Curve for Limiting Current per VDE for D-8 Package

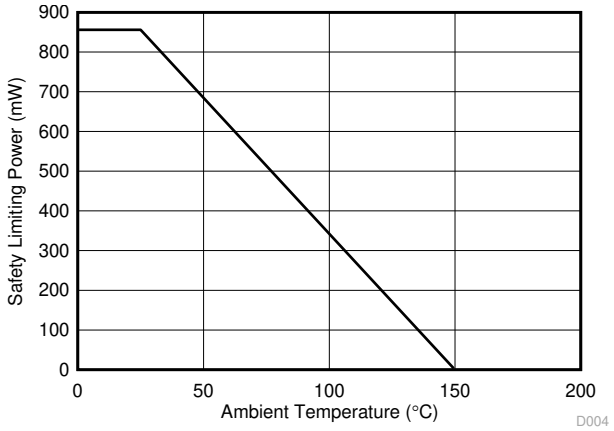

図 6-4. Thermal Derating Curve for Limiting Power per VDE for D-8 Package

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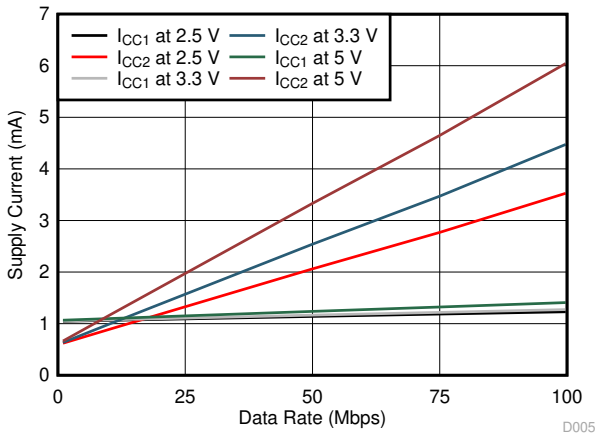
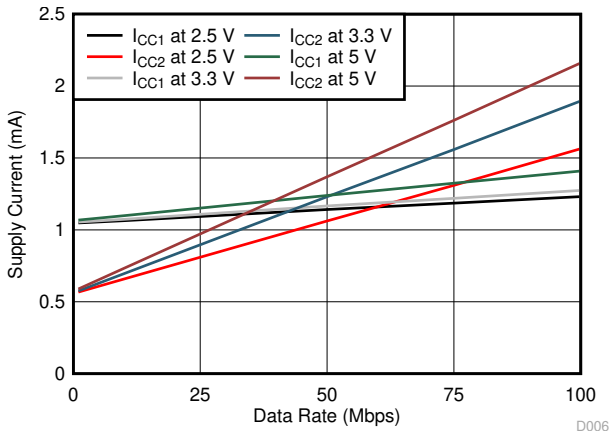
6.19 Typical Characteristics



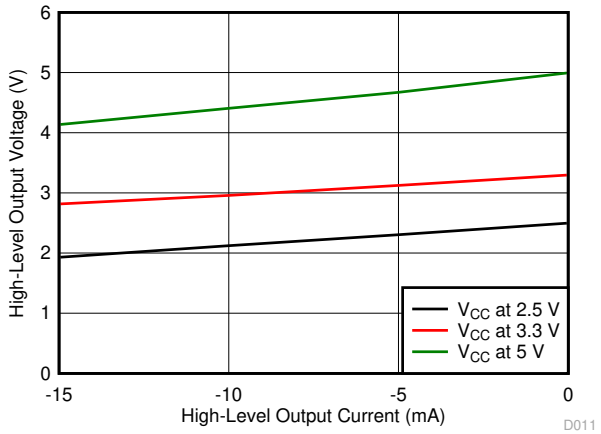
T_A = 25°C C_L = 15 pF

図 6-5. ISO7710 Supply Current vs Data Rate (With 15 pF Load)



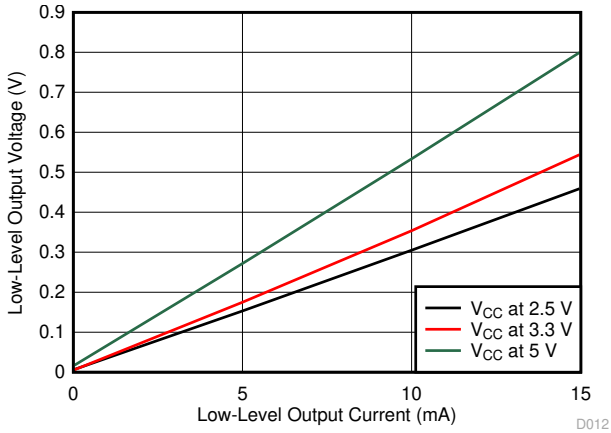
T_A = 25°C C_L = No Load

図 6-6. ISO7710 Supply Current vs Data Rate (With No Load)



T_A = 25°C

図 6-7. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

図 6-8. Low-Level Output Voltage vs Low-Level Output Current

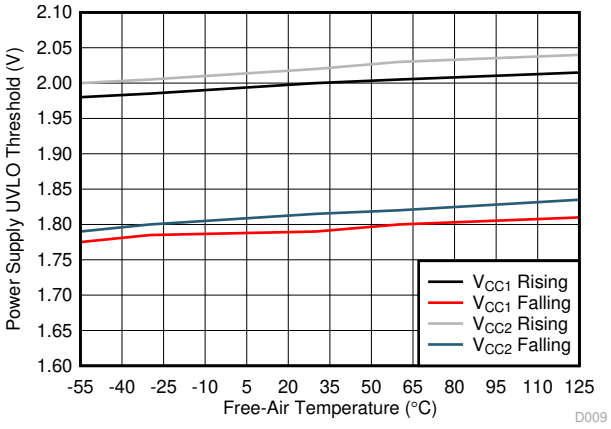


図 6-9. Power Supply Undervoltage Threshold vs Free-Air Temperature

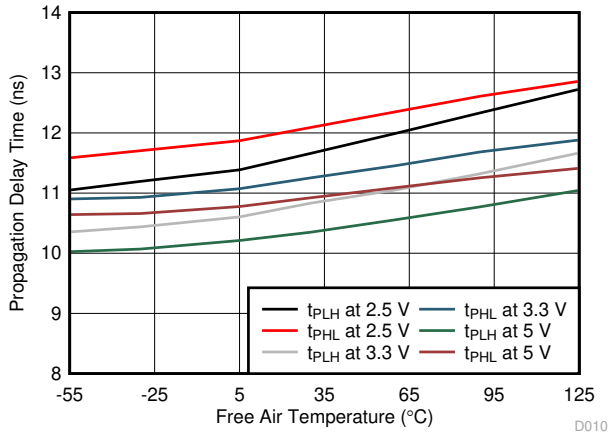


図 6-10. Propagation Delay Time vs Free-Air Temperature

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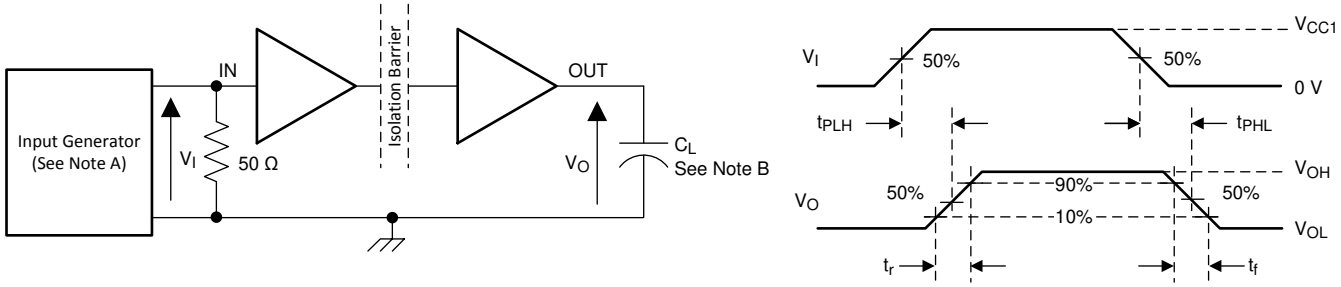
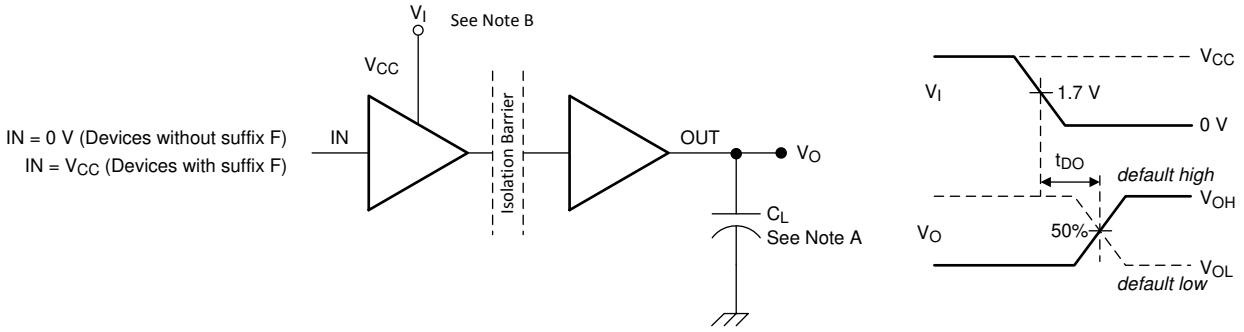
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

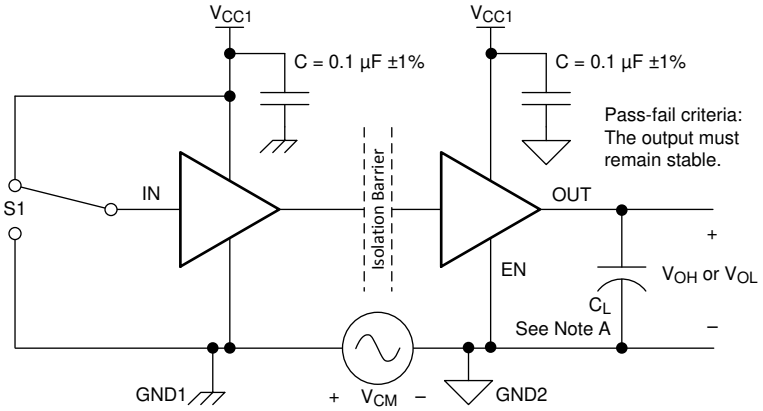
図 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

図 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7710 device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 8-1, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

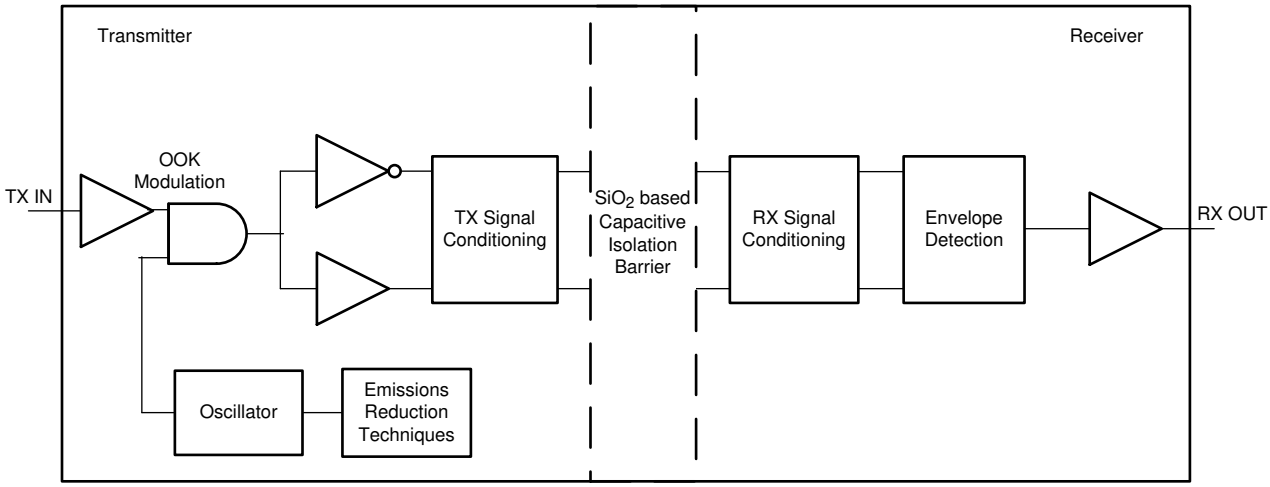


図 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

図 8-2 shows a conceptual detail of how the OOK scheme works.

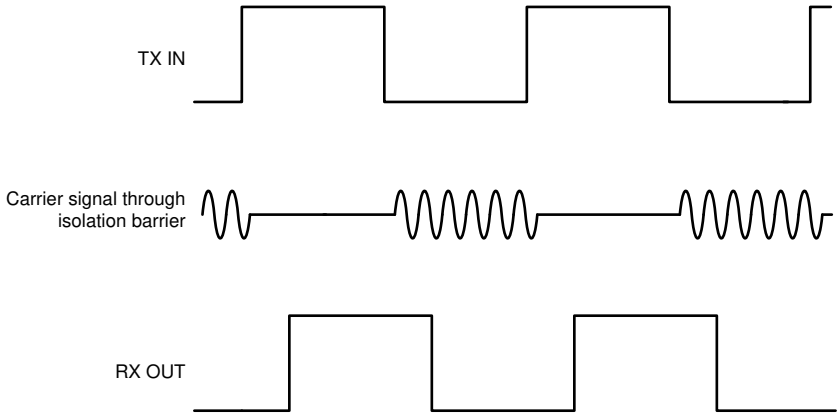


図 8-2. On-Off Keying (OOK) Based Modulation Scheme

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8.3 Feature Description

The ISO7710 device is available in two default output state options to enable a variety of application uses. 表 8-1 lists the device features.

表 8-1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION(1)
ISO7710	100 Mbps	1 Forward, 0 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7710F	100 Mbps	1 Forward, 0 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}

(1) See the Safety-Related Certifications section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7710 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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8.4 Device Functional Modes

表 8-2 lists the functional modes of ISO7710 device.

表 8-2. Function Table

V_{CC1}	V_{CC2}	INPUT (IN)(3)	OUTPUT (OUT)	COMMENTS
PU(1)	PU	H	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	
		Open	Default	Default mode: When IN is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO7710 and *Low* for ISO7710F.
PD	PU	X	Default	Default mode: When V_{CC1} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO7710 and *Low* for ISO7710F. When V_{CC1} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CC1} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CC2} is unpowered, a channel output is undetermined (2). When V_{CC2} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
(2) The outputs are in undetermined state when 1.7 V < V_{CC1}, V_{CC2} < 2.25 V.
(3) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

8.4.1 Device I/O Schematics

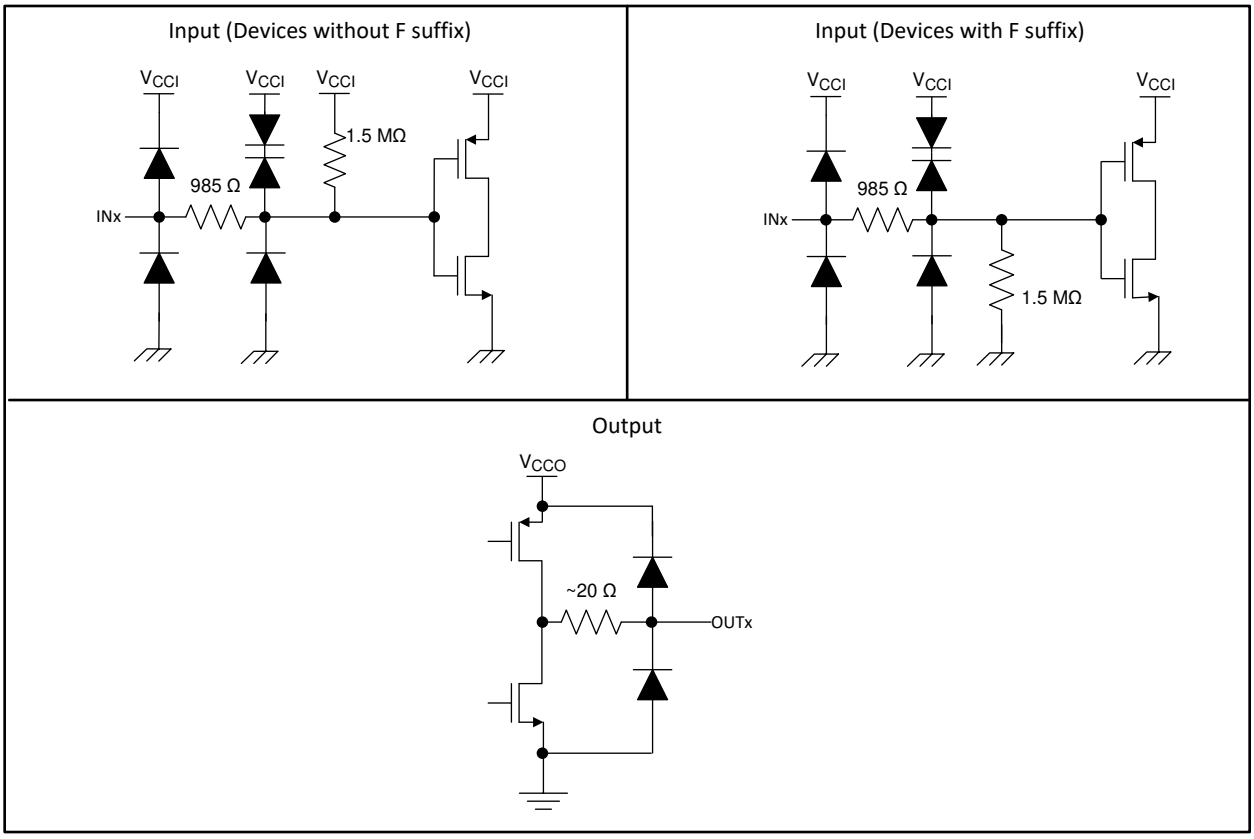

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図 8-3. Device I/O Schematics

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7710 device is a high-performance, single-channel digital isolator. The device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7710 device can be used with Texas Instruments' mixed signal microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown below.

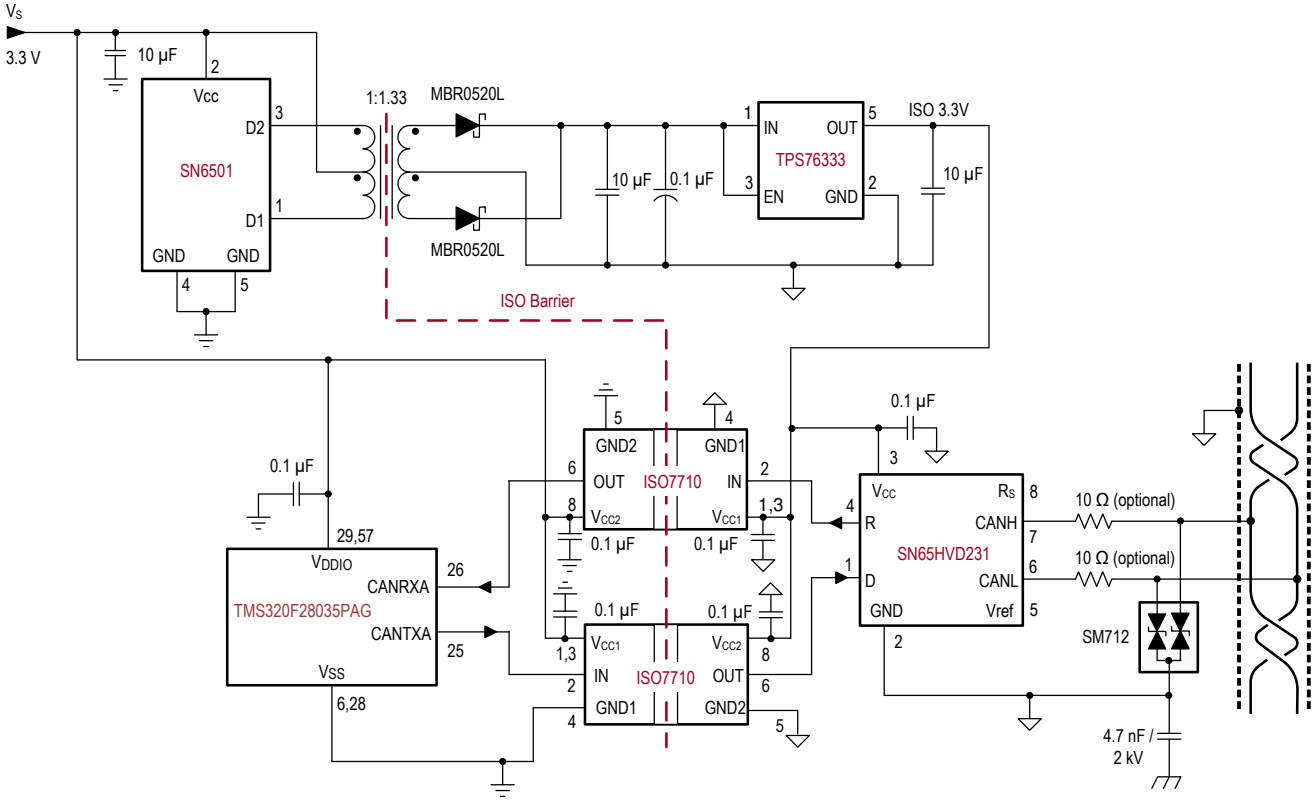

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図 9-1. Isolated CAN Interface

9.2.1 Design Requirements

To design with this device, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require components to improve performance, provide bias, or limit current, the ISO7710 device only requires two external bypass capacitors to operate.

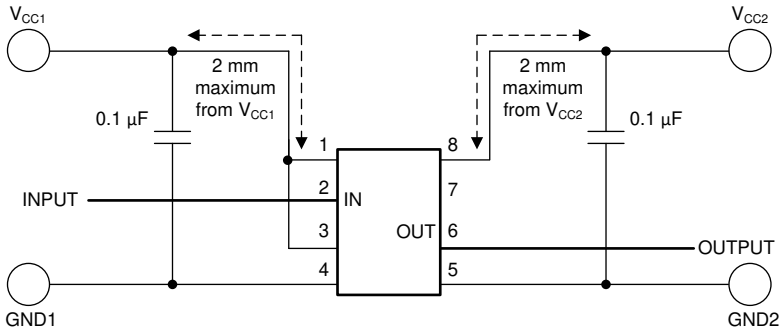

図 9-2. Typical ISO7710 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagram of the ISO7710 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

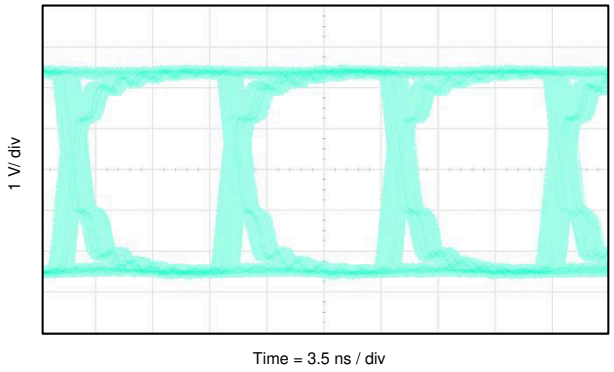

図 9-3. ISO7710 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

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9.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 図 9-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

図 9-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 169 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500 V_{RMS} and D-8 package up to 450 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 169 years.

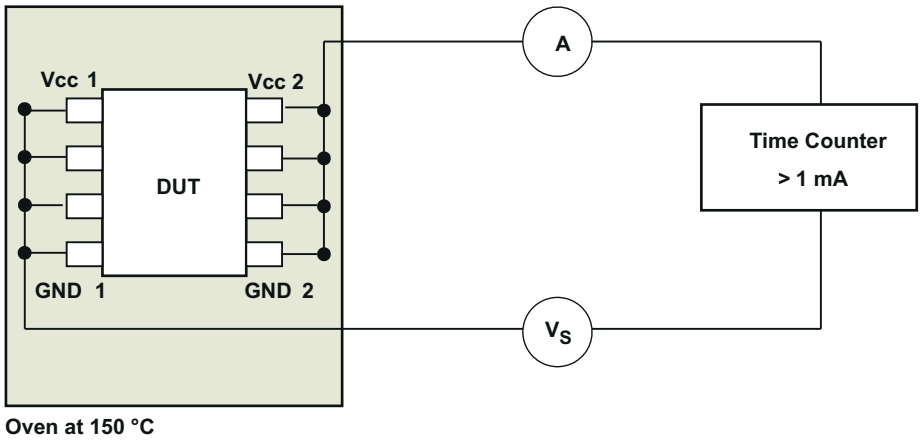

図 9-4. Test Setup for Insulation Lifetime Measurement

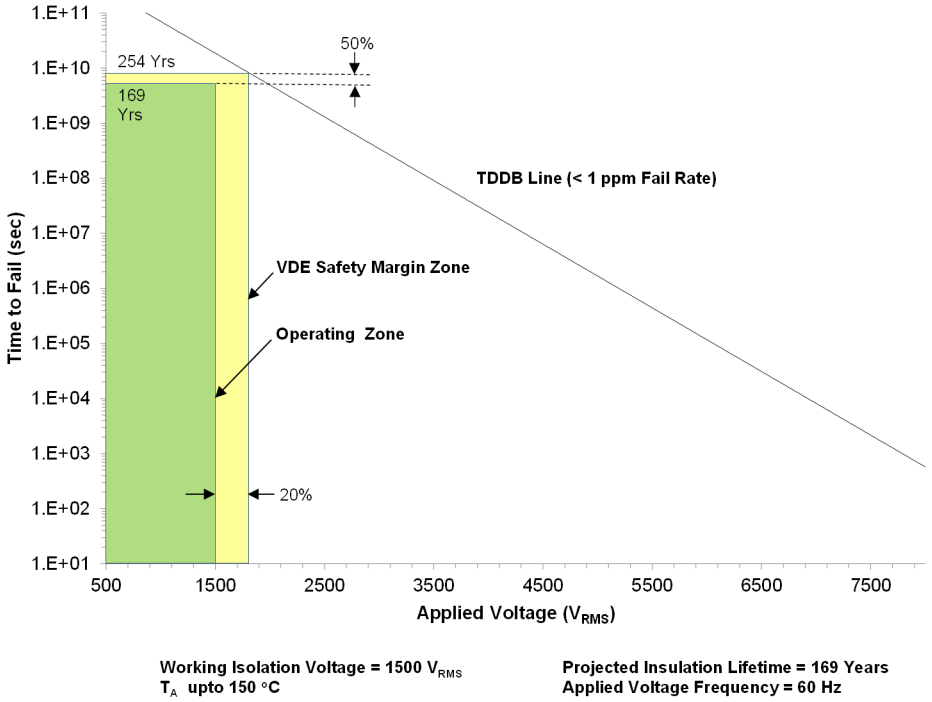

図 9-5. Insulation Lifetime Projection Data

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10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*.

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11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

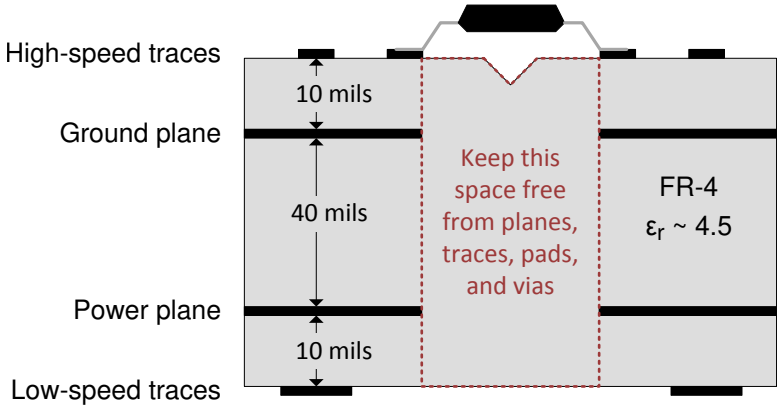

図 11-1. Layout Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Digital Isolator Design Guide*
- *Isolation Glossary*
- *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*
- *SN6501 Transformer Driver for Isolated Power Supplies*
- *SN65HVD23x 3.3-V CAN Bus Transceivers*
- TMS320F28035 *Piccolo™ Microcontrollers*
- TPS76333 *Low-Power 150-mA Low-Dropout Linear Regulators*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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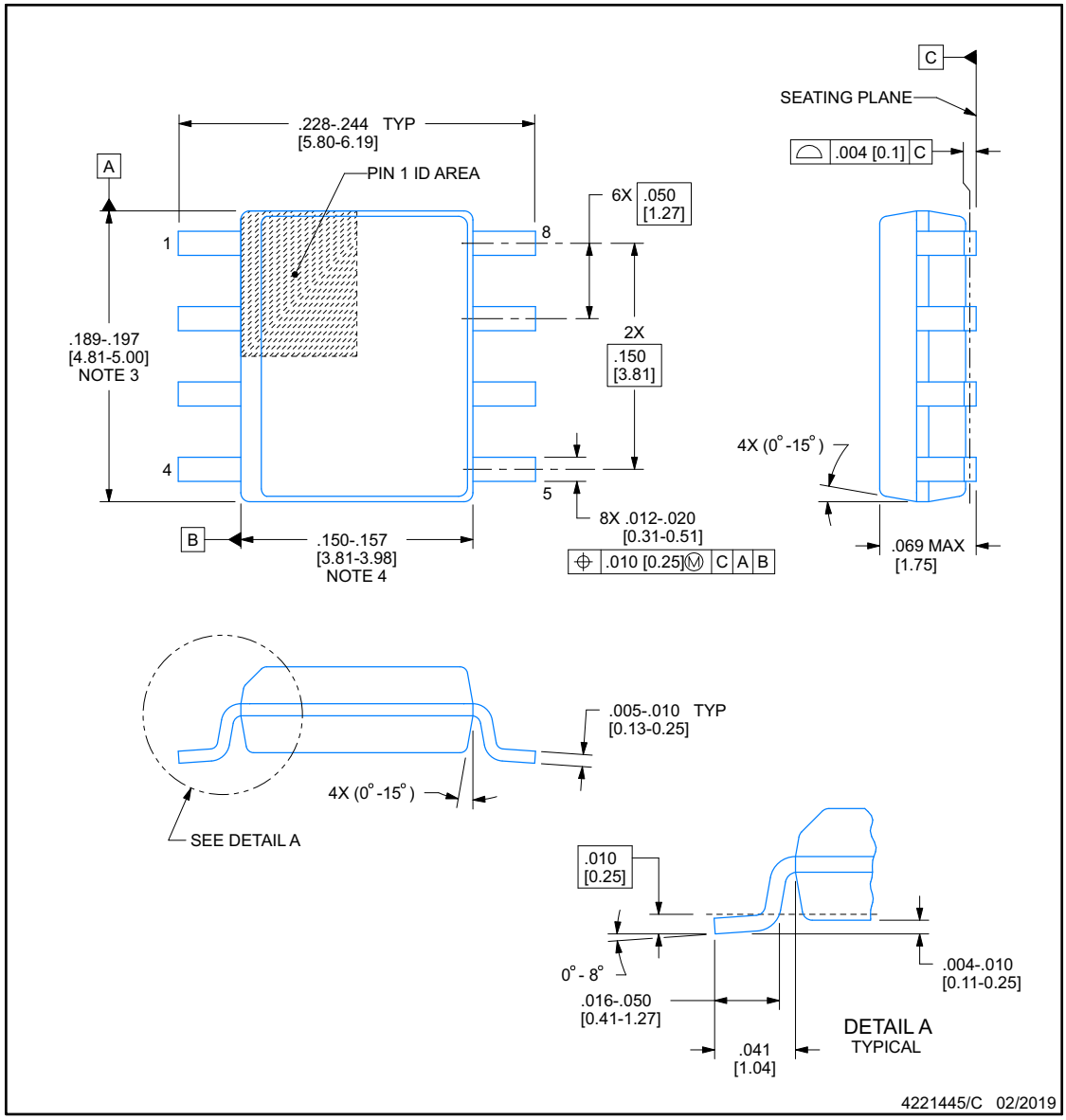
PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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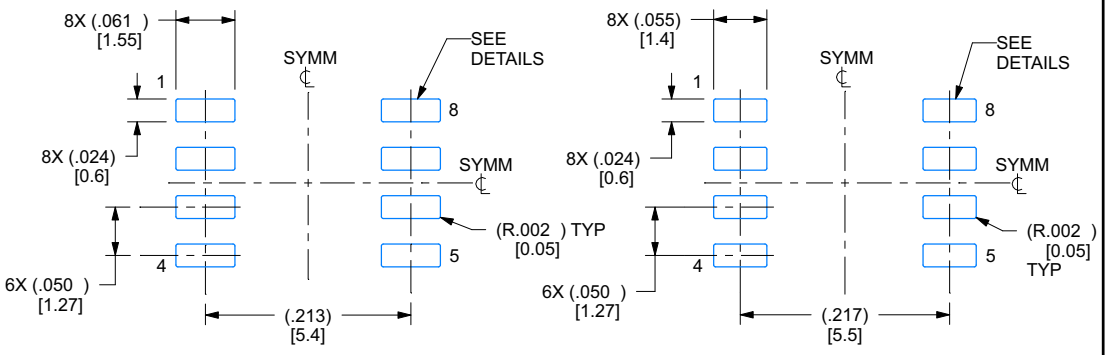
EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

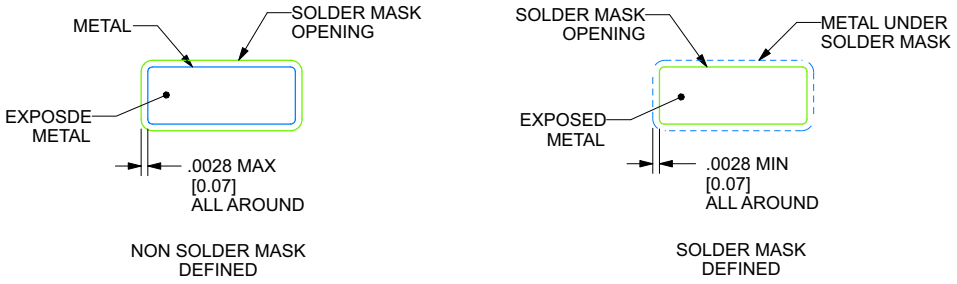
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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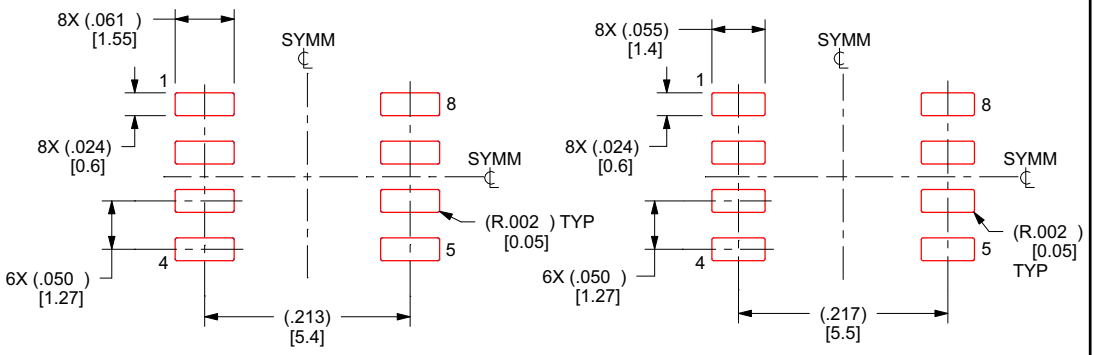
EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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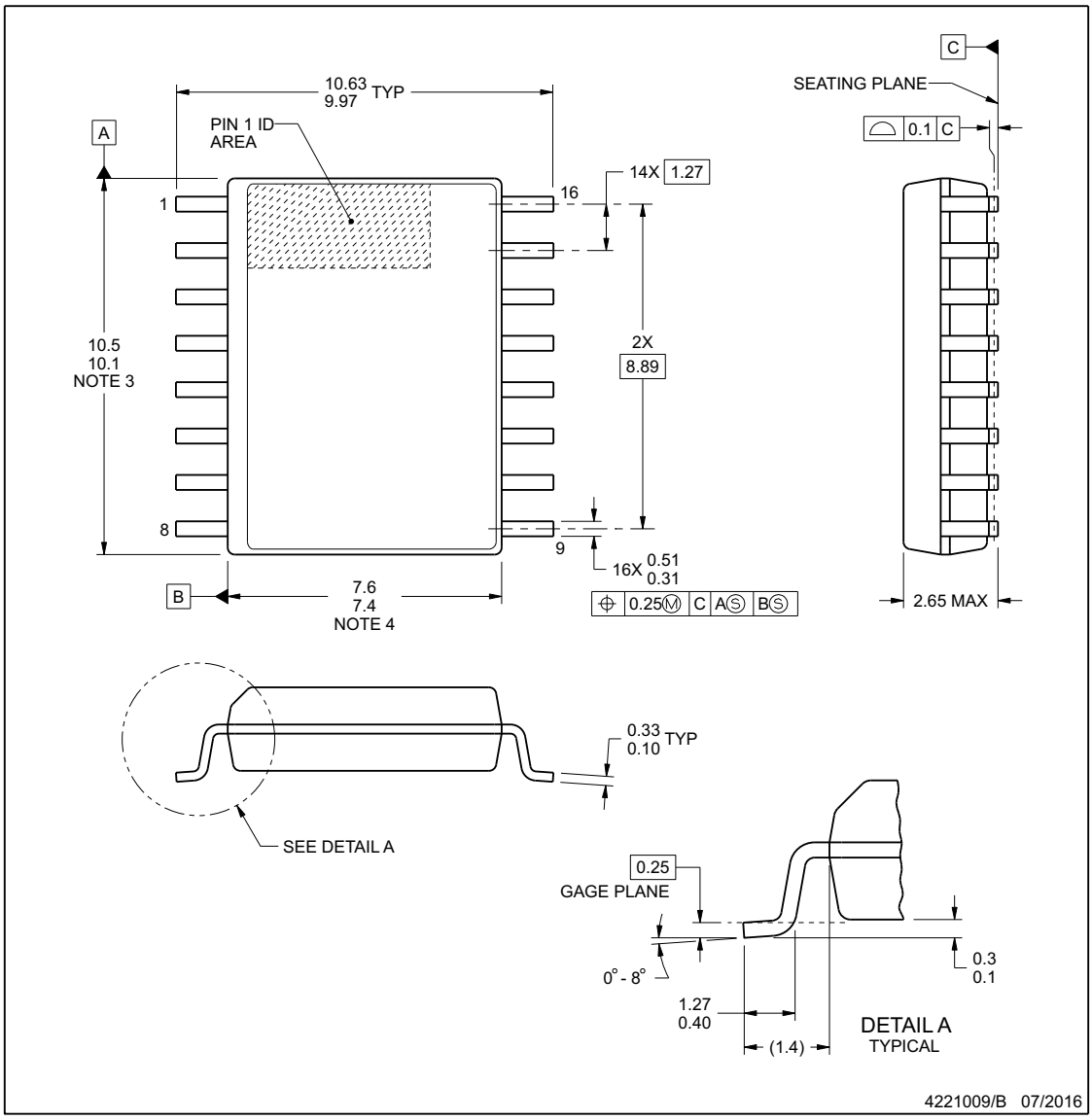
PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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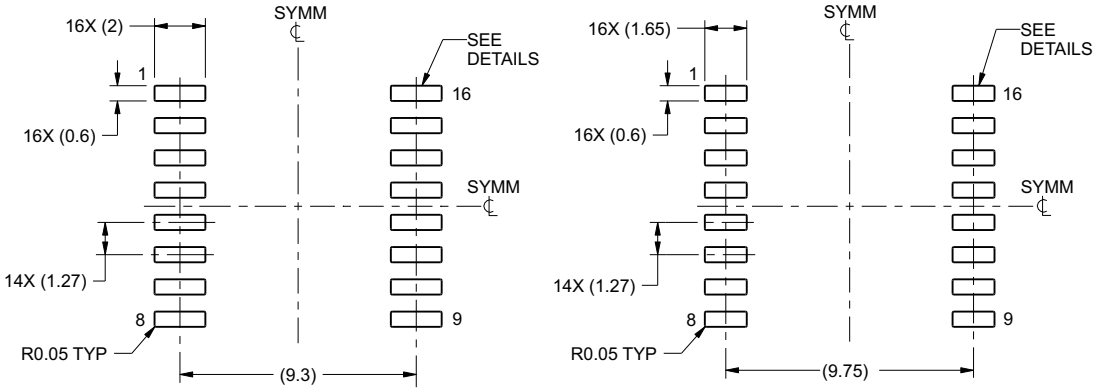
EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

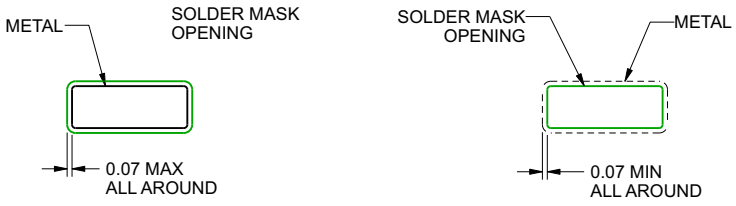
SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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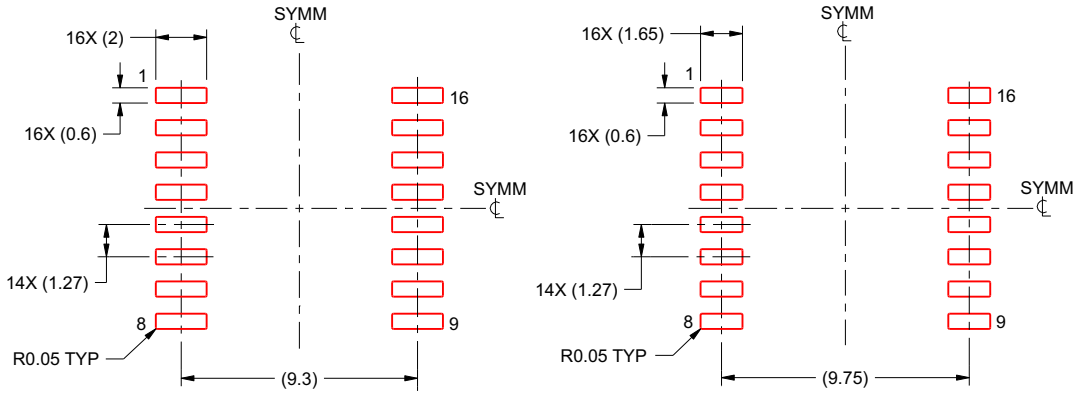
EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7710D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7710	Samples
ISO7710DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7710	Samples
ISO7710DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7710	Samples
ISO7710DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7710	Samples
ISO7710FD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7710F	Samples
ISO7710FDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7710F	Samples
ISO7710FDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7710F	Samples
ISO7710FDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7710F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO7710 :

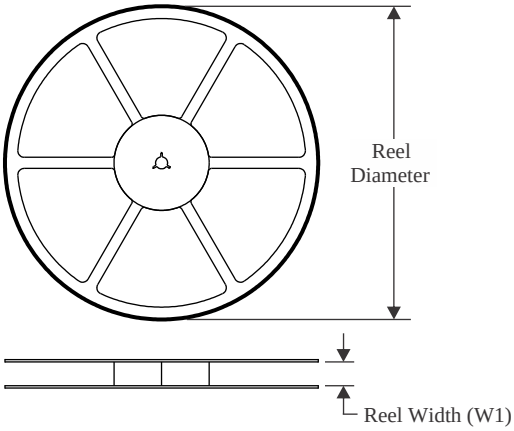
- Automotive : ISO7710-Q1

NOTE: Qualified Version Definitions:

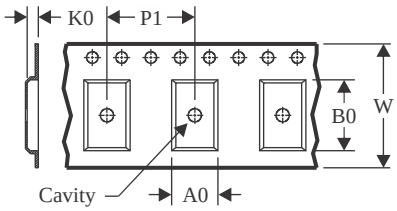
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

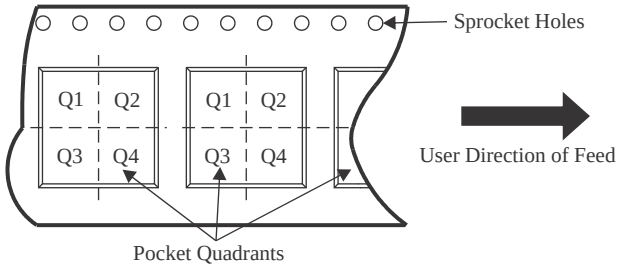


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

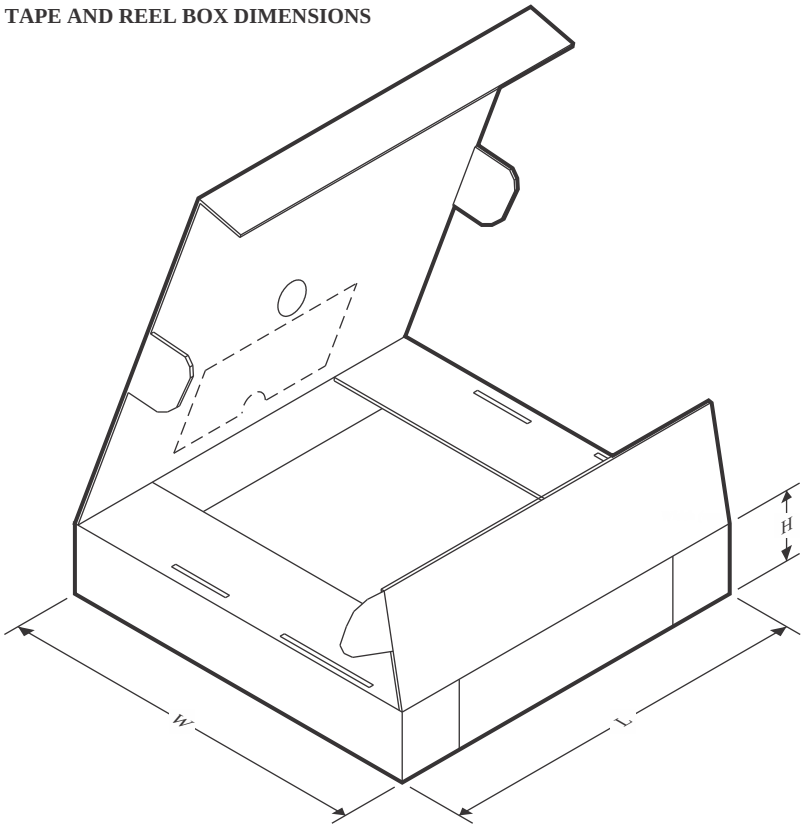
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7710DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7710DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7710FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

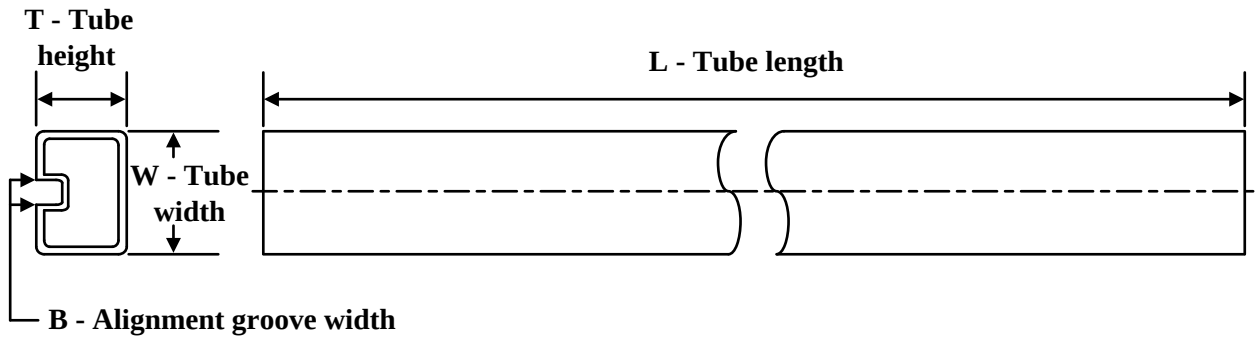
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7710DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7710DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7710DWR	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7710DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7710FDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7710FDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7710FDWR	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7710D	D	SOIC	8	75	505.46	6.76	3810	4
ISO7710DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7710DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7710FD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7710FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7710FDW	DW	SOIC	16	40	507	12.83	5080	6.6

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